TMP20 ±2.5°C Low-Power, Analog Out Temperature Sensor

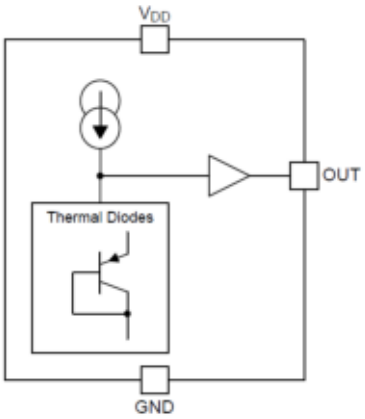
1 Features

- ±2.5°C Accuracy from –55°C to +130°C
- Supply Voltage Range: 1.8 V to 5.5 V
- Low Power: 4 µA (Maximum)
- *Micro*Size Packages: SOT-563, SC70-5
- SC70 Pin-Compatible With LM20

2 Applications

- Cell Phones
- Desktop and Notebook Computers
- Portable Devices
- Consumer Electronics
- Battery Management
- Power Supplies
- HVAC
- Thermal Monitoring
- Disk Drives
- Appliances and White Goods
- Automotive

Device Block Diagram



3 Description

The TMP20 device is a CMOS, precision analog output temperature sensor available in the tiny SOT-563 package. The TMP20 operates from –55°C to +130°C on a supply voltage of 2.7 V to 5.5 V with a supply current of 4 µA. Operation as low as 1.8 V is possible for temperatures between 15°C and 130°C. The linear transfer function has a slope of –11.77 mV/°C (typical) and an output voltage of 1.8639 V (typical) at 0°C. The TMP20 has a ±2.5°C accuracy across the entire specified temperature range of –55°C to +130°C.

The 4-µA (maximum) supply current of the TMP20 limits self-heating of the device to less than 0.01°C. When V+ is less than 0.5 V, the device is in shutdown mode and consumes less than 20 nA (typical).

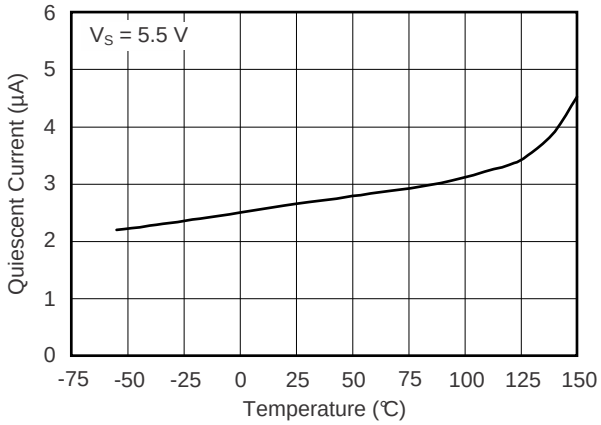
The TMP20 is available in a 5-lead SC70 or 6-lead SOT-563 package that reduces the overall required board space.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP20	SOT-563 (6)	1.60 mm × 1.20 mm
	SC70 (5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Quiescent Current Over Temperature



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 **Features** ... 1
2 **Applications** ... 1
3 **Description** ... 1
4 **Revision History** ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 6
7 **Detailed Description** ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 9
7.4 Device Functional Modes ... 10
8 **Application and Implementation** ... 11
8.1 Application Information ... 11
8.2 Typical Application ... 12
9 **Power Supply Recommendations** ... 13
10 **Layout** ... 13
10.1 Layout Guidelines ... 13
10.2 Layout Example ... 13
11 **Device and Documentation Support** ... 14
11.1 Device Support ... 14
11.2 Receiving Notification of Documentation Updates 16
11.3 Community Resources ... 16
11.4 Trademarks ... 16
11.5 Electrostatic Discharge Caution ... 16
11.6 Glossary ... 16
12 **Mechanical, Packaging, and Orderable Information** ... 17

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2017) to Revision B **Page**

- Changed the y-axis unit of *Device Quiescent Current Over Temperature* graph from: mA to: µA ... 1
- Changed the y-axis unit of *Device Quiescent Current vs Temperature* graph from: mA to: µA ... 6
- Changed the y-axis unit of *Device Quiescent Current vs Temperature* graph from: mA to: µA ... 12
- Added *Receiving Notification of Documentation Updates* section ... 16

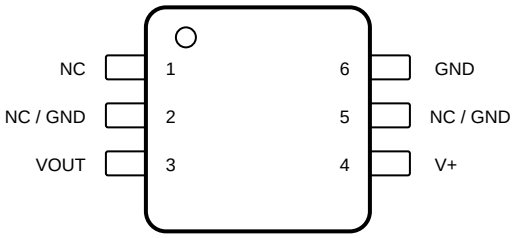
Changes from Original (December 2009) to Revision A **Page**

- Updated data sheet formatting and content to latest TIS documentation and translation standards ... 1
- Added body size information to *Device Information* section ... 1
- Updated Device Block Diagram ... 1
- Updated Device Quiescent Current Over Temperature ... 1
- Reformatted *Absolute Maximum Ratings* table ... 4
- Changed *Thermal Information* table and added thermal information ... 4
- Changed minimum temperature sensitivity value from –11.4 mV/°C to –12.2 mV/°C in *Electrical Characteristics* table ... 5
- Changed maximum temperature sensitivity value from –12.2 mV/°C to –11.4 mV/°C in *Electrical Characteristics* table ... 5
- Updated Figure 1 ... 6
- Updated Figure 3 ... 6
- Updated Figure 7 ... 6
- Added *Functional Block* diagram, key graphics on front page, typical application schematic, application curves, and updated layout images ... 8
- Reformatted equations in *Transfer Function* section ... 9
- Corrected Equation 2 in *Transfer Function* section ... 9
- Added copyright notices to Figure 15 and Figure 16 ... 14

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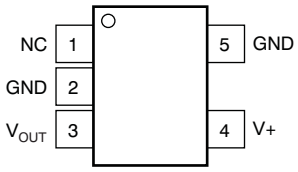
5 Pin Configuration and Functions

DRL Package
6-Pin SOT-563
Top View



Not to scale

DCK Package
5-Pin SC70
Top View



NC- no internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRL (SOT-563)	DCK (SC70)		
GND	6	5	—	Ground pin
NC	1	1	—	This pin must be grounded or left floating. See *Layout Example* for more information.
NC / GND	2, 5	2	—	This pin must be grounded or left floating. For best thermal response, connect to GND plane. See *Layout Example* for more information.
V_{OUT}	3	3	O	Analog output
V+	4	4	I	Positive supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V+		7	V
Operating temperature	–55	150	°C
Junction temperature, $T_{J(max)}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
	Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range	1.8	5.5	V
T_A	Specified temperature range	–55	130	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP20		UNIT
		DRL (SOT563)	DCK (SC70)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	238	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	253	263.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	126.4	76.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	126	51.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	1.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	125.9	50.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MEASUREMENT (1)						
	Accuracy (2)	T_A = –55°C to 130°C	–2.5		2.5	°C
	vs supply	V+ = 1.8 V to 5.5 V T_A = 15°C to 130°C	–0.05		0.05	°C/V
		V+ = 2.7 V to 5.5 V T_A = –50°C to 130°C	–0.05		0.05	°C/V
	Temperature sensitivity (3)	T_A = –30°C to 100°C	–12.2	–11.77	–11.4	mV/°C
	Output voltage (4)	T_A = 0°C		1863.9		mV
		T_A = 25°C		1574		
	Nonlinearity (5)	–20°C ≤ T_A ≤ 80°C		±0.4%		
ANALOG OUTPUT						
	Output resistance	–600 µA ≤ I_{LOAD} ≤ 600 µA		10		Ω
	Load regulation	–600 µA ≤ I_{LOAD} ≤ 600 µA		6		mV
	Maximum capacitive load		1			nF
POWER SUPPLY						
V_S	Specified voltage	T_A = –55°C to 130°C	2.7		5.5	V
		T_A = 15°C to 130°C (6)	1.8		5.5	
I_Q	Quiescent current	V+ = 5.5 V T_A = 25°C		2.6	4	µA
	Over temperature	V+ = 5.5 V T_A = –55°C to 130°C			6	µA
I_{SD}	Shutdown current	V+ < 0.5 V		20		nA
TEMPERATURE RANGE						
	Specified operating	T_A = –55°C to 130°C	–55		130	°C
		T_A = 15°C to 130°C (6)	15		130	°C
	Operating range	V+ = 2.7 V to 5.5 V	–55		150	°C
θ_{JA}	Thermal resistance	SC70		185		°C/W
		SOT-563		238		°C/W
	Self-heating	SC70			0.01	°C
		SOT-563			0.01	°C

(1) 100% production tested at T_A = 25°C. Specifications over temperature range are assured by design.
(2) Power-supply rejection is encompassed in the accuracy specification.
(3) Temperature sensitivity is the average slope to the equation $V_O = (–11.77 \times T) + 1.860$ V.
(4) V_{OUT} is calculated from temperature with the following equation:
$V_O = (–3.88 \times 10^{–6} \times T^2) + (–1.15 \times 10^{–2} \times T) + 1.8639$ V,
where T is in °C.
(5) Nonlinearity is the deviation of the calculated output voltage from the best fit straight line.
(6) The TMP20 transfer function requires the output voltage to rise above the 1.8-V supply as the temperature decreases below 15°C. When operating at a 1.8-V supply, it is normal for the TMP20 output to approach 1.8 V and remain at that voltage as the temperature continues to decrease below 15°C. This condition does not damage the device. Once the temperature rises above 15°C, the output voltage resumes changing as the temperature changes, according to the transfer function specified in this document. For more information about the transfer function, see *Transfer Function* .

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6.6 Typical Characteristics

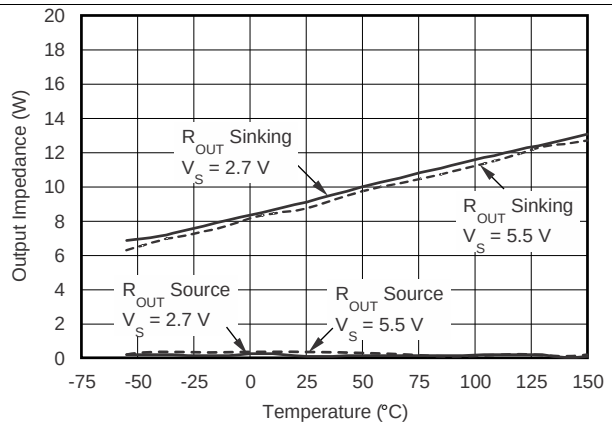


Figure 1. Output Impedance vs Temperature

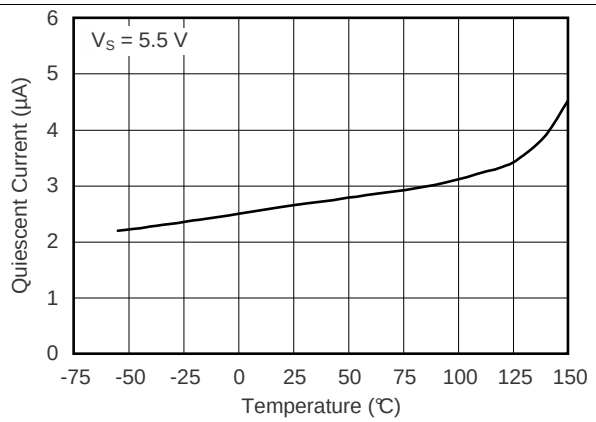


Figure 2. Quiescent Current vs Temperature

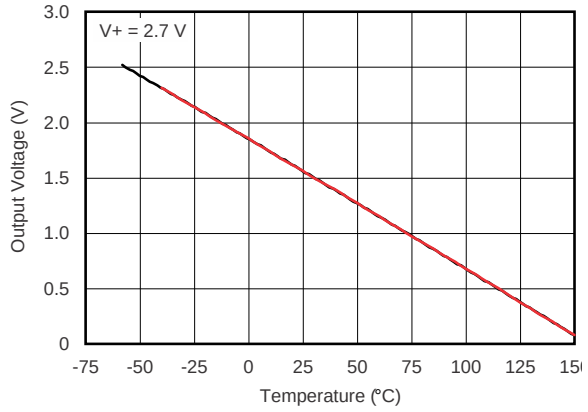


Figure 3. Output Voltage vs Temperature

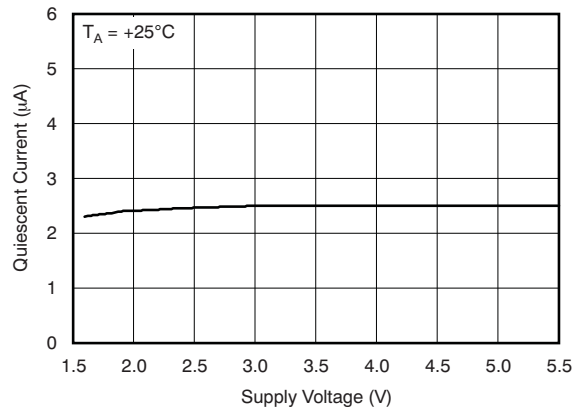


Figure 4. Quiescent Current vs Supply Voltage

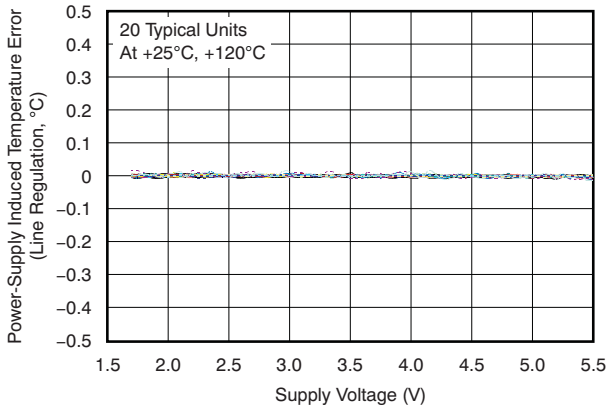


Figure 5. Power-Supply Rejection vs Temperature

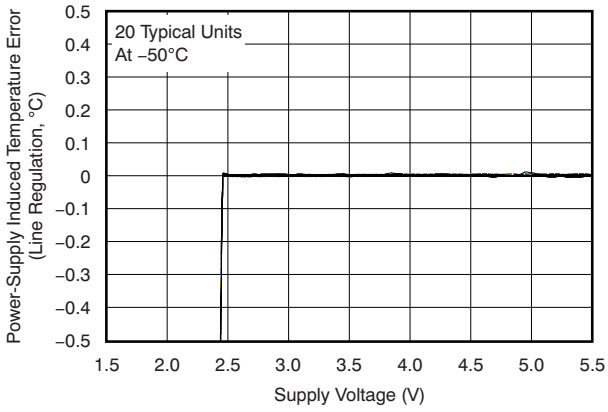


Figure 6. Power-Supply Rejection vs Temperature

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Typical Characteristics (continued)

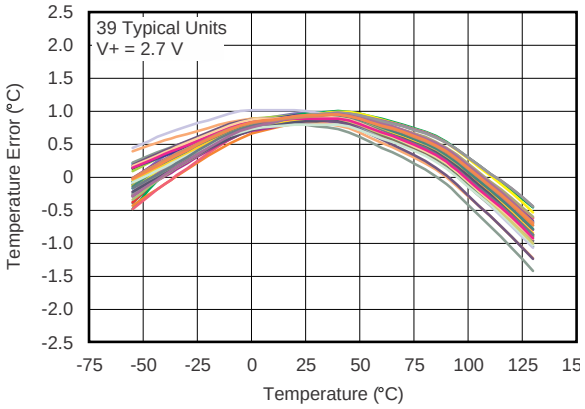


Figure 7. Temperature Error vs Temperature

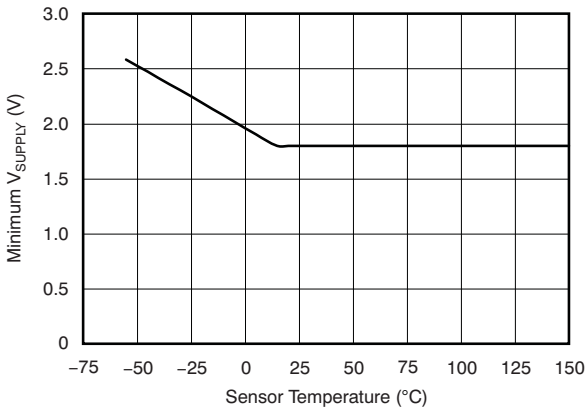


Figure 8. Minimum Supply Voltage vs Temperature

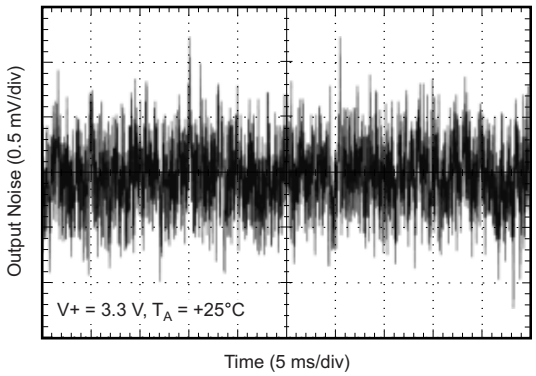


Figure 9. Wideband Output Noise Voltage

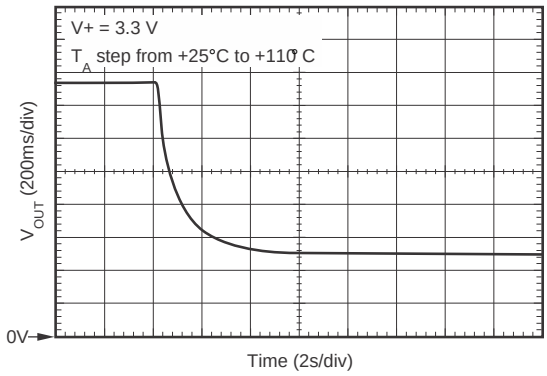


Figure 10. Thermal Settling (Fluid-Filled Temperature Bath)

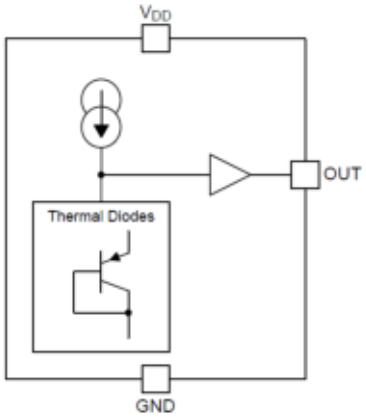
7 Detailed Description

7.1 Overview

The TMP20 device is a precision analog output temperature sensor. The temperature range of operation is –55°C to +130°C with supply voltages of 2.7 V to 5.5 V. The TMP20 operates from power-supply voltages as low as 1.8 V over a temperature range of 15°C to 130°C.

TI recommends power supply bypassing; use a 100-nF capacitor placed as closely as possible to the supply pin.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Transfer Function

The analog output of the TMP20 over the –55°C to +130°C temperature range corresponds to the parabolic transfer function shown in
Added *Receiving Notification of Documentation Updates* section:

$$V_{OUT} = \left(-3.88 \times 10^{-6} \times T^2\right) + \left(-1.15 \times 10^{-2} \times T\right) + 1.8639\ V \quad (1)$$

Where:

- the temperature (T) is in °C.

When solving for temperature, the equation is shown as Equation 2:

$$T = -1481.96 + \sqrt{2.1962 \times 10^{6} + \frac{(1.8639 - V_O)}{3.88 \times 10^{-6}}} \quad (2)$$

These equations apply over the entire operating range of –55°C to +130°C.

A simplified linear transfer function referenced at 25°C is shown in Equation 3:

$$V_{OUT} = -11.69\ mV / °C \times T + 1.8863\ V \quad (3)$$

Linear transfer functions are calculated for limited temperature ranges by calculating the slope and offset for that limited range, where slope is calculated by Equation 4:

$$m = -7.76 \times 10^{-6} \times T - 0.0115 \quad (4)$$

Where:

- T equals the temperature at the middle of the temperature range of interest

The offset in the linear transfer function is calculated with Equation 5:

$$b = \left(V_{OUT}(T_{MAX}) + V_{OUT}(T) - m \times (T_{MAX} + T)\right) / 2 \quad (5)$$

where

- $V_{OUT}(T_{MAX})$ is the calculated output voltage at T_{MAX} as determined from Added *Receiving Notification of Documentation Updates* section.

$V_{OUT}(T)$ is the calculated output voltage at T as calculated by
Added *Receiving Notification of Documentation Updates* section.

7.3.1.1 Example 1

Determine the linear transfer function for –40°C to +110°C.

T_{MIN} = –40°C; T_{MAX} = 110°C; therefore, T = 35°C

m = –11.77mV/°C
V_{OUT} (110°C) = 0.5520 V
V_{OUT} (35°C) = 1.4566 V
b = 1.8576 V

The linear transfer function for –40°C to +110°C is shown in Equation 6:

$$V_{OUT} = -11.77\ mV / °C \times T + 1.8576\ V \quad (6)$$

Feature Description (continued)

Table 1 lists common temperature ranges of interest and the corresponding linear transfer functions for these ranges. Note that the error (maximum deviation) of the linear equation from the parabolic equation increases as the temperature ranges widen.

Table 1. Common Temperature Ranges and Corresponding Linear Transfer Functions

TEMPERATURE RANGE		LINEAR EQUATION (V)	MAXIMUM DEVIATION OF LINEAR EQUATION FROM PARABOLIC EQUATION (°C)
T_{MIN} (°C)	T_{MAX} (°C)		
–55	130	V_{OUT} = –11.79 mV/°C × T + 1.8528	±1.41
–40	110	V_{OUT} = –11.77 mV/°C × T + 1.8577	±0.93
–30	100	V_{OUT} = –11.77 mV/°C × T + 1.8605	±0.70
–40	85	V_{OUT} = –11.67 mV/°C × T + 1.8583	±0.65
–10	65	V_{OUT} = –11.71 mV/°C × T + 1.8641	±0.23
35	45	V_{OUT} = –11.81 mV/°C × T + 1.8701	±0.004
20	30	V_{OUT} = –11.69 mV/°C × T + 1.8663	±0.004

7.4 Device Functional Modes

The singular functional mode of the TMP20 is an analog output inversely proportional to temperature.

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8 Application and Implementation

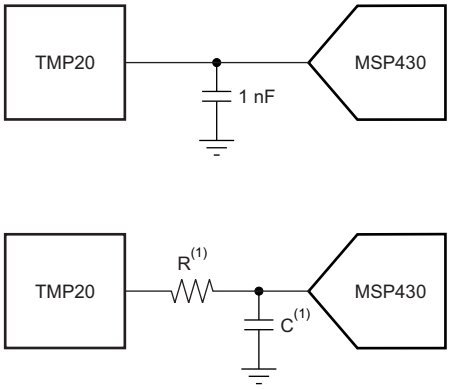
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Drive and Capacitive Loads

When used in noisy environments, adding a capacitor from the output to ground with a series resistor filters the TMP20 output; this configuration is shown in Figure 11. The TMP20 can drive up to 1 nF of load capacitance while sourcing and sinking 600 μA. Under this condition, capacitive loads in the range of 1 nF to 10 μF require a 150-Ω series output resistor to achieve a stable temperature measurement. The output impedance of the TMP20 is typically 10 Ω when sinking currents and less than 1 Ω when sourcing current, as shown in Figure 1.

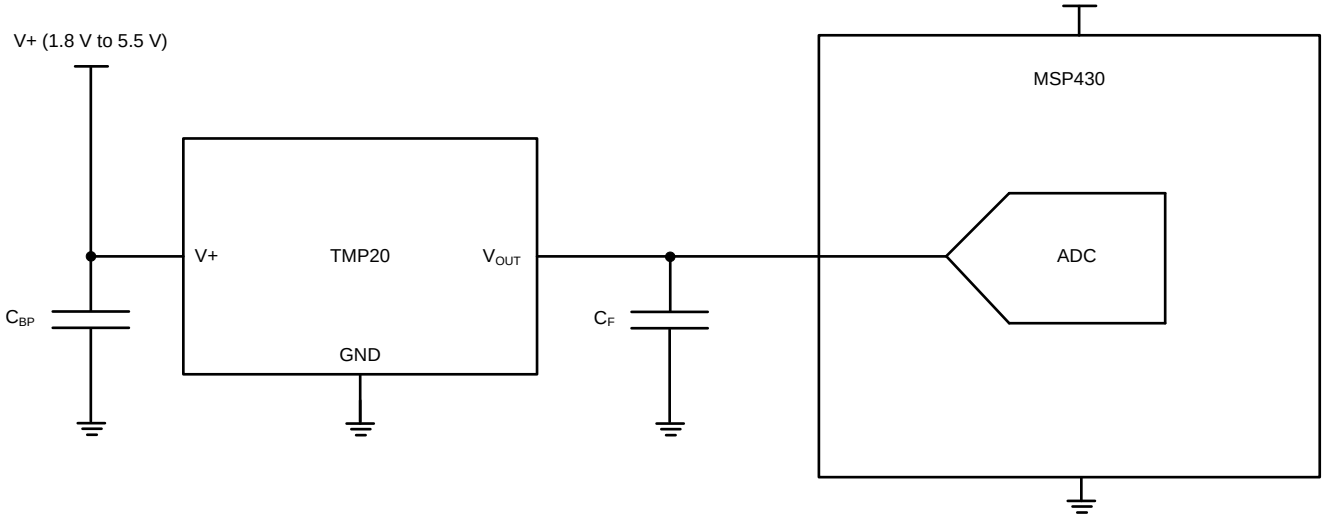


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(1) A series resistor (R) may be required depending upon the amount of capacitance (C) and the amount of source and sink current drawn from the output of the TMP20.

Figure 11. TMP20 Output Filtering

8.2 Typical Application



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Figure 12. Suggested Connections to a MCU ADC

8.2.1 Design Requirements

ADCs that are found in microcontrollers (such as the MSP430 line of microcontrollers) take charge during the sampling phase. A high sampling frequency results in too much charge pulled into the ADC and sags the output voltage of the TMP20, which results in a reading that is hotter than normal. To mitigate this, place a capacitor (C_F) between the TMP20 and the ADC. The capacitor functions as a charge reservoir.

8.2.2 Detailed Design Procedure

The size of C_F depends on the size of the internal sampling capacitor and the sampling frequency. The charge requirements may vary because not all ADCs have identical input stages. This general ADC application is shown as an example only.

8.2.3 Application Curves

Figure 13 shows the quiescent current versus temperature.

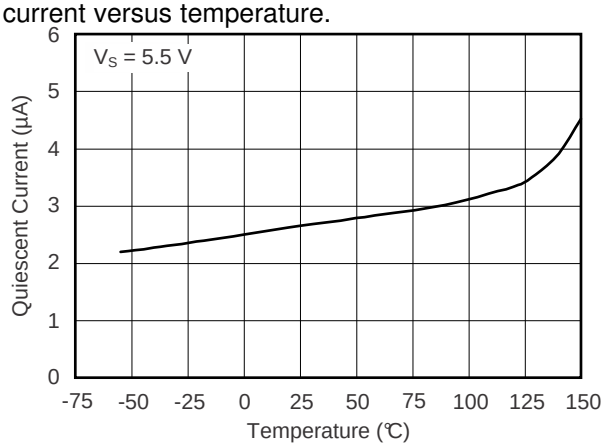


Figure 13. Quiescent Current vs Temperature

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9 Power Supply Recommendations

The low supply current and supply range of 1.8 V to 5.5 V enable the TMP20 to be powered from multiple supply sources.

Power supply bypassing is optional and is typically dependent on the noise of the power supply. In noisy systems, adding bypass capacitors may be necessary to decrease the noise that couples to the output of the TMP20.

10 Layout

10.1 Layout Guidelines

The substrate on the TMP20AIDCK package is directly connected through conductive epoxy to the flag that connects pin 2 on the lead frame. Consequently, pin 2 is the best lead for a conductive thermal connection to the TMP20 die. The optimal electrical connection for this pin is ground (GND).

CAUTION

Do not attempt to connect pin 2 (DCK package) to any electrical potential other than ground.

If it is not possible to connect pin 2 to ground, it is possible to electrically isolate this pin (that is, leave it floating). Take care when electrically isolating this pin because any noise or electromagnetic interference or radio frequency interference (EMI or RFI) spikes that couple in through this pin can cause erroneous temperature results.

shows a proper layout of the TMP20 with correct electrical and thermal connections to pin 2.

10.2 Layout Example

Figure 14 shows a layout of the TMP20 with proper electrical and thermal connections to pin 2.

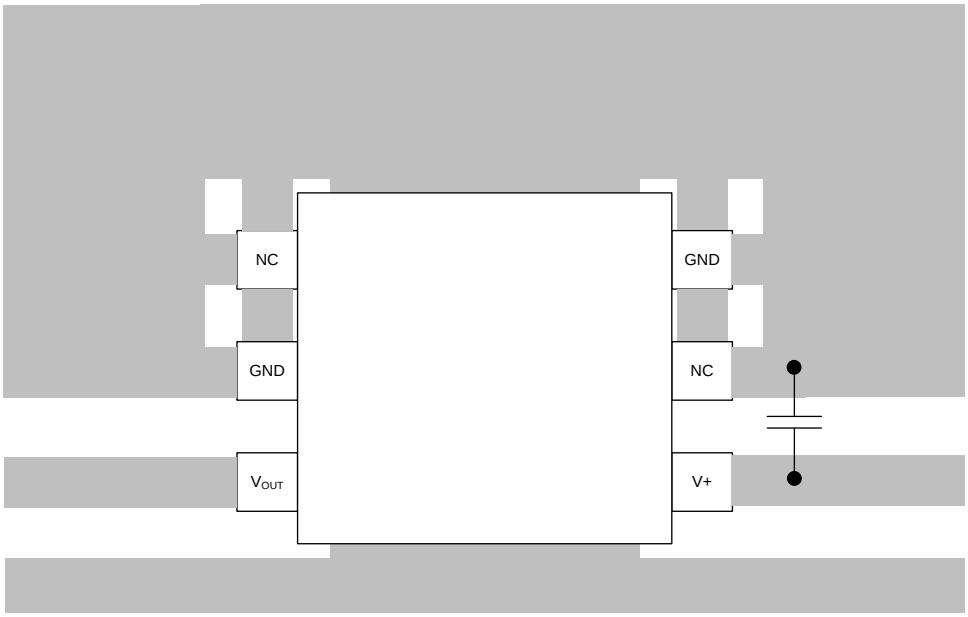


Figure 14. TMP20 Layout With Proper Electrical and Thermal Connections

11 Device and Documentation Support

11.1 Device Support

11.1.1 TINA-TI (Free Download Software)

TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of passive and active models. It provides all the conventional dc, transient, and frequency domain analysis of SPICE and additional design capabilities.

Available as a free download from the WEBENCH® Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

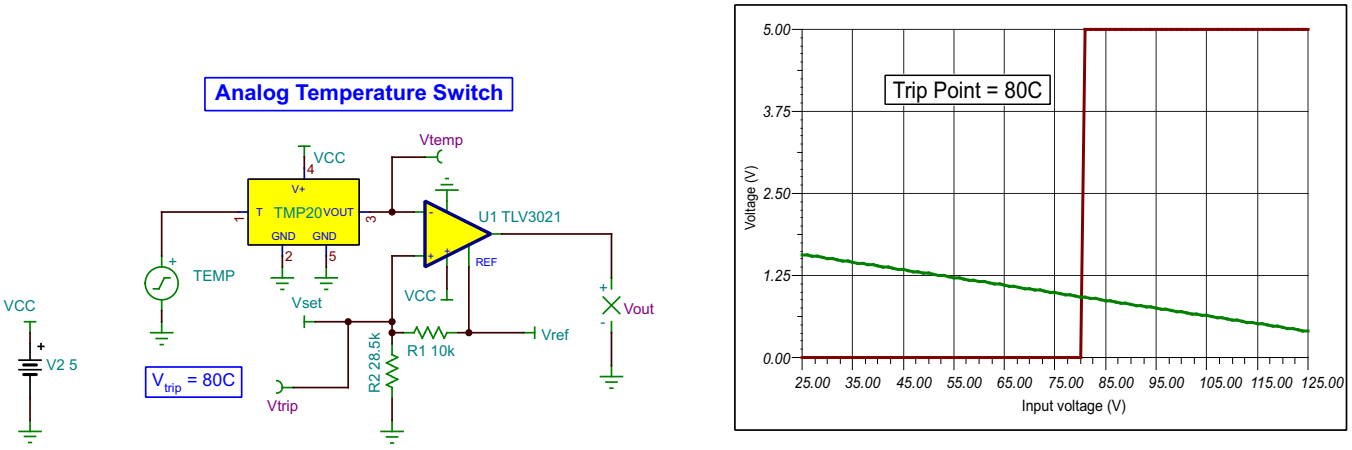
Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 15 and Figure 16 show example TINA-TI circuits for the TMP20 that can develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

11.1.1.1 Using TINA-TI SPICE-Based Analog Simulation Program with the TMP20

NOTE

These files require that the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.



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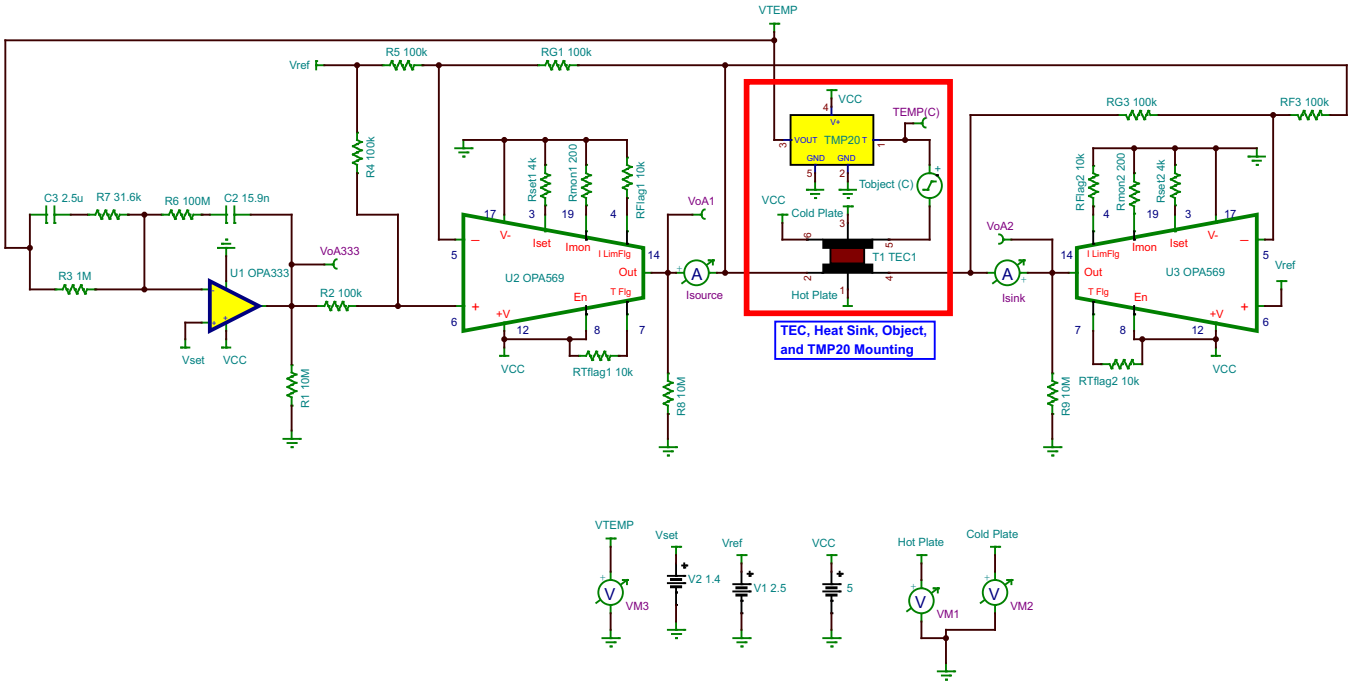
Note: The TMP20 TINA model is preliminary only.

Figure 15. Analog Temperature Switch

To download a compressed file that contains the TINA-TI simulation file for this circuit, visit the WEBENCH® Design Center.

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Device Support (continued)



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(1) The TMP20 TINA model is preliminary only.

(2) Parameters and definitions:

a. T_{object} = Temperature of the object to be cooled (in °C)

b. V_{set} = Voltage that corresponds to the desired output temperature from the TMP20

c. VTEMP = Voltage output of the TMP20

d. Hotplate = TEC plate on opposite side of object

e. Coldplate = TEC plate in contact with object

(3) In this configuration, the TEC driver can cool to –T°C and heating to 41°C; the V_{set} range is 1.38 V to 1.95 V. The OPA569 device outputs = ±1.65 A, ±0.5 V to ±4.5 V. The 10-MΩ resistors are for TINA convergence.

(4) For convergence in TINA software: In **Analysis**/**Set Analysis Parameters** menu, set *shunt conductance* = 1 p.

Figure 16. Thermoelectric Cooler

To download a compressed file that contains the TINA-TI simulation file for this circuit, see Thermoelectric Cooler.

Device Support (continued)

11.1.2 Development Support

WEBENCH® Design Center

TINA-TI folder

Analog Temperature Switch

Thermoelectric Cooler

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP20AIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	ODB
TMP20AIDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	ODB
TMP20AIDRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	ODA
TMP20AIDRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ODA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

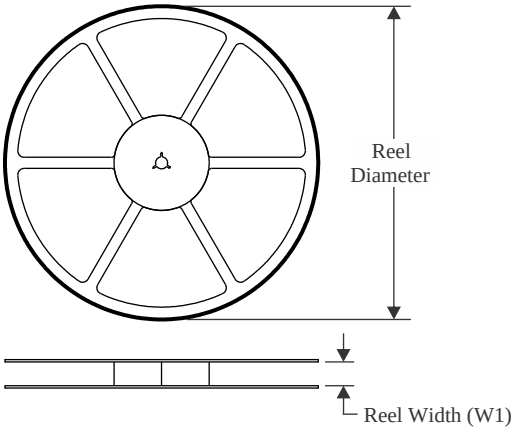
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

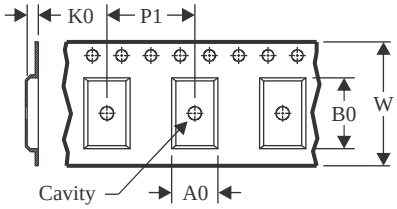
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

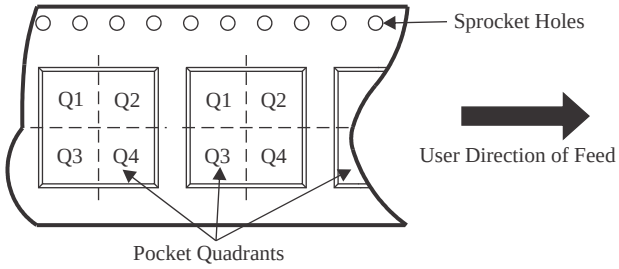


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

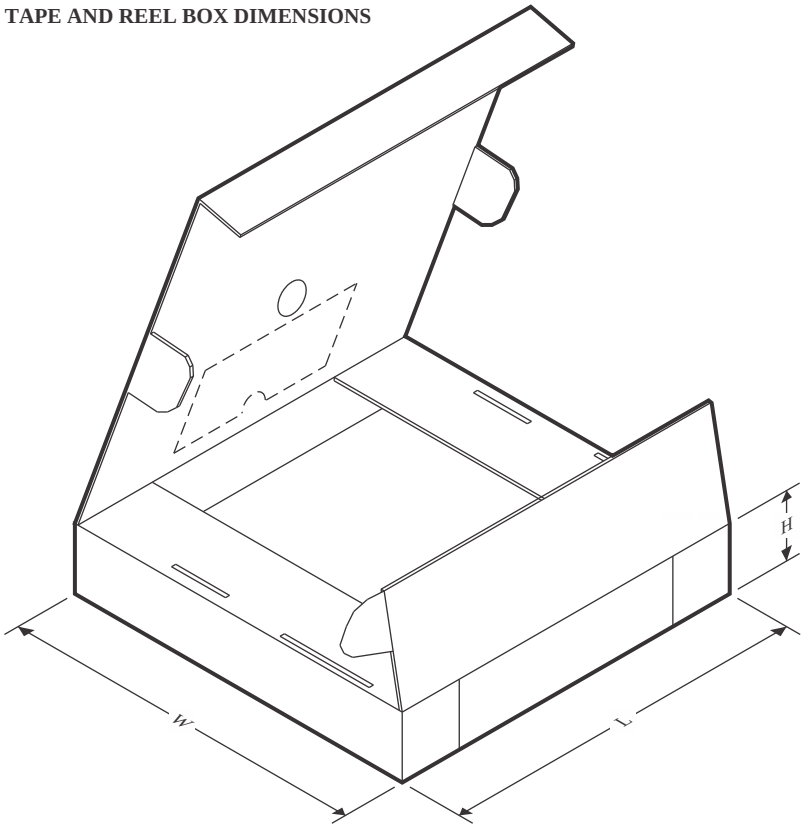
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP20AIDCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TMP20AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMP20AIDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

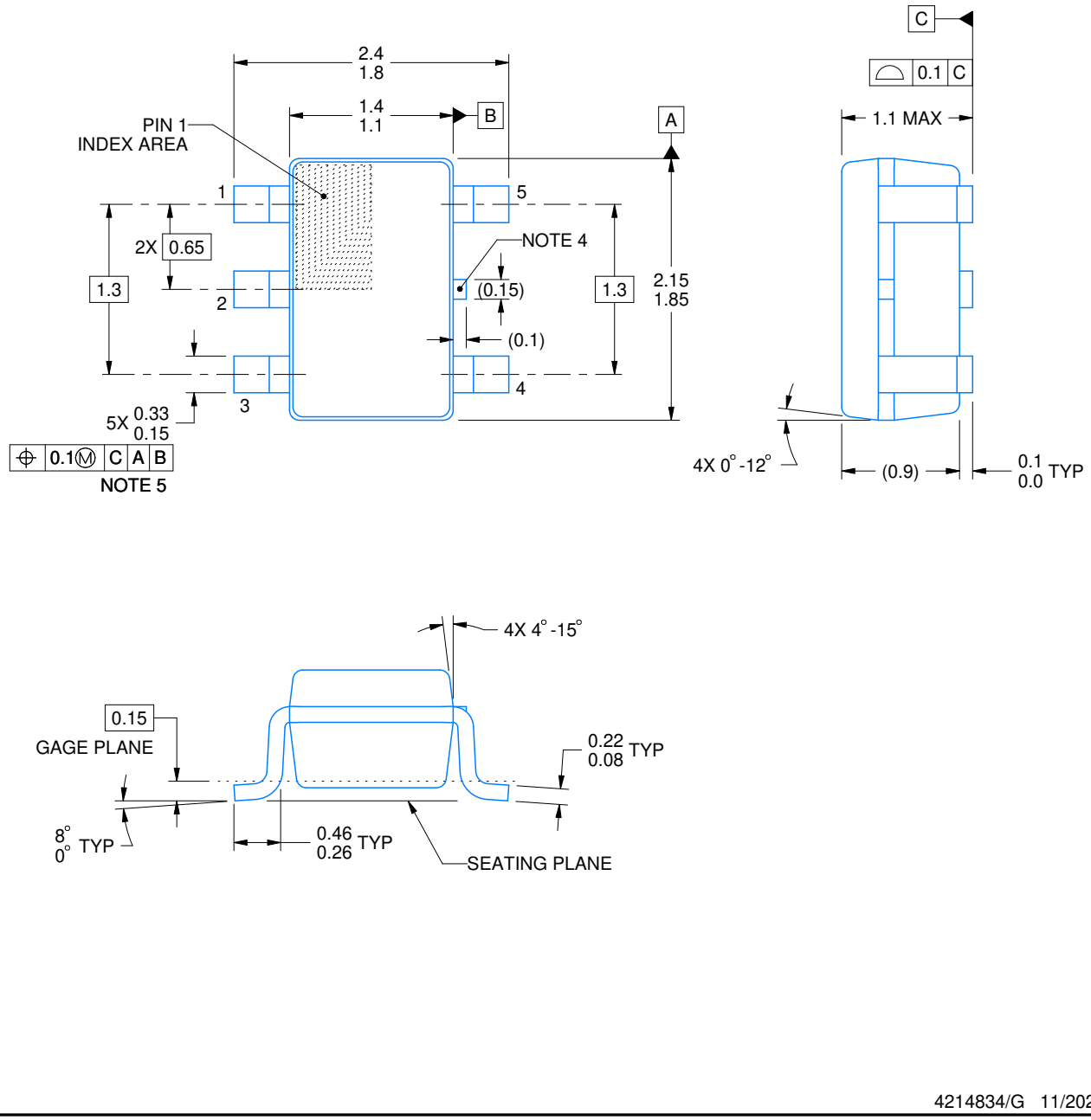
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP20AIDCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TMP20AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TMP20AIDRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

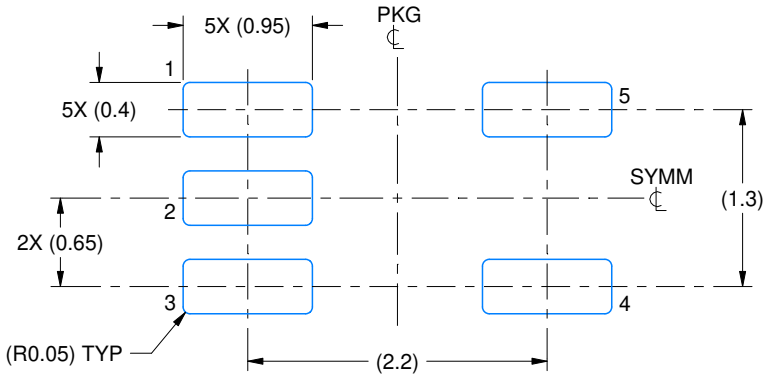
SMALL OUTLINE TRANSISTOR



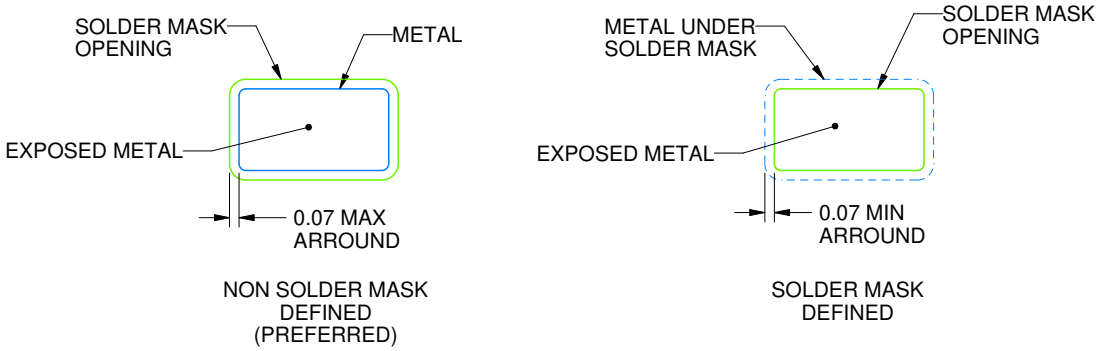
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

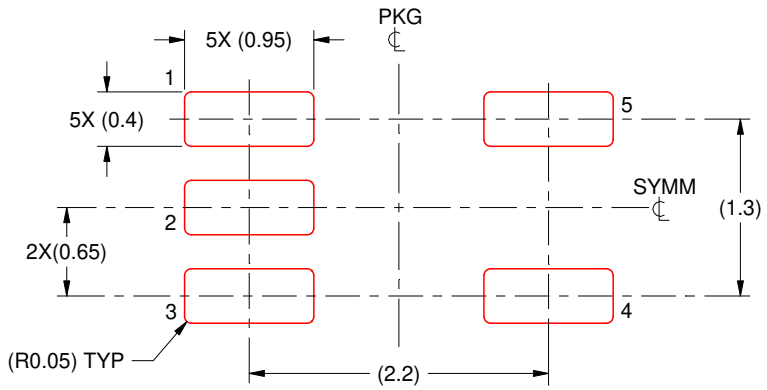


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

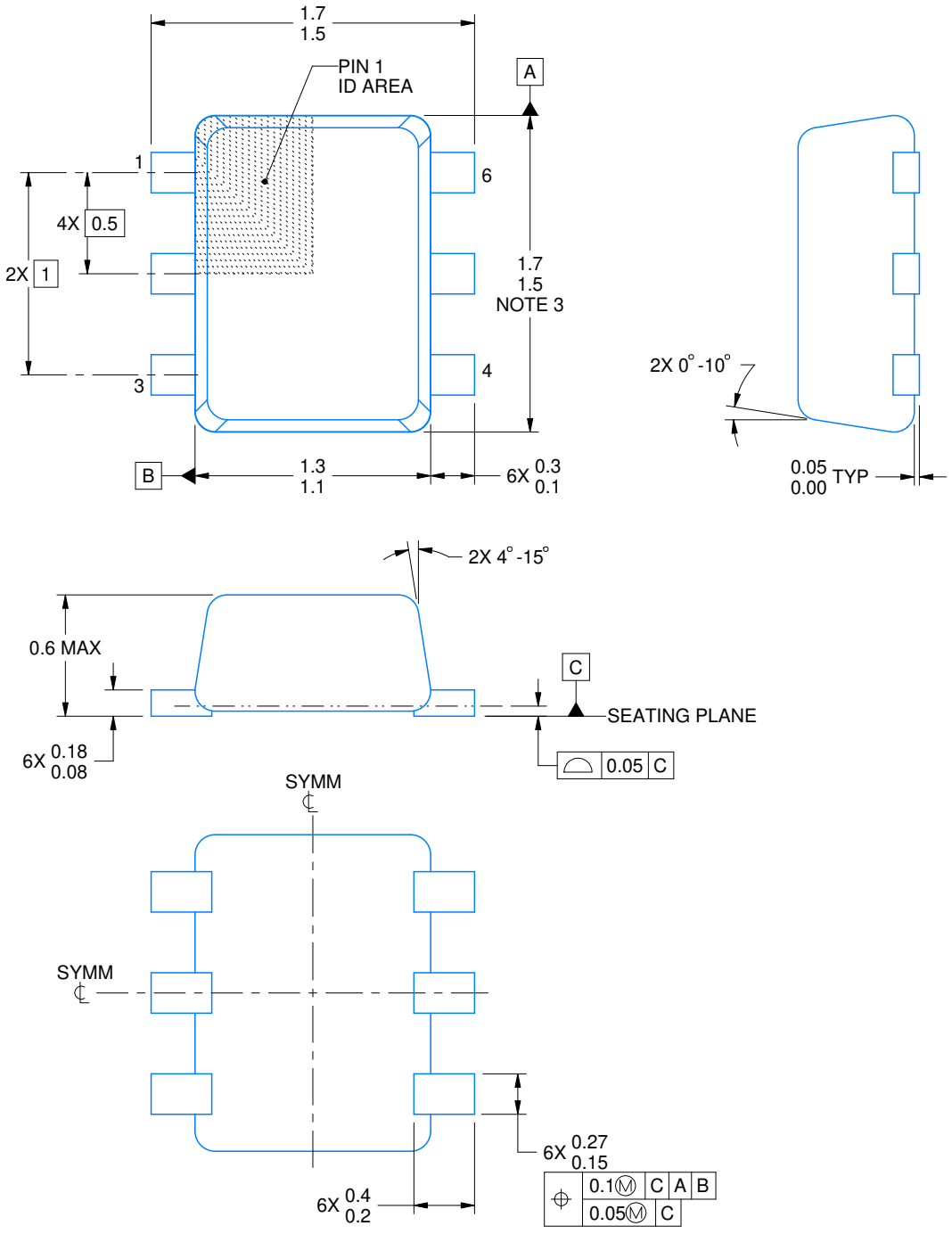
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

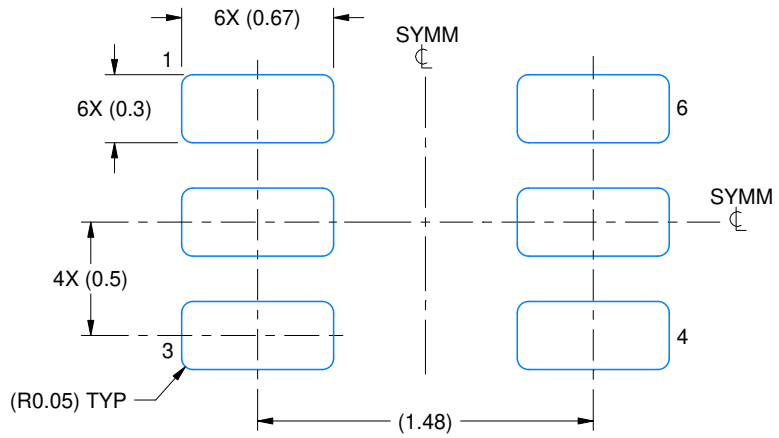
PLASTIC SMALL OUTLINE



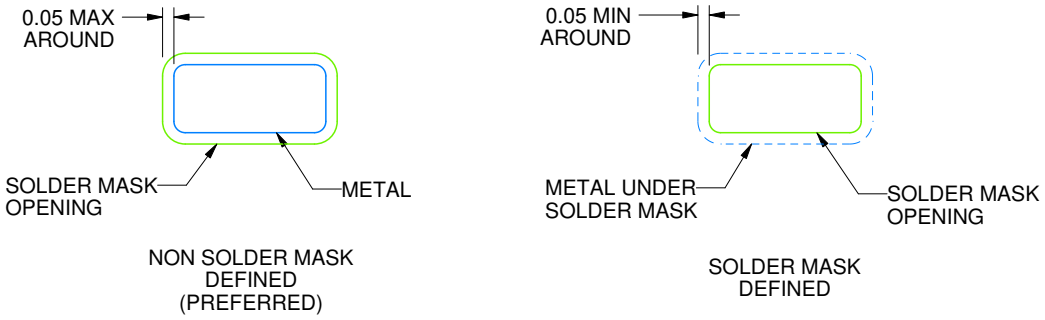
4223266/F 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X

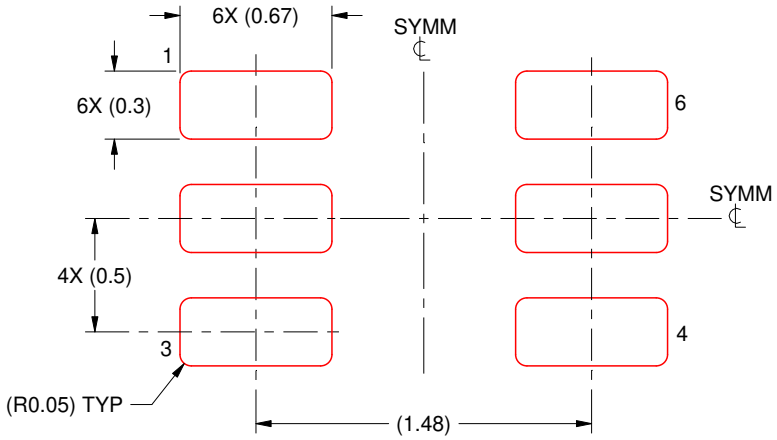


SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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