TMS320F2807x Real-Time Microcontrollers

1 Features

- TMS320C28x 32-bit CPU
  - 120MHz
  - IEEE 754 single-precision Floating-Point Unit (FPU)
  - Trigonometric Math Unit (TMU)
- Programmable Control Law Accelerator (CLA)
  - 120MHz
  - IEEE 754 single-precision floating-point instructions
  - Executes code independently of main CPU
- On-chip memory
  - 512KB (256KW) of flash (ECC-protected)
  - 100KB (50KW) of RAM (ECC-protected or parity-protected)
  - Dual-zone security supporting third-party development
  - Unique identification number
- Clock and system control
  - Two internal zero-pin 10MHz oscillators
  - On-chip crystal oscillator
  - Windowed watchdog timer module
  - Missing clock detection circuitry
- 3.3V I/O with available internal voltage regulator for 1.2V core supply
- System peripherals
  - External Memory Interface (EMIF) with ASRAM and SDRAM support
  - 6-channel Direct Memory Access (DMA) controller
  - Up to 97 individually programmable, multiplexed General-Purpose Input/Output (GPIO) pins with input filtering
  - Expanded Peripheral Interrupt controller (ePIE)
  - Multiple Low-Power Mode (LPM) support with external wakeup
- Communications peripherals
  - USB 2.0 (MAC + PHY)
  - Two Controller Area Network (CAN) modules (pin-bootable)
  - Three high-speed (up to 30MHz) SPI ports (pin-bootable)
  - Two Multichannel Buffered Serial Ports (McBSPs)
  - Four Serial Communications Interfaces (SCI/UART) (pin-bootable)
  - Two I2C interfaces (pin-bootable)
- Analog subsystem
  - Up to three Analog-to-Digital Converters (ADCs)
    - 12-bit mode
      - 3.1MSPS each (up to 9.3MSPS system throughput)
      - Single-ended inputs
      - Up to 17 external channels
    - Single Sample-and-Hold (S/H) on each ADC
    - Hardware-integrated post-processing of ADC conversions
      - Saturating offset calibration
      - Error from setpoint calculation
      - High, low, and zero-crossing compare, with interrupt capability
      - Trigger-to-sample delay capture
  - Eight windowed comparators with 12-bit Digital-to-Analog Converter (DAC) references
  - Three 12-bit buffered DAC outputs
- Enhanced control peripherals
  - 24 PWM channels with enhanced features
  - 16 High-Resolution Pulse Width Modulator (HRPWM) channels
    - High resolution on both A and B channels of 8 PWM modules
    - Dead-band support (on both standard and high resolution)
  - Six Enhanced Capture (eCAP) modules
  - Three Enhanced Quadrature Encoder Pulse (eQEP) modules
  - Up to eight Sigma-Delta Filter Module (SDFM) input channels, 2 parallel filters per channel
    - Standard SDFM data filtering
    - Comparator filter for fast action for out of range
- Configurable Logic Block (CLB)
  - Augments existing peripheral capability
  - Supports position manager solutions
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL D; IEC 61508 up to SIL 3; IEC 60730 up to Class C; and UL 1998 up to Class 2
  - Hardware integrity up to ASIL B, SIL 2
- Safety-related certification
  - ISO 26262 certified up to ASIL B and IEC 61508 certified up to SIL 2 by TUV SUD

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

- Package options:
  - 176-pin PowerPAD™ Thermally Enhanced Low-Profile Quad Flatpack (HLQFP) [PTP suffix]
  - 100-pin PowerPAD Thermally Enhanced Thin Quad Flatpack (HTQFP) [PZP suffix]
- Hardware Built-in Self Test (HWBIST)
- Temperature options:
  - T: –40°C to 105°C junction
  - S: –40°C to 125°C junction
  - Q: –40°C to 125°C free-air (AEC Q100 qualification for automotive applications)

2 Applications

- Medium/short range radar
- Traction inverter motor control
- HVAC large commercial motor control
- Automated sorting equipment
- CNC control
- AC charging (pile) station
- DC charging (pile) station
- EV charging station power module
- Energy storage power conversion system (PCS)
- Central inverter
- Solar power optimizer
- String inverter
- Inverter & motor control
- On-board (OBC) & wireless charger
- AC drive control module
- AC drive power stage module
- Linear motor power stage
- Servo drive control module
- AC-input BLDC motor drive
- DC-input BLDC motor drive
- Industrial AC-DC
- Three phase UPS

3 Description

C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in real-time control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing. The C2000 line includes the Premium performance MCUs and the Entry performance MCUs.

The TMS320F2807x microcontroller family is suited for advanced closed-loop control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; and sensing and signal processing. To accelerate application development, the DigitalPower software development kit (SDK) for C2000 MCUs and the MotorControl software development kit (SDK) for C2000™ MCUs are available.

The F2807x is a 32-bit floating-point microcontroller based on TI's industry-leading C28x core. This core is boosted by the trigonometric hardware accelerator which improves performance of trigonometric-based algorithms with CPU instructions such as sine, cosine, and arctangent functions, which are common in torque-loop and position calculations.

The F2807x microcontroller family features a CLA real-time control coprocessor. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics.

The F2807x device supports up to 512KB (256KW) of ECC-protected onboard flash memory and up to 100KB (50KW) of SRAM with parity. Two independent security zones are also available for 128-bit code protection of the main C28x.

The analog subsystem boasts up to three 12-bit ADCs, which enable simultaneous management of three independent power phases, and up to eight windowed comparator subsystems (CMPSSs), allowing very fast, direct trip of the PWMs in overvoltage or overcurrent conditions. In addition, the device has three 12-bit DACs, and precision control peripherals such as enhanced pulse width modulators (ePWMs) with fault protection, eQEP peripherals, and eCAP units.

Connectivity peripherals such as dual Controller Area Network (CAN) modules (ISO 11898-1/CAN 2.0B-compliant) and a USB 2.0 port with MAC and full-speed PHY let users add universal serial bus (USB) connectivity to their application.

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Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000™ real-time control MCUs page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the TMDSCNCD28379D or LAUNCHXL-F28379D evaluation board sand download C2000Ware.

To learn more about the C2000 MCUs, visit the C2000 Overview at www.ti.com/c2000.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE
TMS320F28076	PTP (HLQFP, 176)	26mm × 26mm	24mm × 24mm
	PZP (HTQFP, 100)	16mm × 16mm	14mm × 14mm
TMS320F28075	PTP (HLQFP, 176)	26mm × 26mm	24mm × 24mm
	PZP (HTQFP, 100)	16mm × 16mm	14mm × 14mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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3.1 Functional Block Diagram

The Functional Block Diagram shows the CPU system and associated peripherals.

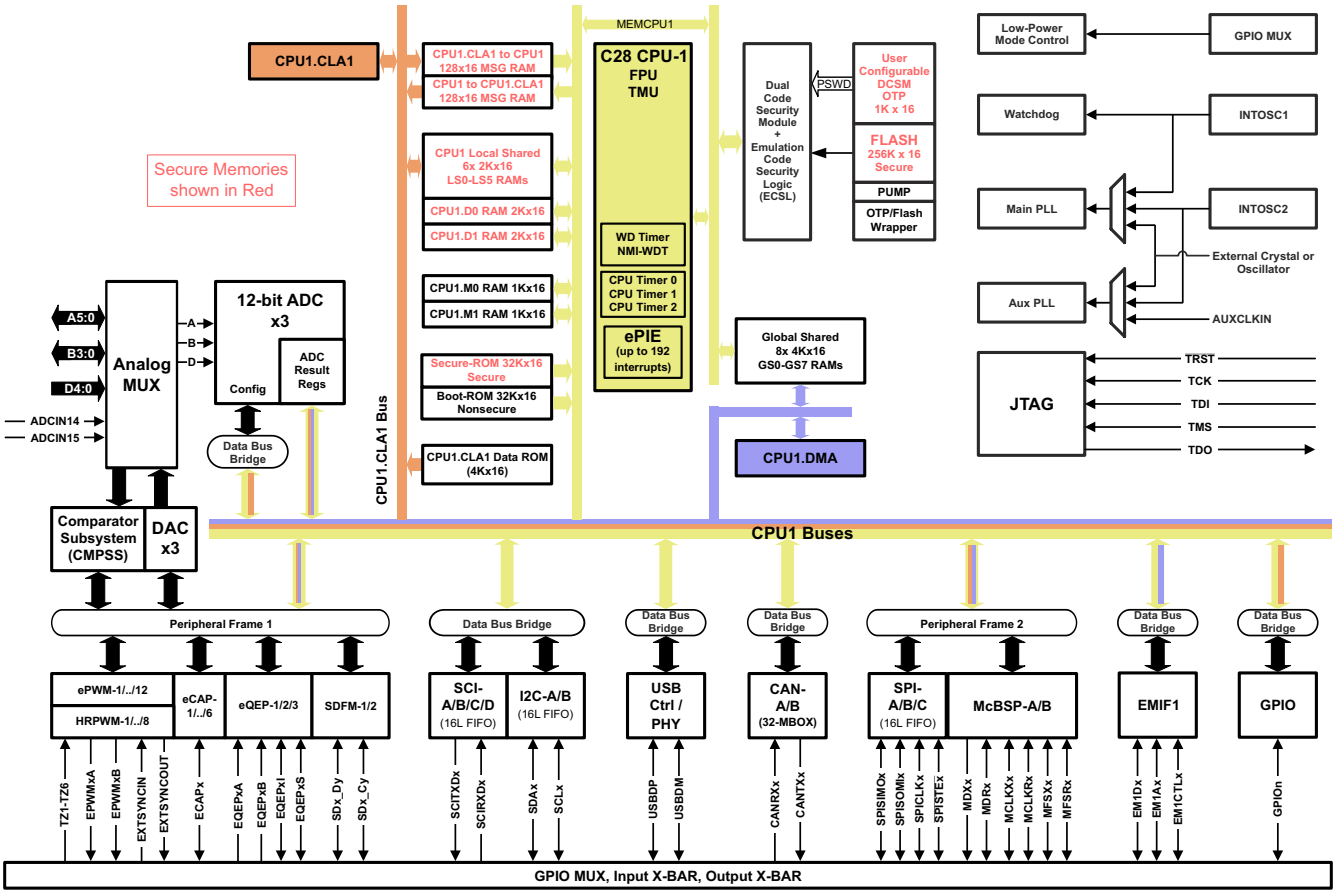


Figure 3-1. Functional Block Diagram

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Table of Contents

1 Features....1
2 Applications....2
3 Description....2
3.1 Functional Block Diagram....4
4 Device Comparison....6
4.1 Related Products....7
5 Pin Configuration and Functions....8
5.1 Pin Diagrams....8
5.2 Signal Descriptions....11
5.3 Pins With Internal Pullup and Pulldown....27
5.4 Pin Multiplexing....28
5.5 Connections for Unused Pins....34
6 Specifications....35
6.1 Absolute Maximum Ratings....35
6.2 ESD Ratings – Commercial....36
6.3 ESD Ratings – Automotive....36
6.4 Recommended Operating Conditions....36
6.5 Power Consumption Summary....37
6.6 Electrical Characteristics....43
6.7 Thermal Resistance Characteristics....44
6.8 Thermal Design Considerations....45
6.9 System....46
6.10 Analog Peripherals....89
6.11 Control Peripherals....114
6.12 Communications Peripherals....134
7 Detailed Description....162
7.1 Overview....162
7.2 Functional Block Diagram....163
7.3 Memory....164
7.4 Identification....171
7.5 Bus Architecture – Peripheral Connectivity....172
7.6 C28x Processor....173
7.7 Control Law Accelerator....174
7.8 Direct Memory Access....175
7.9 Boot ROM and Peripheral Booting....177
7.10 Dual Code Security Module....180
7.11 Timers....181
7.12 Nonmaskable Interrupt With Watchdog Timer (NMIWD)....181
7.13 Watchdog....182
7.14 Configurable Logic Block (CLB)....183
7.15 Functional Safety....185
8 Applications, Implementation, and Layout....187
8.1 Application and Implementation....187
8.2 Key Device Features....187
8.3 Application Information....191
9 Device and Documentation Support....205
9.1 Device and Development Support Tool Nomenclature....205
9.2 Markings....206
9.3 Tools and Software....207
9.4 Documentation Support....209
9.5 Support Resources....210
9.6 Trademarks....210
9.7 Electrostatic Discharge Caution....210
9.8 Glossary....210
10 Revision History....210
11 Mechanical, Packaging, and Orderable Information....213
11.1 Packaging Information....213

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4 Device Comparison

Table 4-1 lists the features of each 2807x device.

Table 4-1. Device Comparison

FEATURE[1]		28076		28075 28075-Q1	
Package Type (PTP is an HLQFP package. PZP is an HTQFP package.)		**176-Pin PTP**	**100-Pin PZP**	**176-Pin PTP**	**100-Pin PZP**
Processor and Accelerators					
C28x	Number	1			
	Frequency (MHz)	120			
	Floating-Point Unit (FPU)	Yes			
	TMU – Type 0	Yes			
CLA – Type 1	Number	1			
	Frequency (MHz)	120			
6-Channel Direct Memory Access (DMA) – Type 0		1			
Memory					
Flash (16-bit words)		512KB (256KW)			
RAM (16-bit words)	Dedicated and Local Shared RAM	36KB (18KW)			
	Global Shared RAM	64KB (32KW)			
	Total RAM	**100KB (50KW)**			
Code security for on-chip flash, RAM, and OTP blocks		Yes			
Boot ROM		Yes			
System					
Configurable Logic Block (CLB)		4 tiles		No	
32-bit CPU timers		3			
Watchdog timers		1			
Nonmaskable Interrupt Watchdog (NMIWD) timers		1			
Crystal oscillator/External clock input		1			
0-pin internal oscillator		2			
I/O pins	GPIO	97	41	97	41
External interrupts		5			
EMIF	EMIF1 (16-bit or 32-bit)	1	–	1	–
Analog Peripherals					
ADC 12-bit mode	MSPS	3.1			
	Conversion Time (ns)[2]	325			
	Input pins	17	14	17	14
Number of 12-bit ADCs		3	2	3	2
Temperature sensor		1			
CMPSS (each CMPSS has two comparators and two internal DACs)		8	4	8	4
Buffered DAC		3			

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Table 4-1. Device Comparison (continued)

FEATURE[1]		28076		28075 28075-Q1	
Package Type (PTP is an HLQFP package. PZP is an HTQFP package.)		**176-Pin PTP**	**100-Pin PZP**	**176-Pin PTP**	**100-Pin PZP**
Control Peripherals [3]					
eCAP inputs – Type 0		6			
ePWM channels – Type 4		24	15	24	15
eQEP modules – Type 0		3	2	3	2
High-resolution ePWM channels – Type 4		16	9	16	9
Sigma-Delta Filter Module (SDFM) channels		8	6	8	6
Communication Peripherals [3]					
Controller Area Network (CAN) – Type 0[4]		2			
Inter-Integrated Circuit (I2C) – Type 0		2			
Multichannel Buffered Serial Port (McBSP) – Type 1		2			
Serial Communications Interface (SCI) – Type 0 (UART Compatible)		4	3	4	3
Serial Peripheral Interface (SPI) – Type 2		3			
Universal Serial Bus (USB) – Type 0		1			
Temperature and Qualification					
Junction Temperature (T_J)	T: –40°C to 105°C	No		Yes	
	S: –40°C to 125°C	Yes			
	Q: –40°C to 150°C[5]	No		Yes	
Free-Air Temperature (T_A)	Q: –40°C to 125°C[5]	No		Yes	

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. For more information, see the *C2000 Real-Time Control Peripherals Reference Guide*.
(2) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
(3) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has less device pins available. The number of peripherals internally present on the device is not reduced compared to the largest package offered within a part number. See Section 5 to identify which peripheral instances are accessible on pins in the smaller package.
(4) The CAN module uses the IP known as *D_CAN*. This document uses the names *CAN* and *D_CAN* interchangeably to reference this peripheral.
(5) The letter Q refers to AEC Q100 qualification for automotive applications.

4.1 Related Products

For information about similar products, see the following links:

TMS320F2807x Microcontrollers

The F2807x series offers the most performance, largest pin counts, flash memory sizes, and peripheral options. The F2807x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

TMS320F28004x Microcontrollers

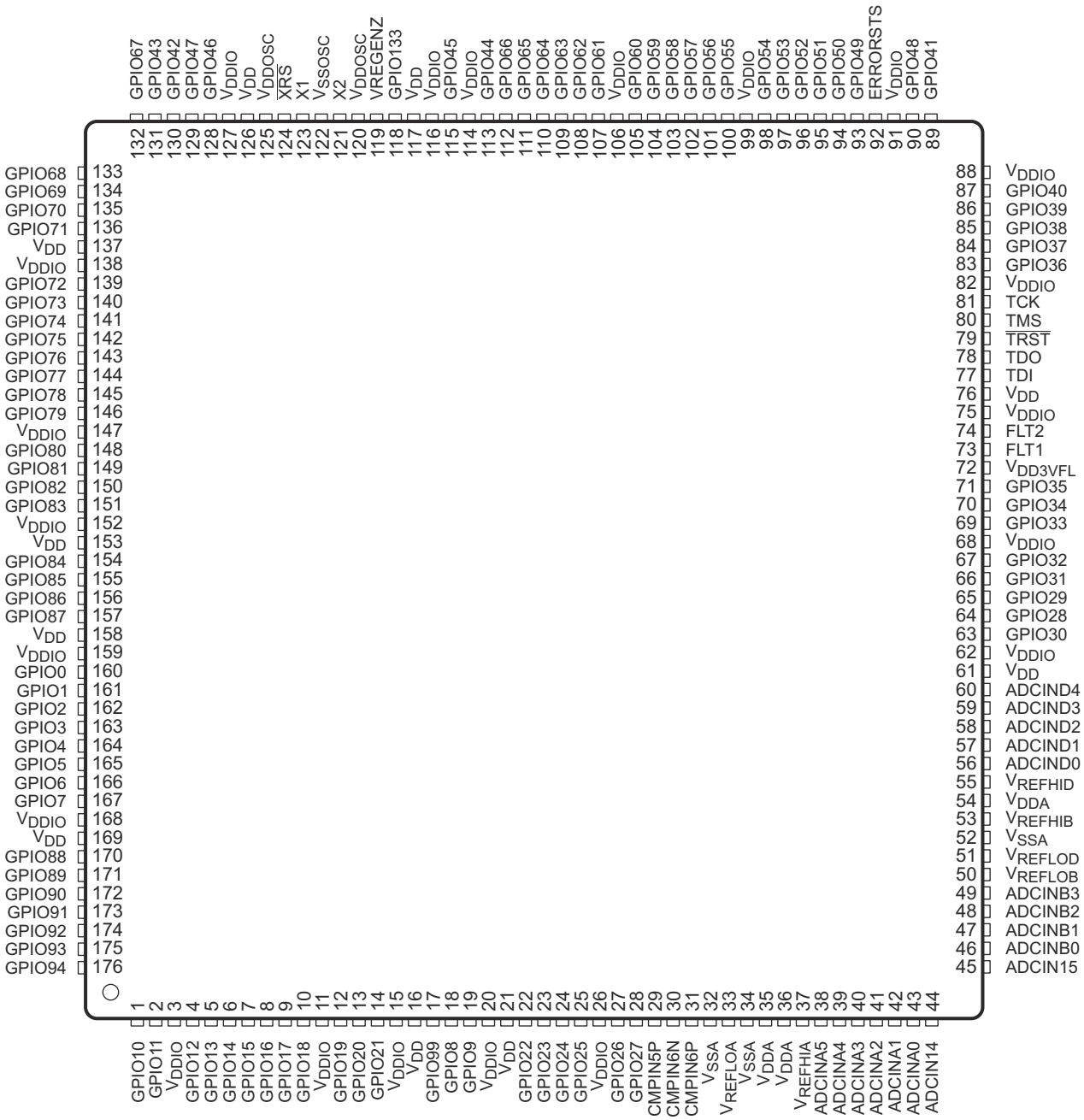
The F28004x series is a reduced version of the F2807x series with the latest generational enhancements. The F28004x series is the best roadmap option for those using the F2806x series. InstaSPIN-FOC and configurable logic block (CLB) versions are available.

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5 Pin Configuration and Functions

5.1 Pin Diagrams

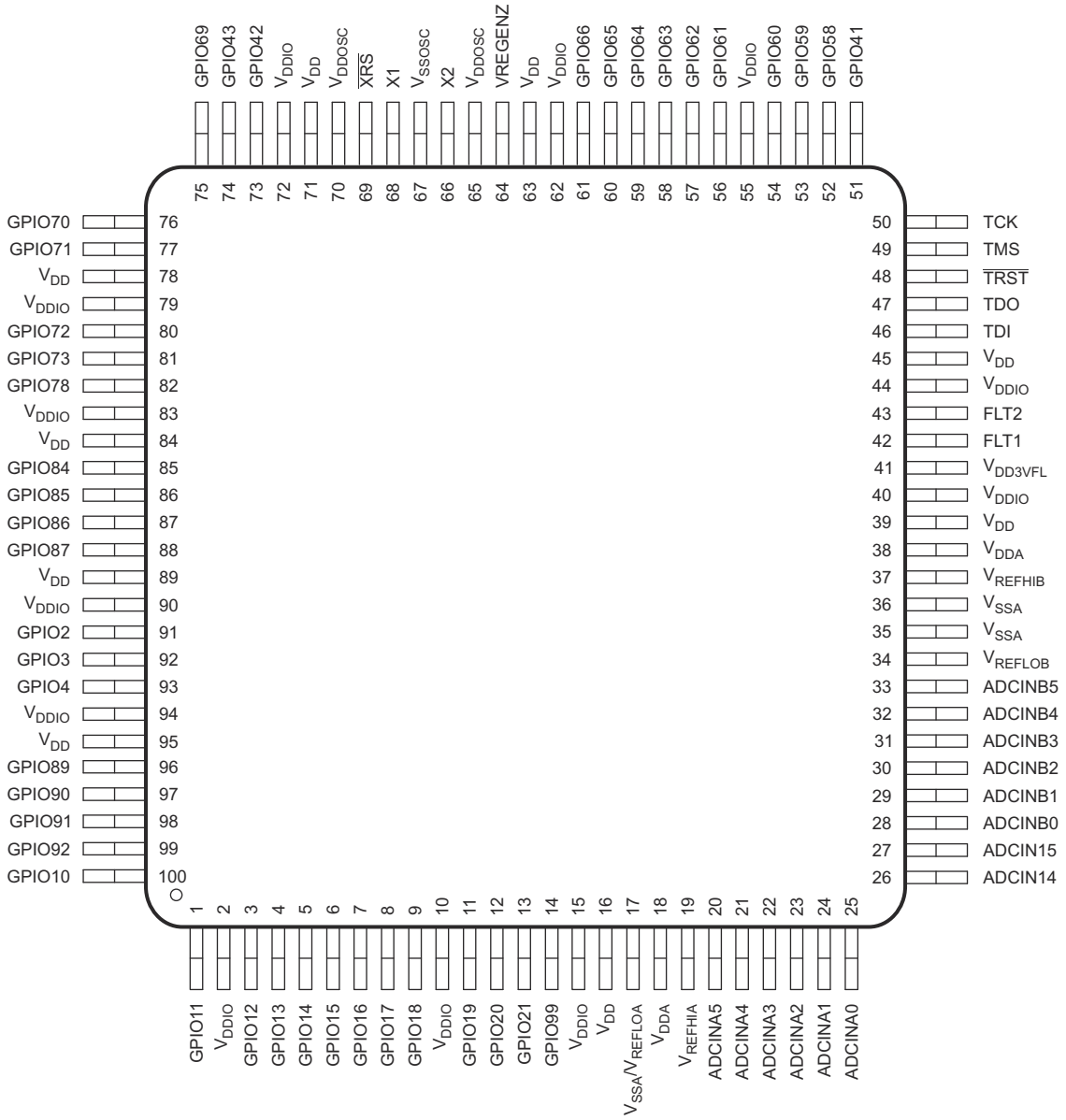
Figure 5-1 shows the pin assignments on the 176-pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack. Figure 5-2 shows the pin assignments on the 100-pin PZP PowerPAD Thermally Enhanced Thin Quad Flatpack.



A. Only the GPIO function is shown on GPIO pins. See Section 5.2.1 for the complete, muxed signal name.

Figure 5-1. 176-Pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack (Top View)

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A. Only the GPIO function is shown on GPIO pins. See Section 5.2.1 for the complete, muxed signal name.

Figure 5-2. 100-Pin PZP PowerPAD HTQFP (Top View)

Note

The exposed lead frame die pad of the PowerPAD™ package serves two functions: to remove heat from the die and to provide ground path for the digital ground (analog ground is provided through dedicated pins). Thus, the PowerPAD should be soldered to the ground (GND) plane of the PCB because this will provide both the digital ground path and good thermal conduction path. To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD. The thermal land should be soldered to the exposed lead frame die pad of the PowerPAD package; the thermal land should be as large as needed to dissipate the required heat. An array of thermal vias should be used to connect the thermal pad to the internal GND plane of the board. See *PowerPAD™ Thermally Enhanced Package* for more details on using the PowerPAD package.

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Note

PCB footprints and schematic symbols are available for download in a vendor-neutral format, which can be exported to the leading EDA CAD/CAE design tools. See the CAD/CAE Symbols section in the product folder for each device, under the Packaging section. These footprints and symbols can also be searched for at https://webench.ti.com/cad/.

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5.2 Signal Descriptions

Section 5.2.1 describes the signals. The GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. See Table 4-1 for details. All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups are not enabled at reset.

5.2.1 Signal Descriptions

Table 5-1. Signal Descriptions

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
ADC, DAC, AND COMPARATOR SIGNALS					
V_{REFHIA}		37	19	I	ADC-A high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the V_{REFHIA} and V_{REFLOA} pins. **NOTE:** Do not load this pin externally.
V_{REFHIB}		53	37	I	ADC-B high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the V_{REFHIB} and V_{REFLOB} pins. **NOTE:** Do not load this pin externally.
V_{REFHID}		55	–	I	ADC-D high reference. This voltage must be driven into the pin from external circuitry. Place at least a 1-µF capacitor on this pin. This capacitor should be placed as close to the device as possible between the V_{REFHID} and V_{REFLOD} pins. **NOTE:** Do not load this pin externally.
V_{REFLOA}		33	17	I	ADC-A low reference. On the PZP package, pin 17 is double-bonded to V_{SSA} and V_{REFLOA}. On the PZP package, pin 17 must be connected to V_{SSA} on the system board.
V_{REFLOB}		50	34	I	ADC-B low reference
V_{REFLOD}		51	–	I	ADC-D low reference
ADCIN14		44	26	I	Input 14 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together from an external reference.
CMPIN4P				I	Comparator 4 positive input
ADCIN15		45	27	I	Input 15 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together from an external reference.
CMPIN4N				I	Comparator 4 negative input
ADCINA0		43	25	I	ADC-A input 0. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTA				O	DAC-A output
ADCINA1		42	24	I	ADC-A input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTB				O	DAC-B output
ADCINA2		41	23	I	ADC-A input 2
CMPIN1P				I	Comparator 1 positive input
ADCINA3		40	22	I	ADC-A input 3
CMPIN1N				I	Comparator 1 negative input

Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
ADCINA4		39	21	I	ADC-A input 4
CMPIN2P				I	Comparator 2 positive input
ADCINA5		38	20	I	ADC-A input 5
CMPIN2N				I	Comparator 2 negative input
ADCINB0		46	28	I	ADC-B input 0. There is a 100-pF capacitor to V_{SSA} on this pin in both ADC input or DAC reference mode which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin.
VDAC				I	Optional external reference voltage for on-chip DACs. There is a 100-pF capacitor to V_{SSA} on this pin in both ADC input or DAC reference mode which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin.
ADCINB1		47	29	I	ADC-B input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTC				O	DAC-C output
ADCINB2		48	30	I	ADC-B input 2
CMPIN3P				I	Comparator 3 positive input
ADCINB3		49	31	I	ADC-B input 3
CMPIN3N				I	Comparator 3 negative input
ADCINB4		–	32	I	ADC-B input 4
ADCINB5		–	33	I	ADC-B input 5
CMPIN6P		31	–	I	Comparator 6 positive input
CMPIN6N		30	–	I	Comparator 6 negative input
CMPIN5P		29	–	I	Comparator 5 positive input
ADCIND0		56	–	I	ADC-D input 0
CMPIN7P				I	Comparator 7 positive input
ADCIND1		57	–	I	ADC-D input 1
CMPIN7N				I	Comparator 7 negative input
ADCIND2		58	–	I	ADC-D input 2
CMPIN8P				I	Comparator 8 positive input
ADCIND3		59	–	I	ADC-D input 3
CMPIN8N				I	Comparator 8 negative input
ADCIND4		60	–	I	ADC-D input 4
GPIO AND PERIPHERAL SIGNALS					
GPIO0	0, 4, 8, 12	160	–	I/O	General-purpose input/output 0
EPWM1A	1			O	Enhanced PWM1 output A (HRPWM-capable)
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
GPIO1	0, 4, 8, 12	161	–	I/O	General-purpose input/output 1
EPWM1B	1			O	Enhanced PWM1 output B (HRPWM-capable)
MFSRB	3			I/O	McBSP-B receive frame synch
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO2	0, 4, 8, 12	162	91	I/O	General-purpose input/output 2
EPWM2A	1			O	Enhanced PWM2 output A (HRPWM-capable)
OUTPUTXBAR1	5			O	Output 1 of the output XBAR
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
GPIO3	0, 4, 8, 12	163	92	I/O	General-purpose input/output 3
EPWM2B	1			O	Enhanced PWM2 output B (HRPWM-capable)
OUTPUTXBAR2	2			O	Output 2 of the output XBAR
MCLKRB	3			I/O	McBSP-B receive clock
OUTPUTXBAR2	5			O	Output 2 of the output XBAR
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO4	0, 4, 8, 12	164	93	I/O	General-purpose input/output 4
EPWM3A	1			O	Enhanced PWM3 output A (HRPWM-capable)
OUTPUTXBAR3	5			O	Output 3 of the output XBAR
CANTXA	6			O	CAN-A transmit
GPIO5	0, 4, 8, 12	165	–	I/O	General-purpose input/output 5
EPWM3B	1			O	Enhanced PWM3 output B (HRPWM-capable)
MFSRA	2			I/O	McBSP-A receive frame synch
OUTPUTXBAR3	3			O	Output 3 of the output XBAR
CANRXA	6			I	CAN-A receive
GPIO6	0, 4, 8, 12	166	–	I/O	General-purpose input/output 6
EPWM4A	1			O	Enhanced PWM4 output A (HRPWM-capable)
OUTPUTXBAR4	2			O	Output 4 of the output XBAR
EXTSYNCOUT	3			O	External ePWM synch pulse output
EQEP3A	5			I	Enhanced QEP3 input A
CANTXB	6			O	CAN-B transmit
GPIO7	0, 4, 8, 12	167	–	I/O	General-purpose input/output 7
EPWM4B	1			O	Enhanced PWM4 output B (HRPWM-capable)
MCLKRA	2			I/O	McBSP-A receive clock
OUTPUTXBAR5	3			O	Output 5 of the output XBAR
EQEP3B	5			I	Enhanced QEP3 input B
CANRXB	6			I	CAN-B receive
GPIO8	0, 4, 8, 12	18	–	I/O	General-purpose input/output 8
EPWM5A	1			O	Enhanced PWM5 output A (HRPWM-capable)
CANTXB	2			O	CAN-B transmit
ADCSOCAO	3			O	ADC start-of-conversion A output for external ADC
EQEP3S	5			I/O	Enhanced QEP3 strobe
SCITXDA	6			O	SCI-A transmit data
GPIO9	0, 4, 8, 12	19	–	I/O	General-purpose input/output 9
EPWM5B	1			O	Enhanced PWM5 output B (HRPWM-capable)
SCITXDB	2			O	SCI-B transmit data
OUTPUTXBAR6	3			O	Output 6 of the output XBAR
EQEP3I	5			I/O	Enhanced QEP3 index
SCIRXDA	6			I	SCI-A receive data

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO10	0, 4, 8, 12	1	100	I/O	General-purpose input/output 10
EPWM6A	1			O	Enhanced PWM6 output A (HRPWM-capable)
CANRXB	2			I	CAN-B receive
ADCSOCBO	3			O	ADC start-of-conversion B output for external ADC
EQEP1A	5			I	Enhanced QEP1 input A
SCITXDB	6			O	SCI-B transmit data
GPIO11	0, 4, 8, 12	2	1	I/O	General-purpose input/output 11
EPWM6B	1			O	Enhanced PWM6 output B (HRPWM-capable)
SCIRXDB	2, 6			I	SCI-B receive data
OUTPUTXBAR7	3			O	Output 7 of the output XBAR
EQEP1B	5			I	Enhanced QEP1 input B
GPIO12	0, 4, 8, 12	4	3	I/O	General-purpose input/output 12
EPWM7A	1			O	Enhanced PWM7 output A (HRPWM-capable)
CANTXB	2			O	CAN-B transmit
MDXB	3			O	McBSP-B transmit serial data
EQEP1S	5			I/O	Enhanced QEP1 strobe
SCITXDC	6			O	SCI-C transmit data
GPIO13	0, 4, 8, 12	5	4	I/O	General-purpose input/output 13
EPWM7B	1			O	Enhanced PWM7 output B (HRPWM-capable)
CANRXB	2			I	CAN-B receive
MDRB	3			I	McBSP-B receive serial data
EQEP1I	5			I/O	Enhanced QEP1 index
SCIRXDC	6			I	SCI-C receive data
GPIO14	0, 4, 8, 12	6	5	I/O	General-purpose input/output 14
EPWM8A	1			O	Enhanced PWM8 output A (HRPWM-capable)
SCITXDB	2			O	SCI-B transmit data
MCLKXB	3			I/O	McBSP-B transmit clock
OUTPUTXBAR3	6			O	Output 3 of the output XBAR
GPIO15	0, 4, 8, 12	7	6	I/O	General-purpose input/output 15
EPWM8B	1			O	Enhanced PWM8 output B (HRPWM-capable)
SCIRXDB	2			I	SCI-B receive data
MFSXB	3			I/O	McBSP-B transmit frame synch
OUTPUTXBAR4	6			O	Output 4 of the output XBAR
GPIO16	0, 4, 8, 12	8	7	I/O	General-purpose input/output 16
SPISIMOA	1			I/O	SPI-A slave in, master out
CANTXB	2			O	CAN-B transmit
OUTPUTXBAR7	3			O	Output 7 of the output XBAR
EPWM9A	5			O	Enhanced PWM9 output A
SD1_D1	7			I	Sigma-Delta 1 channel 1 data input

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO17	0, 4, 8, 12	9	8	I/O	General-purpose input/output 17
SPISOMIA	1			I/O	SPI-A slave out, master in
CANRXB	2			I	CAN-B receive
OUTPUTXBAR8	3			O	Output 8 of the output XBAR
EPWM9B	5			O	Enhanced PWM9 output B
SD1_C1	7			I	Sigma-Delta 1 channel 1 clock input
GPIO18	0, 4, 8, 12	10	9	I/O	General-purpose input/output 18
SPICLKA	1			I/O	SPI-A clock
SCITXDB	2			O	SCI-B transmit data
CANRXA	3			I	CAN-A receive
EPWM10A	5			O	Enhanced PWM10 output A
SD1_D2	7			I	Sigma-Delta 1 channel 2 data input
GPIO19	0, 4, 8, 12	12	11	I/O	General-purpose input/output 19
$\overline{\text{SPISTEA}}$	1			I/O	SPI-A slave transmit enable
SCIRXDB	2			I	SCI-B receive data
CANTXA	3			O	CAN-A transmit
EPWM10B	5			O	Enhanced PWM10 output B
SD1_C2	7			I	Sigma-Delta 1 channel 2 clock input
GPIO20	0, 4, 8, 12	13	12	I/O	General-purpose input/output 20
EQEP1A	1			I	Enhanced QEP1 input A
MDXA	2			O	McBSP-A transmit serial data
CANTXB	3			O	CAN-B transmit
EPWM11A	5			O	Enhanced PWM11 output A
SD1_D3	7			I	Sigma-Delta 1 channel 3 data input
GPIO21	0, 4, 8, 12	14	13	I/O	General-purpose input/output 21
EQEP1B	1			I	Enhanced QEP1 input B
MDRA	2			I	McBSP-A receive serial data
CANRXB	3			I	CAN-B receive
EPWM11B	5			O	Enhanced PWM11 output B
SD1_C3	7			I	Sigma-Delta 1 channel 3 clock input
GPIO22	0, 4, 8, 12	22	–	I/O	General-purpose input/output 22
EQEP1S	1			I/O	Enhanced QEP1 strobe
MCLKXA	2			I/O	McBSP-A transmit clock
SCITXDB	3			O	SCI-B transmit data
EPWM12A	5			O	Enhanced PWM12 output A
SPICLKB	6			I/O	SPI-B clock
SD1_D4	7			I	Sigma-Delta 1 channel 4 data input
GPIO23	0, 4, 8, 12	23	–	I/O	General-purpose input/output 23
EQEP1I	1			I/O	Enhanced QEP1 index
MFSXA	2			I/O	McBSP-A transmit frame synch
SCIRXDB	3			I	SCI-B receive data
EPWM12B	5			O	Enhanced PWM12 output B
$\overline{\text{SPISTEB}}$	6			I/O	SPI-B slave transmit enable
SD1_C4	7			I	Sigma-Delta 1 channel 4 clock input

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO24	0, 4, 8, 12	24	–	I/O	General-purpose input/output 24
OUTPUTXBAR1	1			O	Output 1 of the output XBAR
EQEP2A	2			I	Enhanced QEP2 input A
MDXB	3			O	McBSP-B transmit serial data
SPISIMOB	6			I/O	SPI-B slave in, master out
SD2_D1	7			I	Sigma-Delta 2 channel 1 data input
GPIO25	0, 4, 8, 12	25	–	I/O	General-purpose input/output 25
OUTPUTXBAR2	1			O	Output 2 of the output XBAR
EQEP2B	2			I	Enhanced QEP2 input B
MDRB	3			I	McBSP-B receive serial data
SPISOMIB	6			I/O	SPI-B slave out, master in
SD2_C1	7			I	Sigma-Delta 2 channel 1 clock input
GPIO26	0, 4, 8, 12	27	–	I/O	General-purpose input/output 26
OUTPUTXBAR3	1			O	Output 3 of the output XBAR
EQEP2I	2			I/O	Enhanced QEP2 index
MCLKXB	3			I/O	McBSP-B transmit clock
OUTPUTXBAR3	5			O	Output 3 of the output XBAR
SPICLKB	6			I/O	SPI-B clock
SD2_D2	7			I	Sigma-Delta 2 channel 2 data input
GPIO27	0, 4, 8, 12	28	–	I/O	General-purpose input/output 27
OUTPUTXBAR4	1			O	Output 4 of the output XBAR
EQEP2S	2			I/O	Enhanced QEP2 strobe
MFSXB	3			I/O	McBSP-B transmit frame synch
OUTPUTXBAR4	5			O	Output 4 of the output XBAR
$\overline{\text{SPISTEB}}$	6			I/O	SPI-B slave transmit enable
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input
GPIO28	0, 4, 8, 12	64	–	I/O	General-purpose input/output 28
SCIRXDA	1			I	SCI-A receive data
$\overline{\text{EM1CS4}}$	2			O	External memory interface 1 chip select 4
OUTPUTXBAR5	5			O	Output 5 of the output XBAR
EQEP3A	6			I	Enhanced QEP3 input A
SD2_D3	7			I	Sigma-Delta 2 channel 3 data input
GPIO29	0, 4, 8, 12	65	–	I/O	General-purpose input/output 29
SCITXDA	1			O	SCI-A transmit data
EM1SDCKE	2			O	External memory interface 1 SDRAM clock enable
OUTPUTXBAR6	5			O	Output 6 of the output XBAR
EQEP3B	6			I	Enhanced QEP3 input B
SD2_C3	7			I	Sigma-Delta 2 channel 3 clock input
GPIO30	0, 4, 8, 12	63	–	I/O	General-purpose input/output 30
CANRXA	1			I	CAN-A receive
EM1CLK	2			O	External memory interface 1 clock
OUTPUTXBAR7	5			O	Output 7 of the output XBAR
EQEP3S	6			I/O	Enhanced QEP3 strobe
SD2_D4	7			I	Sigma-Delta 2 channel 4 data input

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO31	0, 4, 8, 12	66	–	I/O	General-purpose input/output 31
CANTXA	1			O	CAN-A transmit
$\overline{\text{EM1WE}}$	2			O	External memory interface 1 write enable
OUTPUTXBAR8	5			O	Output 8 of the output XBAR
EQEP3I	6			I/O	Enhanced QEP3 index
SD2_C4	7			I	Sigma-Delta 2 channel 4 clock input
GPIO32	0, 4, 8, 12	67	–	I/O	General-purpose input/output 32
SDAA	1			I/OD	I2C-A data open-drain bidirectional port
$\overline{\text{EM1CS0}}$	2			O	External memory interface 1 chip select 0
GPIO33	0, 4, 8, 12	69	–	I/O	General-purpose input/output 33
SCLA	1			I/OD	I2C-A clock open-drain bidirectional port
EM1RNW	2			O	External memory interface 1 read not write
GPIO34	0, 4, 8, 12	70	–	I/O	General-purpose input/output 34
OUTPUTXBAR1	1			O	Output 1 of the output XBAR
$\overline{\text{EM1CS2}}$	2			O	External memory interface 1 chip select 2
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
GPIO35	0, 4, 8, 12	71	–	I/O	General-purpose input/output 35
SCIRXDA	1			I	SCI-A receive data
$\overline{\text{EM1CS3}}$	2			O	External memory interface 1 chip select 3
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO36	0, 4, 8, 12	83	–	I/O	General-purpose input/output 36
SCITXDA	1			O	SCI-A transmit data
EM1WAIT	2			I	External memory interface 1 Asynchronous SRAM WAIT
CANRXA	6			I	CAN-A receive
GPIO37	0, 4, 8, 12	84	–	I/O	General-purpose input/output 37
OUTPUTXBAR2	1			O	Output 2 of the output XBAR
$\overline{\text{EM1OE}}$	2			O	External memory interface 1 output enable
CANTXA	6			O	CAN-A transmit
GPIO38	0, 4, 8, 12	85	–	I/O	General-purpose input/output 38
EM1A0	2			O	External memory interface 1 address line 0
SCITXDC	5			O	SCI-C transmit data
CANTXB	6			O	CAN-B transmit
GPIO39	0, 4, 8, 12	86	–	I/O	General-purpose input/output 39
EM1A1	2			O	External memory interface 1 address line 1
SCIRXDC	5			I	SCI-C receive data
CANRXB	6			I	CAN-B receive
GPIO40	0, 4, 8, 12	87	–	I/O	General-purpose input/output 40
EM1A2	2			O	External memory interface 1 address line 2
SDAB	6			I/OD	I2C-B data open-drain bidirectional port

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO41	0, 4, 8, 12	89	51	I/O	General-purpose input/output 41. For applications using the Hibernate low-power mode, this pin serves as the GPIOHIBWAKE signal. For details, see the Low Power Modes section of the System Control chapter in the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.
EM1A3	2			O	External memory interface 1 address line 3
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
GPIO42	0, 4, 8, 12	130	73	I/O	General-purpose input/output 42
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
SCITXDA	15			O	SCI-A transmit data
USB0DM	Analog			I/O	USB PHY differential data
GPIO43	0, 4, 8, 12	131	74	I/O	General-purpose input/output 43
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port
SCIRXDA	15			I	SCI-A receive data
USB0DP	Analog			I/O	USB PHY differential data
GPIO44	0, 4, 8, 12	113	–	I/O	General-purpose input/output 44
EM1A4	2			O	External memory interface 1 address line 4
GPIO45	0, 4, 8, 12	115	–	I/O	General-purpose input/output 45
EM1A5	2			O	External memory interface 1 address line 5
GPIO46	0, 4, 8, 12	128	–	I/O	General-purpose input/output 46
EM1A6	2			O	External memory interface 1 address line 6
SCIRXDD	6			I	SCI-D receive data
GPIO47	0, 4, 8, 12	129	–	I/O	General-purpose input/output 47
EM1A7	2			O	External memory interface 1 address line 7
SCITXDD	6			O	SCI-D transmit data
GPIO48	0, 4, 8, 12	90	–	I/O	General-purpose input/output 48
OUTPUTXBAR3	1			O	Output 3 of the output XBAR
EM1A8	2			O	External memory interface 1 address line 8
SCITXDA	6			O	SCI-A transmit data
SD1_D1	7			I	Sigma-Delta 1 channel 1 data input
GPIO49	0, 4, 8, 12	93	–	I/O	General-purpose input/output 49
OUTPUTXBAR4	1			O	Output 4 of the output XBAR
EM1A9	2			O	External memory interface 1 address line 9
SCIRXDA	6			I	SCI-A receive data
SD1_C1	7			I	Sigma-Delta 1 channel 1 clock input
GPIO50	0, 4, 8, 12	94	–	I/O	General-purpose input/output 50
EQEP1A	1			I	Enhanced QEP1 input A
EM1A10	2			O	External memory interface 1 address line 10
SPISIMOC	6			I/O	SPI-C slave in, master out
SD1_D2	7			I	Sigma-Delta 1 channel 2 data input
GPIO51	0, 4, 8, 12	95	–	I/O	General-purpose input/output 51
EQEP1B	1			I	Enhanced QEP1 input B
EM1A11	2			O	External memory interface 1 address line 11
SPISOMIC	6			I/O	SPI-C slave out, master in
SD1_C2	7			I	Sigma-Delta 1 channel 2 clock input

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO52	0, 4, 8, 12	96	–	I/O	General-purpose input/output 52
EQEP1S	1			I/O	Enhanced QEP1 strobe
EM1A12	2			O	External memory interface 1 address line 12
SPICLKC	6			I/O	SPI-C clock
SD1_D3	7			I	Sigma-Delta 1 channel 3 data input
GPIO53	0, 4, 8, 12	97	–	I/O	General-purpose input/output 53
EQEP1I	1			I/O	Enhanced QEP1 index
EM1D31	2			I/O	External memory interface 1 data line 31
$\overline{\text{SPISTEC}}$	6			I/O	SPI-C slave transmit enable
SD1_C3	7			I	Sigma-Delta 1 channel 3 clock input
GPIO54	0, 4, 8, 12	98	–	I/O	General-purpose input/output 54
SPISIMOA	1			I/O	SPI-A slave in, master out
EM1D30	2			I/O	External memory interface 1 data line 30
EQEP2A	5			I	Enhanced QEP2 input A
SCITXDB	6			O	SCI-B transmit data
SD1_D4	7			I	Sigma-Delta 1 channel 4 data input
GPIO55	0, 4, 8, 12	100	–	I/O	General-purpose input/output 55
SPISOMIA	1			I/O	SPI-A slave out, master in
EM1D29	2			I/O	External memory interface 1 data line 29
EQEP2B	5			I	Enhanced QEP2 input B
SCIRXDB	6			I	SCI-B receive data
SD1_C4	7			I	Sigma-Delta 1 channel 4 clock input
GPIO56	0, 4, 8, 12	101	–	I/O	General-purpose input/output 56
SPICLKA	1			I/O	SPI-A clock
EM1D28	2			I/O	External memory interface 1 data line 28
EQEP2S	5			I/O	Enhanced QEP2 strobe
SCITXDC	6			O	SCI-C transmit data
SD2_D1	7			I	Sigma-Delta 2 channel 1 data input
GPIO57	0, 4, 8, 12	102	–	I/O	General-purpose input/output 57
$\overline{\text{SPISTEA}}$	1			I/O	SPI-A slave transmit enable
EM1D27	2			I/O	External memory interface 1 data line 27
EQEP2I	5			I/O	Enhanced QEP2 index
SCIRXDC	6			I	SCI-C receive data
SD2_C1	7			I	Sigma-Delta 2 channel 1 clock input
GPIO58	0, 4, 8, 12	103	52	I/O	General-purpose input/output 58
MCLKRA	1			I/O	McBSP-A receive clock
EM1D26	2			I/O	External memory interface 1 data line 26
OUTPUTXBAR1	5			O	Output 1 of the output XBAR
SPICLKB	6			I/O	SPI-B clock
SD2_D2	7			I	Sigma-Delta 2 channel 2 data input
SPISIMOA	15			I/O	SPI-A slave in, master out[2]

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO59	0, 4, 8, 12			I/O	General-purpose input/output 59[3]
MFSRA	1			I/O	McBSP-A receive frame synch
EM1D25	2			I/O	External memory interface 1 data line 25
OUTPUTXBAR2	5	104	53	O	Output 2 of the output XBAR
SPISTEB	6			I/O	SPI-B slave transmit enable
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input
SPISOMIA	15			I/O	SPI-A slave out, master in[2]
GPIO60	0, 4, 8, 12			I/O	General-purpose input/output 60
MCLKRB	1			I/O	McBSP-B receive clock
EM1D24	2			I/O	External memory interface 1 data line 24
OUTPUTXBAR3	5	105	54	O	Output 3 of the output XBAR
SPISIMOB	6			I/O	SPI-B slave in, master out
SD2_D3	7			I	Sigma-Delta 2 channel 3 data input
SPICLKA	15			I/O	SPI-A clock[2]
GPIO61	0, 4, 8, 12			I/O	General-purpose input/output 61[3]
MFSRB	1			I/O	McBSP-B receive frame synch
EM1D23	2			I/O	External memory interface 1 data line 23
OUTPUTXBAR4	5	107	56	O	Output 4 of the output XBAR
SPISOMIB	6			I/O	SPI-B slave out, master in
SD2_C3	7			I	Sigma-Delta 2 channel 3 clock input
SPISTEA	15			I/O	SPI-A slave transmit enable[2]
GPIO62	0, 4, 8, 12			I/O	General-purpose input/output 62
SCIRXDC	1			I	SCI-C receive data
EM1D22	2	108	57	I/O	External memory interface 1 data line 22
EQEP3A	5			I	Enhanced QEP3 input A
CANRXA	6			I	CAN-A receive
SD2_D4	7			I	Sigma-Delta 2 channel 4 data input
GPIO63	0, 4, 8, 12			I/O	General-purpose input/output 63
SCITXDC	1			O	SCI-C transmit data
EM1D21	2			I/O	External memory interface 1 data line 21
EQEP3B	5	109	58	I	Enhanced QEP3 input B
CANTXA	6			O	CAN-A transmit
SD2_C4	7			I	Sigma-Delta 2 channel 4 clock input
SPISIMOB	15			I/O	SPI-B slave in, master out[2]
GPIO64	0, 4, 8, 12			I/O	General-purpose input/output 64[3]
EM1D20	2			I/O	External memory interface 1 data line 20
EQEP3S	5	110	59	I/O	Enhanced QEP3 strobe
SCIRXDA	6			I	SCI-A receive data
SPISOMIB	15			I/O	SPI-B slave out, master in[2]
GPIO65	0, 4, 8, 12			I/O	General-purpose input/output 65
EM1D19	2			I/O	External memory interface 1 data line 19
EQEP3I	5	111	60	I/O	Enhanced QEP3 index
SCITXDA	6			O	SCI-A transmit data
SPICLKB	15			I/O	SPI-B clock[2]

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO66	0, 4, 8, 12	112	61	I/O	General-purpose input/output 66[3]
EM1D18	2			I/O	External memory interface 1 data line 18
SDAB	6			I/OD	I2C-B data open-drain bidirectional port
$\overline{\text{SPISTEB}}$	15			I/O	SPI-B slave transmit enable[2]
GPIO67	0, 4, 8, 12	132	–	I/O	General-purpose input/output 67
EM1D17	2			I/O	External memory interface 1 data line 17
GPIO68	0, 4, 8, 12	133	–	I/O	General-purpose input/output 68
EM1D16	2			I/O	External memory interface 1 data line 16
GPIO69	0, 4, 8, 12	134	75	I/O	General-purpose input/output 69
EM1D15	2			I/O	External memory interface 1 data line 15
SCLB	6			I/OD	I2C-B clock open-drain bidirectional port
SPISIMOC	15			I/O	SPI-C slave in, master out[2]
GPIO70	0, 4, 8, 12	135	76	I/O	General-purpose input/output 70[3]
EM1D14	2			I/O	External memory interface 1 data line 14
CANRXA	5			I	CAN-A receive
SCITXDB	6			O	SCI-B transmit data
SPISOMIC	15			I/O	SPI-C slave out, master in[2]
GPIO71	0, 4, 8, 12	136	77	I/O	General-purpose input/output 71
EM1D13	2			I/O	External memory interface 1 data line 13
CANTXA	5			O	CAN-A transmit
SCIRXDB	6			I	SCI-B receive data
SPICLKC	15			I/O	SPI-C clock[2]
GPIO72	0, 4, 8, 12	139	80	I/O	General-purpose input/output 72.[3] This is the factory default boot mode select pin 1.
EM1D12	2			I/O	External memory interface 1 data line 12
CANTXB	5			O	CAN-B transmit
SCITXDC	6			O	SCI-C transmit data
$\overline{\text{SPISTEC}}$	15			I/O	SPI-C slave transmit enable[2]
GPIO73	0, 4, 8, 12	140	81	I/O	General-purpose input/output 73
EM1D11	2			I/O	External memory interface 1 data line 11
XCLKOUT	3			O/Z	External clock output. This pin outputs a divided-down version of a chosen clock signal from within the device. The clock signal is chosen using the CLKSRCCTL3.XCLKOUTSEL bit field while the divide ratio is chosen using the XCLKOUTDIVSEL.XCLKOUTDIV bit field.
CANRXB	5			I	CAN-B receive
SCIRXDC	6			I	SCI-C receive
GPIO74	0, 4, 8, 12	141	–	I/O	General-purpose input/output 74
EM1D10	2			I/O	External memory interface 1 data line 10
GPIO75	0, 4, 8, 12	142	–	I/O	General-purpose input/output 75
EM1D9	2			I/O	External memory interface 1 data line 9
GPIO76	0, 4, 8, 12	143	–	I/O	General-purpose input/output 76
EM1D8	2			I/O	External memory interface 1 data line 8
SCITXDD	6			O	SCI-D transmit data

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO77	0, 4, 8, 12	144	–	I/O	General-purpose input/output 77
EM1D7	2			I/O	External memory interface 1 data line 7
SCIRXDD	6			I	SCI-D receive data
GPIO78	0, 4, 8, 12	145	82	I/O	General-purpose input/output 78
EM1D6	2			I/O	External memory interface 1 data line 6
EQEP2A	6			I	Enhanced QEP2 input A
GPIO79	0, 4, 8, 12	146	–	I/O	General-purpose input/output 79
EM1D5	2			I/O	External memory interface 1 data line 5
EQEP2B	6			I	Enhanced QEP2 input B
GPIO80	0, 4, 8, 12	148	–	I/O	General-purpose input/output 80
EM1D4	2			I/O	External memory interface 1 data line 4
EQEP2S	6			I/O	Enhanced QEP2 strobe
GPIO81	0, 4, 8, 12	149	–	I/O	General-purpose input/output 81
EM1D3	2			I/O	External memory interface 1 data line 3
EQEP2I	6			I/O	Enhanced QEP2 index
GPIO82	0, 4, 8, 12	150	–	I/O	General-purpose input/output 82
EM1D2	2			I/O	External memory interface 1 data line 2
GPIO83	0, 4, 8, 12	151	–	I/O	General-purpose input/output 83
EM1D1	2			I/O	External memory interface 1 data line 1
GPIO84	0, 4, 8, 12	154	85	I/O	General-purpose input/output 84. This is the factory default boot mode select pin 0.
SCITXDA	5			O	SCI-A transmit data
MDXB	6			O	McBSP-B transmit serial data
MDXA	15			O	McBSP-A transmit serial data
GPIO85	0, 4, 8, 12	155	86	I/O	General-purpose input/output 85
EM1D0	2			I/O	External memory interface 1 data line 0
SCIRXDA	5			I	SCI-A receive data
MDRB	6			I	McBSP-B receive serial data
MDRA	15			I	McBSP-A receive serial data
GPIO86	0, 4, 8, 12	156	87	I/O	General-purpose input/output 86
EM1A13	2			O	External memory interface 1 address line 13
EM1CAS	3			O	External memory interface 1 column address strobe
SCITXDB	5			O	SCI-B transmit data
MCLKXB	6			I/O	McBSP-B transmit clock
MCLKXA	15			I/O	McBSP-A transmit clock
GPIO87	0, 4, 8, 12	157	88	I/O	General-purpose input/output 87
EM1A14	2			O	External memory interface 1 address line 14
EM1RAS	3			O	External memory interface 1 row address strobe
SCIRXDB	5			I	SCI-B receive data
MFSXB	6			I/O	McBSP-B transmit frame synch
MFSXA	15			I/O	McBSP-A transmit frame synch
GPIO88	0, 4, 8, 12	170	–	I/O	General-purpose input/output 88
EM1A15	2			O	External memory interface 1 address line 15
EM1DQM0	3			O	External memory interface 1 Input/output mask for byte 0

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
GPIO89	0, 4, 8, 12	171	96	I/O	General-purpose input/output 89
EM1A16	2			O	External memory interface 1 address line 16
EM1DQM1	3			O	External memory interface 1 Input/output mask for byte 1
SCITXDC	6			O	SCI-C transmit data
GPIO90	0, 4, 8, 12	172	97	I/O	General-purpose input/output 90
EM1A17	2			O	External memory interface 1 address line 17
EM1DQM2	3			O	External memory interface 1 Input/output mask for byte 2
SCIRXDC	6			I	SCI-C receive data
GPIO91	0, 4, 8, 12	173	98	I/O	General-purpose input/output 91
EM1A18	2			O	External memory interface 1 address line 18
EM1DQM3	3			O	External memory interface 1 Input/output mask for byte 3
SDAA	6			I/OD	I2C-A data open-drain bidirectional port
GPIO92	0, 4, 8, 12	174	99	I/O	General-purpose input/output 92
EM1A19	2			O	External memory interface 1 address line 19
EM1BA1	3			O	External memory interface 1 bank address 1
SCLA	6			I/OD	I2C-A clock open-drain bidirectional port
GPIO93	0, 4, 8, 12	175	–	I/O	General-purpose input/output 93
EM1BA0	3			O	External memory interface 1 bank address 0
SCITXDD	6			O	SCI-D transmit data
GPIO94	0, 4, 8, 12	176	–	I/O	General-purpose input/output 94
SCIRXDD	6			I	SCI-D receive data
GPIO99	0, 4, 8, 12	17	14	I/O	General-purpose input/output 99
EQEP1I	5			I/O	Enhanced QEP1 index
GPIO133/AUXCLKIN	0, 4, 8, 12	118	–	I/O	General-purpose input/output 133. The AUXCLKIN function of this GPIO pin could be used to provide a single-ended 3.3-V level clock signal to the Auxiliary Phase-Locked Loop (AUXPLL), whose output is used for the USB module. The AUXCLKIN clock may also be used for the CAN module.
SD2_C2	7			I	Sigma-Delta 2 channel 2 clock input
RESET					
$\overline{\text{XRS}}$		124	69	I/OD	Device Reset (in) and Watchdog Reset (out). The devices have a built-in power-on reset (POR) circuit. During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset or NMI watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between $\overline{\text{XRS}}$ and V_{DDIO}. If a capacitor is placed between $\overline{\text{XRS}}$ and V_{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. The output buffer of this pin is an open drain with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
CLOCKS					
X1		123	68	I	On-chip crystal-oscillator input. To use this oscillator, a quartz crystal must be connected across X1 and X2. If this pin is not used, it must be tied to GND. This pin can also be used to feed a single-ended 3.3-V level clock. In this case, X2 is a No Connect (NC).
X2		121	66	O	On-chip crystal-oscillator output. A quartz crystal may be connected across X1 and X2. If X2 is not used, it must be left unconnected.
JTAG					
TCK		81	50	I	JTAG test clock with internal pullup (see Section 6.6)
TDI		77	46	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO		78	47	O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.[3]
TMS		80	49	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$		79	48	I	JTAG test reset with internal pulldown. TRST, when driven high, gives the scan system control of the operations of the device. If this signal is driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: TRST must be maintained low at all times during normal device operation, so an external pulldown resistor is required on this pin for protection against noise spikes. The value of this resistor should be as small as possible, so long as the JTAG debug probe is still able to drive the TRST pin high. A resistor between 2.2-kΩ and 10-kΩ generally offers adequate protection. Since the value of the resistor is application-specific, TI recommends that each target board be validated for proper operation of the debug probe and the application. This pin has an internal 50-ns (nominal) glitch filter.
INTERNAL VOLTAGE REGULATOR CONTROL					
VREGENZ		119	64	I	Internal voltage regulator enable with internal pulldown. To enable the 1.2-V VREG, tie directly to V_{SS}. To disable and use an external supply for the 1.2-V rail, tie directly to V_{DDIO}.

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
ANALOG, DIGITAL, AND I/O POWER					
V_{DD}		16	16		1.2-V digital logic power pins. There are two options for placing the decoupling capacitors. • Option 1 - Even Distribution: Distribute decoupling capacitance evenly across each V_{DD} pin with a minimum total capacitance of approximately: – 12uF to 26 uF for internal VREG – 20uF for externally supplied V_{DD} If the internal VREG is used, it is not required to have an external net connecting all V_{DD} pins. • Option 2 - Bulk Capacitance: Place a 1uF capacitor near each V_{DD} pin and place the remainder of the minimum total: – 12uF to 26uF for internal VREG – 20uF for externally supplied V_{DD} capacitance as bulk capacitance on the V_{DD} net If the internal VREG is used, this option requires a common V_{DD} net so that the bulk capacitance is available to all pins. The exact value of the decoupling capacitance for the external supply option should be determined by your system voltage regulation solution.
		21	39		
		61	45		
		76	63		
		117	71		
		126	78		
		137	84		
		153	89		
		158	95		
		169	–		
V_{DD3VFL}		72	41		3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin.
V_{DDA}		35	18		3.3-V analog power pins. Place a minimum 2.2-µF decoupling capacitor to V_{SSA} on each pin.
		36	38		
		54	–		

Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
V_{DDIO}		3	2		3.3-V digital I/O power pins. Place a minimum 0.1-µF decoupling capacitor on each pin. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution.
		11	10		
		15	15		
		20	40		
		26	44		
		62	55		
		68	62		
		75	72		
		82	79		
		88	83		
		91	90		
		99	94		
		106	–		
		114	–		
		116	–		
		127	–		
		138	–		
		147	–		
		152	–		
		159	–		
		168	–		
V_{DDOSC}		120	65		Power pins for the 3.3-V on-chip crystal oscillator (X1 and X2) and the two zero-pin internal oscillators (INTOSC). Place a 0.1-µF (minimum) decoupling capacitor on each pin.
		125	70		
V_{SS}		PWR PAD (177)	PWR PAD (101)		Device ground. For Quad Flatpacks (QFPs), the PowerPAD on the bottom of the package must be soldered to the ground plane of the PCB.
V_{SSOSC}		122	67		Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.
V_{SSA}		32	17		Analog ground. On the PZP package, pin 17 is double-bonded to V_{SSA} and V_{REFLOA}. This pin must be connect to V_{SSA}.
		34	35		
		52	36		
SPECIAL FUNCTIONS					
ERRORSTS		92	–	O	Error status output. This pin has an internal pulldown.

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Table 5-1. Signal Descriptions (continued)

TERMINAL				I/O/Z[1]	DESCRIPTION
NAME	MUX POSITION	PTP PIN NO.	PZP PIN NO.		
TEST PINS					
FLT1		73	42	I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.
FLT2		74	43	I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.

(1) I = Input, O = Output, OD = Open Drain, Z = High Impedance
(2) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).
(3) This pin has output impedance that can be as low as 22 Ω. This output could have fast edges and ringing depending on the system PCB characteristics. If this is a concern, the user should take precautions such as adding a 39Ω (10% tolerance) series termination resistor or implement some other termination scheme. It is also recommended that a system-level signal integrity analysis be performed with the provided IBIS models. The termination is not required if this pin is used for input function.

5.3 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 5-2 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. In order to avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 5-2 with pullups and pulldowns are always on and cannot be disabled.

Table 5-2. Pins With Internal Pullup and Pulldown

PIN	RESET ($\overline{\text{XRS}}$ = 0)	DEVICE BOOT	APPLICATION SOFTWARE
GPIOx	Pullup disabled	Pullup disabled[1]	Pullup enable is application-defined
$\overline{\text{TRST}}$	Pulldown active		
TCK	Pullup active		
TMS	Pullup active		
TDI	Pullup active		
$\overline{\text{XRS}}$	Pullup active		
VREGENZ	Pulldown active		
ERRORSTS	Pulldown active		
Other pins	No pullup or pulldown present		

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

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5.4 Pin Multiplexing

5.4.1 GPIO Muxed Pins

Table 5-3 shows the GPIO muxed pins. The default for each pin is the GPIO function, secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured prior to the GPyMUXn to avoid transient pulses on GPIO's from alternate mux selections. Columns not shown and blank cells are reserved GPIO Mux settings.

Table 5-3. GPIO Muxed Pins

	GPIO Mux Selection[1] [2]							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn.GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn.GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO0	EPWM1A (O)				SDAA (I/OD)		
	GPIO1	EPWM1B (O)		MFSRB (I/O)		SCLA (I/OD)		
	GPIO2	EPWM2A (O)			OUTPUTXBAR1 (O)	SDAB (I/OD)		
	GPIO3	EPWM2B (O)	OUTPUTXBAR2 (O)	MCLKRB (I/O)	OUTPUTXBAR2 (O)	SCLB (I/OD)		
	GPIO4	EPWM3A (O)			OUTPUTXBAR3 (O)	CANTXA (O)		
	GPIO5	EPWM3B (O)	MFSRA (I/O)	OUTPUTXBAR3 (O)		CANRXA (I)		
	GPIO6	EPWM4A (O)	OUTPUTXBAR4 (O)	EXTSYNCOUT (O)	EQEP3A (I)	CANTXB (O)		
	GPIO7	EPWM4B (O)	MCLKRA (I/O)	OUTPUTXBAR5 (O)	EQEP3B (I)	CANRXB (I)		
	GPIO8	EPWM5A (O)	CANTXB (O)	ADCSOCAO (O)	EQEP3S (I/O)	SCITXDA (O)		
	GPIO9	EPWM5B (O)	SCITXDB (O)	OUTPUTXBAR6 (O)	EQEP3I (I/O)	SCIRXDA (I)		
	GPIO10	EPWM6A (O)	CANRXB (I)	ADCSOCBO (O)	EQEP1A (I)	SCITXDB (O)		
	GPIO11	EPWM6B (O)	SCIRXDB (I)	OUTPUTXBAR7 (O)	EQEP1B (I)	SCIRXDB (I)		
	GPIO12	EPWM7A (O)	CANTXB (O)	MDXB (O)	EQEP1S (I/O)	SCITXDC (O)		
	GPIO13	EPWM7B (O)	CANRXB (I)	MDRB (I)	EQEP1I (I/O)	SCIRXDC (I)		
	GPIO14	EPWM8A (O)	SCITXDB (O)	MCLKXB (I/O)		OUTPUTXBAR3 (O)		
	GPIO15	EPWM8B (O)	SCIRXDB (I)	MFSXB (I/O)		OUTPUTXBAR4 (O)		
	GPIO16	SPISIMOA (I/O)	CANTXB (O)	OUTPUTXBAR7 (O)	EPWM9A (O)		SD1_D1 (I)	
	GPIO17	SPISOMIA (I/O)	CANRXB (I)	OUTPUTXBAR8 (O)	EPWM9B (O)		SD1_C1 (I)	
	GPIO18	SPICLKA (I/O)	SCITXDB (O)	CANRXA (I)	EPWM10A (O)		SD1_D2 (I)	
	GPIO19	$\overline{\text{SPISTEA}}$ (I/O)	SCIRXDB (I)	CANTXA (O)	EPWM10B (O)		SD1_C2 (I)	
	GPIO20	EQEP1A (I)	MDXA (O)	CANTXB (O)	EPWM11A (O)		SD1_D3 (I)	
	GPIO21	EQEP1B (I)	MDRA (I)	CANRXB (I)	EPWM11B (O)		SD1_C3 (I)	
	GPIO22	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)	EPWM12A (O)	SPICLKB (I/O)	SD1_D4 (I)	
	GPIO23	EQEP1I (I/O)	MFSXA (I/O)	SCIRXDB (I)	EPWM12B (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD1_C4 (I)	
	GPIO24	OUTPUTXBAR1 (O)	EQEP2A (I)	MDXB (O)		SPISIMOB (I/O)	SD2_D1 (I)	
	GPIO25	OUTPUTXBAR2 (O)	EQEP2B (I)	MDRB (I)		SPISOMIB (I/O)	SD2_C1 (I)	
	GPIO26	OUTPUTXBAR3 (O)	EQEP2I (I/O)	MCLKXB (I/O)	OUTPUTXBAR3 (O)	SPICLKB (I/O)	SD2_D2 (I)	
	GPIO27	OUTPUTXBAR4 (O)	EQEP2S (I/O)	MFSXB (I/O)	OUTPUTXBAR4 (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD2_C2 (I)	
	GPIO28	SCIRXDA (I)	$\overline{\text{EM1CS4}}$ (O)		OUTPUTXBAR5 (O)	EQEP3A (I)	SD2_D3 (I)	
	GPIO29	SCITXDA (O)	EM1SDCKE (O)		OUTPUTXBAR6 (O)	EQEP3B (I)	SD2_C3 (I)	
	GPIO30	CANRXA (I)	EM1CLK (O)		OUTPUTXBAR7 (O)	EQEP3S (I/O)	SD2_D4 (I)	
	GPIO31	CANTXA (O)	$\overline{\text{EM1WE}}$ (O)		OUTPUTXBAR8 (O)	EQEP3I (I/O)	SD2_C4 (I)	
	GPIO32	SDAA (I/OD)	$\overline{\text{EM1CS0}}$ (O)					
	GPIO33	SCLA (I/OD)	EM1RNW (O)					
	GPIO34	OUTPUTXBAR1 (O)	$\overline{\text{EM1CS2}}$ (O)			SDAB (I/OD)		
	GPIO35	SCIRXDA (I)	$\overline{\text{EM1CS3}}$ (O)			SCLB (I/OD)		
	GPIO36	SCITXDA (O)	EM1WAIT (I)			CANRXA (I)		
	GPIO37	OUTPUTXBAR2 (O)	$\overline{\text{EM1OE}}$ (O)			CANTXA (O)		
	GPIO38		EM1A0 (O)		SCITXDC (O)	CANTXB (O)		
	GPIO39		EM1A1 (O)		SCIRXDC (I)	CANRXB (I)		
	GPIO40		EM1A2 (O)			SDAB (I/OD)		
	GPIO41		EM1A3 (O)			SCLB (I/OD)		
	GPIO42					SDAA (I/OD)		SCITXDA (O)

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Table 5-3. GPIO Muxed Pins (continued)

	GPIO Mux Selection[1] [2]							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO43					SCLA (I/OD)		SCIRXDA (I)
	GPIO44		EM1A4 (O)					
	GPIO45		EM1A5 (O)					
	GPIO46		EM1A6 (O)			SCIRXDD (I)		
	GPIO47		EM1A7 (O)			SCITXDD (O)		
	GPIO48	OUTPUTXBAR3 (O)	EM1A8 (O)			SCITXDA (O)	SD1_D1 (I)	
	GPIO49	OUTPUTXBAR4 (O)	EM1A9 (O)			SCIRXDA (I)	SD1_C1 (I)	
	GPIO50	EQEP1A (I)	EM1A10 (O)			SPISIMOC (I/O)	SD1_D2 (I)	
	GPIO51	EQEP1B (I)	EM1A11 (O)			SPISOMIC (I/O)	SD1_C2 (I)	
	GPIO52	EQEP1S (I/O)	EM1A12 (O)			SPICLKC (I/O)	SD1_D3 (I)	
	GPIO53	EQEP1I (I/O)	EM1D31 (I/O)			$\overline{\text{SPISTEC}}$ (I/O)	SD1_C3 (I)	
	GPIO54	SPISIMOA (I/O)	EM1D30 (I/O)		EQEP2A (I)	SCITXDB (O)	SD1_D4 (I)	
	GPIO55	SPISOMIA (I/O)	EM1D29 (I/O)		EQEP2B (I)	SCIRXDB (I)	SD1_C4 (I)	
	GPIO56	SPICLKA (I/O)	EM1D28 (I/O)		EQEP2S (I/O)	SCITXDC (O)	SD2_D1 (I)	
	GPIO57	$\overline{\text{SPISTEA}}$ (I/O)	EM1D27 (I/O)		EQEP2I (I/O)	SCIRXDC (I)	SD2_C1 (I)	
	GPIO58	MCLKRA (I/O)	EM1D26 (I/O)		OUTPUTXBAR1 (O)	SPICLKB (I/O)	SD2_D2 (I)	SPISIMOA[3] (I/O)
	GPIO59	MFSRA (I/O)	EM1D25 (I/O)		OUTPUTXBAR2 (O)	$\overline{\text{SPISTEB}}$ (I/O)	SD2_C2 (I)	SPISOMIA[3] (I/O)
	GPIO60	MCLKRB (I/O)	EM1D24 (I/O)		OUTPUTXBAR3 (O)	SPISIMOB (I/O)	SD2_D3 (I)	SPICLKA[3] (I/O)
	GPIO61	MFSRB (I/O)	EM1D23 (I/O)		OUTPUTXBAR4 (O)	SPISOMIB (I/O)	SD2_C3 (I)	$\overline{\text{SPISTEA}}$ [3] (I/O)
	GPIO62	SCIRXDC (I)	EM1D22 (I/O)		EQEP3A (I)	CANRXA (I)	SD2_D4 (I)	
	GPIO63	SCITXDC (O)	EM1D21 (I/O)		EQEP3B (I)	CANTXA (O)	SD2_C4 (I)	SPISIMOB[3] (I/O)
	GPIO64		EM1D20 (I/O)		EQEP3S (I/O)	SCIRXDA (I)		SPISOMIB[3] (I/O)
	GPIO65		EM1D19 (I/O)		EQEP3I (I/O)	SCITXDA (O)		SPICLKB[3] (I/O)
	GPIO66		EM1D18 (I/O)			SDAB (I/OD)		$\overline{\text{SPISTEB}}$ [3] (I/O)
	GPIO67		EM1D17 (I/O)					
	GPIO68		EM1D16 (I/O)					
	GPIO69		EM1D15 (I/O)			SCLB (I/OD)		SPISIMOC[3] (I/O)
	GPIO70		EM1D14 (I/O)		CANRXA (I)	SCITXDB (O)		SPISOMIC[3] (I/O)
	GPIO71		EM1D13 (I/O)		CANTXA (O)	SCIRXDB (I)		SPICLKC[3] (I/O)
	GPIO72		EM1D12 (I/O)		CANTXB (O)	SCITXDC (O)		$\overline{\text{SPISTEC}}$ [3] (I/O)
	GPIO73		EM1D11 (I/O)	XCLKOUT (O)	CANRXB (I)	SCIRXDC (I)		
	GPIO74		EM1D10 (I/O)					
	GPIO75		EM1D9 (I/O)					
	GPIO76		EM1D8 (I/O)			SCITXDD (O)		
	GPIO77		EM1D7 (I/O)			SCIRXDD (I)		
	GPIO78		EM1D6 (I/O)			EQEP2A (I)		
	GPIO79		EM1D5 (I/O)			EQEP2B (I)		
	GPIO80		EM1D4 (I/O)			EQEP2S (I/O)		
	GPIO81		EM1D3 (I/O)			EQEP2I (I/O)		
	GPIO82		EM1D2 (I/O)					
	GPIO83		EM1D1 (I/O)					
	GPIO84				SCITXDA (O)	MDXB (O)		MDXA (O)
	GPIO85		EM1D0 (I/O)		SCIRXDA (I)	MDRB (I)		MDRA (I)
	GPIO86		EM1A13 (O)	EM1CAS (O)	SCITXDB (O)	MCLKXB (I/O)		MCLKXA (I/O)
	GPIO87		EM1A14 (O)	EM1RAS (O)	SCIRXDB (I)	MFSXB (I/O)		MFSXA (I/O)
	GPIO88		EM1A15 (O)	EM1DQM0 (O)				
	GPIO89		EM1A16 (O)	EM1DQM1 (O)		SCITXDC (O)		
	GPIO90		EM1A17 (O)	EM1DQM2 (O)		SCIRXDC (I)		
	GPIO91		EM1A18 (O)	EM1DQM3 (O)		SDAA (I/OD)		
	GPIO92		EM1A19 (O)	EM1BA1 (O)		SCLA (I/OD)		
	GPIO93			EM1BA0 (O)		SCITXDD (O)		

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Table 5-3. GPIO Muxed Pins (continued)

	GPIO Mux Selection[1] [2]							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO94					SCIRXDD (I)		
	GPIO99				EQEP1I (I/O)			
	GPIO133/ AUXCLKIN						SD2_C2 (I)	

(1) I = Input, O = Output, OD = Open Drain
(2) GPIO Index settings of 9, 10, 11, 13, and 14 are reserved.
(3) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

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5.4.2 Input X-BAR

The Input X-BAR is used to route any GPIO input to the ADC, eCAP, and ePWM peripherals as well as to external interrupts (XINT) (see Figure 5-3). Table 5-4 shows the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

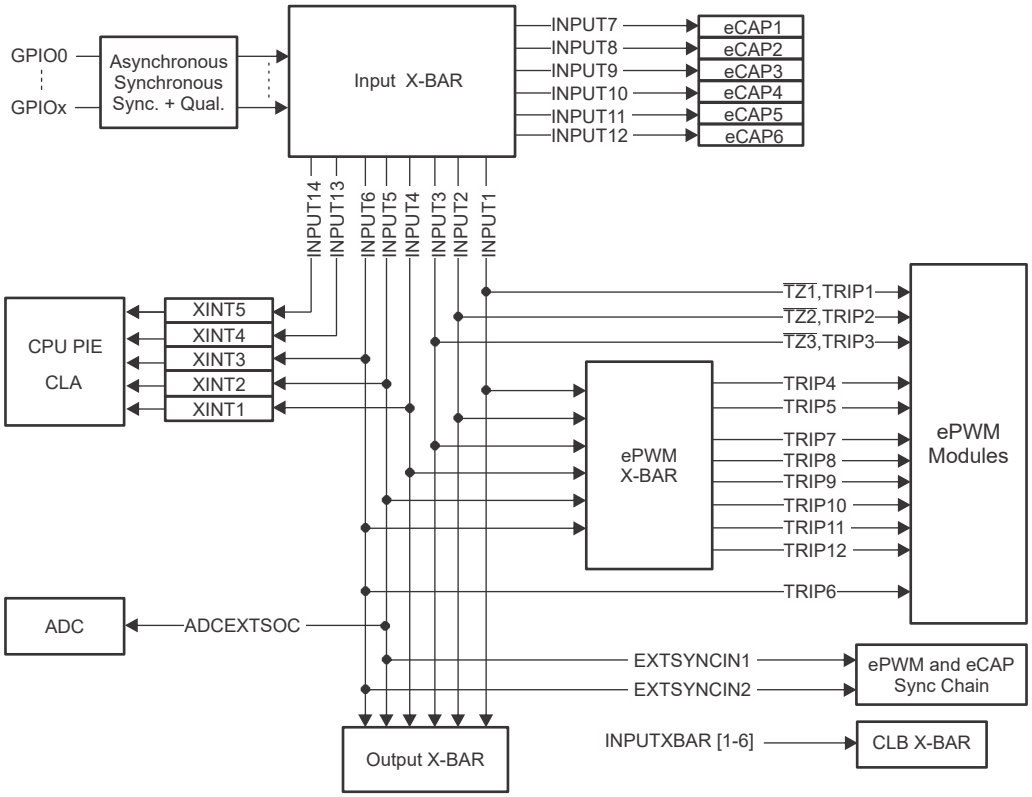


Figure 5-3. Input X-BAR

Table 5-4. Input X-BAR Destinations

INPUT	DESTINATIONS
INPUT1	EPWM[TZ1,TRIP1], EPWM X-BAR, Output X-BAR
INPUT2	EPWM[TZ2,TRIP2], EPWM X-BAR, Output X-BAR
INPUT3	EPWM[TZ3,TRIP3], EPWM X-BAR, Output X-BAR
INPUT4	XINT1, EPWM X-BAR, Output X-BAR
INPUT5	XINT2, ADCEXTSOC, EXTSYNCIN1, EPWM X-BAR, Output X-BAR
INPUT6	XINT3, EPWM[TRIP6], EXTSYNCIN2, EPWM X-BAR, Output X-BAR
INPUT7	ECAP1
INPUT8	ECAP2
INPUT9	ECAP3
INPUT10	ECAP4
INPUT11	ECAP5
INPUT12	ECAP6
INPUT13	XINT4
INPUT14	XINT5

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5.4.3 Output X-BAR and ePWM X-BAR

The Output X-BAR has eight outputs which can be selected on the GPIO mux as OUTPUTXBARx. The ePWM X-BAR has eight outputs which are connected to the TRIPx inputs of the ePWM. The sources for both the Output X-BAR and ePWM X-BAR are shown in Figure 5-4. For details on the Output X-BAR and ePWM X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

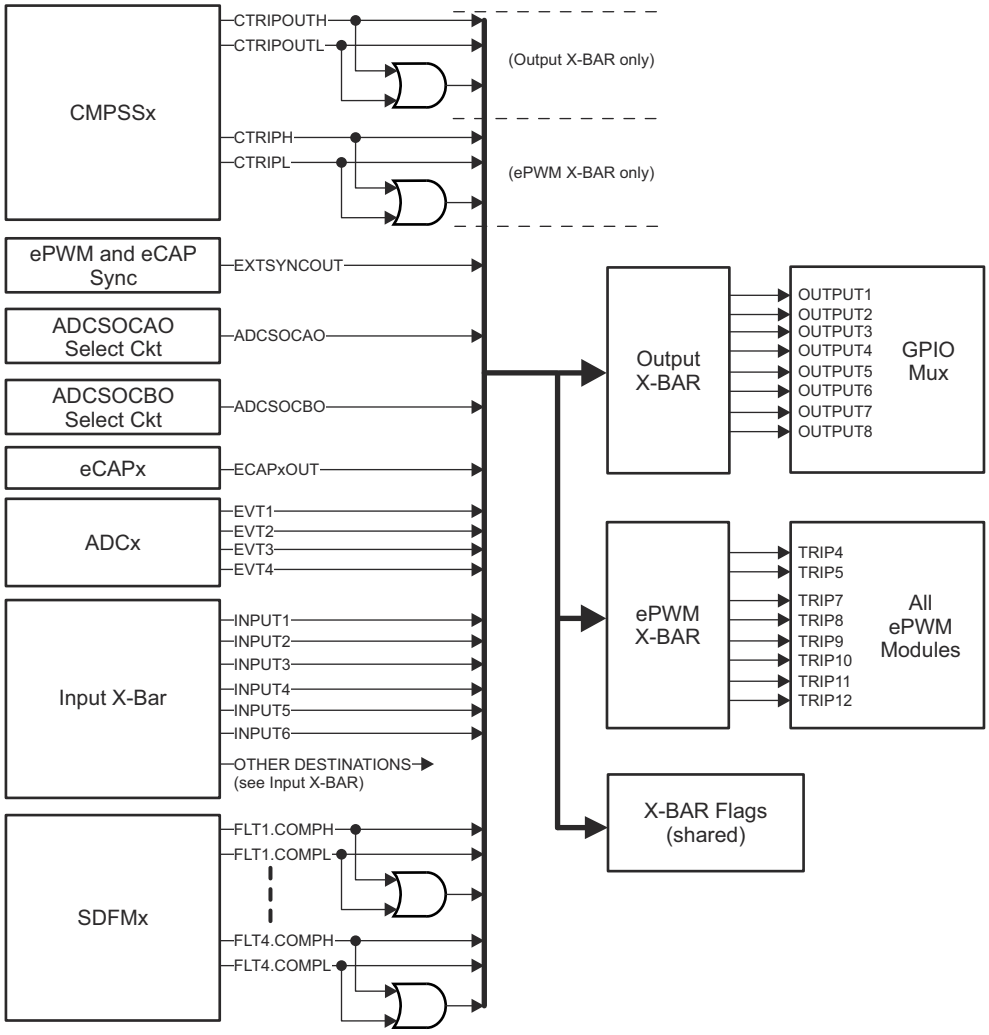


Figure 5-4. Output X-BAR and ePWM X-BAR

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5.4.4 USB Pin Muxing

Table 5-5 shows assignment of the alternate USB function mapping. These can be configured with the GPBAMSEL register.

Table 5-5. Alternate USB Function

GPIO	GPBAMSEL SETTING	USB FUNCTION
GPIO42	GPBAMSEL[10] = 1b	USB0DM
GPIO43	GPBAMSEL[11] = 1b	USB0DP

5.4.5 High-Speed SPI Pin Muxing

The SPI module on this device has a high-speed mode. To achieve the highest possible speed, a special GPIO configuration is used on a single GPIO mux option for each SPI. These GPIOs may also be used by the SPI when not in high-speed mode (HS_MODE = 0).

To select the mux options that enable the SPI high-speed mode, configure the GPyGMUX and GPyMUX registers as shown in Table 5-6.

Table 5-6. GPIO Configuration for High-Speed SPI

GPIO	SPI SIGNAL	MUX CONFIGURATION	
SPIA			
GPIO58	SPISIMOA	GPBGMUX2[21:20]=11b	GPBMUX2[21:20]=11b
GPIO59	SPISOMIA	GPBGMUX2[23:22]=11b	GPBMUX2[23:22]=11b
GPIO60	SPICLKA	GPBGMUX2[25:24]=11b	GPBMUX2[25:24]=11b
GPIO61	$\overline{\text{SPISTEA}}$	GPBGMUX2[27:26]=11b	GPBMUX2[27:26]=11b
SPIB			
GPIO63	SPISIMOB	GPBGMUX2[31:30]=11b	GPBMUX2[31:30]=11b
GPIO64	SPISOMIB	GPCGMUX1[1:0]=11b	GPCMUX1[1:0]=11b
GPIO65	SPICLKB	GPCGMUX1[3:2]=11b	GPCMUX1[3:2]=11b
GPIO66	$\overline{\text{SPISTEB}}$	GPCGMUX1[5:4]=11b	GPCMUX1[5:4]=11b
SPIC			
GPIO69	SPISIMOC	GPCGMUX1[11:10]=11b	GPCMUX1[11:10]=11b
GPIO70	SPISOMIC	GPCGMUX1[13:12]=11b	GPCMUX1[13:12]=11b
GPIO71	SPICLKC	GPCGMUX1[15:14]=11b	GPCMUX1[15:14]=11b
GPIO72	$\overline{\text{SPISTEC}}$	GPCGMUX1[17:16]=11b	GPCMUX1[17:16]=11b

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5.5 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 5-7 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 5-7, any are acceptable. Pins not listed in Table 5-7 must be connected according to Section 5.2.1.

Table 5-7. Connections for Unused Pins

SIGNAL NAME	ACCEPTABLE PRACTICE
Analog	
V_{REFHIx}	Tie to V_{DDA}
V_{REFLOx}	Tie to V_{SSA}
ADCINx	• No Connect • Tie to V_{SSA}
Digital	
GPIOx	• No connection (input mode with internal pullup enabled) • No connection (output mode with internal pullup disabled) • Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled)
X1	Tie to V_{SS}
X2	No Connect
TCK	• No Connect • Pullup resistor
TDI	• No Connect • Pullup resistor
TDO	No Connect
TMS	No Connect
$\overline{TRST}$	Pulldown resistor (2.2 kΩ or smaller)
VREGENZ	Tie to V_{DDIO}
ERRORSTS	No Connect
FLT1	No Connect
FLT2	No Connect
Power and Ground	
V_{DD}	All V_{DD} pins must be connected per Section 5.2.1.
V_{DDA}	If a dedicated analog supply is not used, tie to V_{DDIO}.
V_{DDIO}	All V_{DDIO} pins must be connected per Section 5.2.1.
V_{DD3VFL}	Must be tied to V_{DDIO}
V_{DDOSC}	Must be tied to V_{DDIO}
V_{SS}	All V_{SS} pins must be connected to board ground.
V_{SSA}	If a dedicated analog ground is not used, tie to V_{SS}.
V_{SSOSC}	If an external crystal is not used, this pin may be connected to the board ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX[1] [2]	UNIT
Supply voltage	V_{DDIO} with respect to V_{SS}	–0.3	4.6	V
	V_{DD3VFL} with respect to V_{SS}	–0.3	4.6	
	V_{DDOSC} with respect to V_{SS}	–0.3	4.6	
	V_{DD} with respect to V_{SS}	–0.3	1.5	
Analog voltage	V_{DDA} with respect to V_{SSA}	–0.3	4.6	V
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital/analog input (per pin), I_{IK} ($V_{IN} < V_{SS}/V_{SSA}$ or $V_{IN} > V_{DDIO}/V_{DDA}$)[3]	–20	20	mA
	Total for all inputs, $I_{IKTOTAL}$ ($V_{IN} < V_{SS}/V_{SSA}$ or $V_{IN} > V_{DDIO}/V_{DDA}$)	–20	20	
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Free-Air temperature	T_A	–40	125	°C
Operating junction temperature	T_J	–40	150	°C
Storage temperature[4]	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 6.4 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ±2 mA. Do not operate in this condition continuously as V_{DDIO}/V_{DDA} voltage may internally rise and impact other electrical specifications.
(4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *Semiconductor and IC Package Thermal Metrics*.

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6.2 ESD Ratings – Commercial

			VALUE	UNIT
TMS320F28075 and TMS320F28076 in 176-pin PTP package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002[2]	±500	
TMS320F28075 and TMS320F28076 in 100-pin PZP package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Automotive

				VALUE	UNIT
TMS320F28075-Q1 in 176-pin PTP package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 176-pin PTP: 1, 44, 45, 88, 89, 132, 133, 176	±750	
TMS320F28075-Q1 in 100-pin PZP package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 100-pin PZP: 1, 25, 26, 50, 51, 75, 76, 100	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO} [1]		3.14	3.3	3.47	V
Device supply voltage, V_{DD}		1.14	1.2	1.26	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA}		3.14	3.3	3.47	V
Analog ground, V_{SSA}			0		V
Junction temperature, T_J	T version	–40		105	°C
	S version[2]	–40		125	
	Q version (AEC Q100 qualification)[2]	–40		150	
Free-Air temperature, T_A	Q version (AEC Q100 qualification)	–40		125	°C

(1) V_{DDIO}, V_{DD3VFL}, and V_{DDOSC} should be maintained within 0.3 V of each other.
(2) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See *Calculating Useful Lifetimes of Embedded Processors* for more information.

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6.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. Section 6.5.1 shows the device current consumption at 120-MHz SYSCLK. Section 6.5.2 shows the device current consumption at 120-MHz SYSCLK with the internal VREG enabled.

6.5.1 Device Current Consumption at 120-MHz SYSCLK

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO} [1]		I_{DDA}		I_{DD3VFL}	
		TYP[3]	MAX[2]	TYP[3]	MAX[2]	TYP[3]	MAX[2]	TYP[3]	MAX[2]
Operational	• Code is running out of RAM.[4] • All I/O pins are left unconnected. • Peripherals not active have their clocks disabled. • FLASH is read and in active state. • XCLKOUT is enabled at SYSCLK/4.	140 mA	295 mA	25 mA		13 mA	20 mA	33 mA	40 mA
IDLE	• CPU1 is in IDLE mode. • Flash is powered down. • XCLKOUT is turned off.	50 mA	185 mA	3 mA	10 mA	10 µA	150 µA	10 µA	150 µA
STANDBY	• CPU1 is in STANDBY mode. • Flash is powered down. • XCLKOUT is turned off.	25 mA	170 mA	3 mA	10 mA	5 µA	150 µA	10 µA	150 µA
HALT	• CPU1 watchdog is running. • Flash is powered down. • XCLKOUT is turned off.	1.5 mA	120 mA	750 µA	2 mA	5 µA	150 µA	10 µA	150 µA
HIBERNATE	• CPU1.M0 and CPU1.M1 RAMs are in low-power data retention mode.	300 µA	5 mA	750 µA	2 mA	5 µA	75 µA	1 µA	50 µA
Flash Erase/Program[5]	• CPU1 is running from RAM. • All I/O pins are left unconnected. • Peripheral clocks are disabled. • CPU1 is performing Flash Erase and Programming. • XCLKOUT is turned off.	97 mA	145 mA	3 mA	10 mA	10 µA	150 µA	45 mA	55 mA

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6.5.1 Device Current Consumption at 120-MHz SYSCLK (continued)

MODE	TEST CONDITIONS	I_{DD}		I_{DDIO} (1)		I_{DDA}		I_{DD3VFL}	
		TYP(3)	MAX(2)	TYP(3)	MAX(2)	TYP(3)	MAX(2)	TYP(3)	MAX(2)
RESET	• CPU is held in reset via external low signal driven onto XRSn • XRSn held low through power-up	10 mA	20 mA	0.01 mA	0.8 mA	0.02 mA	1 mA	2.5 mA	8 mA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) MAX: V_{max}, 125°C
(3) TYP: V_{nom}, 30°C
(4) The following is executed in a loop on CPU1:
- All of the communication peripherals are exercised in loop-back mode: CAN-A to CAN-B; SPI-A to SPI-C; SCI-A to SCI-D; I2C-A to I2C-B; McBSP-A to McBSP-B; USB
- ePWM1 to ePWM12 generate 400-kHz PWM output on 24 pins
- CPU TIMERs active
- DMA does 32-bit burst transfers
- CLA1 does multiply-accumulate tasks
- All ADCs perform continuous conversion
- All DACs ramp voltage up/down at 150 kHz
- CMPSS1 to CMPSS8 active
- TMU calculates a cosine
- FPU does multiply/accumulate with parallel load

(5) Brownout events during flash programming can corrupt flash data. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.

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6.5.2 Device Current Consumption at 120-MHz SYSCLK With the Internal VREG Enabled

MODE(1)	TEST CONDITIONS	I_{DDIO} (2)		I_{DDA}		I_{DD3VFL}	
		TYP(4)	MAX(3)	TYP(4)	MAX(3)	TYP(4)	MAX(3)
Operational (RAM)	• Code is running out of RAM.(5) • All I/O pins are left unconnected. • Peripherals not active have their clocks disabled. • FLASH is read and in active state. • XCLKOUT is enabled at SYSCLK/4.	165 mA	375 mA	13 mA	25 mA	33 mA	40 mA
IDLE	• CPU1 is in IDLE mode. • Flash is powered down. • XCLKOUT is turned off.	53 mA	200 mA	10 µA	150 µA	10 µA	150 µA
STANDBY	• CPU1 is in STANDBY mode. • Flash is powered down. • XCLKOUT is turned off.	28 mA	185 mA	5 µA	150 µA	10 µA	150 µA
HALT	• CPU1 watchdog is running. • Flash is powered down. • XCLKOUT is turned off.	2.25 mA	125 mA	5 µA	150 µA	10 µA	150 µA
HIBERNATE	• CPU1.M0 and CPU1.M1 RAMs are in low-power data retention mode.	1.2 mA	8 mA	5 µA	75 µA	1 µA	50 µA

(1) The internal voltage regulator is described in Section 6.9.1.1.
(2) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(3) MAX: V_{max}, 125°C
(4) TYP: V_{nom}, 30°C
(5) The following is executed in a loop on CPU1:
- All of the communication peripherals are exercised in loop-back mode: CAN-A to CAN-B; SPI-A to SPI-C; SCI-A to SCI-D; I2C-A to I2C-B; McBSP-A to McBSP-B; USB
- ePWM1 to ePWM12 generate 400-kHz PWM output on 24 pins
- CPU TIMERs active
- DMA does 32-bit burst transfers
- CLA1 does multiply-accumulate tasks
- All ADCs perform continuous conversion
- All DACs ramp voltage up/down at 150 kHz
- CMPSS1 to CMPSS8 active
- TMU calculates a cosine
- FPU does multiply/accumulate with parallel load

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6.5.3 Current Consumption Graphs

Figure 6-1 and Figure 6-2 are a typical representation of the relationship between frequency and current consumption/power on the device. The operational test from Section 6.5.1 was run across frequency at V_{max} and high temperature. Actual results will vary based on the system implementation and conditions.

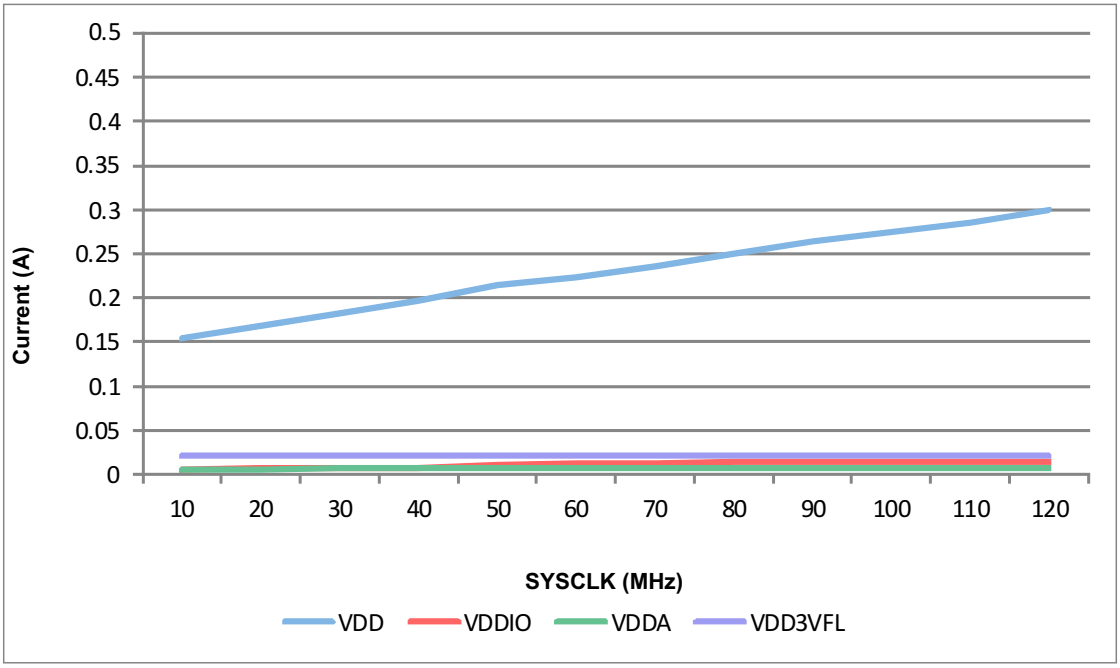


Figure 6-1. Operational Current Versus Frequency

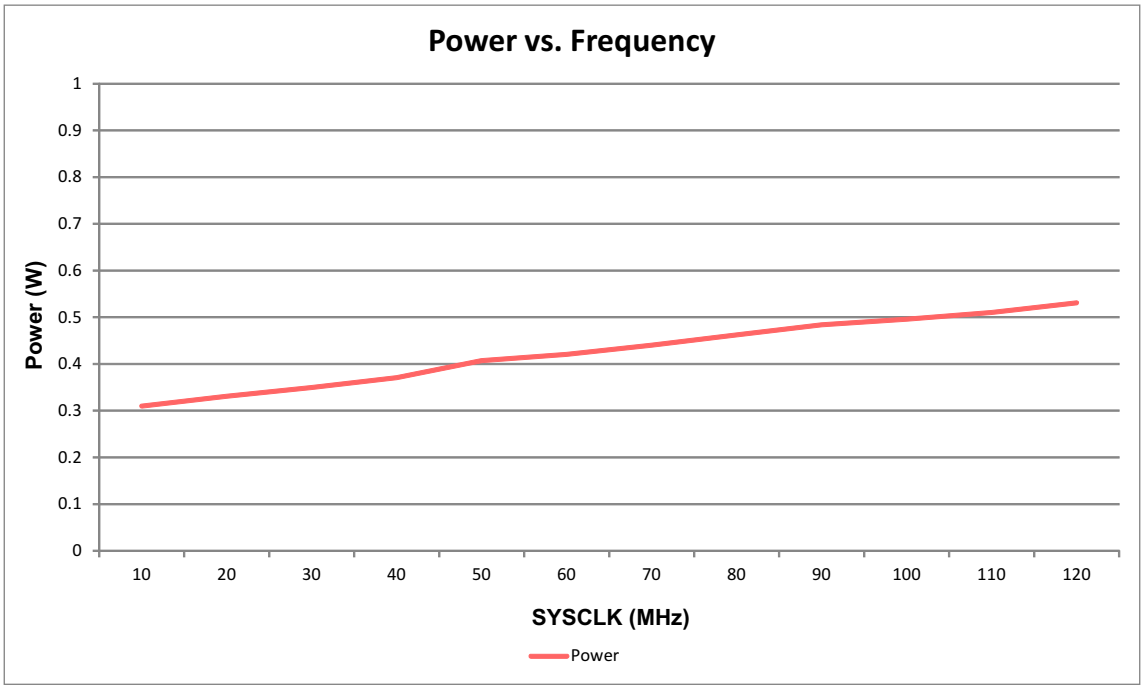


Figure 6-2. Power Versus Frequency

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Leakage current will increase with operating temperature in a nonlinear manner. The difference in V_{DD} current between TYP and MAX conditions can be seen in Figure 6-3. The current consumption in HALT mode is primarily leakage current as there is no active switching if the internal oscillator has been powered down.

Figure 6-3 shows the typical leakage current across temperature. The device was placed into HALT mode under nominal voltage conditions.

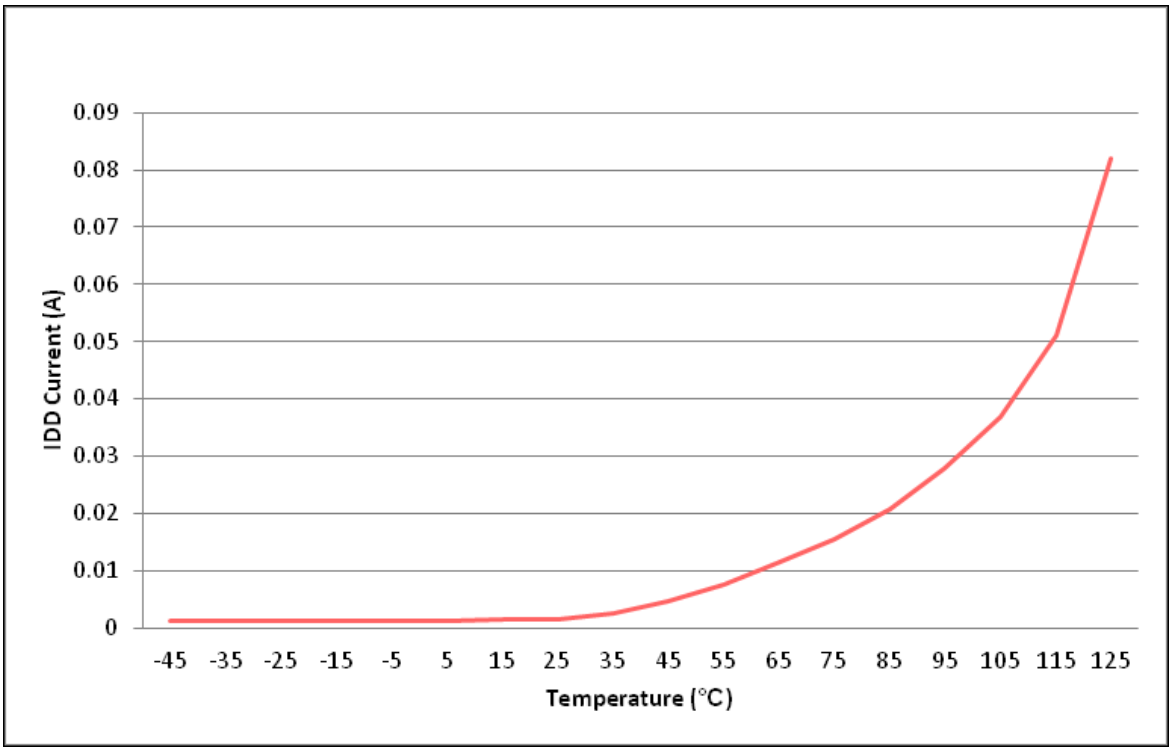


Figure 6-3. I_{DD} Leakage Current Versus Temperature

6.5.4 Reducing Current Consumption

The F2807x devices provide some methods to reduce the device current consumption:

- Any one of the four low-power modes—IDLE, STANDBY, HALT, and HIBERNATE—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. Table 6-1 indicates the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest V_{DDA} current consumption in a low-power mode, see the respective analog chapter of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual* to ensure each module is powered down as well.

Table 6-1. Current on V_{DD} Supply by Various Peripherals (at 120 MHz)

PERIPHERAL MODULE(1) (2)	I_{DD} CURRENT REDUCTION (mA)
ADC(3)	2.1
CAN	2.1
CLA	0.9
CMPSS(3)	0.9
CPUTIMER	0.2
DAC(3)	0.4
DMA	1.8
eCAP	0.4
EMIF1	1.8
ePWM1 to ePWM4(4)	2.8
ePWM5 to ePWM12(4)	1.1
HRPWM(4)	1.1
I2C	0.9
McBSP	1
SCI	0.6
SDFM	1.3
SPI	0.4
USB and AUXPLL at 60 MHz	14.8

(1) At V_{max} and 125°C.
(2) All peripherals are disabled upon reset. Use the PCLKCRx register to individually enable peripherals. For peripherals with multiple instances, the current quoted is for a single module.
(3) This number represents the current drawn by the digital portion of the ADC, CMPSS, and DAC modules.
(4) The ePWM is at /2 of SYSCLK.

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6.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	V_{DDIO} * 0.8			V
			I_{OH} = –100 µA	V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.4	V
			I_{OL} = 100 µA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
V_{IH}	High-level input voltage (3.3 V)	GPIO0–GPIO7, GPIO42–GPIO43, GPIO46–GPIO47		V_{DDIO} * 0.7		V_{DDIO} + 0.3	V
		All other pins		2.0		V_{DDIO} + 0.3	
V_{IL}	Low-level input voltage (3.3 V)			V_{SS} – 0.3		0.8	V
$V_{HYSTERESIS}$	Input hysteresis			150			mV
$I_{pulldown}$	Input current	Digital inputs with pulldown(1)	V_{DDIO} = 3.3 V V_{IN} = V_{DDIO}		120		µA
I_{pullup}	Input current	Digital inputs with pullup enabled(1)	V_{DDIO} = 3.3 V V_{IN} = 0 V		150		µA
I_{LEAK}	Pin leakage	Digital	Pullups disabled 0 V ≤ V_{IN} ≤ V_{DDIO}			2	µA
		Analog (except ADCINB0 or DACOUTx)	0 V ≤ V_{IN} ≤ V_{DDA}			2	
		ADCINB0			2	11(2)	
		DACOUTx			66		
C_I	Input capacitance				2		pF
$V_{DDIO-POR}$	V_{DDIO} power-on reset voltage				2.3		V

(1) See Table 5-2 for a list of pins with a pullup or pulldown.
(2) The MAX input leakage shown on ADCINB0 is at high temperature.

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6.7 Thermal Resistance Characteristics

6.7.1 PTP Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	6.97	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	6.05	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	17.8	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	12.8	150
		11.4	250
		10.1	500
Psi_{JT}	Junction-to-package top	0.11	0
		0.24	150
		0.33	250
		0.42	500
Psi_{JB}	Junction-to-board	6.1	0
		5.5	150
		5.4	250
		5.3	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

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6.7.2 PZP Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	4.3	N/A
$R\Theta_{JB}$	Junction-to-board thermal resistance	5.9	N/A
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	19.1	0
$R\Theta_{JMA}$	Junction-to-moving air thermal resistance	14.3	150
		12.8	250
		11.4	500
Psi_{JT}	Junction-to-package top	0.03	0
		0.09	150
		0.12	250
		0.20	500
Psi_{JB}	Junction-to-board	6.0	0
		5.5	150
		5.5	250
		5.3	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

6.8 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

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6.9 System

6.9.1 Power Management

6.9.1.1 Internal 1.2-V VREG

The internal VREG is supplied by V_{DDIO} and generates the 1.2 V required to power the V_{DD} pins. If the internal VREG is enabled there is no need to supply 1.2 V to the device. Enable this functionality by pulling the VREGENZ pin low to V_{SS}. Although the internal VREG eliminates the need to use an external power supply for V_{DD}, decoupling capacitors are required on each V_{DD} pin for VREG stability (see the description of V_{DD} in Section 5.2.1). Driving an external load with the internal VREG is not supported.

6.9.1.2 Power Sequencing

6.9.1.2.1 Signal Pin Requirements

Before powering the device, no voltage larger than 0.3 V above V_{DDIO} can be applied to any digital pin, and no voltage larger than 0.3 V above V_{DDA} can be applied to any analog pin (including V_{REFHI}).

6.9.1.2.2 V_{DDIO}, V_{DDA}, V_{DD3VFL}, and V_{DDOSC} Requirements

The 3.3-V supplies should be powered up together and kept within 0.3 V of each other during functional operation.

6.9.1.2.3 V_{DD} Requirements

When VREGENZ is tied to V_{SS}, the V_{DD} sequencing requirements are handled by the device.

When using an external source for V_{DD} (VREGENZ tied to V_{DDIO}), V_{DDOSC} and V_{DD} must be powered on and off at the same time. V_{DDOSC} should not be powered on when V_{DD} is off. During the ramp, V_{DD} should be kept no more than 0.3 V above V_{DDIO}.

For applications not powering V_{DDOSC} and V_{DD} at the same time, see the "INTOSC: VDDOSC Powered Without VDD Can Cause INTOSC Frequency Drift" advisory in the *TMS320F2807x Real-Time MCUs Silicon Errata*.

There is an internal 12.8-mA current source from V_{DD3VFL} to V_{DD} when the flash is active. When the flash is active and the device is in a low-activity state (for example, a low-power mode), this internal current source can cause V_{DD} to rise to approximately 1.3 V . There will be zero current load to the external system V_{DD} regulator while in this condition. This is not an issue for most regulators; however, if the system voltage regulator requires a minimum load for proper operation, then an external 82Ω resistor can be added to the board to ensure a minimal current load on V_{DD}. See the "Low-Power Modes: Power Down Flash or Maintain Minimum Device Activity" advisory in the *TMS320F2807x Real-Time MCUs Silicon Errata*.

6.9.1.2.4 Supply Ramp Rate

The supplies should ramp to full rail within 10 ms. Section 6.9.1.2.4.1 shows the supply ramp rate.

6.9.1.2.4.1 Supply Ramp Rate

		MIN	MAX	UNIT
Supply ramp rate	V_{DDIO}, V_{DD}, V_{DDA}, V_{DD3VFL}, V_{DDOSC} with respect to V_{SS}	330	10^5	V/s

6.9.1.2.5 Supply Supervision

An internal power-on-reset (POR) circuit keeps the I/Os in a high-impedance state during power up. External supply voltage supervisors (SVS) can be used to monitor the voltage on the 3.3-V and 1.2-V rails and drive $\overline{XRS}$ low when supplies are outside operational specifications.

Note

If the supply voltage is held near the POR threshold, then the device may drive periodic resets onto the $\overline{XRS}$ pin.

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6.9.2 Reset Timing

$\overline{\text{XRS}}$ is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR). During power up, the POR circuit drives the $\overline{\text{XRS}}$ pin low. A watchdog or NMI watchdog reset also drives the pin low. An external circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between $\overline{\text{XRS}}$ and V_{DDIO}. A capacitor should be placed between $\overline{\text{XRS}}$ and V_{SS} for noise filtering; the capacitance should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{\text{XRS}}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-4 shows the recommended reset circuit.

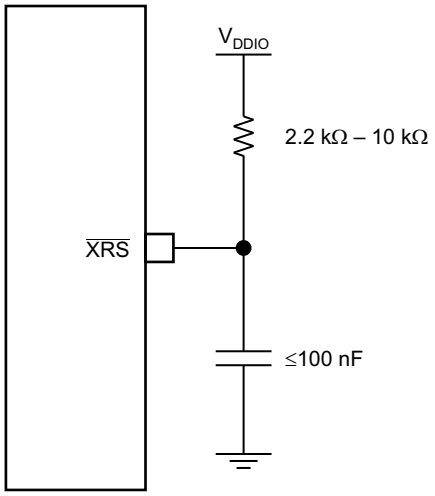


Figure 6-4. Reset Circuit

6.9.2.1 Reset Sources

The following reset sources exist on this device: $\overline{\text{XRS}}$, $\overline{\text{WDRS}}$, $\overline{\text{NMIWDRS}}$, $\overline{\text{SYSRS}}$, $\overline{\text{SCCRESET}}$, and $\overline{\text{HIBRESET}}$. See the Reset Signals table in the System Control chapter of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

The parameter $t_{h(boot\text{-}mode)}$ must account for a reset initiated from any of these sources.

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive $\overline{\text{XRS}}$ low. Use this to disable any other devices driving the boot pins. The $\overline{\text{SCCRESET}}$ and debugger reset sources do not drive $\overline{\text{XRS}}$; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP; for more details, see the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

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6.9.2.2 Reset Electrical Data and Timing

Section 6.9.2.2.1 shows the reset ($\overline{XRS}$) timing requirements. Section 6.9.2.2.2 shows the reset ($\overline{XRS}$) switching characteristics. Figure 6-5 shows the power-on reset. Figure 6-6 shows the warm reset.

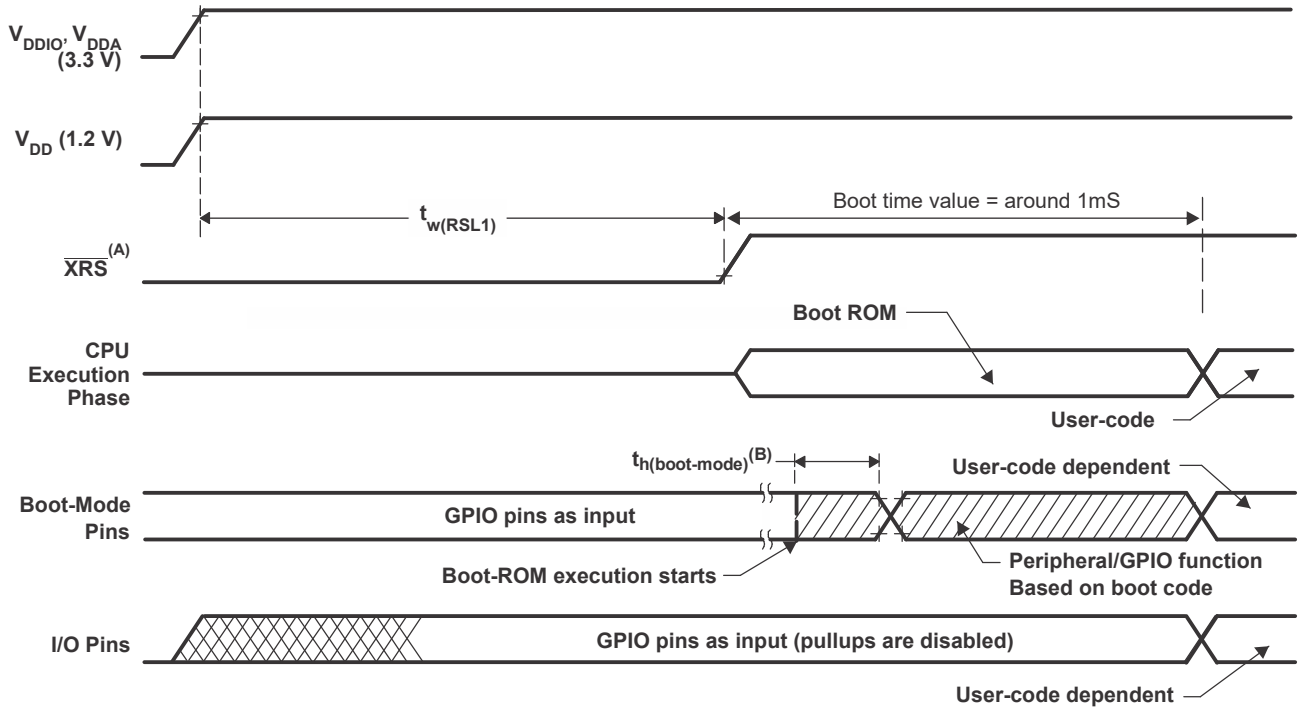
6.9.2.2.1 Reset ($\overline{XRS}$) Timing Requirements

			MIN	MAX	UNIT
$t_{h(boot-mode)}$	Hold time for boot-mode pins		1.5		ms
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low on warm reset	All cases	3.2		µs
		Low-power modes used in application and SYSCLKDIV > 16	3.2 * (SYSCLKDIV/16)		

6.9.2.2.2 Reset ($\overline{XRS}$) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{XRS}$ driven low by device after supplies are stable		100		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles

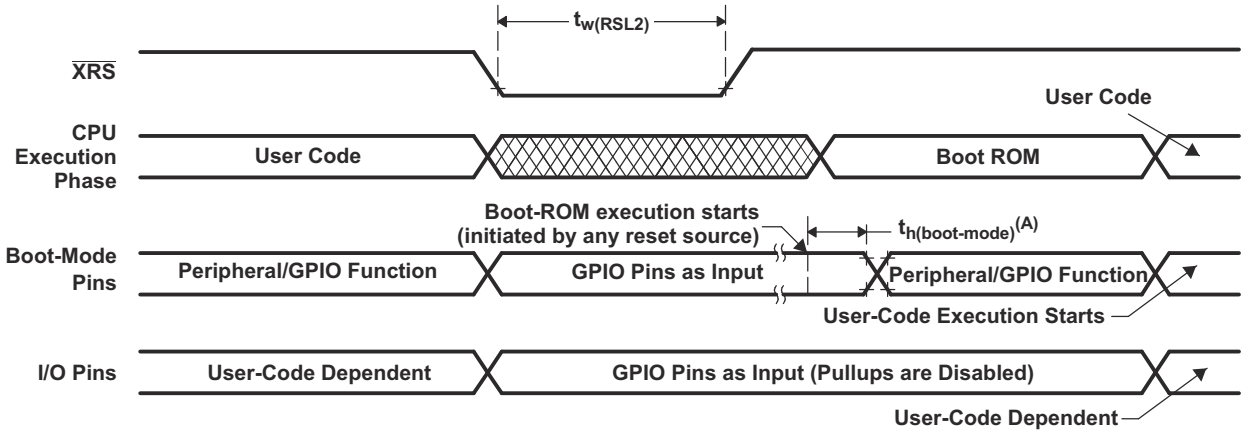


A. The $\overline{XRS}$ pin can be driven externally by a supervisor or an external pullup resistor, see Section 5.2.1.

B. After reset from any source (see Section 6.9.2.1), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-5. Power-on Reset

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A. After reset from any source (see Section 6.9.2.1), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-6. Warm Reset

6.9.3 Clock Specifications

6.9.3.1 Clock Sources

Table 6-2 lists four possible clock sources. Figure 6-7 provides an overview of the device's clocking system.

Table 6-2. Possible Reference Clock Sources

CLOCK SOURCE	MODULES CLOCKED	COMMENTS
INTOSC1	Can be used to provide clock for: • Watchdog block • CPU-Timer 2	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2(1)	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL	Can be used to provide clock for: • Main PLL • Auxiliary PLL • CPU-Timer 2	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.
AUXCLKIN	Can be used to provide clock for: • Auxiliary PLL • CPU-Timer 2	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

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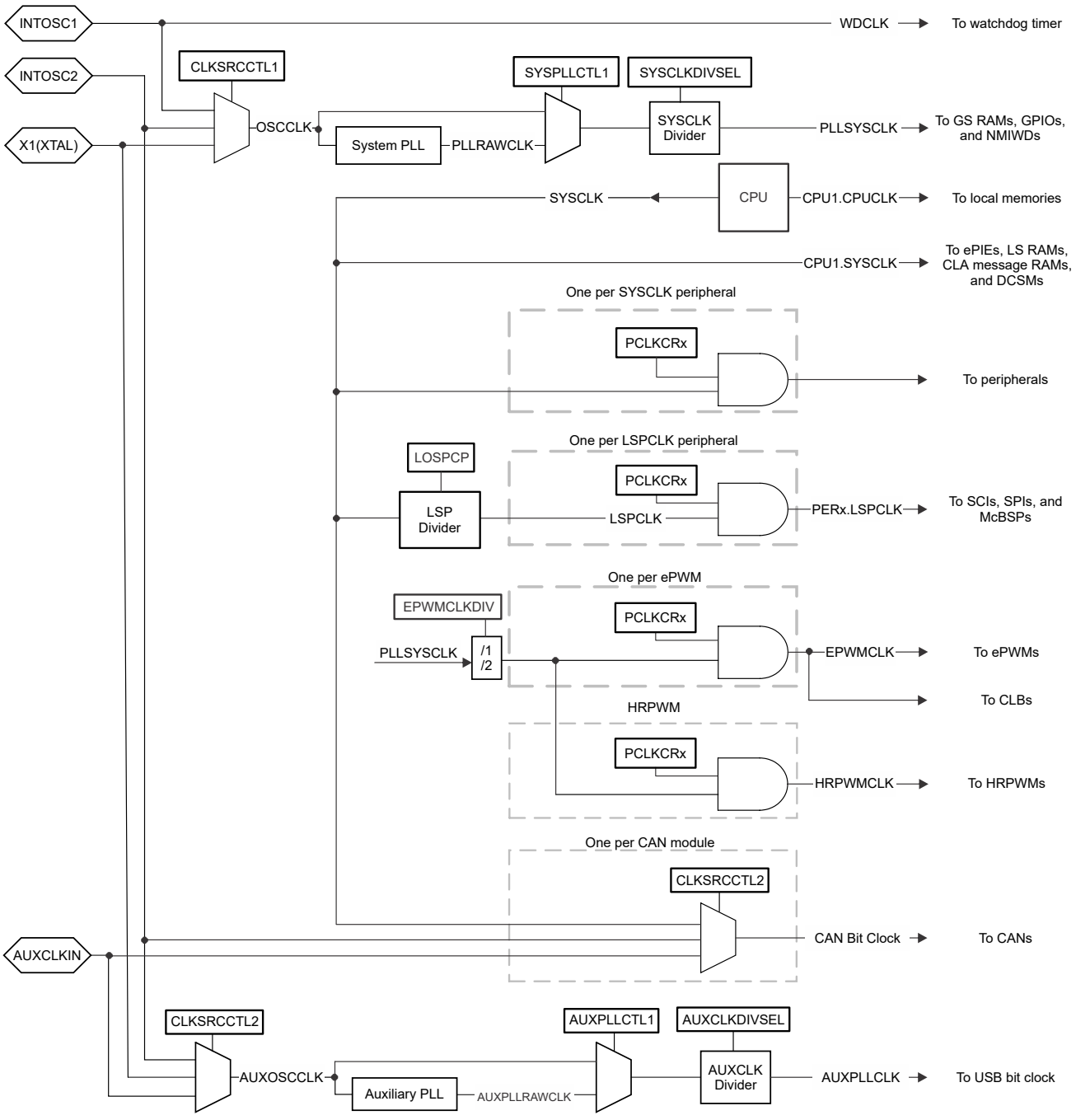


Figure 6-7. Clocking System

6.9.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.9.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

Section 6.9.3.2.1.1 shows the frequency requirements for the input clocks. The *Crystal Equivalent Series Resistance (ESR) Requirements* table shows the crystal equivalent series resistance requirements. Section 6.9.3.2.1.2 shows the X1 input level characteristics when using an external clock source. Section 6.9.3.2.1.4 and Section 6.9.3.2.1.5 show the timing requirements for the input clocks. Section 6.9.3.2.1.6 shows the PLL lock times for the Main PLL and the USB PLL.

6.9.3.2.1.1 Input Clock Frequency

		MIN	MAX	UNIT
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	2	25	MHz
$f_{(AUXI)}$	Frequency, AUXCLKIN, from external oscillator	2	60	MHz

6.9.3.2.1.2 X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3	0.3 * V_{DDIO}	V
X1 V_{IH}	Valid high-level input voltage	0.7 * V_{DDIO}	V_{DDIO} + 0.3	V

6.9.3.2.1.3 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3		0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

6.9.3.2.1.4 X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(X1)}$	Fall time, X1		6	ns
$t_{r(X1)}$	Rise time, X1		6	ns
$t_{w(X1L)}$	Pulse duration, X1 low as a percentage of $t_{c(X1)}$	45%	55%	
$t_{w(X1H)}$	Pulse duration, X1 high as a percentage of $t_{c(X1)}$	45%	55%	

6.9.3.2.1.5 AUXCLKIN Timing Requirements

		MIN	MAX	UNIT
$t_{f(AUXI)}$	Fall time, AUXCLKIN		6	ns
$t_{r(AUXI)}$	Rise time, AUXCLKIN		6	ns
$t_{w(AUXL)}$	Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$	45%	55%	
$t_{w(AUXH)}$	Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$	45%	55%	

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6.9.3.2.1.6 PLL Lock Times

		MIN	NOM	MAX	UNIT
$t_{(PLL)}$	Lock time, Main PLL (X1, from external oscillator)		50 µs + 2500 * $t_{c(OSCCLK)}$ (1)		µs
$t_{(USB)}$	Lock time, USB PLL (AUXCLKIN, from external oscillator)		50 µs + 2500 * $t_{c(OSCCLK)}$ (1)		µs

(1) The PLL lock time here defines the typical time of execution for the PLL workaround as defined in the *TMS320F2807x Real-Time MCUs Silicon Errata*. Cycle count includes code execution of the PLL initialization routine, which could vary depending on compiler optimizations and flash wait states. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock(). For the auxiliary PLL, see InitAuxPll() or SysCtl_setAuxClock().

6.9.3.2.2 Internal Clock Frequencies

Section 6.9.3.2.2.1 provides the clock frequencies for the internal clocks.

6.9.3.2.2.1 Internal Clock Frequencies

		MIN	NOM	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		120	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	8.33		500	ns
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	120		400	MHz
$f_{(AUXPLLRAWCLK)}$	Frequency, auxiliary PLL output (before AUXCLK divider)	120		400	MHz
$f_{(AUXPLL)}$	Frequency, AUXPLLCLK	2	60	60	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		120	MHz
$f_{(LSP)}$	Frequency, LSPCLK	2		120	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	8.33		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1)		See respective clock		MHz
$f_{(EPWM)}$	Frequency, EPWMCLK(1)			100	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60		100	MHz

(1) For SYSCLK above 100 MHz, the EPWMCLK must be half of SYSCLK.

6.9.3.2.3 Output Clock Frequency and Switching Characteristics

Section 6.9.3.2.3.1 provides the frequency of the output clock. Section 6.9.3.2.3.2 shows the switching characteristics of the output clock, XCLKOUT.

6.9.3.2.3.1 Output Clock Frequency

		MIN	MAX	UNIT
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

6.9.3.2.3.2 XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)

over recommended operating conditions (unless otherwise noted)

PARAMETER(1) (2)		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2	H + 2	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2	H + 2	ns

(1) A load of 40 pF is assumed for these parameters.
(2) H = 0.5$t_{c(XCO)}$

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6.9.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, multiple external clock source options are available. Figure 6-8 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 (also referred to as XTAL) and AUXCLKIN.

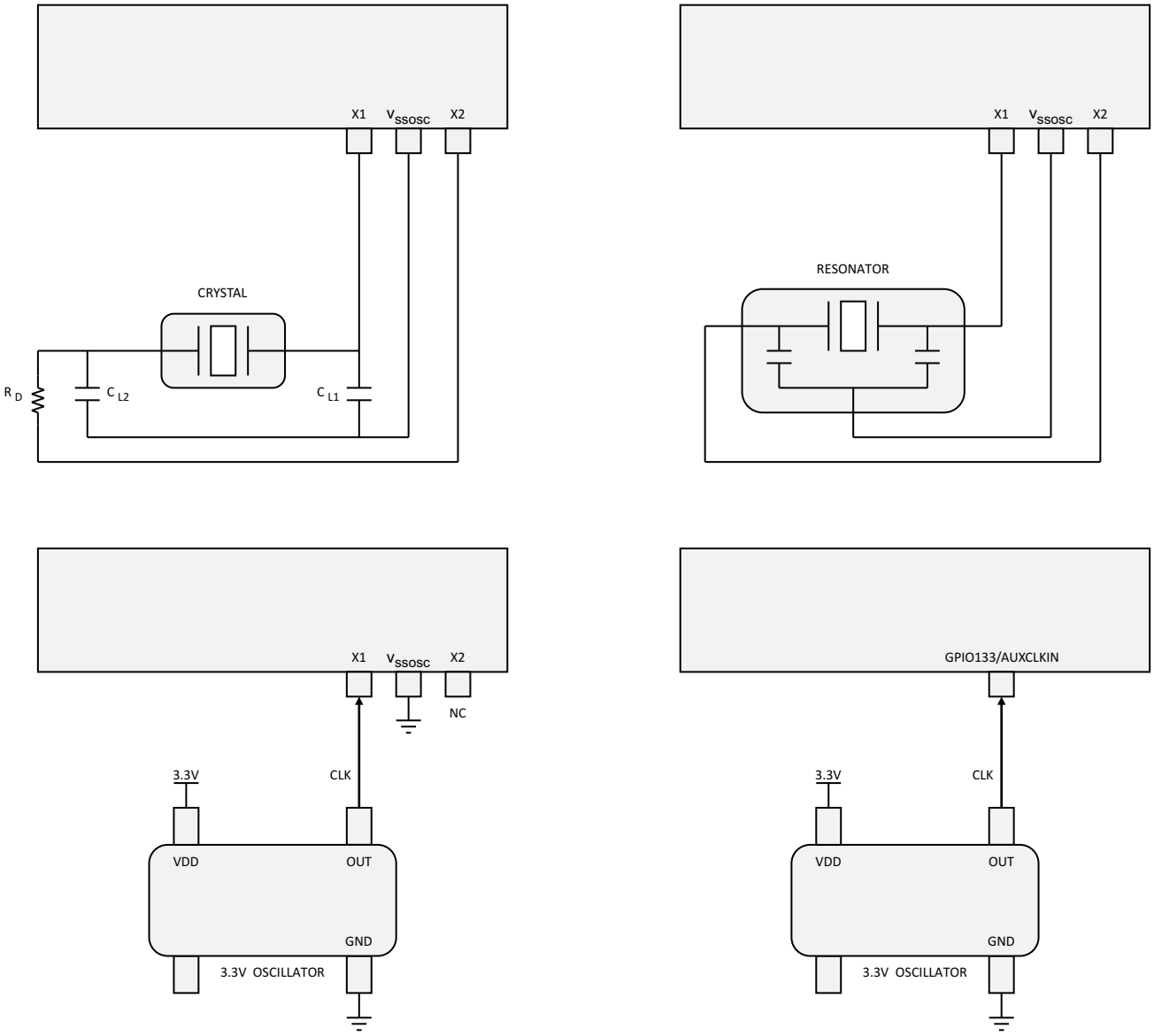


Figure 6-8. Connecting Input Clocks to a 2807x Device

6.9.3.4 XTAL Oscillator

6.9.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.9.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

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6.9.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). Figure 6-9 illustrates the components of the electrical oscillator and the tank circuit.

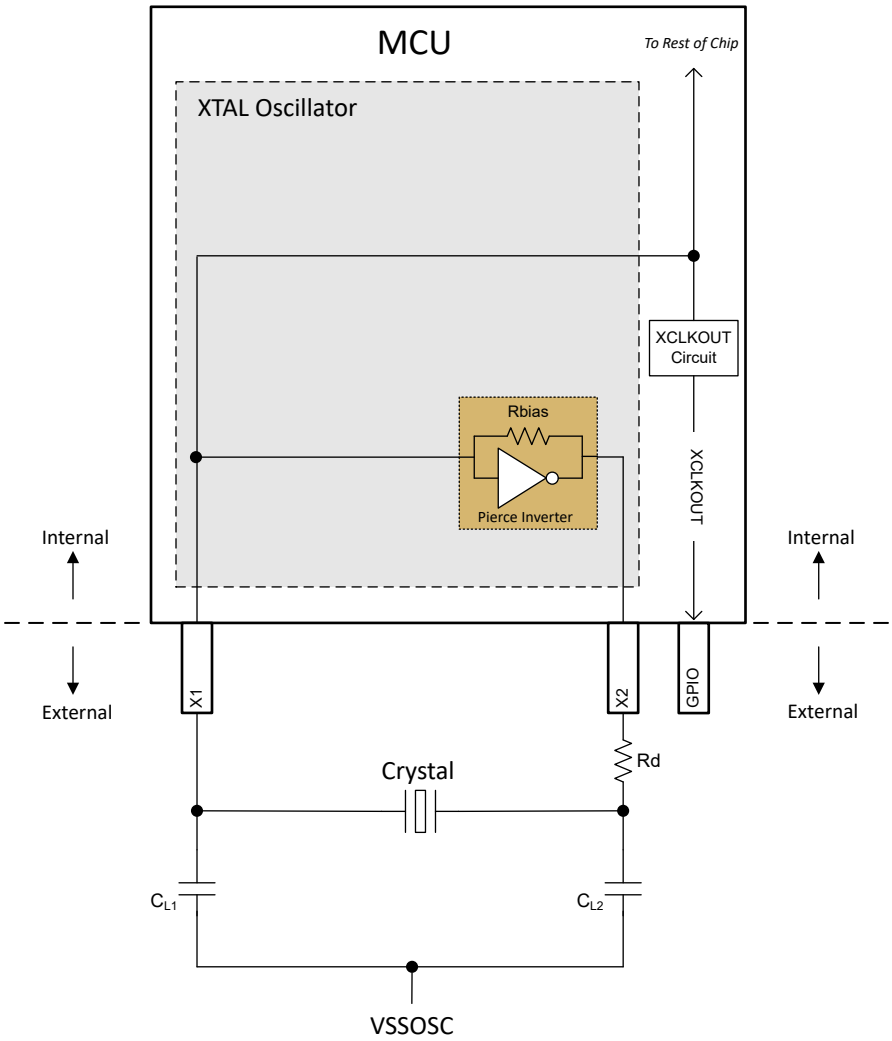


Figure 6-9. Electrical Oscillator Block Diagram

6.9.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.9.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal Rbias, moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed to the rest of the chip. The clock on X1 needs to meet the VIH and VIL of the comparator. See the *XTAL Oscillator Characteristics* table for the VIH and VIL requirements of the comparator.

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6.9.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

In this mode of operation, the clock on X1 is passed to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

A single-ended clock may also be connected to GPIO133/AUXCLKIN pin.

6.9.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the GPIO Muxed Pins table for a list of GPIOs that XCLKOUT comes out on.

6.9.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in Figure 6-10 and explained below.

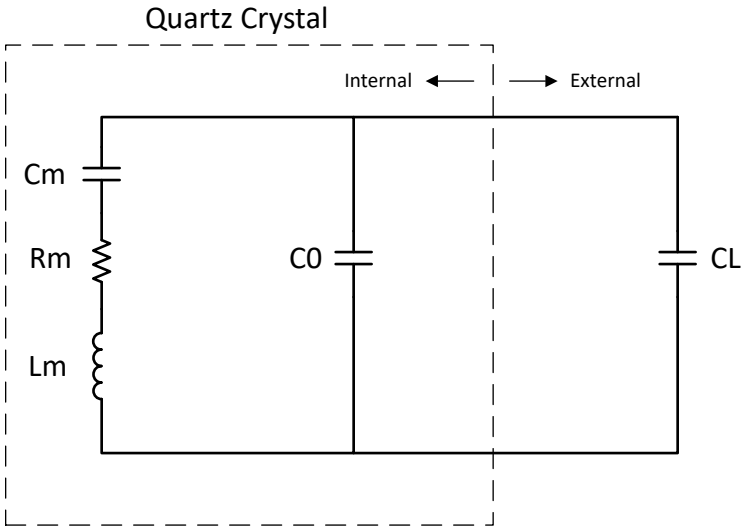


Figure 6-10. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From Figure 6-9, CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to [CL1]/2 if CL1 = CL2.

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It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.9.3.4.3 Functional Operation

6.9.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = Rm * \left(1 + \frac{C0}{CL}\right)^2 \quad (1)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.9.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

Figure 6-11 and Figure 6-12 show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to Table 6-3 for minimum and maximum values for design considerations.

6.9.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the Rneg – Negative Resistance section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to Crystal Oscillator Specifications for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.9.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer's data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

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For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (Rd) should be installed to limit the current and reduce the power dissipated by the crystal. Note that Rd reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.9.3.4.4 How to Choose a Crystal

Using Crystal Oscillator Specifications as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal <=50 Ω per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
   - As mentioned, CL1 and CL2 are in series; so, provided CL1 = CL2, effective load capacitance CL = [CL1]/2.
   - Adding board parasitics to this results in CL = [CL1]/2 + Cstray
4. Check that the maximum drive level of the crystal >= 1 mW. If this requirement is not met, a dampening resistor Rd can be used. Refer to DL – Drive Level on other points to consider when using Rd.

6.9.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1-pF input capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal's actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.9.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the How to Choose a Crystal section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor Rd is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

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6.9.3.4.7 Crystal Oscillator Specifications

6.9.3.4.7.1 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time[1]	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF		4		ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.9.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the Crystal Equivalent Series Resistance (ESR) Requirements table:

1. Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
2. ESR = Negative Resistance/3

Table 6-3. Crystal Equivalent Series Resistance (ESR) Requirements

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

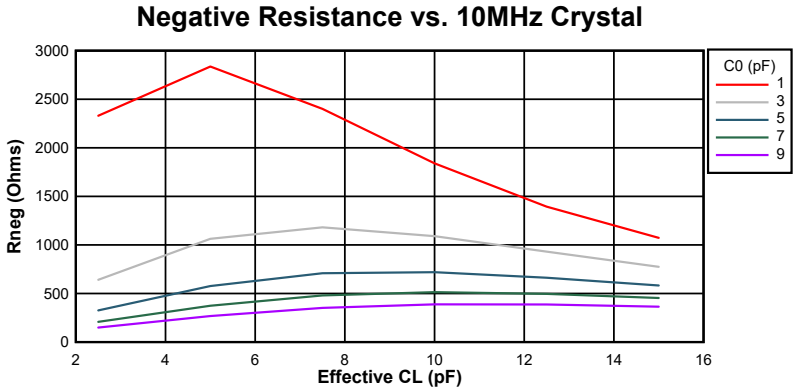


Figure 6-11. Negative Resistance Variation at 10 MHz

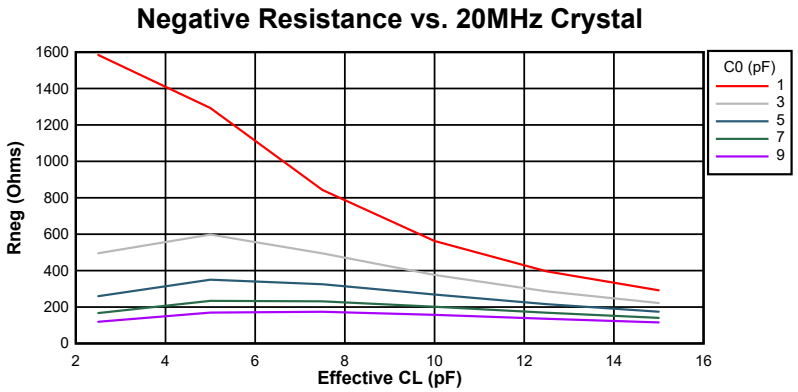


Figure 6-12. Negative Resistance Variation at 20 MHz

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6.9.3.5 Internal Oscillators

To reduce production board costs and application development time, all F2807x devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, both oscillators are enabled at power up. INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source. INTOSC1 can also be manually configured as the system reference clock (OSCCLK). Section 6.9.3.5.1 provides the electrical characteristics of the internal oscillators to determine if this module meets the clocking requirements of the application.

Section 6.9.3.5.1 provides the electrical characteristics of the two internal oscillators.

6.9.3.5.1 Internal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(INTOSC)}$	Frequency, INTOSC1 and INTOSC2		9.7	10.0	10.3	MHz
$f_{(INTOSC-STABILITY)}$	Frequency stability at room temperature	30°C, Nominal V_{DD}		±0.1%		
	Frequency stability over V_{DD}	30°C		±0.2%		
	Frequency stability		–3.0%		3.0%	
$f_{(INTOSC-ST)}$	Start-up and settling time				20	µs

6.9.4 Flash Parameters

The on-chip flash memory is tightly integrated to the CPU, allowing code execution directly from flash through 128-bit-wide prefetch reads and a pipeline buffer. Flash performance for sequential code is equal to execution from RAM. Factoring in discontinuities, most applications will run with an efficiency of approximately 80% relative to code executing from RAM.

This device also has an OTP (One-Time-Programmable) sector used for the dual code security module (DCSM), which cannot be erased after it is programmed.

Table 6-4 shows the minimum required flash wait states at different frequencies. Section 6.9.4.1 shows the flash parameters.

Table 6-4. Flash Wait States

CPUCLK (MHz)		MINIMUM WAIT STATES (1)
EXTERNAL OSCILLATOR OR CRYSTAL	INTOSC1 OR INTOSC2	
100 < CPUCLK ≤ 120	97 < CPUCLK ≤ 120	2
50 < CPUCLK ≤ 100	48 < CPUCLK ≤ 97	1
CPUCLK ≤ 50	CPUCLK ≤ 48	0

(1) Minimum required FRDCNTL[RWAIT].

6.9.4.1 Flash Parameters

PARAMETER			MIN	TYP	MAX	UNIT
	Program Time(1)	128 data bits + 16 ECC bits		40	300	µs
		8KW sector		100	200	ms
		32KW sector		400	800	ms
	Erase Time(2) at < 25 cycles	8KW or 32KW sector		30	55	ms
	Erase Time(2) at < 1000 cycles	8KW or 32KW sector		40	350	
	Erase Time(2) at 2000 cycles	8KW or 32KWsector		50	600	ms
	Erase Time(2) at 20k cycles	8KW or 32KW sector		110	4000	
N_{wec}	Write/erase cycles per sector				20000	cycles
N_{wec}	Write/Erase Cycles for entire Flash (combined all sectors)(3)				100000	cycles
$t_{retention}$	Data retention duration at T_J = 85°C		20			years

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

(3) Each sector, by itself, can only be erased/programmed 20,000 times. If you choose to use a sector (or multiple sectors) like an EEPROM, you can erase/program only those sectors (still limited to 20,000 cycles) without erasing/programming the entire Flash memory. Therefore, the total number of W/E cycles from a device perspective can exceed 20,000 cycles. However, even this number should not exceed 100,000 cycles.

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Note

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle. For more details, see the "Flash: Minimum Programming Word Size" advisory in the *TMS320F2807x Real-Time MCUs Silicon Errata*.

6.9.5 RAM Specifications

Table 6-5. CPU RAM Parameters

RAM TYPE	SIZE	FETCH TIME (Cycles)	READ TIME (Cycles)	STORE TIME (Cycles)	BUS WIDTH	NUMBER OF BUSSES AVAILABLE(1)	NUMBER OF WAIT STATES	BURST ACCESS
GS RAM	64KB	2	2	1	16/32 bits	4	0	No
LS RAM	24KB	2	2	1	16/32 bits	2	0	No
M0	2KB	2	2	1	16/32 bits	1	0	No
M1	2KB	2	2	1	16/32 bits	1	0	No
CLA to CPU Message RAM	256B	2	2	1	16/32 bits	2	0	No
CPU to CLA Message RAM	256B	2	2	1	16/32 bits	2	0	No

(1) “Number of Buses Available” indicates how many masters (CLA, DMA, CPU) have access to this memory.

6.9.6 ROM Specifications

Table 6-6. CPU ROM Parameters

ROM TYPE	SIZE	FETCH TIME (Cycles)	READ TIME (Cycles)	STORE TIME (Cycles)	BUS WIDTH	NUMBER OF BUSSES AVAILABLE(1)	NUMBER OF WAIT STATES	BURST ACCESS
Boot ROM	64KB	2	2	1	16/32 bits	1	1	No
Secure ROM	64KB	2	2	1	16/32 bits	1	1	No
CLA Data ROM	8KB	2	2	1	16/32 bits	2	0	No

(1) “Number of Buses Available” indicates how many masters (CLA, DMA, CPU) have access to this memory.

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6.9.7 Emulation/JTAG

The JTAG port has five dedicated pins: $\overline{\text{TRST}}$, TMS, TDI, TDO, and TCK. The $\overline{\text{TRST}}$ signal should always be pulled down through a 2.2-kΩ pulldown resistor on the board. This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

See Figure 6-13 to see how the 14-pin JTAG header connects to the MCU's JTAG port signals. Figure 6-14 shows how to connect to the 20-pin header. The 20-pin JTAG header terminals EMU2, EMU3, and EMU4 are not used and should be grounded.

The PD (Power Detect) terminal of the JTAG debug probe header should be connected to the board 3.3-V supply. Header GND terminals should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output terminal back to the RTCK input terminal of the header (to sense clock continuity by the JTAG debug probe). Header terminal $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header).

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints for C28x in CCS.

For more information about JTAG emulation, see the *XDS Target Connection Guide*.

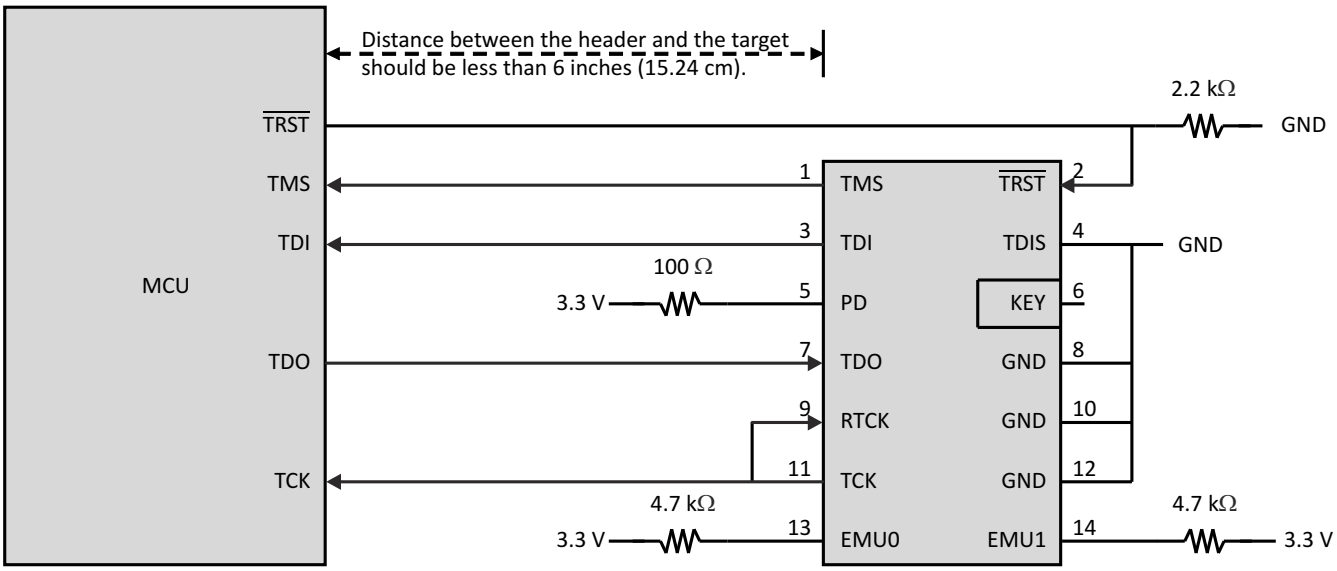


Figure 6-13. Connecting to the 14-Pin JTAG Header

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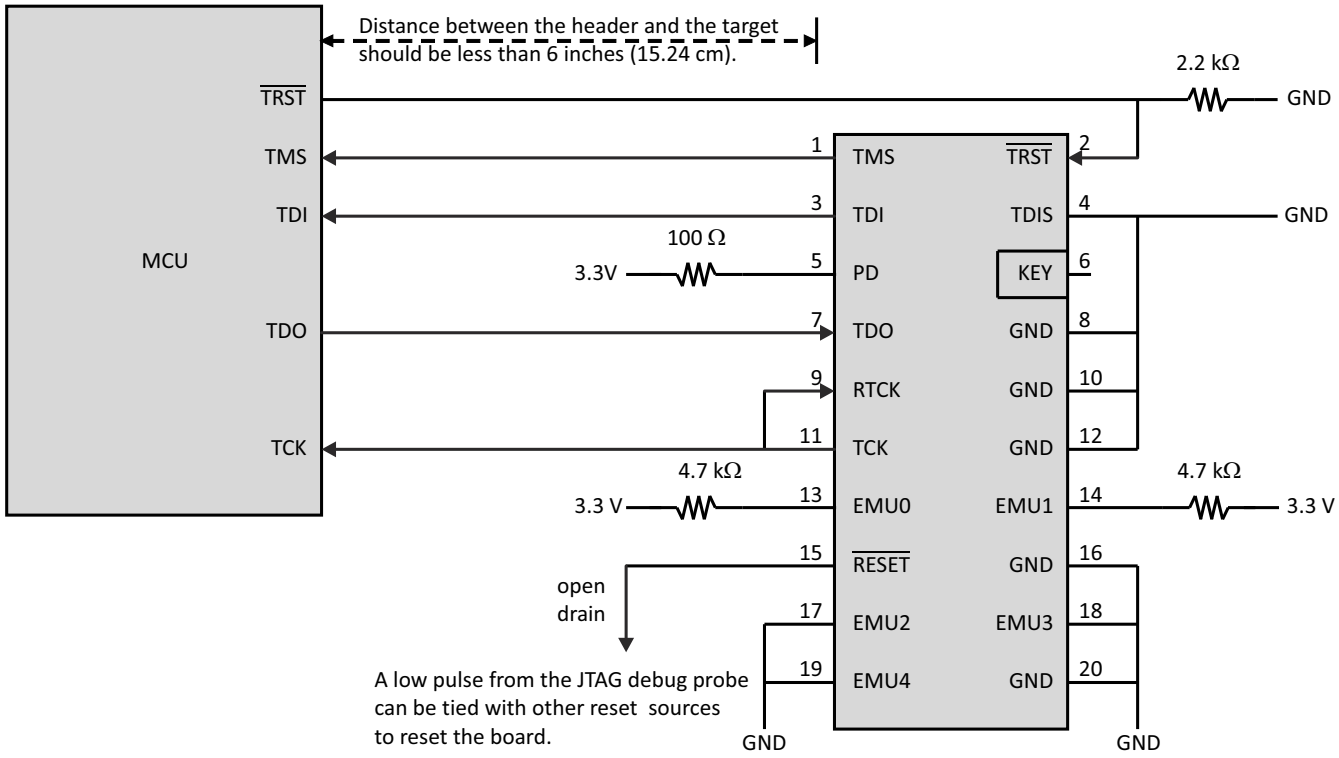


Figure 6-14. Connecting to the 20-Pin JTAG Header

6.9.7.1 JTAG Electrical Data and Timing

Section 6.9.7.1.1 lists the JTAG timing requirements. Section 6.9.7.1.2 lists the JTAG switching characteristics. Figure 6-15 shows the JTAG timing.

6.9.7.1.1 JTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	13		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	13		ns
4	$t_{h(TCKH-TDI)}$	Input hold time, TDI valid from TCK high	7		ns
	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	7		ns

6.9.7.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid	6	25	ns

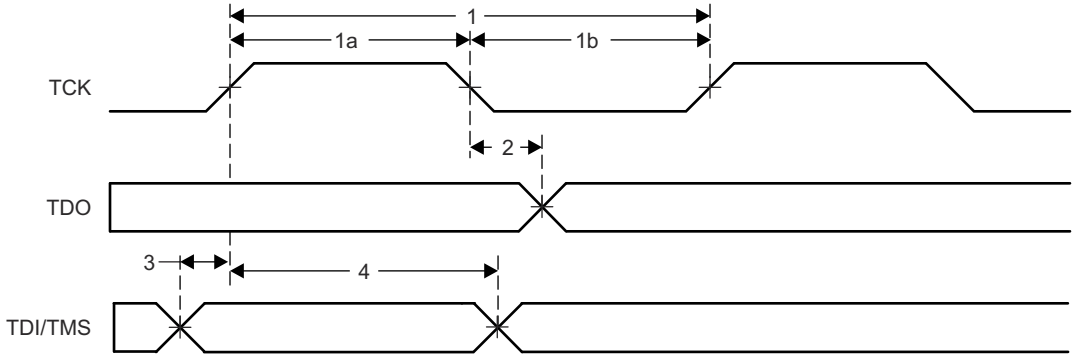


Figure 6-15. JTAG Timing

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6.9.8 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADC(s), eCAP(s), ePWM(s), and external interrupts. For more details, see the X-BAR chapter in the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

6.9.8.1 GPIO - Output Timing

Section 6.9.8.1.1 shows the general-purpose output switching characteristics. Figure 6-16 shows the general-purpose output timing.

6.9.8.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8(1)	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8(1)	ns
t_{fGPO}	Toggling frequency, GPO pins			25	MHz

(1) Rise time and fall time vary with load. These values assume a 40-pF load.

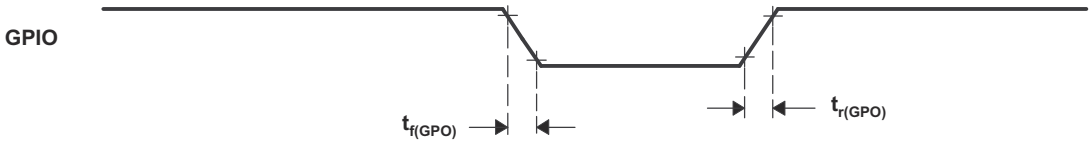


Figure 6-16. General-Purpose Output Timing

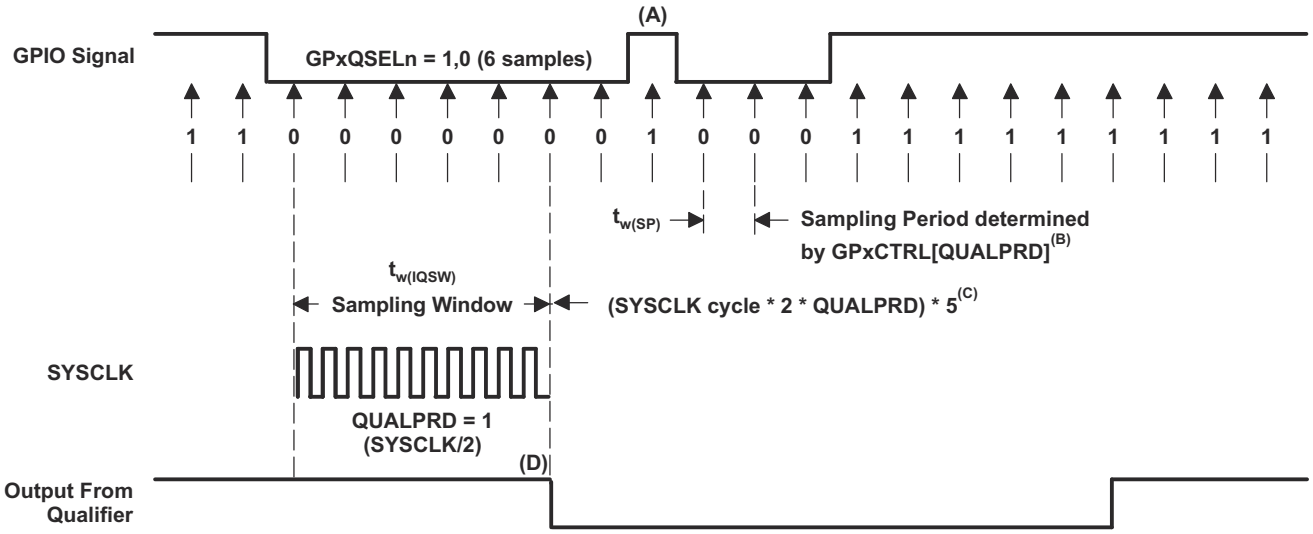
6.9.8.2 GPIO - Input Timing

Section 6.9.8.2.1 shows the general-purpose input timing requirements. Figure 6-17 shows the sampling mode.

6.9.8.2.1 General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
B. The qualification period selected through the GPxCTRL register applies to groups of 8 GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 6-17. Sampling Mode

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6.9.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

$$\text{Sampling frequency} = \text{SYSCLK}/(2 \times \text{QUALPRD}), \text{ if QUALPRD} \neq 0 \quad (2)$$

$$\text{Sampling frequency} = \text{SYSCLK}, \text{ if QUALPRD} = 0 \quad (3)$$

$$\text{Sampling period} = \text{SYSCLK cycle} \times 2 \times \text{QUALPRD}, \text{ if QUALPRD} \neq 0 \quad (4)$$

In Equation 2, Equation 3, and Equation 4, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

Figure 6-18 shows the general-purpose input timing.

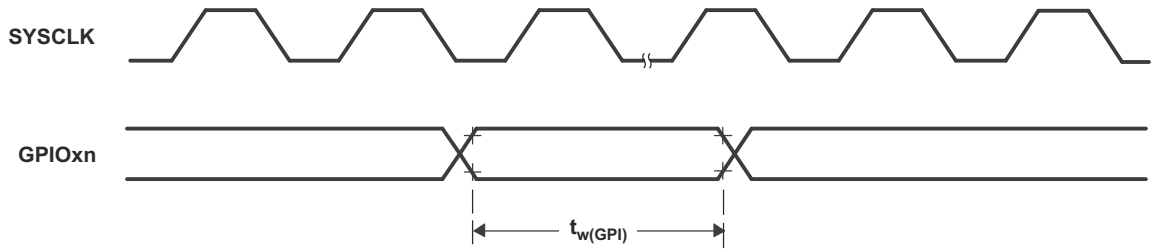


Figure 6-18. General-Purpose Input Timing

6.9.9 Interrupts

Figure 6-19 provides a high-level view of the interrupt architecture.

As shown in Figure 6-19, the devices support five external interrupts (XINT1 to XINT5) that can be mapped onto any of the GPIO pins.

In this device, 16 ePIE block interrupts are grouped into 1 CPU interrupt. In total, there are 12 CPU interrupt groups, with 16 interrupts per group.

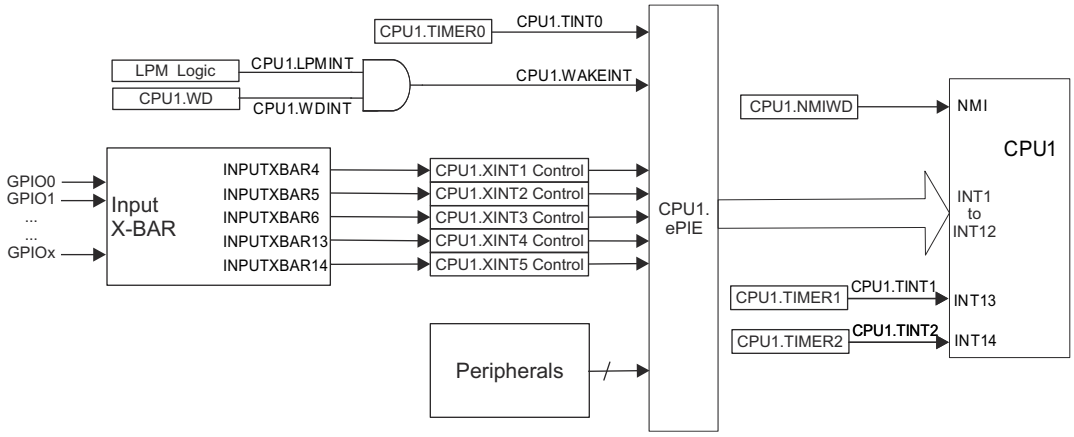


Figure 6-19. External and ePIE Interrupt Sources

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6.9.9.1 External Interrupt (XINT) Electrical Data and Timing

Section 6.9.9.1.1 lists the external interrupt timing requirements. Section 6.9.9.1.2 lists the external interrupt switching characteristics. Figure 6-20 shows the external interrupt timing.

6.9.9.1.1 External Interrupt Timing Requirements

			MIN	MAX	UNIT[1]
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.

6.9.9.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)[1]

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch[2]	$t_{w(IQSW)} + 14t_{c(SYSCLK)}$	$t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$	cycles

(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.
(2) This assumes that the ISR is in a single-cycle memory.

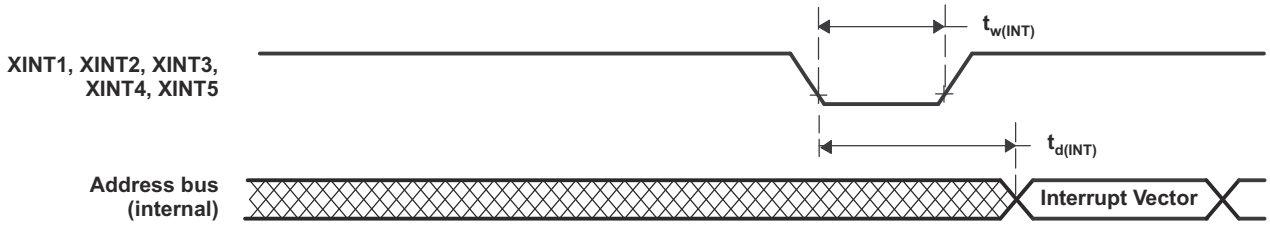


Figure 6-20. External Interrupt Timing

6.9.10 Low-Power Modes

This device has three clock-gating low-power modes and a special power-gating mode.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the Low Power Modes section of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

6.9.10.1 Clock-Gating Low-Power Modes

IDLE, STANDBY, and HALT modes on this device are similar to those on other C28x devices. Table 6-7 describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-7. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/ CLOCK DOMAIN	CPU1 IDLE	CPU1 STANDBY	HALT
CPU1.CLKIN	Active	Gated	Gated
CPU1.SYSCLK	Active	Gated	Gated
CPU1.CPUCLK	Gated	Gated	Gated
Clock to modules Connected to PERx.SYSCLK	Active	Gated	Gated
CPU1.WDCLK	Active	Active	Gated if CLKSRCCTL1.WDHALTI = 0
AUXPLLCLK	Active	Active	Gated
PLL	Powered	Powered	Software must power down PLL before entering HALT
INTOSC1	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
INTOSC2	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash	Powered	Powered	Software-Controlled
X1/X2 Crystal Oscillator	Powered	Powered	Powered-Down

6.9.10.2 Power-Gating Low-Power Modes

HIBERNATE mode is the lowest power mode on this device. It is a global low-power mode that gates the supply voltages to most of the system. HIBERNATE is essentially a controlled power-down with remote wakeup capability, and can be used to save power during long periods of inactivity. Table 6-8 describes the effects on the system when the HIBERNATE mode is entered.

Table 6-8. Effect of Power-Gating Low-Power Mode on the Device

MODULES/POWER DOMAINS	HIBERNATE
M0 and M1 memories	• Remain on with memory retention if LPMCR.M0M1MODE = 0x00 • Are off when LPMCR.M0M1MODE = 0x01
CPU1 digital peripherals	Powered down
Dx, LSx, GSx memories	Power down, memory contents are lost
I/Os	On with output state preserved
Oscillators, PLL, analog peripherals, Flash	Enters Low-Power Mode

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6.9.10.3 Low-Power Mode Wakeup Timing

Section 6.9.10.3.1 shows the IDLE mode timing requirements, Section 6.9.10.3.2 shows the switching characteristics, and Figure 6-21 shows the timing diagram for IDLE mode.

6.9.10.3.1 IDLE Mode Timing Requirements

			MIN	MAX	UNIT(1)
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

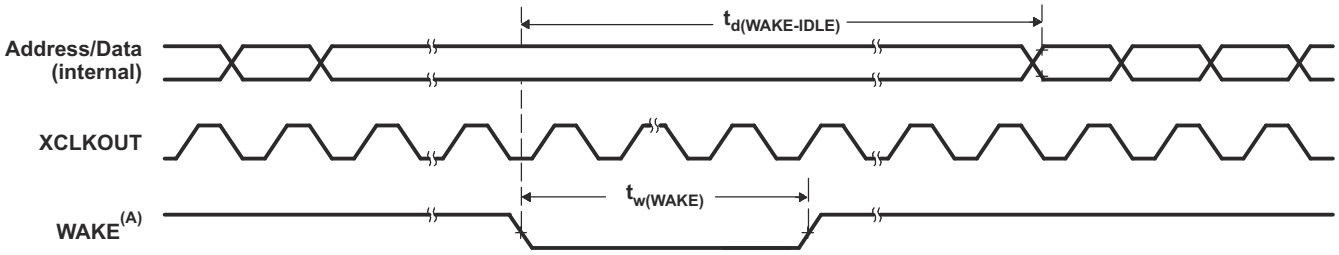
(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.

6.9.10.3.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)				cycles
	• Wakeup from Flash – Flash module in active state	Without input qualifier		$40t_{c(SYSCLK)}$	
		With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	
	• Wakeup from Flash – Flash module in sleep state	Without input qualifier		$6700t_{c(SYSCLK)}$ (3)	
		With input qualifier		$6700t_{c(SYSCLK)}$ (3) $+ t_{w(WAKE)}$	
	• Wakeup from RAM	Without input qualifier		$25t_{c(SYSCLK)}$	
		With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	

(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.
(3) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*. This value can be realized when SYSCLK is 120 MHz, RWAIT is 2, and FPAC1[PSLEEP] is 0x860.



A. WAKE can be any enabled interrupt, $\overline{WDINT}$ or $\overline{XRS}$. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-21. IDLE Entry and Exit Timing Diagram

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Section 6.9.10.3.3 shows the STANDBY mode timing requirements, Section 6.9.10.3.4 shows the switching characteristics, and Figure 6-22 shows the timing diagram for STANDBY mode.

6.9.10.3.3 STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	QUALSTDBY = 0 | $2t_{c(OSCCLK)}$	$3t_{c(OSCCLK)}$		cycles
		QUALSTDBY > 0 | (2 + QUALSTDBY)$t_{c(OSCCLK)}$ (1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

6.9.10.3.4 STANDBY Mode Switching Characteristics

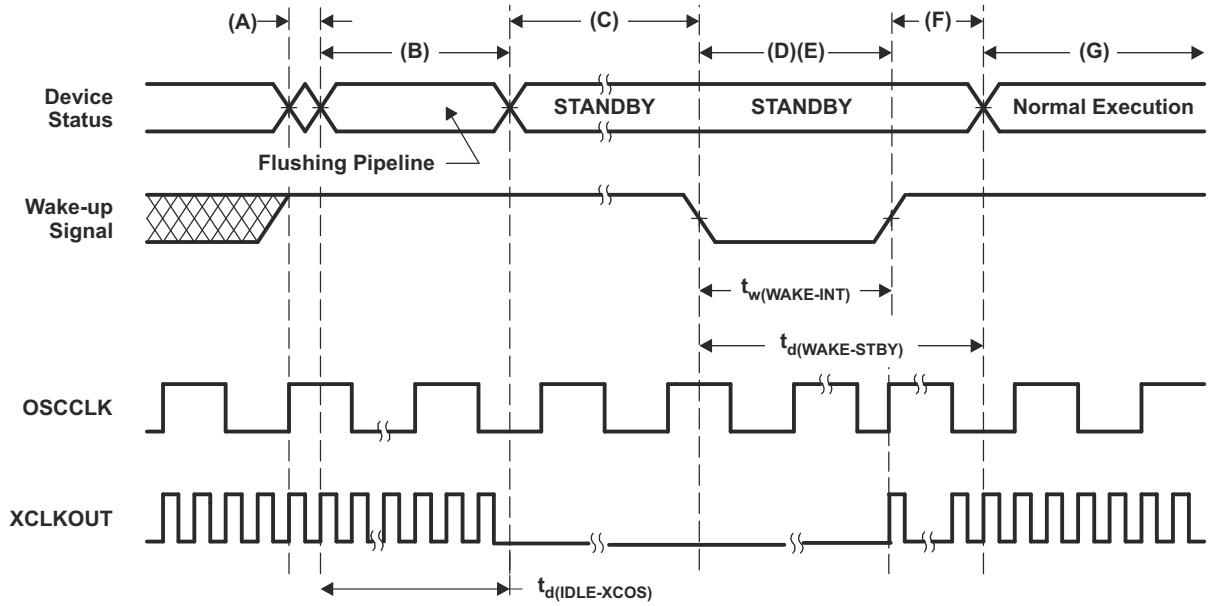
over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)				cycles
	• Wakeup from flash – Flash module in active state			$175t_{c(SYSCLK)}$ + $t_{w(WAKE-INT)}$	
	• Wakeup from flash – Flash module in sleep state			$6700t_{c(SYSCLK)}$ (2) + $t_{w(WAKE-INT)}$	
	• Wakeup from RAM			$3t_{c(OSC)}$ + $15t_{c(SYSCLK)}$ + $t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

(2) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*. This value can be realized when SYSCLK is 120 MHz, RWAIT is 2, and FPAC1[PSLEEP] is 0x860.

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A. IDLE instruction is executed to put the device into STANDBY mode.
B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wakeup behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wakeup pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-22. STANDBY Entry and Exit Timing Diagram

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Section 6.9.10.3.5 shows the HALT mode timing requirements, Section 6.9.10.3.6 shows the switching characteristics, and Figure 6-23 shows the timing diagram for HALT mode.

6.9.10.3.5 HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal[1]	$t_{oscst} + 2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal[1]	$t_{oscst} + 8t_{c(OSCCLK)}$		cycles

(1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See the *Crystal Oscillator Electrical Characteristics* section for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see Section 6.9.3.5 for t_{oscst}. Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

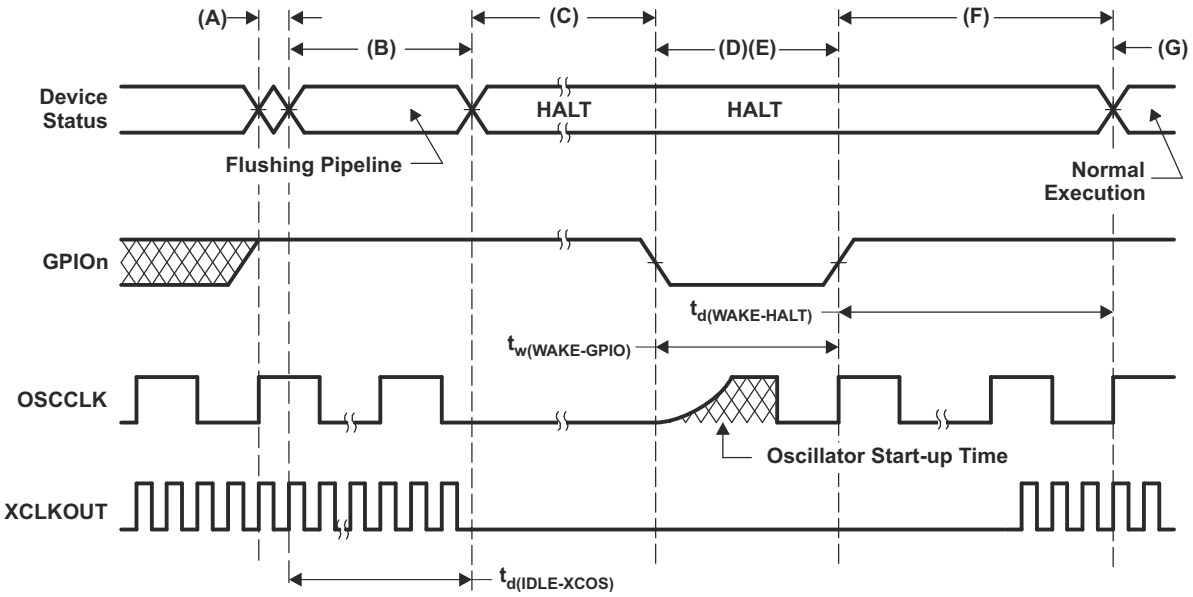
6.9.10.3.6 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$16t_{c(INTOSC1)}$	cycles
$t_{d(WAKE-HALT)}$	Delay time, external wake signal end to CPU1 program execution resume			cycles
	• Wakeup from flash – Flash module in active state		$75t_{c(OSCCLK)}$	
	• Wakeup from flash – Flash module in sleep state		$17500t_{c(OSCCLK)}$ [1]	
	• Wakeup from RAM		$75t_{c(OSCCLK)}$	

(1) This value is based on the flash power-up time, which is a function of the SYSCLK frequency, flash wait states (RWAIT), and FPAC1[PSLEEP]. For more information, see the Flash and OTP Power-Down Modes and Wakeup section of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*. This value can be realized when SYSCLK is 120 MHz, RWAIT is 2, and FPAC1[PSLEEP] is 0x860.

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A. IDLE instruction is executed to put the device into HALT mode.
B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing a 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wakeup sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wakeup behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wakeup pulses.
F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
G. Normal operation resumes.
H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 6-23. HALT Entry and Exit Timing Diagram

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Section 6.9.10.3.7 shows the HIBERNATE mode timing requirements, Section 6.9.10.3.8 shows the switching characteristics, and Figure 6-24 shows the timing diagram for HIBERNATE mode.

6.9.10.3.7 HIBERNATE Mode Timing Requirements

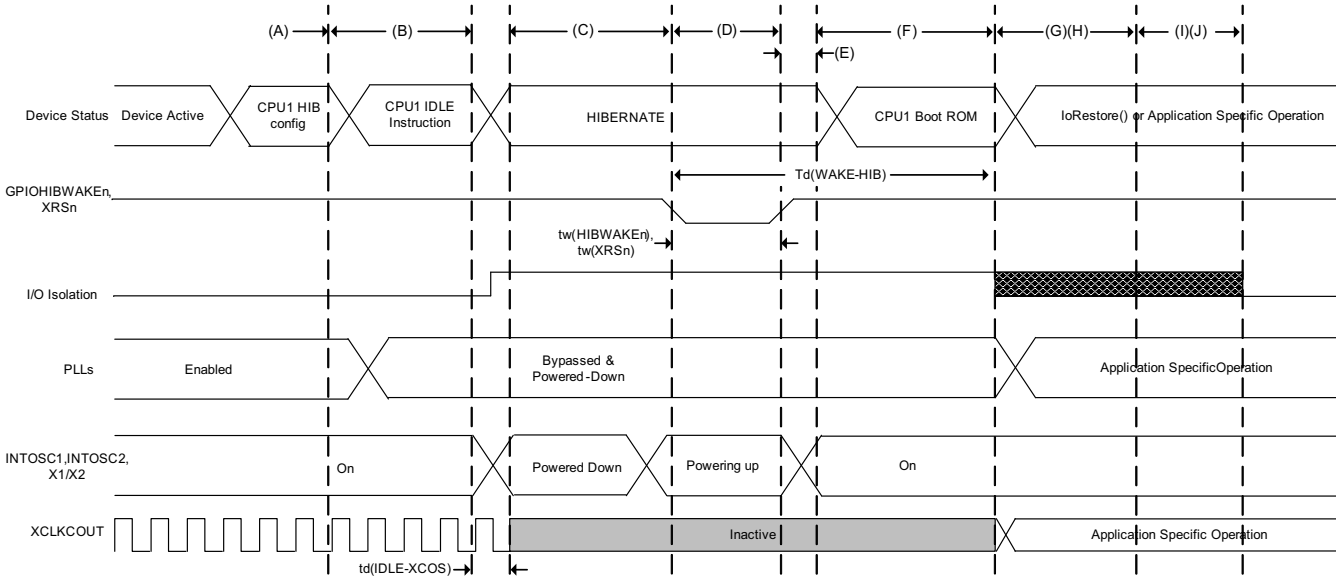
		MIN	MAX	UNIT
$t_{w(HIBWAKE)}$	Pulse duration, $\overline{\text{HIBWAKE}}$ signal	40		µs
$t_{w(WAKEXRS)}$	Pulse duration, $\overline{\text{XRS}}$ wake-up signal	40		µs

6.9.10.3.8 HIBERNATE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$30t_{c(SYSCLK)}$	cycles
$t_{d(WAKE-HIB)}$	Delay time, external wake signal to IORestore function start		1.5	ms

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A. CPU1 does necessary application-specific context save to M0/M1 memories if required. This includes GPIO state if using I/O Isolation. Configures the LPMCR register of CPU1 for HIBERNATE mode. Powers down Flash Pump/Bank, USB-PHY, CMPSS, DAC, and ADC using their register configurations. The application should also power down the PLL and peripheral clocks before entering HIBERNATE.
B. IDLE instruction is executed to put the device into HIBERNATE mode.
C. The device is now in HIBERNATE mode. If configured, I/O isolation is turned on, M0 and M1 memories are retained. CPU1 is powered down. Digital peripherals are powered down. The oscillators, PLLs, analog peripherals, and Flash are in their software-controlled Low-Power modes. Dx, LSx, and GSx memories are also powered down, and their memory contents lost.
D. A falling edge on the GPIOHIBWAKEn pin will drive the wakeup of the devices clock sources INTOSC1, INTOSC2, and X1/X2 OSC. The wakeup source must keep the GPIOHIBWAKEn pin low long enough to ensure full power-up of these clock sources.
E. After the clock sources are powered up, the GPIOHIBWAKEn must be driven high to trigger the wakeup sequence of the remainder of the device.
F. The BootROM will then begin to execute. The BootROM can distinguish a HIBERNATE wakeup by reading the CPU1.REC.HIBRESETn bit. After the TI OTP trims are loaded, the BootROM code will branch to the user-defined IoRestore function if it has been configured.
G. At this point, the device is out of HIBERNATE mode, and the application may continue.
H. The IoRestore function is a user-defined function where the application may reconfigure GPIO states, disable I/O isolation, reconfigure the PLL, restore peripheral configurations, or branch to application code. This is up to the application requirements.
I. If the application has not branched to application code, the BootROM will continue after completing IoRestore. It will disable I/O isolation automatically if it was not taken care of inside of IoRestore.
J. BootROM will then boot as determined by the HIBBOOTMODE register. Refer to the ROM Code and Peripheral Booting chapter of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual* for more information.

Figure 6-24. HIBERNATE Entry and Exit Timing Diagram

Note

1. If the IORESTOREADDR is configured as the default value, the BootROM will continue its execution to boot as determined by the HIBBOOTMODE register. Refer to the ROM Code and Peripheral Booting chapter of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual* for more information.
2. The user may choose to disable I/O Isolation at any point in the IoRestore function. Regardless if the user has disabled Isolation in the IoRestore function or if IoRestore is not defined, the BootROM will automatically disable isolation before booting as determined by the HIBBOOTMODE register.

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6.9.11 External Memory Interface (EMIF)

The EMIF provides a means of connecting the CPU to various external storage devices like asynchronous memories (SRAM, NOR flash) or synchronous memory (SDRAM).

6.9.11.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects ($\overline{\text{EMIF_CS}}$[4:2]). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable time-out
- Select strobe option

6.9.11.2 Synchronous DRAM Support

The EMIF memory controller is compliant with the JESD21-C SDR SDRAMs that use a 32-bit or 16-bit data bus. The EMIF has a single SDRAM chip select ($\overline{\text{EMIF_CS}}$[0]).

The address space of the EMIF, for the synchronous memory (SDRAM), lies beyond the 22-bit range of the program address bus and can only be accessed through the data bus, which places a restriction on the C compiler being able to work effectively on data in this space. Therefore, when using SDRAM, the user is advised to copy data (using the DMA) from external memory to RAM before working on it. See the examples in C2000Ware (C2000Ware for C2000 MCUs) and the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with 8-, 9-, 10-, and 11-column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents because the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. The EMIF module does not support mobile SDRAM devices.

On this device, the EMIF does not support burst access for SDRAM configurations. This means every access to an external SDRAM device will have CAS latency.

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6.9.11.3 EMIF Electrical Data and Timing

Note

This device has one EMIF interface. In this section, EMx denotes EM1.

6.9.11.3.1 Asynchronous RAM

Section 6.9.11.3.1.1 shows the EMIF asynchronous memory timing requirements. Section 6.9.11.3.1.2 shows the EMIF asynchronous memory switching characteristics. Figure 6-25 through Figure 6-28 show the EMIF asynchronous memory timing diagrams.

6.9.11.3.1.1 EMIF Asynchronous Memory Timing Requirements

NO.(1)			MIN	MAX	UNIT
Reads and Writes					
	E	EMIF clock period	$t_{c(SYSCLK)}$		ns
2	$t_{w(EM_WAIT)}$	Pulse duration, EMxWAIT assertion and deassertion	2E		ns
Reads					
12	$t_{su(EMDV-EMOEH)}$	Setup time, EMxD[y:0] valid before $\overline{EMxOE}$ high	15		ns
13	$t_{h(EMOEH-EMDIV)}$	Hold time, EMxD[y:0] valid after $\overline{EMxOE}$ high	0		ns
14	$t_{su(EMOEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20		ns
Writes					
28	$t_{su(EMWEL-EMWAIT)}$	Setup Time, EMxWAIT asserted before end of Strobe Phase(2)	4E+20		ns

(1) E = EMxCLK period in ns.
(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EMxWAIT must be asserted to add extended wait states. Figure 6-26 and Figure 6-28 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

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6.9.11.3.1.2 EMIF Asynchronous Memory Switching Characteristics

NO.[1] [2] [3]	PARAMETER		MIN	MAX	UNIT
Reads and Writes					
1	$t_{d(TURNAROUND)}$	Turn around time	(TA)*E–3	(TA)*E+2	ns
Reads					
3	$t_{c(EMRCYCLE)}$	EMIF read cycle time (EW = 0)	(RS+RST+RH)*E–3	(RS+RST+RH)*E+2	ns
		EMIF read cycle time (EW = 1)[4]	(RS+RST+RH+ (MEWC*16))*E–3	(RS+RST+RH+ (MEWC*16))*E+2	ns
4	$t_{su(EMCEL-EMOEL)}$	Output setup time, $\overline{EMxCS}$[y:2] low to $\overline{EMxOE}$ low (SS = 0)	(RS)*E–3	(RS)*E+2	ns
		Output setup time, $\overline{EMxCS}$[y:2] low to $\overline{EMxOE}$ low (SS = 1)	–3	2	ns
5	$t_{h(EMOEH-EMCEH)}$	Output hold time, $\overline{EMxOE}$ high to $\overline{EMxCS}$[y:2] high (SS = 0)	(RH)*E–3	(RH)*E	ns
		Output hold time, $\overline{EMxOE}$ high to $\overline{EMxCS}$[y:2] high (SS = 1)	–3	0	ns
6	$t_{su(EMBAV-EMOEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
7	$t_{h(EMOEH-EMBAIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxBA[y:0] invalid	(RH)*E–3	(RH)*E	ns
8	$t_{su(EMAV-EMOEL)}$	Output setup time, EMxA[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
9	$t_{h(EMOEH-EMAIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxA[y:0] invalid	(RH)*E–3	(RH)*E	ns
10	$t_{w(EMOEL)}$	$\overline{EMxOE}$ active low width (EW = 0)	(RST)*E–1	(RST)*E+1	ns
		$\overline{EMxOE}$ active low width (EW = 1) [4]	(RST+(MEWC*16))*E–1	(RST+(MEWC*16))*E+1	ns
11	$t_{d(EMWAITH-EMOEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxOE}$ high	4E+10	5E+15	ns
29	$t_{su(EMDQMV-EMOEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{EMxOE}$ low	(RS)*E–3	(RS)*E+2	ns
30	$t_{h(EMOEH-EMDQMIV)}$	Output hold time, $\overline{EMxOE}$ high to EMxDQM[y:0] invalid	(RH)*E–3	(RH)*E	ns
Writes					
15	$t_{c(EMWCYCLE)}$	EMIF write cycle time (EW = 0)	(WS+WST+WH)*E–3	(WS+WST+WH)*E+1	ns
		EMIF write cycle time (EW = 1)[4]	(WS+WST+WH+ (MEWC*16))*E–3	(WS+WST+WH+ (MEWC*16))*E+1	ns
16	$t_{su(EMCEL-EMWEL)}$	Output setup time, $\overline{EMxCS}$[y:2] low to $\overline{EMxWE}$ low (SS = 0)	(WS)*E–3	(WS)*E+1	ns
		Output setup time, $\overline{EMxCS}$[y:2] low to $\overline{EMxWE}$ low (SS = 1)	–3	1	ns
17	$t_{h(EMWEH-EMCEH)}$	Output hold time, $\overline{EMxWE}$ high to $\overline{EMxCS}$[y:2] high (SS = 0)	(WH)*E–3	(WH)*E	ns
		Output hold time, $\overline{EMxWE}$ high to $\overline{EMxCS}$[y:2] high (SS = 1)	–3	0	ns
18	$t_{su(EMDQMV-EMWEL)}$	Output setup time, EMxDQM[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
19	$t_{h(EMWEH-EMDQMIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxDQM[y:0] invalid	(WH)*E–3	(WH)*E	ns
20	$t_{su(EMBAV-EMWEL)}$	Output setup time, EMxBA[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
21	$t_{h(EMWEH-EMBAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxBA[y:0] invalid	(WH)*E–3	(WH)*E	ns

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6.9.11.3.1.2 EMIF Asynchronous Memory Switching Characteristics (continued)

NO.[1] [2] [3]	PARAMETER		MIN	MAX	UNIT
22	$t_{su(EMAV-EMWEL)}$	Output setup time, EMxA[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
23	$t_{h(EMWEH-EMAIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxA[y:0] invalid	(WH)*E–3	(WH)*E	ns
24	$t_{w(EMWEL)}$	$\overline{EMxWE}$ active low width (EW = 0)	(WST)*E–1	(WST)*E+1	ns
		$\overline{EMxWE}$ active low width (EW = 1)[4]	(WST+(MEWC*16))*E–1	(WST+(MEWC*16))*E+1	ns
25	$t_{d(EMWAITH-EMWEH)}$	Delay time from EMxWAIT deasserted to $\overline{EMxWE}$ high	4E+10	5E+15	ns
26	$t_{su(EMDV-EMWEL)}$	Output setup time, EMxD[y:0] valid to $\overline{EMxWE}$ low	(WS)*E–3	(WS)*E+1	ns
27	$t_{h(EMWEH-EMDIV)}$	Output hold time, $\overline{EMxWE}$ high to EMxD[y:0] invalid	(WH)*E–3	(WH)*E	ns

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed through the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following ranges of values: TA[4–1], RS[16–1], RST[64–4], RH[8–1], WS[16–1], WST[64–1], WH[8–1], and MEWC[1–256]. See the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual* for more information.
(2) E = EMxCLK period in ns.
(3) EWC = external wait cycles determined by EMxWAIT input signal. EWC supports the following range of values. EWC[256–1]. The maximum wait time before time-out is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register. See the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual* for more information.
(4) Maximum wait time-out condition.

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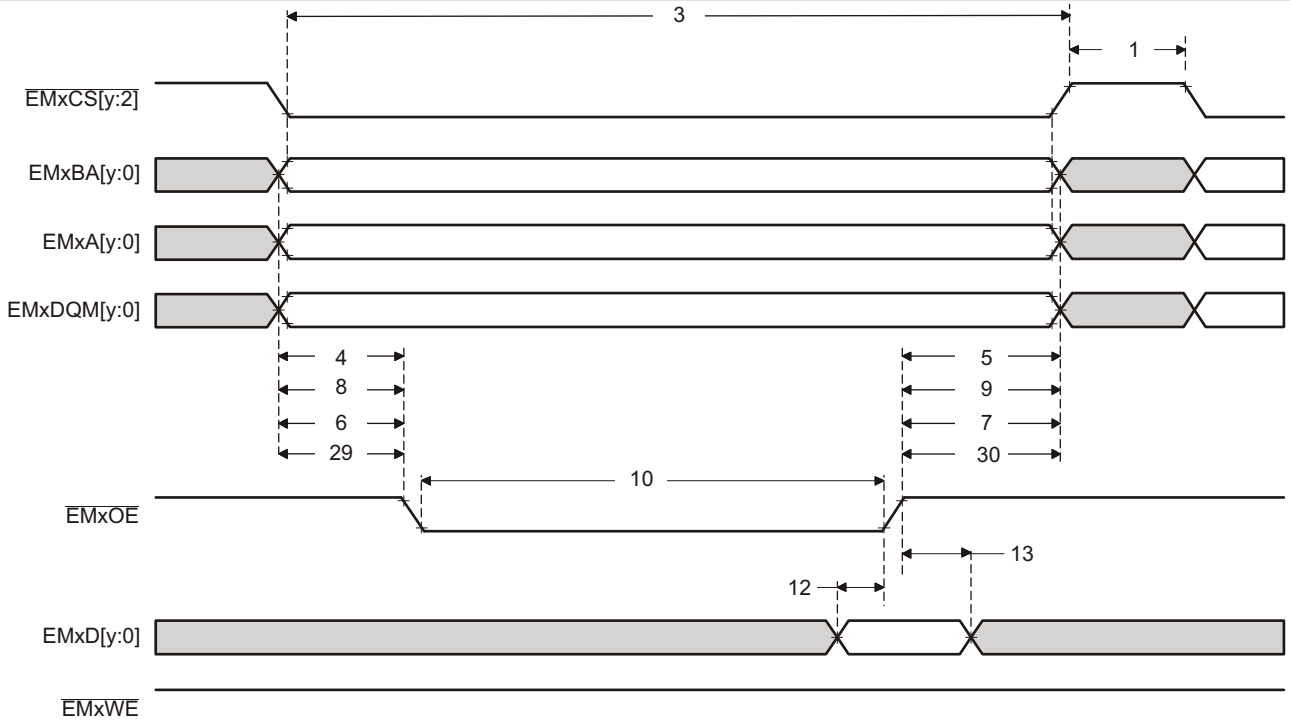


Figure 6-25. Asynchronous Memory Read Timing

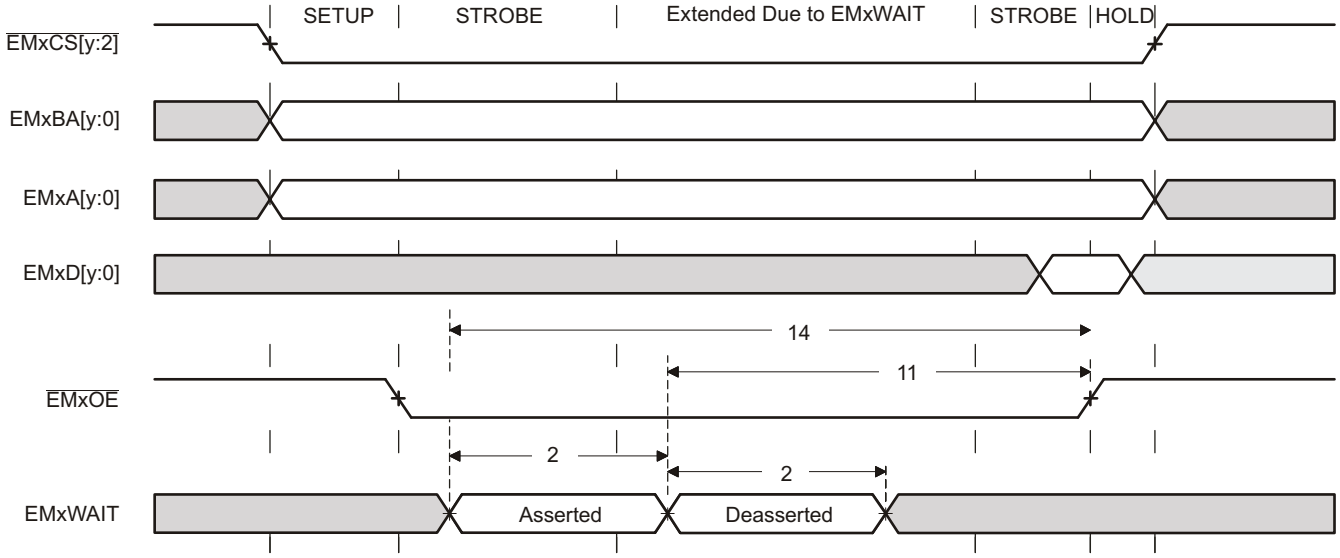


Figure 6-26. EMxWAIT Read Timing Requirements

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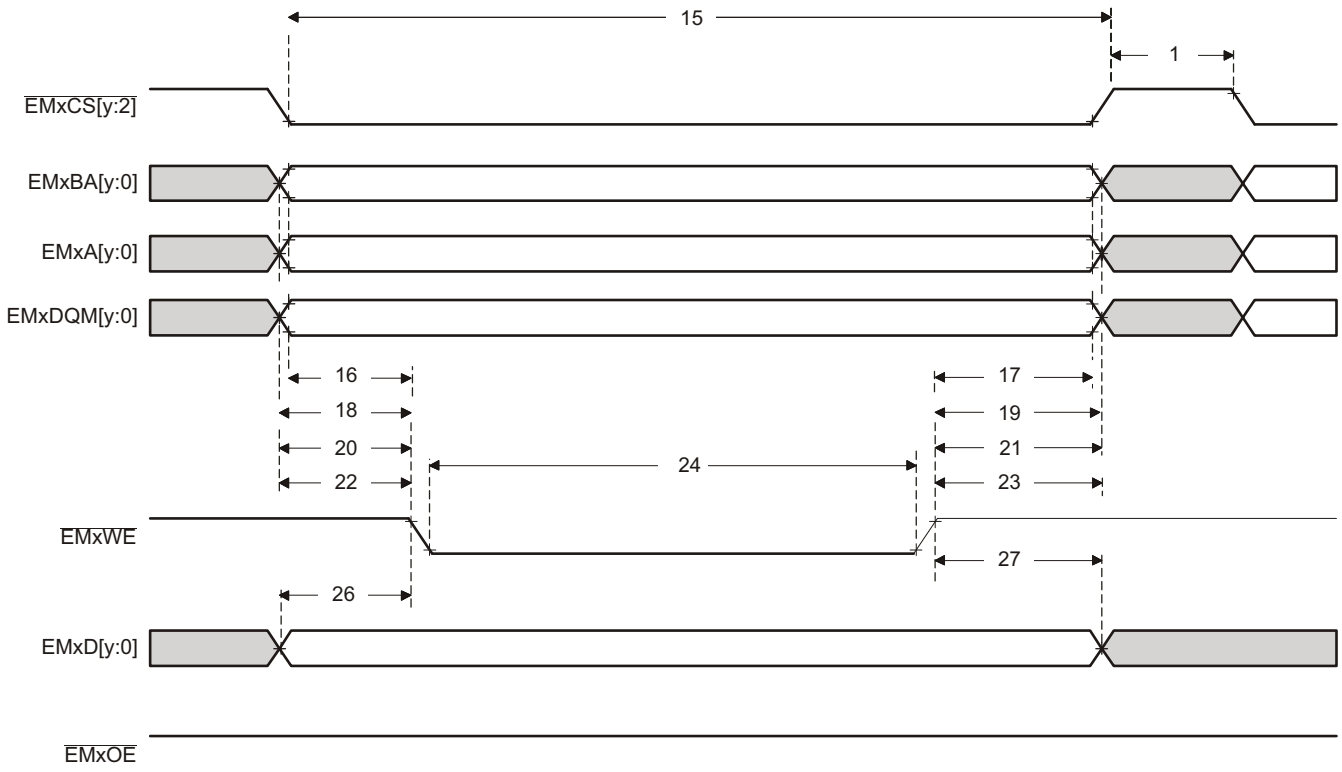


Figure 6-27. Asynchronous Memory Write Timing

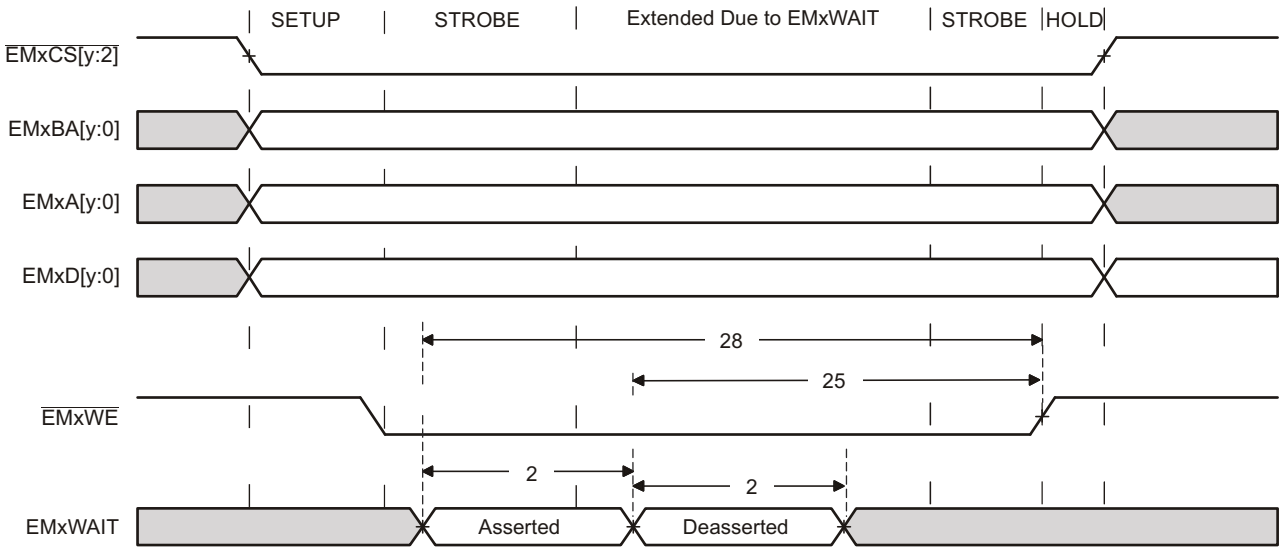


Figure 6-28. EMxWAIT Write Timing Requirements

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6.9.11.3.2 Synchronous RAM

Section 6.9.11.3.2.1 shows the EMIF synchronous memory timing requirements. Section 6.9.11.3.2.2 shows the EMIF synchronous memory switching characteristics. Figure 6-29 and Figure 6-30 show the synchronous memory timing diagrams.

6.9.11.3.2.1 EMIF Synchronous Memory Timing Requirements

NO.			MIN	MAX	UNIT
19	$t_{su(EMIFDV-EM_CLKH)}$	Input setup time, read data valid on EMxD[y:0] before EMxCLK rising	2		ns
20	$t_{h(CLKH-DIV)}$	Input hold time, read data valid on EMxD[y:0] after EMxCLK rising	1.5		ns

6.9.11.3.2.2 EMIF Synchronous Memory Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(CLK)}$	Cycle time, EMIF clock EMxCLK	10		ns
2	$t_{w(CLK)}$	Pulse width, EMIF clock EMxCLK high or low	3		ns
3	$t_{d(CLKH-CSV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ valid		8	ns
4	$t_{oh(CLKH-CSIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxCS[y:2]}}$ invalid	1		ns
5	$t_{d(CLKH-DQMV)}$	Delay time, EMxCLK rising to EMxDQM[y:0] valid		8	ns
6	$t_{oh(CLKH-DQMIV)}$	Output hold time, EMxCLK rising to EMxDQM[y:0] invalid	1		ns
7	$t_{d(CLKH-AV)}$	Delay time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] valid		8	ns
8	$t_{oh(CLKH-AIV)}$	Output hold time, EMxCLK rising to EMxA[y:0] and EMxBA[y:0] invalid	1		ns
9	$t_{d(CLKH-DV)}$	Delay time, EMxCLK rising to EMxD[y:0] valid		8	ns
10	$t_{oh(CLKH-DIV)}$	Output hold time, EMxCLK rising to EMxD[y:0] invalid	1		ns
11	$t_{d(CLKH-RASV)}$	Delay time, EMxCLK rising to EMxRAS valid		8	ns
12	$t_{oh(CLKH-RASIV)}$	Output hold time, EMxCLK rising to EMxRAS invalid	1		ns
13	$t_{d(CLKH-CASV)}$	Delay time, EMxCLK rising to EMxCAS valid		8	ns
14	$t_{oh(CLKH-CASIV)}$	Output hold time, EMxCLK rising to EMxCAS invalid	1		ns
15	$t_{d(CLKH-WEV)}$	Delay time, EMxCLK rising to $\overline{\text{EMxWE}}$ valid		8	ns
16	$t_{oh(CLKH-WEIV)}$	Output hold time, EMxCLK rising to $\overline{\text{EMxWE}}$ invalid	1		ns
17	$t_{d(CLKH-DHZ)}$	Delay time, EMxCLK rising to EMxD[y:0] tri-stated		8	ns
18	$t_{oh(CLKH-DLZ)}$	Output hold time, EMxCLK rising to EMxD[y:0] driving	1		ns

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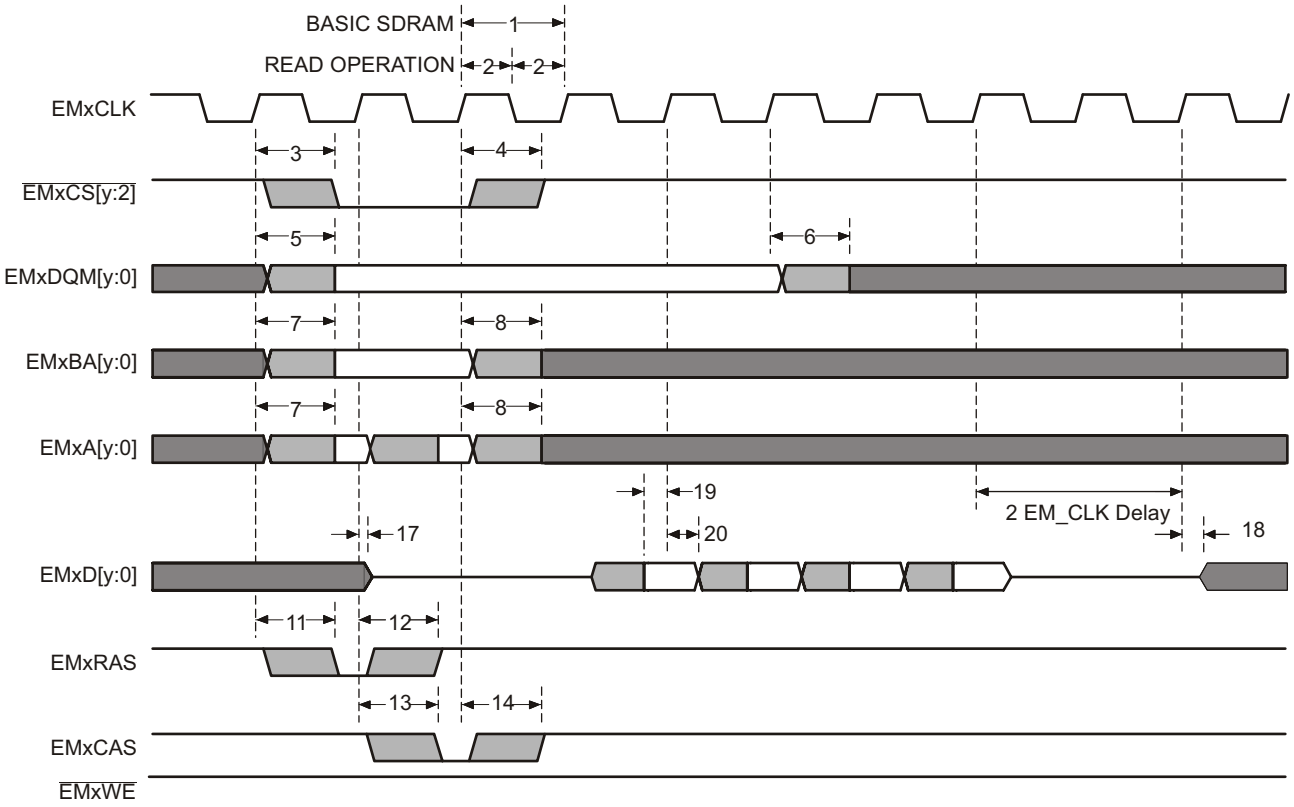


Figure 6-29. Basic SDRAM Read Operation

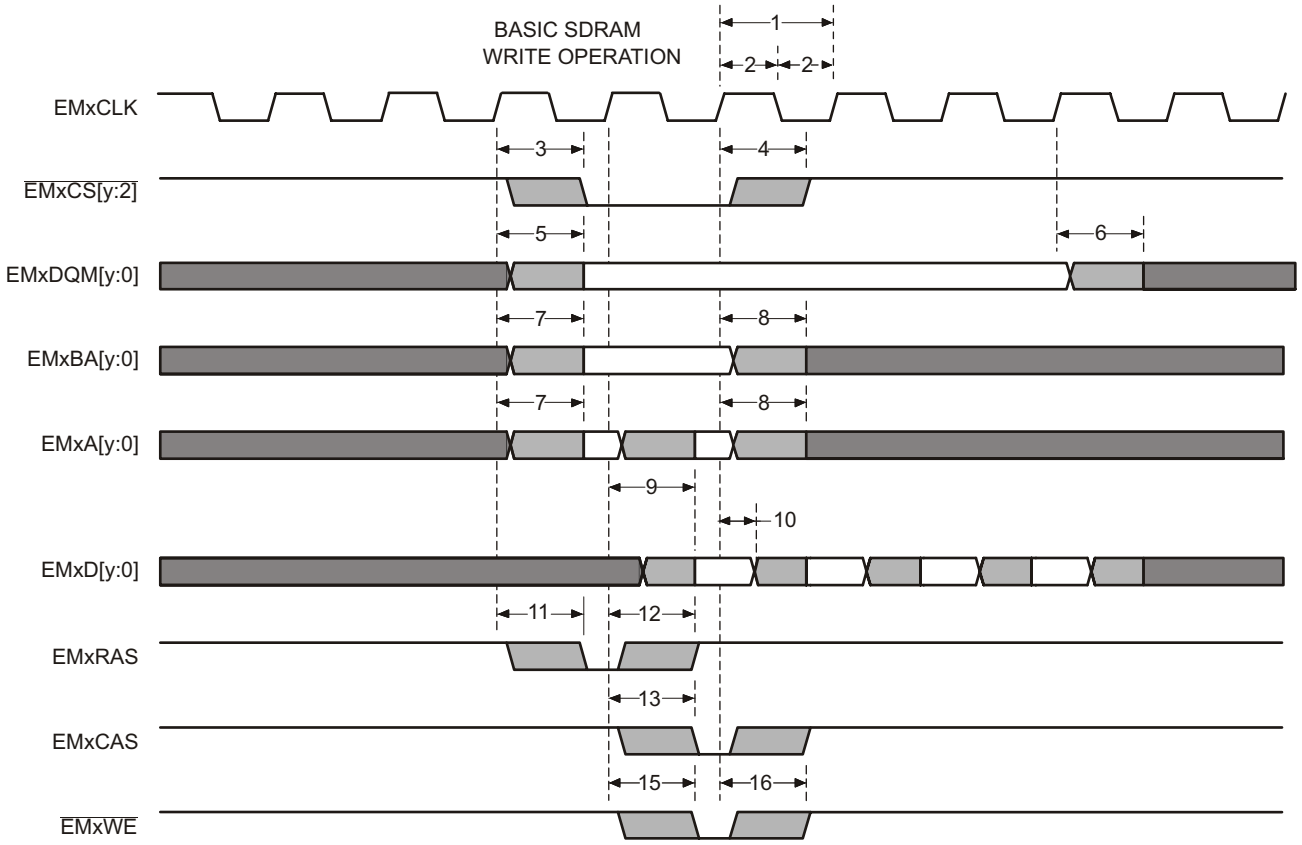


Figure 6-30. Basic SDRAM Write Operation

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6.10 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the ADC, temperature sensor, buffered DAC, and CMPSS.

The analog subsystem has the following features:

- Flexible voltage references
  - The ADCs are referenced to V_{REFHIx} and V_{REFLOx} pins.
    - V_{REFHIx} pin voltage must be driven in externally.
- The buffered DACs are referenced to V_{REFHIx} and V_{SSA}.
  - Alternately, these DACs can be referenced to the VDAC pin and V_{SSA}.
- The comparator DACs are referenced to V_{DDA} and V_{SSA}.
  - Alternately, these DACs can be referenced to the VDAC pin and V_{SSA}.
- Flexible pin usage
  - Buffered DAC and comparator subsystem functions multiplexed with ADC inputs
- Internal connection to V_{REFLO} on all ADCs for offset self-calibration

Figure 6-31 shows the Analog Subsystem Block Diagram for the 176-pin PTP package. Figure 6-32 shows the Analog Subsystem Block Diagram for the 100-pin PZP package.

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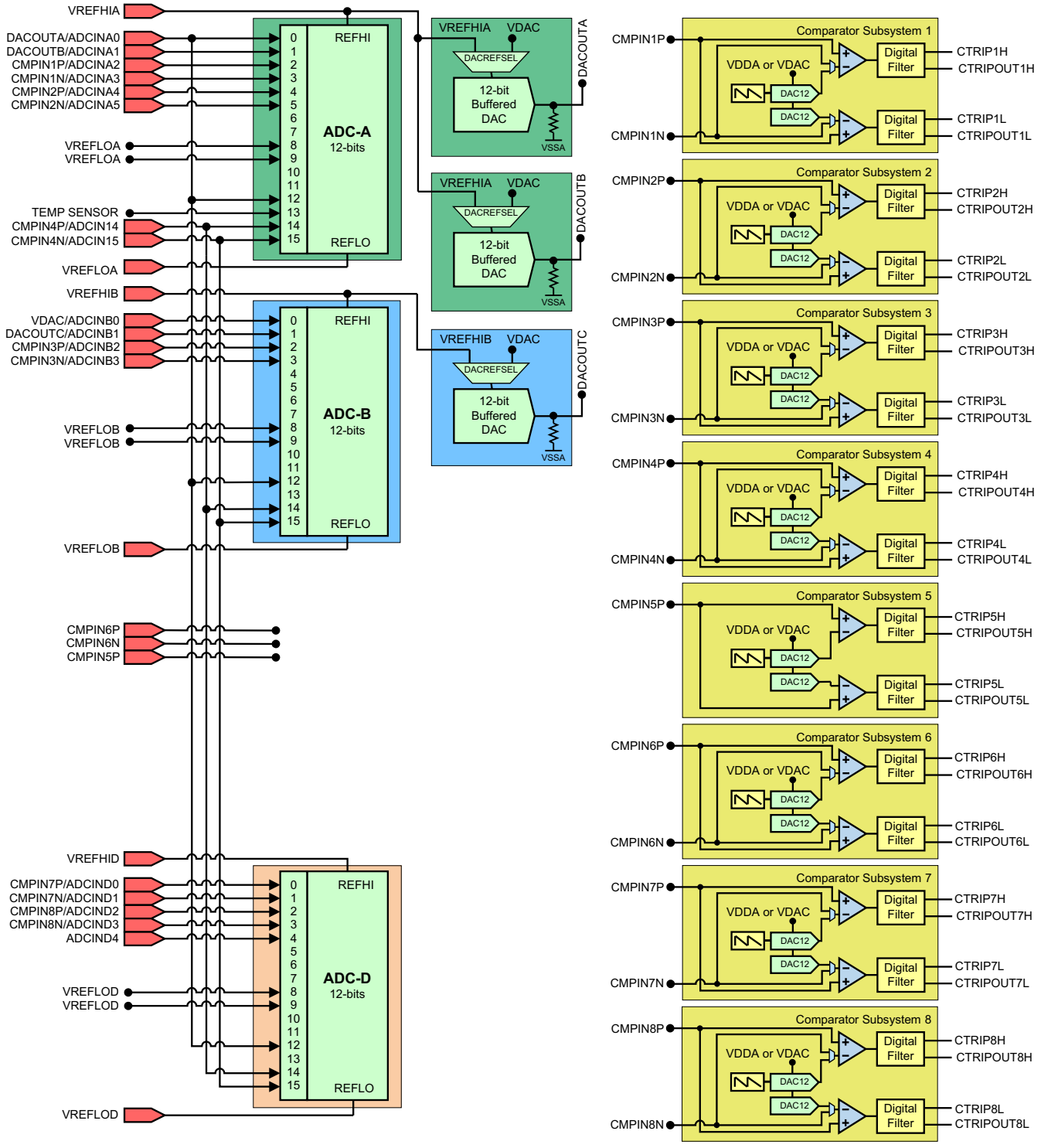


Figure 6-31. Analog Subsystem Block Diagram (176-Pin PTP)

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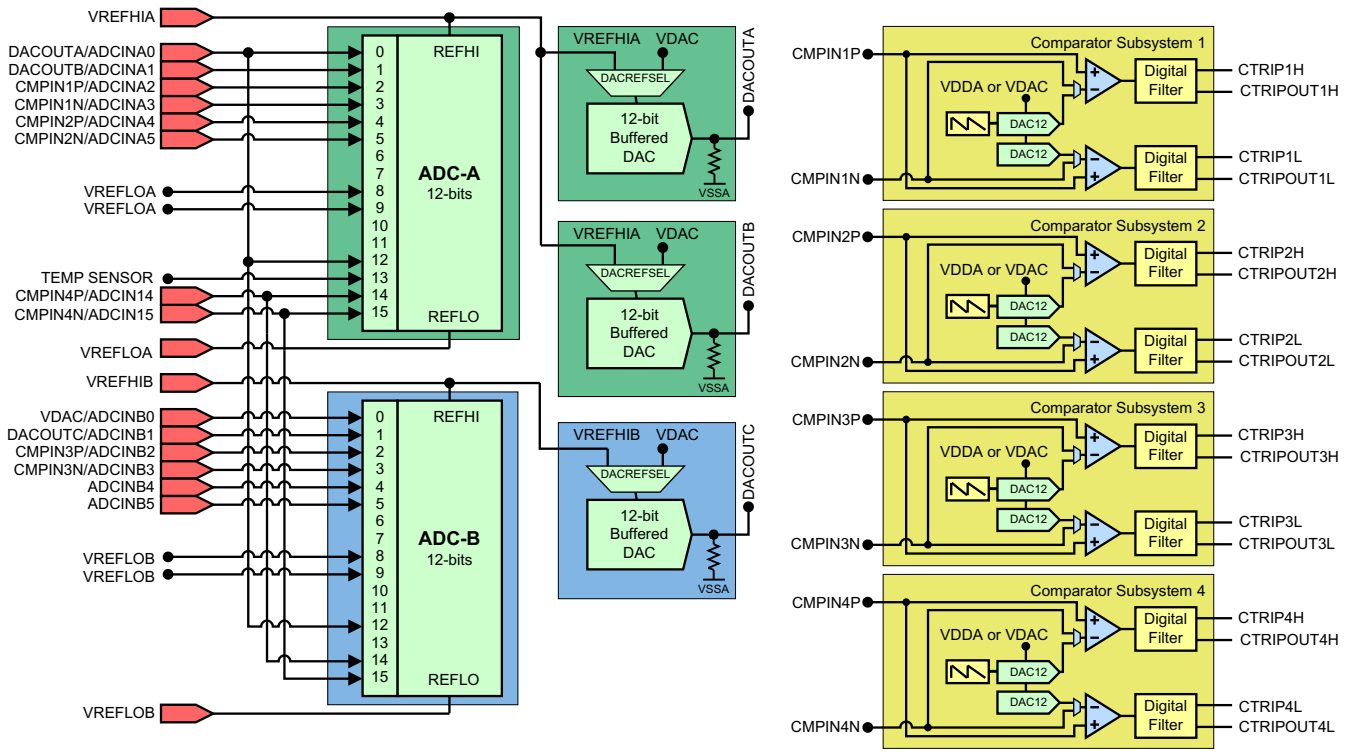


Figure 6-32. Analog Subsystem Block Diagram (100-Pin PZP)

6.10.1 Analog-to-Digital Converter (ADC)

The ADCs on this device are successive approximation (SAR) style ADCs with 12-bit resolution. There are multiple ADC modules which allow simultaneous sampling. The ADC wrapper is start-of-conversion (SOC) based [see the SOC Principle of Operation section of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

Each ADC has the following features:

- 12-bit resolution
- Ratiometric external reference set by V_{REFHI} and V_{REFLO}
- Single-ended signal conversions
- Input multiplexer with up to 16 channels
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - Software immediate start
  - All ePWMs
  - GPIO XINT2
  - CPU timers
  - ADCINT1 or 2
- Four flexible PIE interrupts
- Burst mode
- Four post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
  - Trigger-to-sample delay capture

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Figure 6-33 shows the ADC module block diagram.

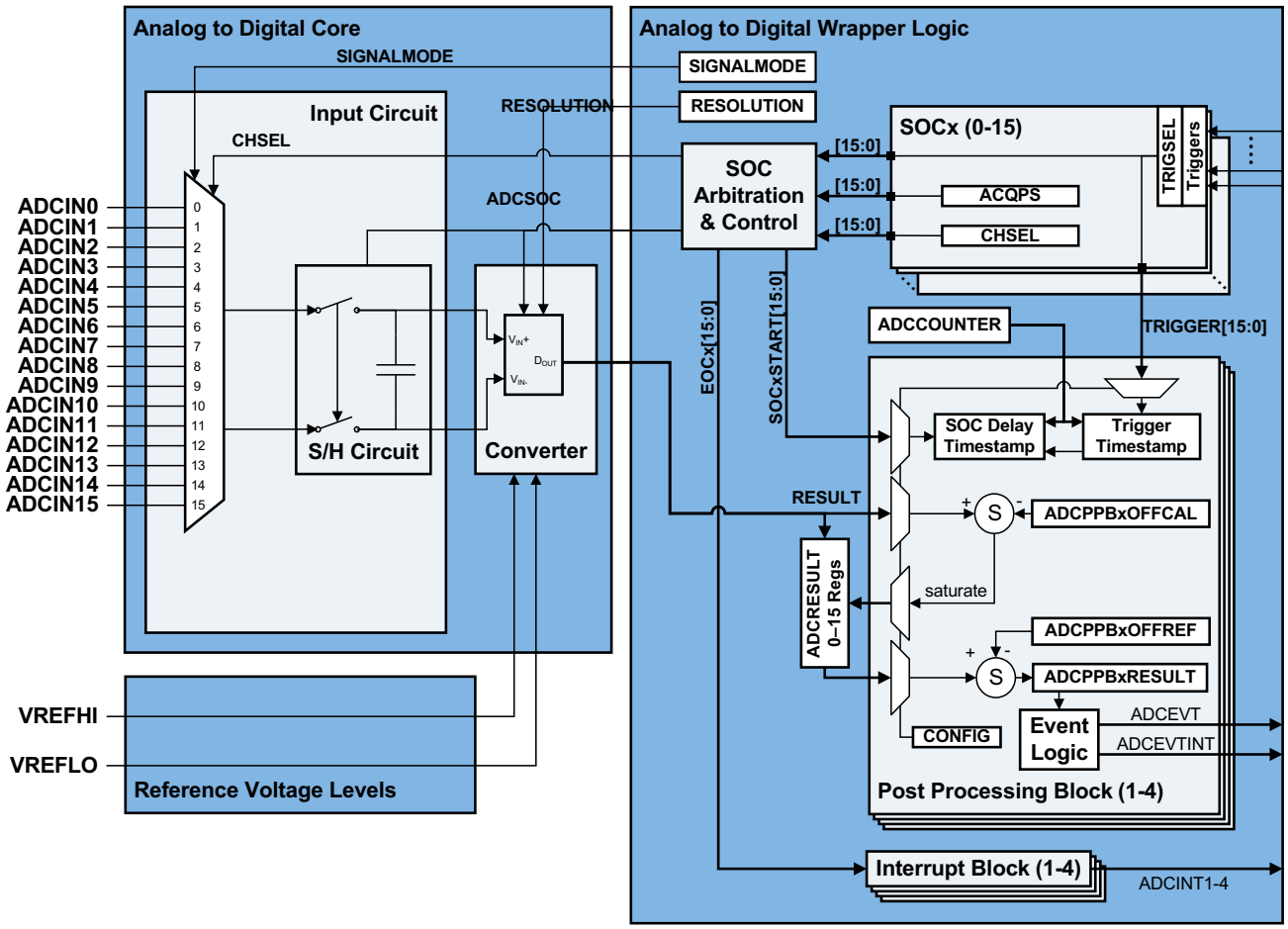


Figure 6-33. ADC Module Block Diagram

6.10.1.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are controlled by each ADC module. Table 6-9 summarizes the basic ADC options and their level of configurability.

Table 6-9. ADC Options and Configuration Levels

OPTIONS	CONFIGURABILITY
Clock	By the module(1)
Resolution	Not configurable (12-bit resolution only)
Signal mode	Not configurable (single-ended signal mode only)
Reference voltage source	Not configurable (external reference only)
Trigger source	By the SOC(1)
Converted channel	By the SOC
Acquisition window duration	By the SOC(1)
EOC location	By the module
Burst mode	By the module(1)

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the Ensuring Synchronous Operation section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

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6.10.1.1.1 Signal Mode

The ADC supports single-ended signaling. In single-ended mode, the input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO. Figure 6-34 shows the single-ended signaling mode.

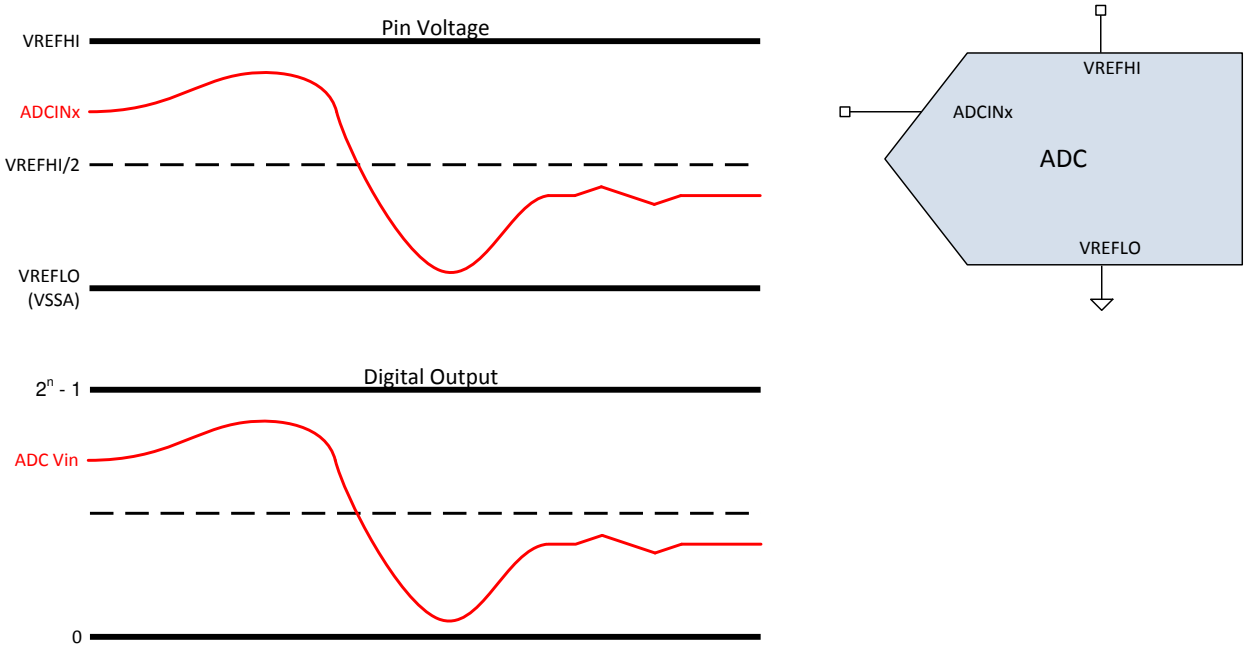


Figure 6-34. Single-ended Signaling Mode

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6.10.1.2 ADC Electrical Data and Timing

Section 6.10.1.2.1 shows the ADC operating conditions. Section 6.10.1.2.2 shows the ADC characteristics. Section 6.10.1.2.3 shows the ADCEXTSOC timing requirements.

6.10.1.2.1 ADC Operating Conditions

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)	5		50	MHz
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	100			ns
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V
$V_{REFHI} – V_{REFLO}$	2.4		V_{DDA}	V
ADC input conversion range	V_{REFLO}		V_{REFHI}	V

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

Note

The ADC inputs should be kept below V_{DDA} + 0.3 V during operation. If an ADC input exceeds this level, the V_{REF} internal to the device may be disturbed, which can impact results for other ADC or DAC inputs using the same V_{REF}.

Note

The V_{REFHI} pin must be kept below V_{DDA} + 0.3 V to ensure proper functional operation. If the V_{REFHI} pin exceeds this level, a blocking circuit may activate, and the internal value of V_{REFHI} may float to 0 V internally, giving improper ADC conversion or DAC output.

6.10.1.2.2 ADC Characteristics

over recommended operating conditions (unless otherwise noted)(5)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC conversion cycles(1)		10.1		11	ADCCLKs
Power-up time				500	µs
Gain error		–5	±3	5	LSBs
Offset error		–4	±2	4	LSBs
Channel-to-channel gain error			±4		LSBs
Channel-to-channel offset error			±2		LSBs
ADC-to-ADC gain error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±4		LSBs
ADC-to-ADC offset error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±2		LSBs
DNL(2)		> –1	±0.5	1	LSBs
INL		–2	±1.0	2	LSBs
SNR(3) (10)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		69.1		dB
THD(3) (10)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		–88		dB
SFDR(3) (10)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		89		dB
SINAD(3) (10)	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		69.0		dB

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6.10.1.2.2 ADC Characteristics (continued)

over recommended operating conditions (unless otherwise noted)[5]

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB[3] [10]	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, single ADC[6], all packages		11.2		bits
	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, synchronous ADCs[7], all packages		11.2		
	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, asynchronous ADCs[8], 100-pin PZP package		Not supported		
	V_{REFHI} = 2.5 V, f_{in} = 100 kHz, asynchronous ADCs[8], 176-pin PTP package		9.7		
PSRR	V_{DDA} = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		dB
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz		57		dB
ADC-to-ADC isolation[10] [4] [9]	V_{REFHI} = 2.5 V, synchronous ADCs[7], all packages	–1		1	LSBs
	V_{REFHI} = 2.5 V, asynchronous ADCs[8], 100-pin PZP package		Not supported		
	V_{REFHI} = 2.5 V, asynchronous ADCs[8], 176-pin PTP package	–9		9	
V_{REFHI} input current			130		µA

(1) See Section 6.10.1.2.5.
(2) No missing codes.
(3) AC parameters will be impacted by clock source accuracy and jitter, this should be taken into account when selecting the clock source for the system. The clock source used for these parameters was a high-accuracy external clock fed through the PLL. The on-chip Internal Oscillator has higher jitter than an external crystal and these parameters will degrade if it is used as a clock source.
(4) Maximum DC code deviation due to operation of multiple ADCs simultaneously.
(5) Typical values are measured with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V. Minimum and Maximum values are tested or characterized with V_{REFHI} = 2.5 V and V_{REFLO} = 0 V.
(6) One ADC operating while all other ADCs are idle.
(7) All ADCs operating with identical ADCCLK, S+H durations, triggers, and resolution.
(8) Any ADCs operating with heterogeneous ADCCLK, S+H durations, triggers, or resolution.
(9) Value based on characterization.
(10) I/O activity is minimized on pins adjacent to ADC input and V_{REFHI} pins as part of best practices to reduce capacitive coupling and crosstalk.

6.10.1.2.3 ADCEXTSOC Timing Requirements

			MIN[1]	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.

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6.10.1.2.4 ADC Input Model

Note

ADC channels ADCINA0, ADCINA1, and ADCINB1 have a 50-kΩ pulldown resistor to V_{SSA}.

6.10.1.2.4.1 Single-Ended Input Model Parameters

	DESCRIPTION	VALUE
C_p	Parasitic input capacitance	See Table 6-10
R_{on}	Sampling switch resistance	600 Ω
C_h	Sampling capacitor	16.5 pF
R_s	Nominal source impedance	50 Ω

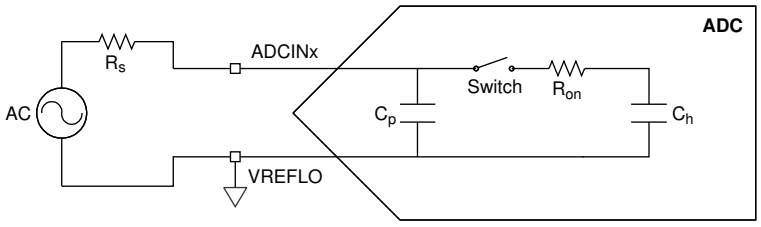


Figure 6-35. Single-Ended Input Model

Table 6-10 shows the parasitic capacitance on each channel. Also, enabling a comparator adds approximately 1.4 pF of capacitance on positive comparator inputs and 2.5 pF of capacitance on negative comparator inputs.

Table 6-10. Per-Channel Parasitic Capacitance

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
ADCINA0	12.9	N/A
ADCINA1	10.3	N/A
ADCINA2	5.9	7.3
ADCINA3	6.3	8.8
ADCINA4	5.9	7.3
ADCINA5	6.3	8.8
ADCINB0(1)	117.0	N/A
ADCINB1	10.6	N/A
ADCINB2	5.9	7.3
ADCINB3	6.2	8.7
ADCINB4	5.2	N/A
ADCINB5	5.1	N/A
ADCIND0	5.3	6.7
ADCIND1	5.7	8.2
ADCIND2	5.3	6.7
ADCIND3	5.6	8.1
ADCIND4	4.3	N/A
ADCIN14	8.6	10.0
ADCIN15	9.0	11.5

(1) The increased capacitance is due to VDAC functionality.

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This input model should be used along with actual signal source impedance to determine the acquisition window duration. See the Choosing an Acquisition Window Duration section of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual* for more information. Also refer to *Charge-Sharing Driving Circuits for C2000 ADCs* and *ADC Input Circuit Evaluation for C2000 MCUs* for more details on evaluating ADC circuit performance.

The user should analyze the ADC input setting assuming worst-case initial conditions on C_h. This will require assuming that C_h could start the S+H window completely charged to V_{REFHI} or completely discharged to V_{REFLO}. When the ADC transitions from an odd-numbered channel to an even-numbered channel, or vice-versa, the actual initial voltage on C_h will be close to being completely discharged to V_{REFLO}. For even-to-even or odd-to-odd channel transitions, the initial voltage on C_h will be close to the voltage of the previously converted channel.

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6.10.1.2.5 ADC Timing Diagrams

Section 6.10.1.2.5.1 lists the ADC timings in 12-bit mode (SYSCLK cycles). Figure 6-36 shows the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 6-11 lists the descriptions of the ADC timing parameters that are in Figure 6-36 .

Table 6-11. ADC Timing Parameters

PARAMETER	DESCRIPTION
t_{SH}	The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} will not necessarily be the same for different SOCs. **Note:** The value on the S+H capacitor will be captured approximately 5 ns before the end of the S+H window regardless of device clock settings.
t_{LAT}	The time from the end of the S+H window until the ADC conversion results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results will be returned.
t_{EOC}	The time from the end of the S+H window until the next ADC conversion S+H window can begin. The subsequent sample can start before the conversion results are latched.
t_{INT}	The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} will coincide with the conversion results being latched into the result register. If the INTPULSEPOS bit is 0, t_{INT} will coincide with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (directly through DMA or indirectly by triggering an ISR that reads the result), care must be taken to ensure the read occurs after the results latch (otherwise, the previous results will be read).

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6.10.1.2.5.1 ADC Timings in 12-Bit Mode (SYSCLK Cycles)

ADCCLK PRESCALE		SYSCLK CYCLES				ADCCLK CYCLES
ADCCTL2 [PRESCALE]	RATIO ADCCLK:SYSCLK	t_{EOC}	t_{LAT} (1)	$t_{INT(EARLY)}$	$t_{INT(LATE)}$	t_{EOC}
0	1	11	13	1	11	11.0
1	1.5	Invalid				
2	2	21	23	1	21	10.5
3	2.5	26	28	1	26	10.4
4	3	31	34	1	31	10.3
5	3.5	36	39	1	36	10.3
6	4	41	44	1	41	10.3
7	4.5	46	49	1	46	10.2
8	5	51	55	1	51	10.2
9	5.5	56	60	1	56	10.2
10	6	61	65	1	61	10.2
11	6.5	66	70	1	66	10.2
12	7	71	76	1	71	10.1
13	7.5	76	81	1	76	10.1
14	8	81	86	1	81	10.1
15	8.5	86	91	1	86	10.1

(1) Refer to the "ADC: DMA Read of Stale Result" advisory in the *TMS320F2807x Real-Time MCUs Silicon Errata*.

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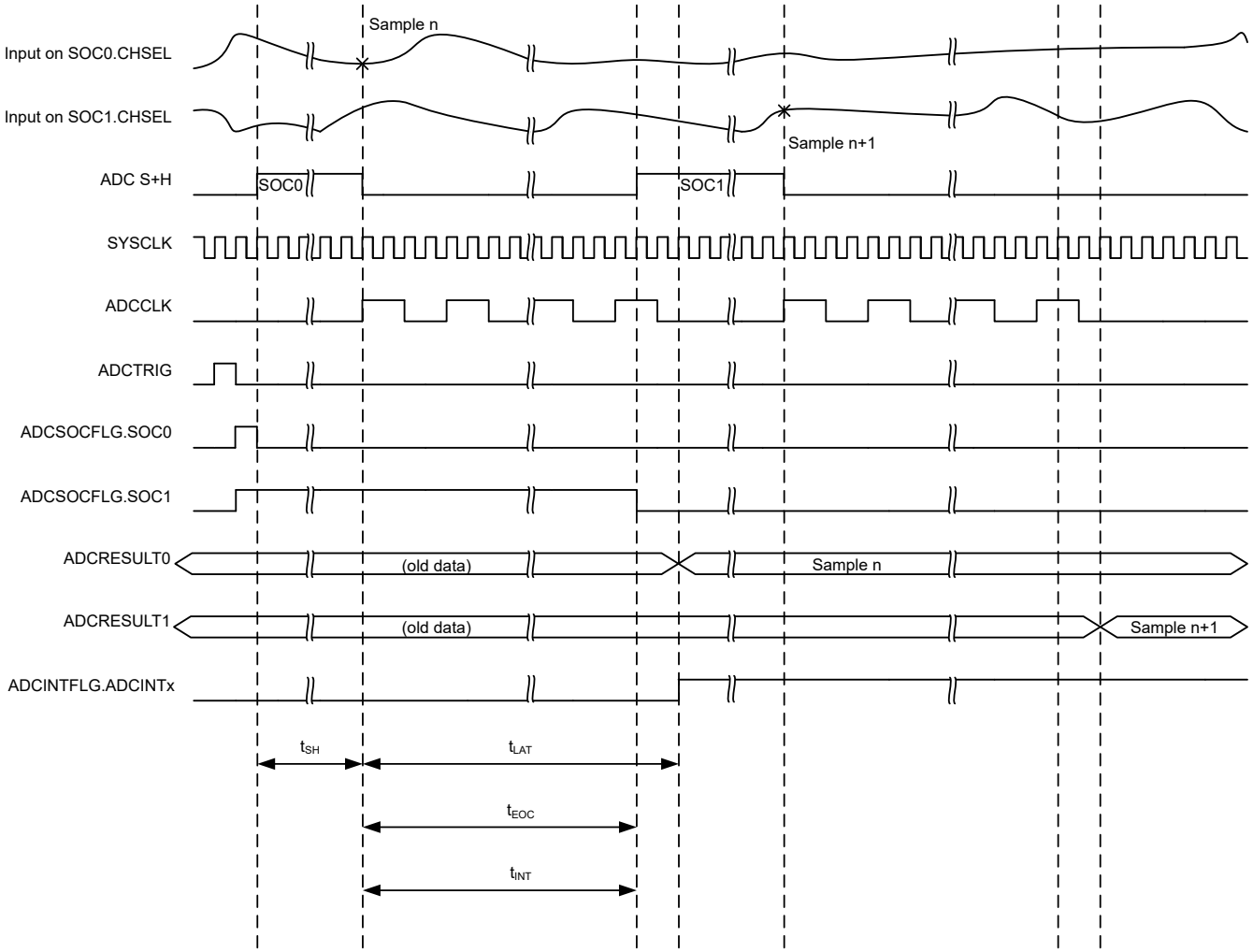


Figure 6-36. ADC Timings for 12-Bit Mode

6.10.1.3 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in Section 6.10.1.3.1.

6.10.1.3.1 Temperature Sensor Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Temperature accuracy		±15		°C
Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor)		500		µs
ADC acquisition time	700			ns

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6.10.2 Comparator Subsystem (CMPSS)

Each CMPSS module includes two comparators, two internal voltage reference DACs (CMPSS DACs), two digital glitch filters, and one ramp generator. There are two inputs, CMPINxP and CMPINxN. Each of these inputs will be internally connected to an ADCIN pin. The CMPINxP pin is always connected to the positive input of the CMPSS comparators. CMPINxN can be used instead of the DAC output to drive the negative comparator inputs. There are two comparators, and therefore two outputs from the CMPSS module, which are connected to the input of a digital filter module before being passed on to the Comparator TRIP crossbar and either PWM modules or directly to a GPIO pin. Figure 6-37 shows CMPSS connectivity on the 176-pin PTP package. Figure 6-38 shows CMPSS connectivity on the 100-pin PZP package.

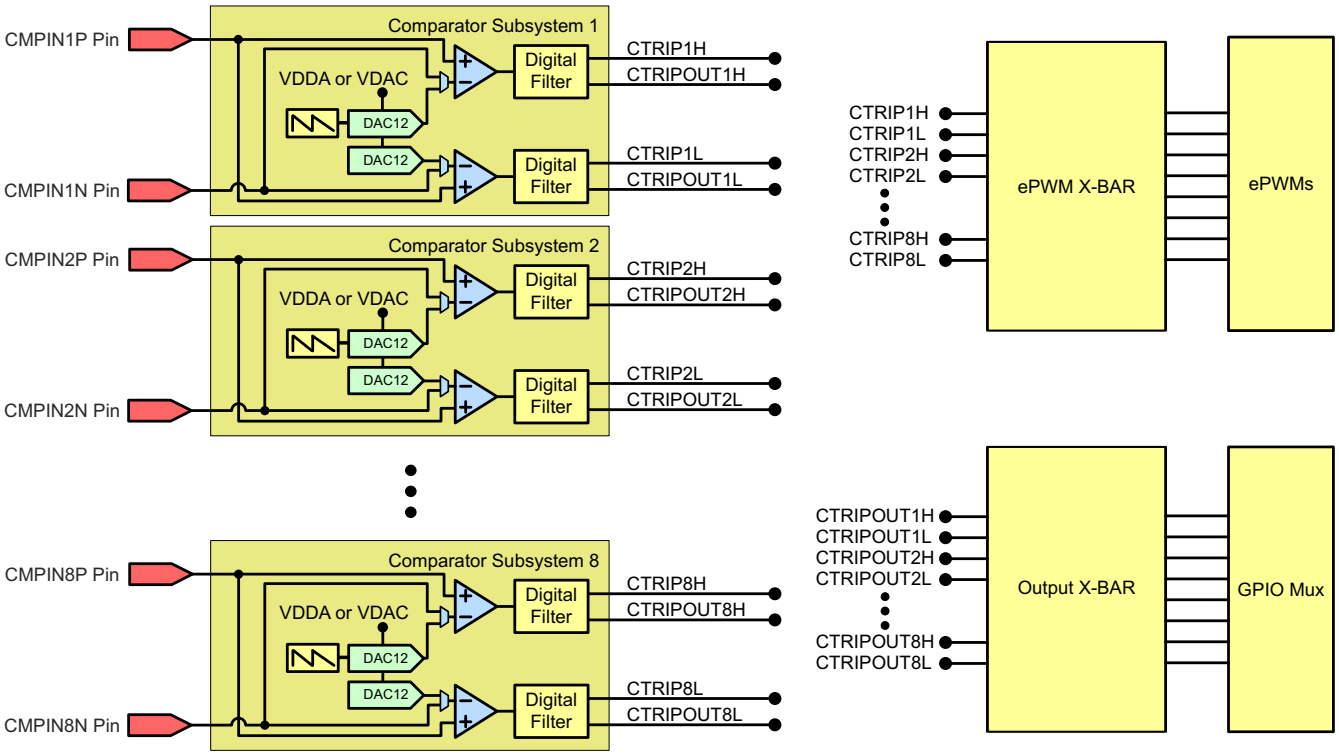


Figure 6-37. CMPSS Connectivity (176-Pin PTP)

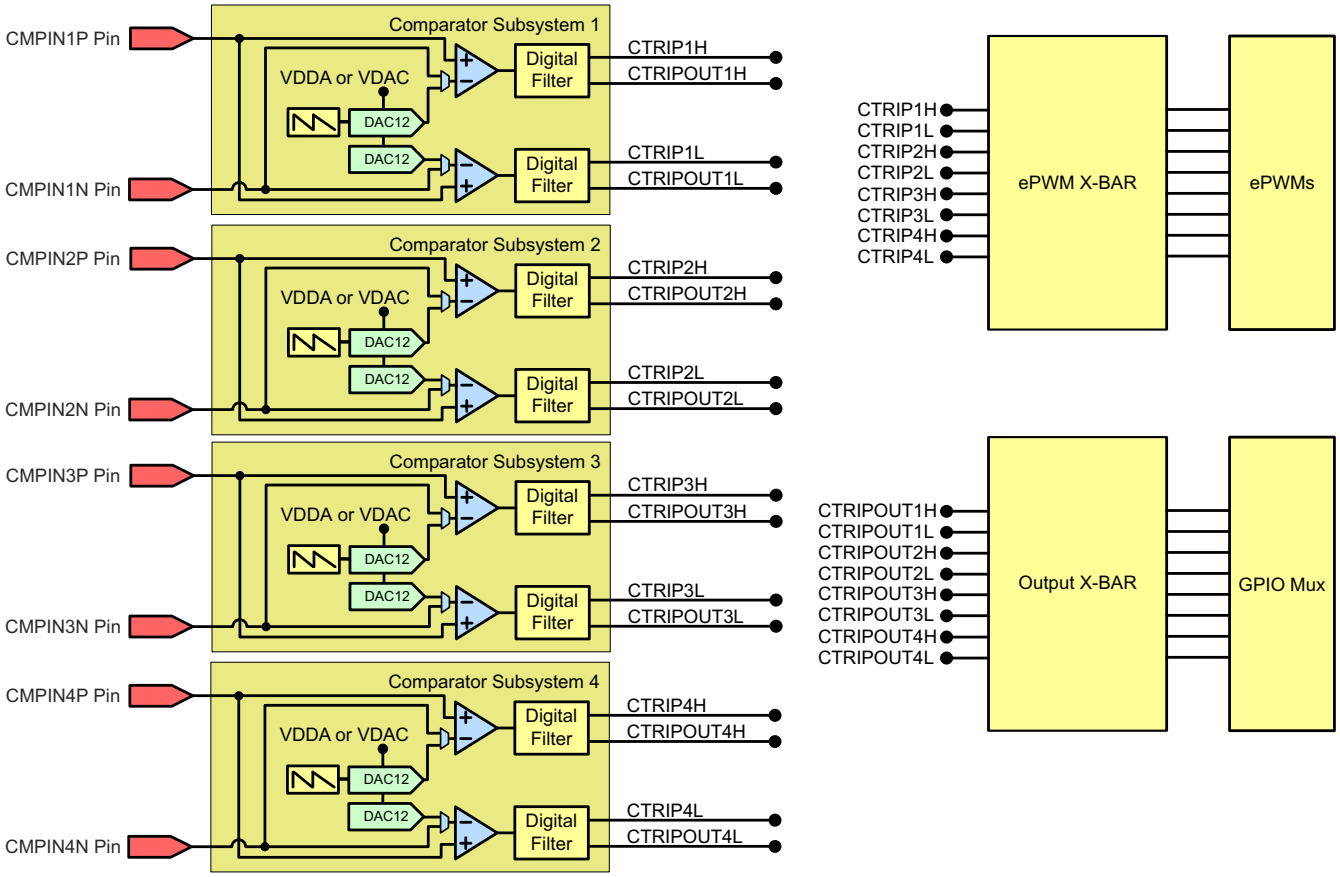


Figure 6-38. CMPSS Connectivity (100-Pin PZP)

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6.10.2.1 CMPSS Electrical Data and Timing

Section 6.10.2.1.1 shows the comparator electrical characteristics. Figure 6-39 shows the CMPSS comparator input referred offset. Figure 6-40 shows the CMPSS comparator hysteresis.

6.10.2.1.1 Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time				500[2]	µs
Comparator input (CMPINxx) range		0		V_{DDA}	V
Input referred offset error	Low common mode, inverting input set to 50 mV	–20		20	mV
Hysteresis[1]	1x	4	12	20	CMPSS DAC LSB
	2x	17	24	33	
	3x	25	36	50	
	4x	30	48	67	
Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR)	Step response		21	60	ns
	Ramp response (1.65 V/µs)		26		
	Ramp response (8.25 mV/µs)		30		
Power Supply Rejection Ratio (PSRR)	Up to 250 kHz		46		dB
Common Mode Rejection Ratio (CMRR)		40			dB

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.
(2) See the "Analog Bandgap References" advisory of the *TMS320F2807x Real-Time MCUs Silicon Errata*.

Note

The CMPSS inputs must be kept below V_{DDA} + 0.3 V to ensure proper functional operation. If a CMPSS input exceeds this level, an internal blocking circuit will isolate the internal comparator from the external pin until the external pin voltage returns below V_{DDA} + 0.3 V. During this time, the internal comparator input will be floating and can decay below V_{DDA} within approximately 0.5 µs. After this time, the comparator could begin to output an incorrect result depending on the value of the other comparator input.

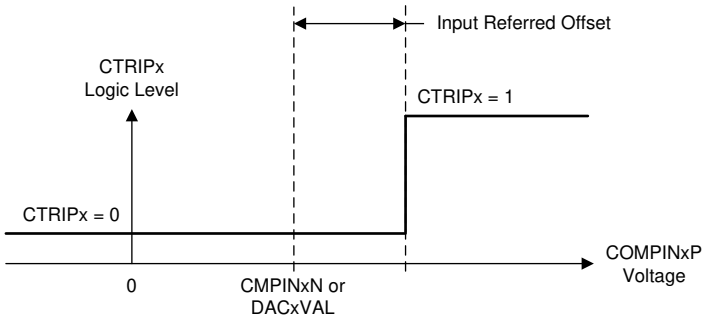


Figure 6-39. CMPSS Comparator Input Referred Offset

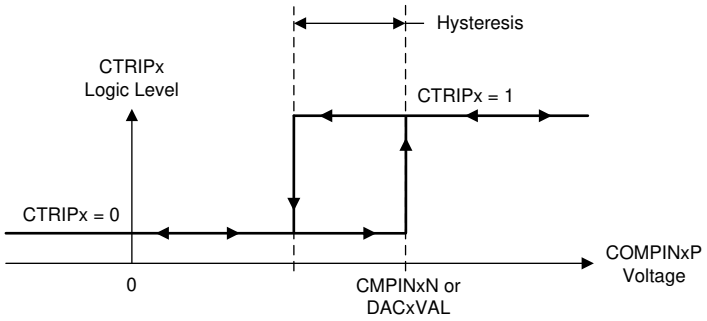


Figure 6-40. CMPSS Comparator Hysteresis

Section 6.10.2.1.2 shows the CMPSS DAC static electrical characteristics. Figure 6-41 shows the CMPSS DAC static offset. Figure 6-42 shows the CMPSS DAC static gain. Figure 6-43 shows the CMPSS DAC static linearity.

6.10.2.1.2 CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS DAC output range	Internal reference	0		V_{DDA} (1)	V
	External reference	0		VDAC	
Static offset error(2)		–25		25	mV
Static gain error(2)		–2		2	% of FSR
Static DNL	Endpoint corrected	>–1		4	LSB
Static INL	Endpoint corrected	–16		16	LSB
Settling time	Settling to 1 LSB after full-scale output change			1	µs
Resolution			12		bits
CMPSS DAC output disturbance(3)	Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module	–100		100	LSB
CMPSS DAC disturbance time(3)			200		ns
VDAC reference voltage	When VDAC is reference	2.4	2.5 or 3.0	V_{DDA}	V
VDAC load(4)	When VDAC is reference		6		kΩ

(1) The maximum output voltage is V_{DDA} when VDAC > V_{DDA}.
(2) Includes comparator input referred errors.
(3) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.
(4) Per active CMPSS module.

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Note

Figures not drawn to scale.

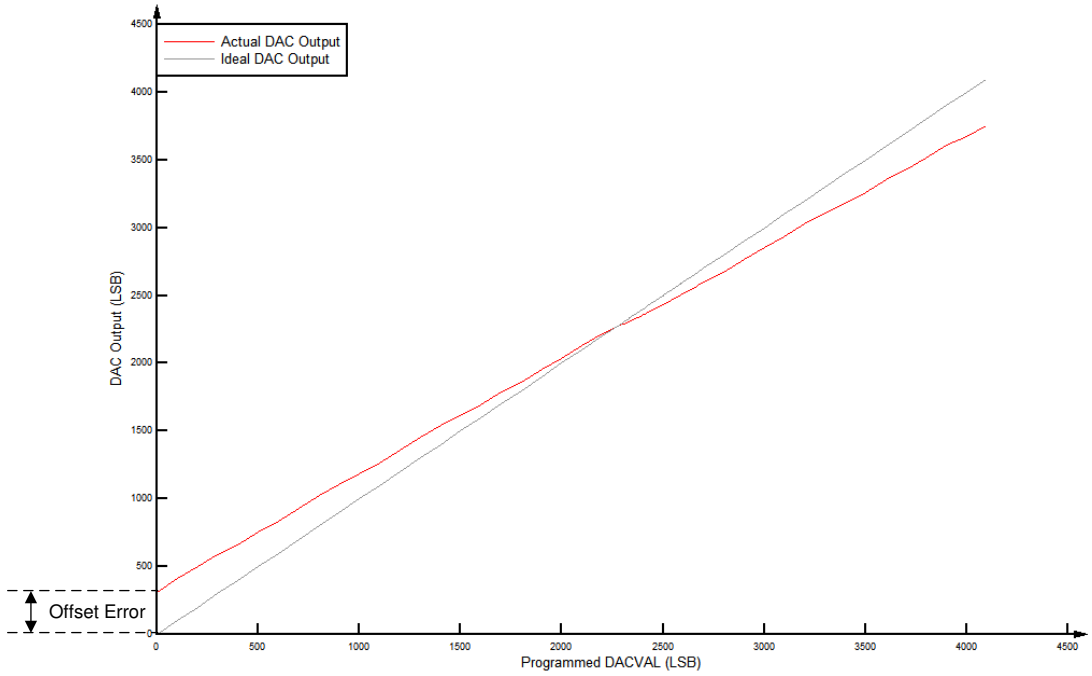


Figure 6-41. CMPSS DAC Static Offset

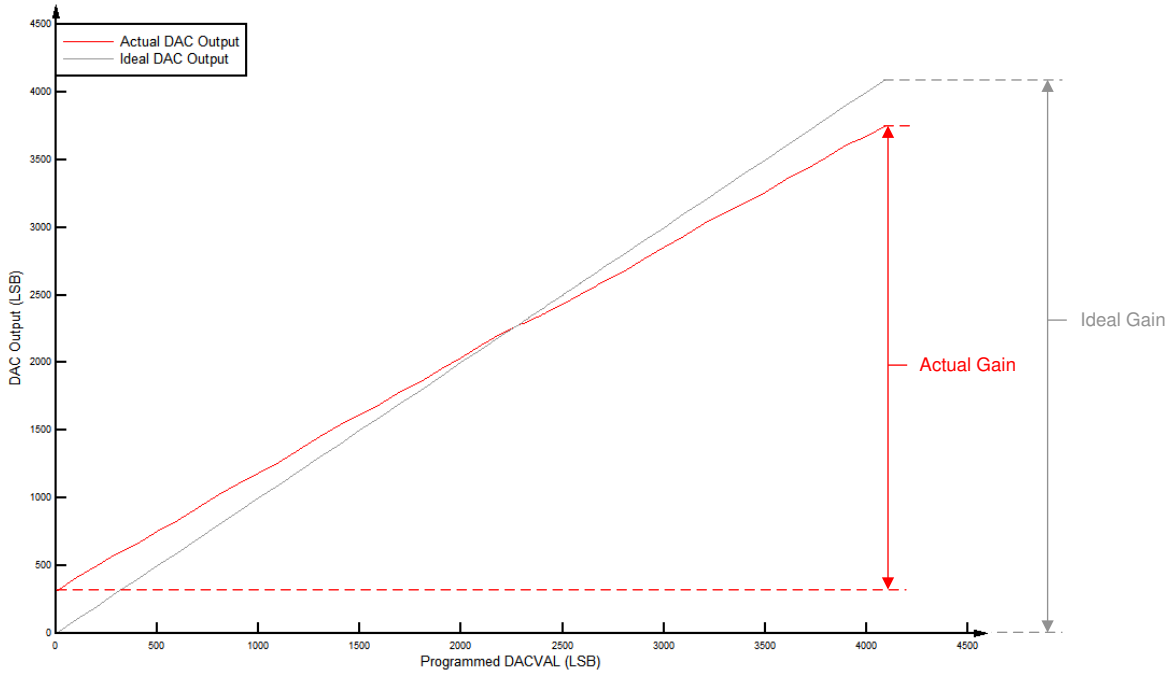


Figure 6-42. CMPSS DAC Static Gain

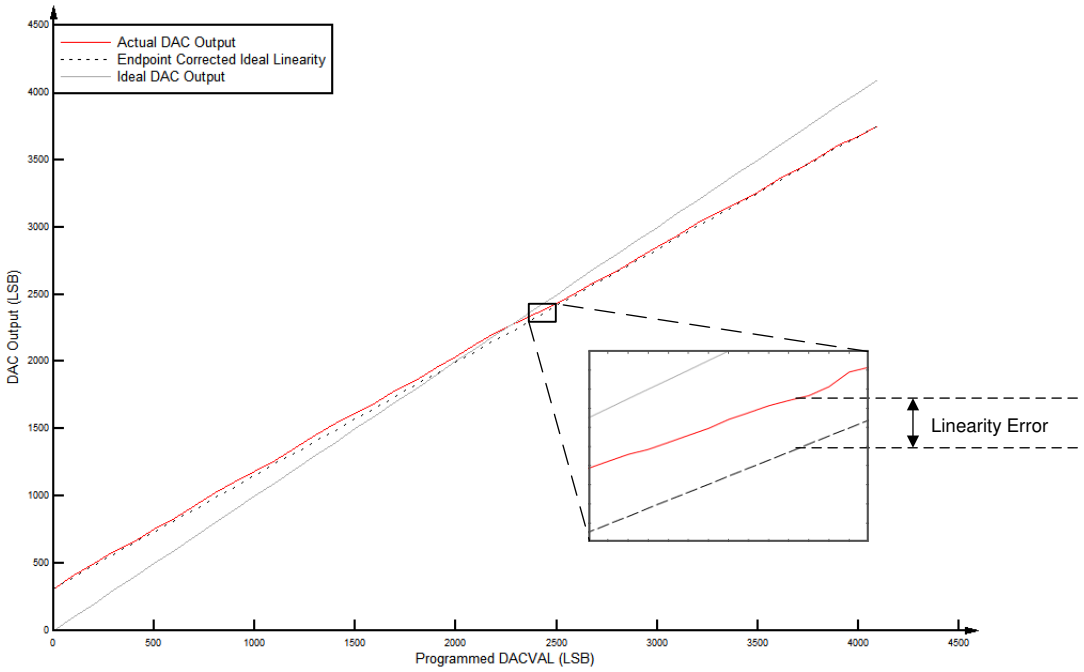


Figure 6-43. CMPSS DAC Static Linearity

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6.10.3 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal 12-bit DAC and an analog output buffer that is capable of driving an external load. An integrated pulldown resistor on the DAC output helps to provide a known pin voltage when the output buffer is disabled. This pulldown resistor cannot be disabled and remains as a passive component on the pin, even for other shared pin mux functions. Software writes to the DAC value register can take effect immediately or can be synchronized with EPWMSYNCPER events.

Each buffered DAC has the following features:

- 12-bit programmable internal DAC
- Selectable reference voltage
- Pulldown resistor on output
- Ability to synchronize with EPWMSYNCPER

The block diagram for the buffered DAC is shown in Figure 6-44.

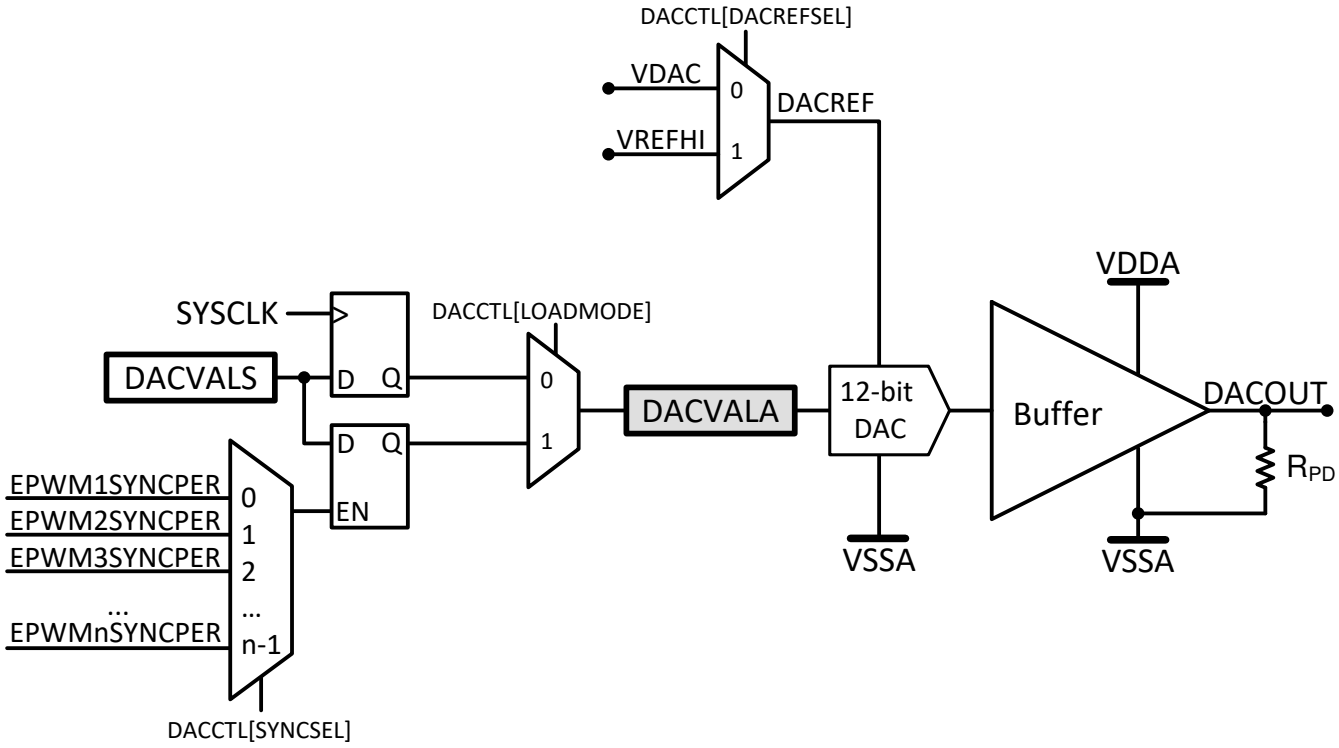


Figure 6-44. DAC Module Block Diagram

6.10.3.1 Buffered DAC Electrical Data and Timing

Section 6.10.3.1.1 shows the buffered DAC electrical characteristics. Figure 6-45 shows the buffered DAC offset. Figure 6-46 shows the buffered DAC gain. Figure 6-47 shows the buffered DAC linearity.

6.10.3.1.1 Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time				500(8)	µs
Offset error	Midpoint	–10		10	mV
Gain error(2)		–2.5		2.5	% of FSR
DNL(3)	Endpoint corrected	> –1	±0.4	1	LSB
INL	Endpoint corrected	–5	±2	5	LSB
DACOUTx settling time	Settling to 2 LSBs after 0.3V-to-3V transition		2		µs
Resolution			12		bits
Voltage output range(4)		0.3		V_{DDA} – 0.3	V
Capacitive load	Output drive capability			100	pF
Resistive load	Output drive capability	5			kΩ
R_{PD} pulldown resistor			50		kΩ
Reference voltage(5)	VDAC or V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
Reference input resistance(6)	VDAC or V_{REFHI}		170		kΩ
Output noise	Integrated noise from 100 Hz to 100 kHz		500		µVrms
	Noise density at 10 kHz		711		nVrms/√Hz
Glitch energy			1.5		V-ns
PSRR(7)	DC up to 1 kHz		70		dB
	100 kHz		30		
SNR	1020 Hz		67		dB
THD	1020 Hz		–63		dB
SFDR	1020 Hz, including harmonics and spurs		66		dBc
	1020 Hz, including only spurs		104		

(1) Typical values are measured with V_{REFHI} = 3.3 V unless otherwise noted. Minimum and Maximum values are tested or characterized with V_{REFHI} = 2.5 V.
(2) Gain error is calculated for linear output range.
(3) The DAC output is monotonic.
(4) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
(5) For best PSRR performance, VDAC or V_{REFHI} should be less than V_{DDA}.
(6) Per active Buffered DAC module.
(7) V_{REFHI} = 3.2 V, V_{DDA} = 3.3 V DC + 100 mV Sine.
(8) See the "Analog Bandgap References" advisory of the *TMS320F2807x Real-Time MCUs Silicon Errata*.

Note

The VDAC pin must be kept below V_{DDA} + 0.3 V to ensure proper functional operation. If the VDAC pin exceeds this level, a blocking circuit may activate, and the internal value of VDAC may float to 0 V internally, giving improper DAC output.

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Note

The V_{REFHI} pin must be kept below V_{DDA} + 0.3 V to ensure proper functional operation. If the V_{REFHI} pin exceeds this level, a blocking circuit may activate, and the internal value of V_{REFHI} may float to 0 V internally, giving improper ADC conversion or DAC output.

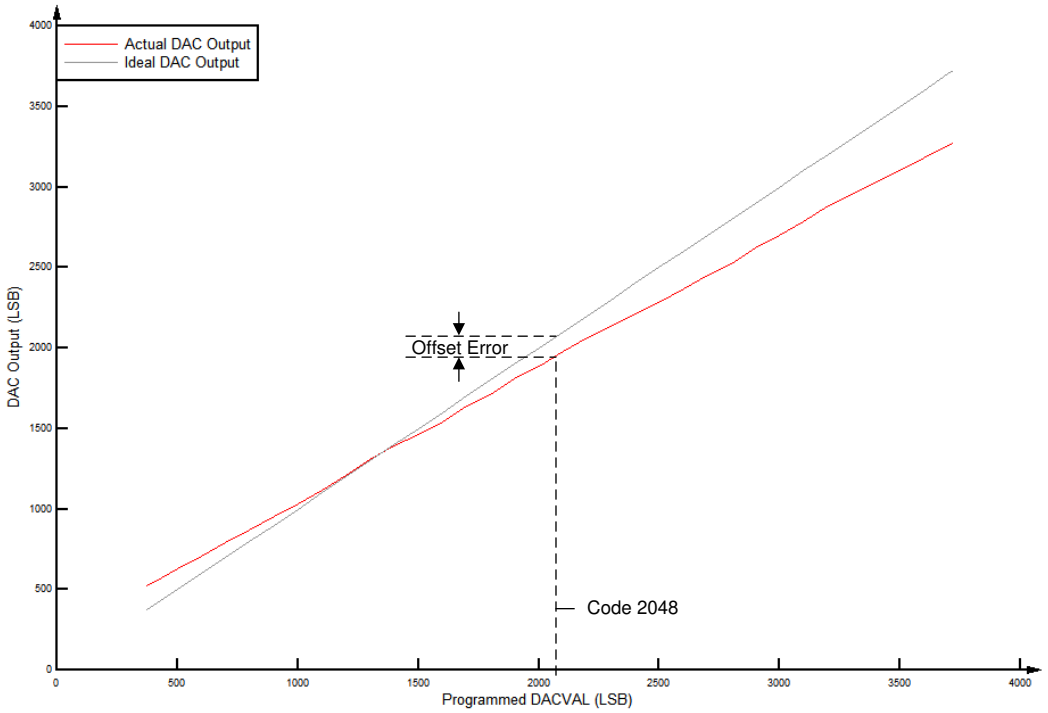


Figure 6-45. Buffered DAC Offset

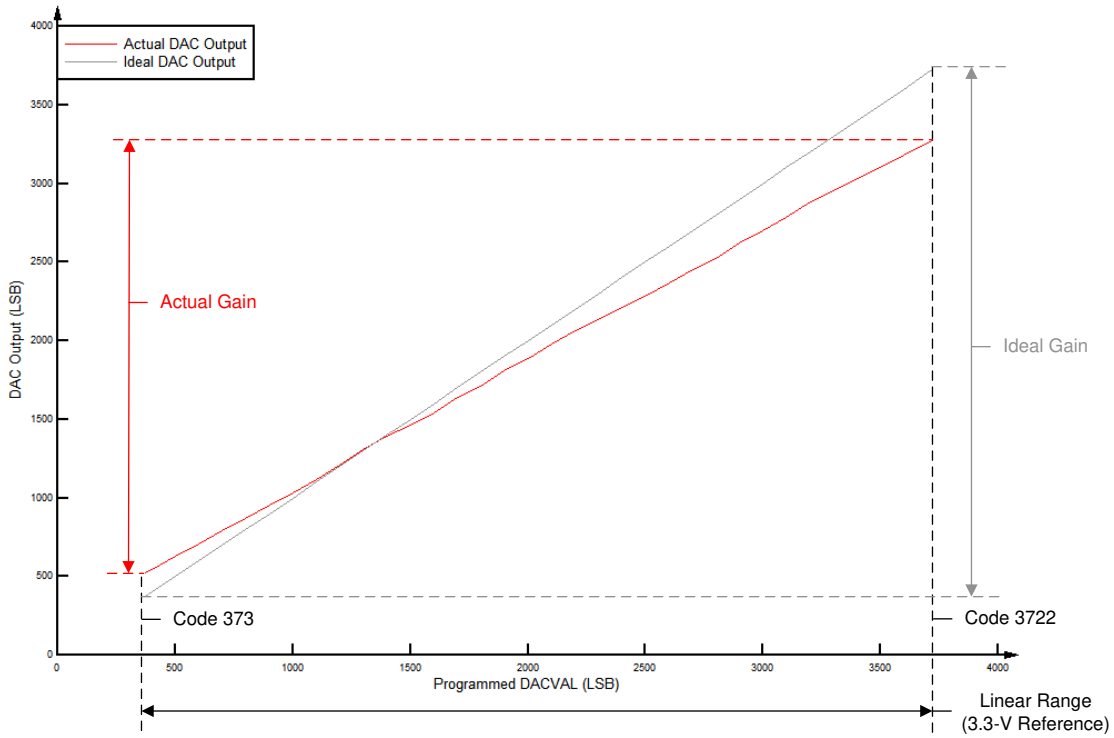


Figure 6-46. Buffered DAC Gain

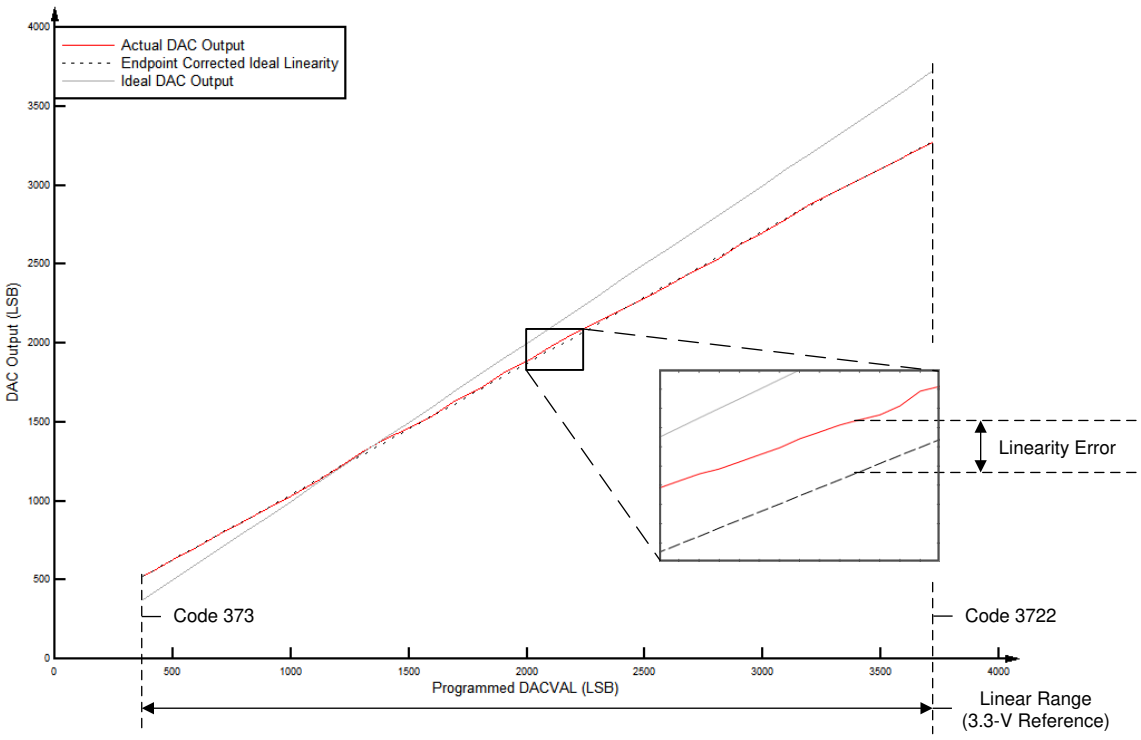


Figure 6-47. Buffered DAC Linearity

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6.10.3.2 CMPSS DAC Dynamic Error

When using the ramp generator to control the internal DAC, the step size can vary based on the application need. Since the step size of the DAC is less than a full scale transition, the settling time is improved from the electrical specification listed in the *CMPSS DAC Static Electrical Characteristics* table. The equation below and Figure 6-48 can give guidance on the expected voltage error from ideal based on different RAMPxDECVALA values.

$$DYNAMICERROR = (m \times RAMPxDECVALA) + b \quad (5)$$

Table 6-12. DAC Max Dynamic Error Terms

EQUATION PARAMETER	MIN (LSB)	MAX (LSB)
m	0.167	0.30
b	3.7	5.6

Note

Above error terms are based on the max SYSCLK of the target device. If operating below the max SYSCLK then the "m" error term should be scaled accordingly.

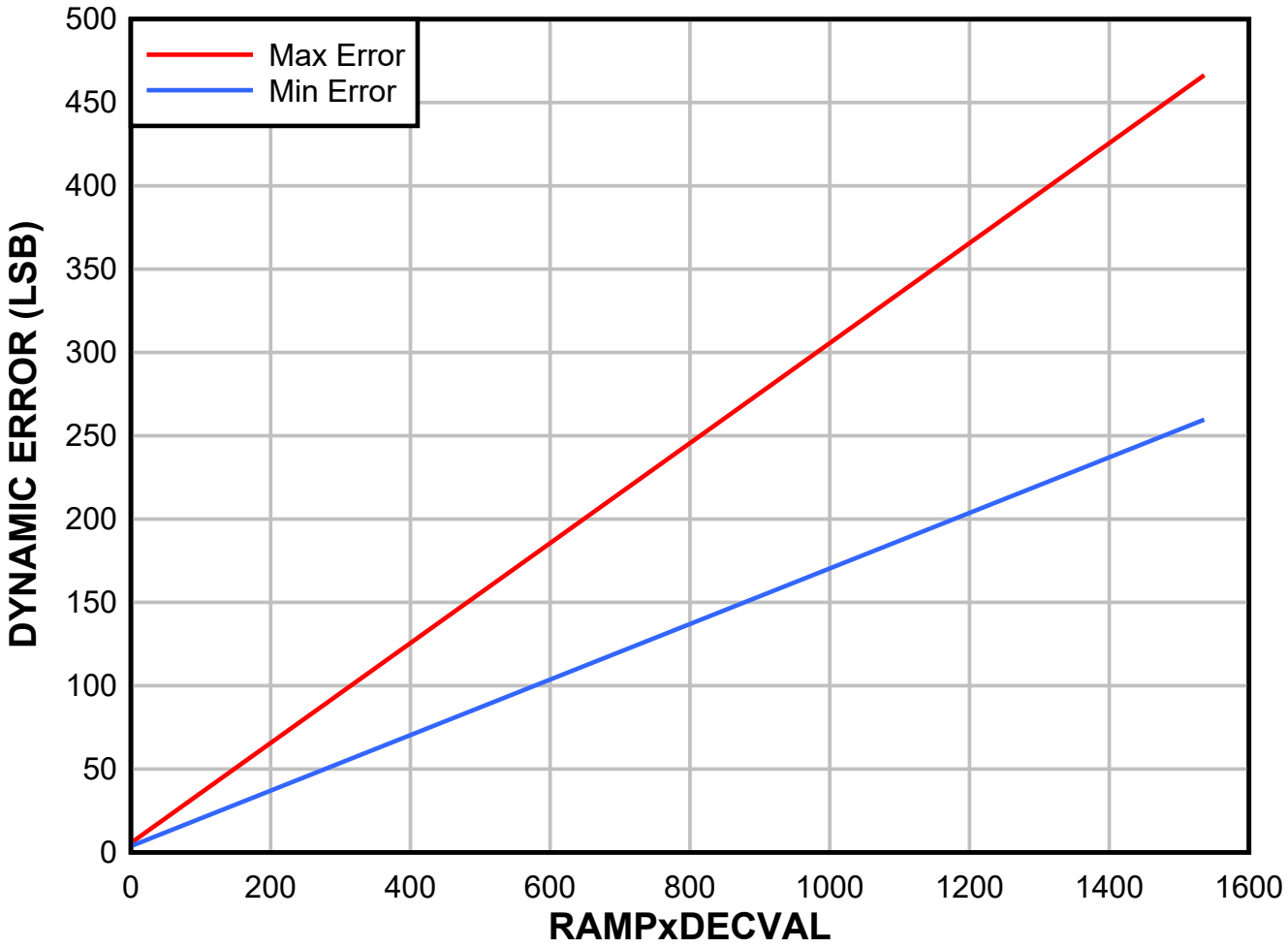


Figure 6-48. CMPSS DAC Dynamic Error

6.11 Control Peripherals

Note

For the actual number of each peripheral on a specific device, see Table 4-1.

6.11.1 Enhanced Capture (eCAP)

The eCAP module can be used in systems where accurate timing of external events is important.

Applications for eCAP include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module includes the following features:

- 4-event time-stamp registers (each 32 bits)
- Edge-polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event timestamps
- Continuous mode capture of timestamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All of the above resources dedicated to a single input pin
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).

The eCAP inputs connect to any GPIO input through the Input X-BAR. The APWM outputs connect to GPIO pins through the Output X-BAR to OUTPUTx positions in the GPIO mux. See Section 5.4.2 and Section 5.4.3.

Figure 6-49 shows the block diagram of an eCAP module.

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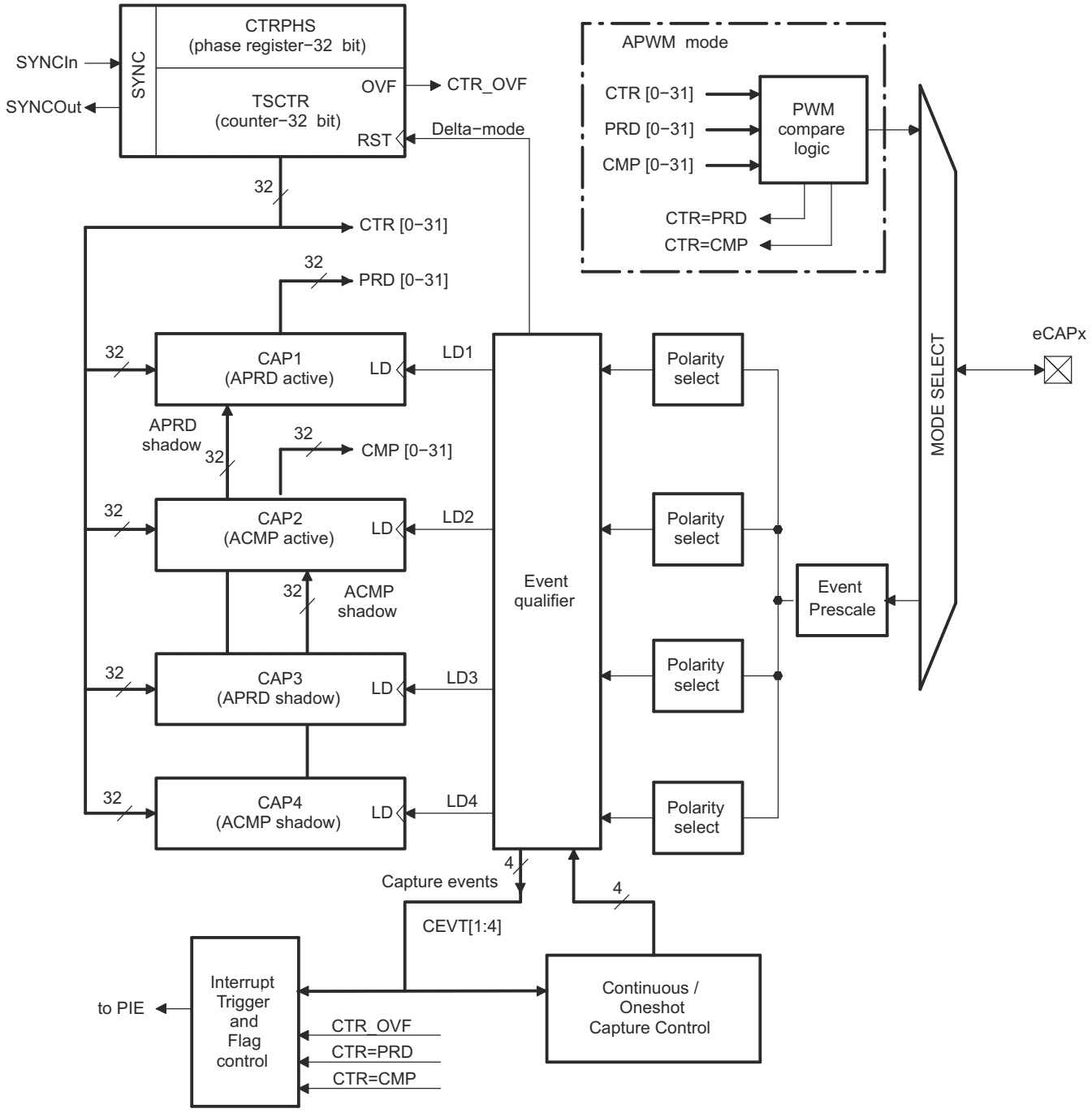


Figure 6-49. eCAP Block Diagram

The eCAP module is clocked by PERx.SYSCLK.

The clock enable bits (ECAP1–ECAP6) in the PCLKCR3 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

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6.11.1.1 eCAP Electrical Data and Timing

Section 6.11.1.1.1 shows the eCAP timing requirement and Section 6.11.1.1.2 shows the eCAP switching characteristics.

6.11.1.1.1 eCAP Timing Requirement

			MIN[1]	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SYSCLK)}$		cycles
		Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$1t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.

6.11.1.1.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20		ns

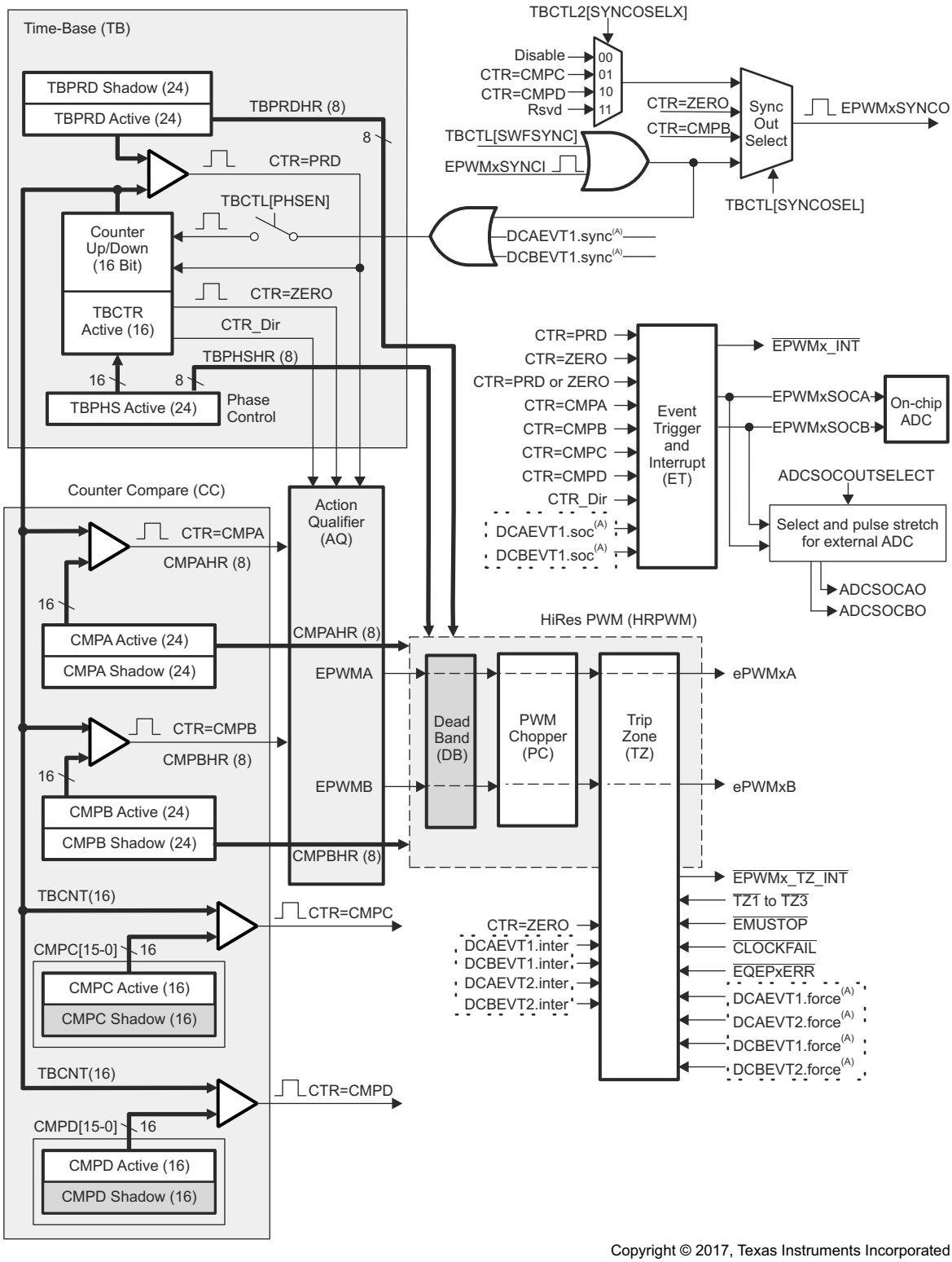
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6.11.2 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

Figure 6-50 shows the signal interconnections with the ePWM. Figure 6-51 shows the ePWM trip input connectivity.

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A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-50. ePWM Submodules and Critical Internal Signal Interconnects

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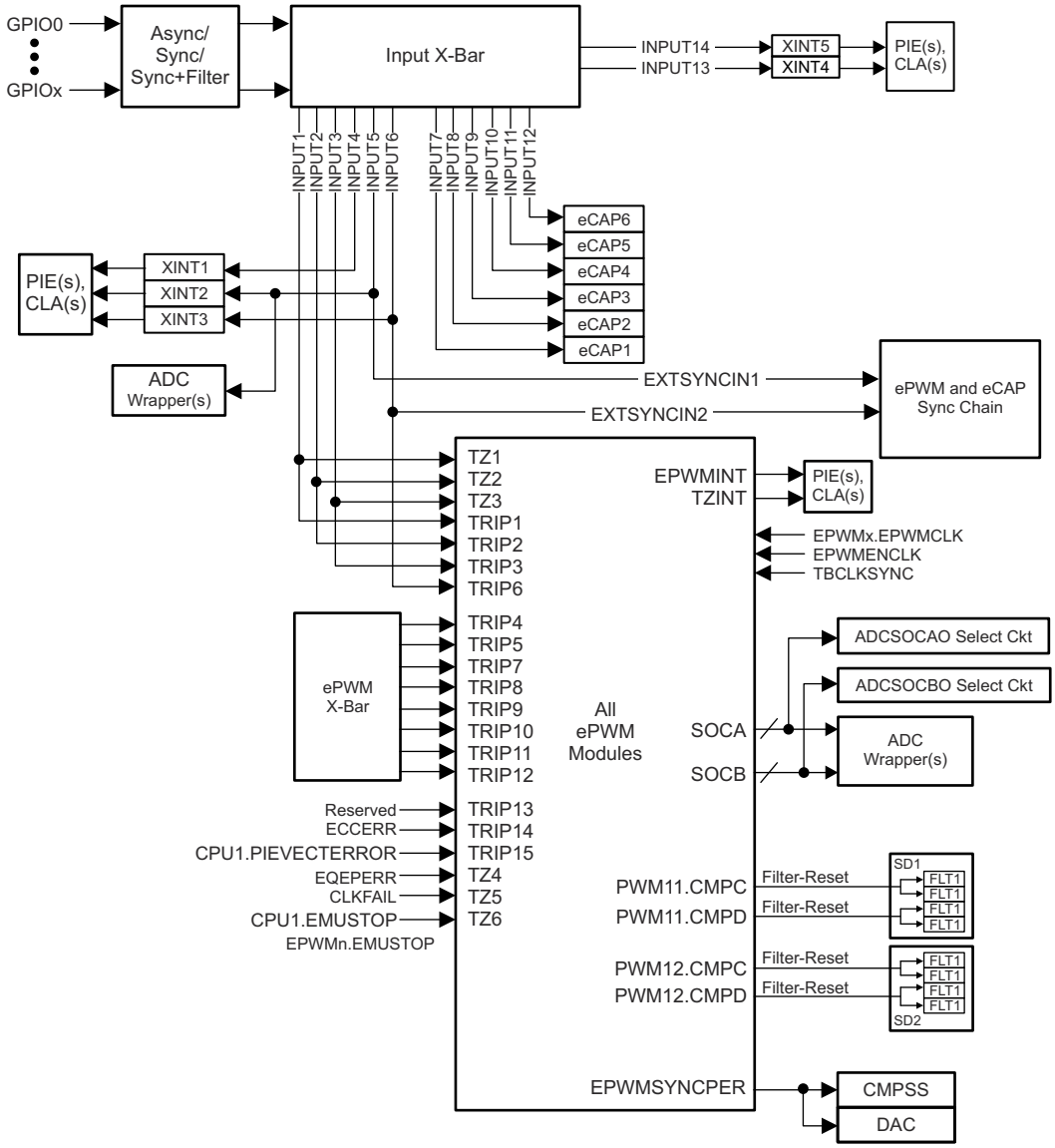


Figure 6-51. ePWM Trip Input Connectivity

6.11.2.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization chain allows synchronization between multiple modules for the system. Figure 6-52 shows the synchronization chain architecture.

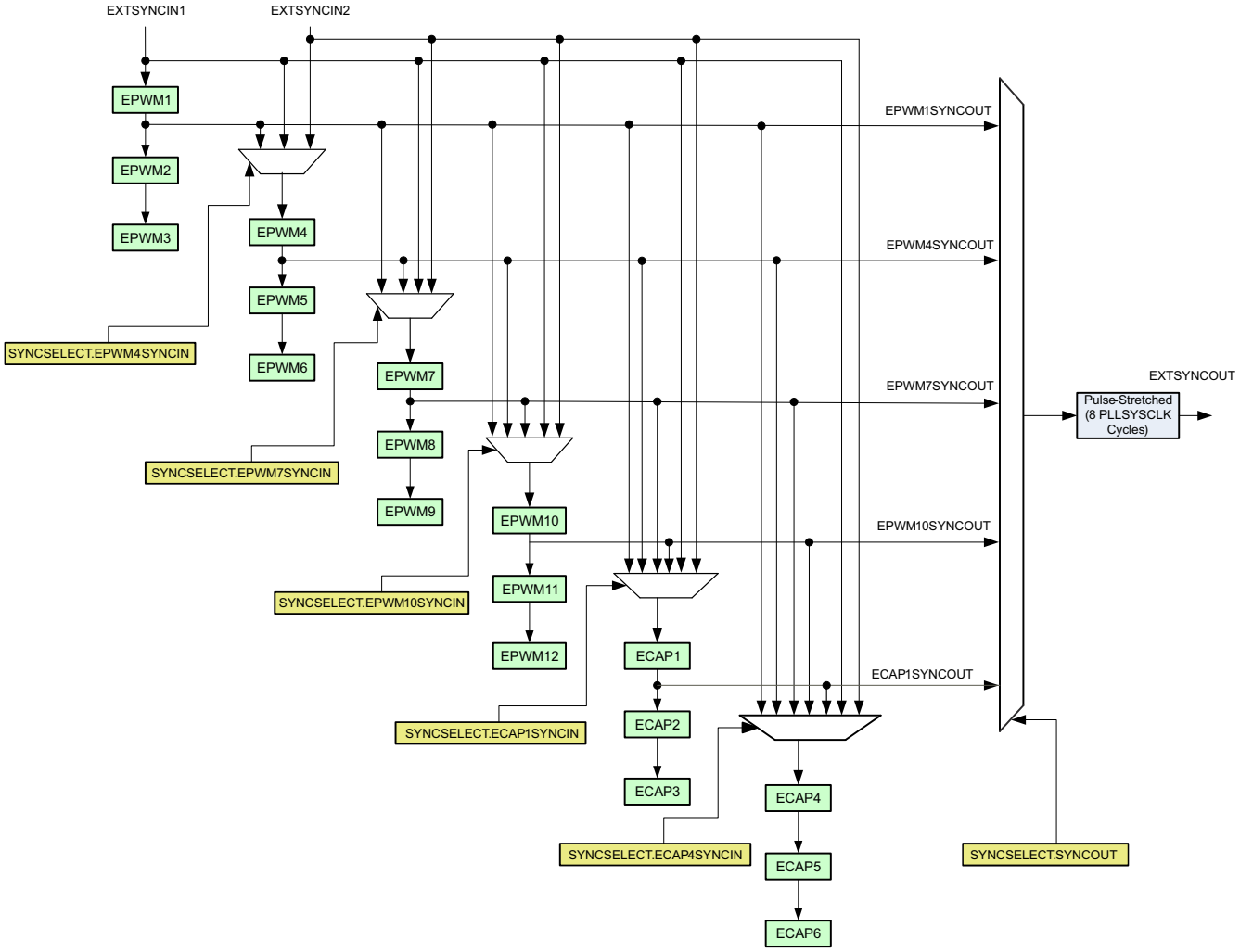


Figure 6-52. Synchronization Chain Architecture

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6.11.2.2 ePWM Electrical Data and Timing

Section 6.11.2.2.1 shows the PWM timing requirements and Section 6.11.2.2.2 shows the PWM switching characteristics.

6.11.2.2.1 ePWM Timing Requirements

			MIN(1)	MAX	UNIT
$f_{(EPWM)}$	Frequency, EPWMCLK(2)			100	MHz
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.
(2) For SYSCLK above 100 MHz, the EPWMCLK must be half of SYSCLK.

6.11.2.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		25	ns

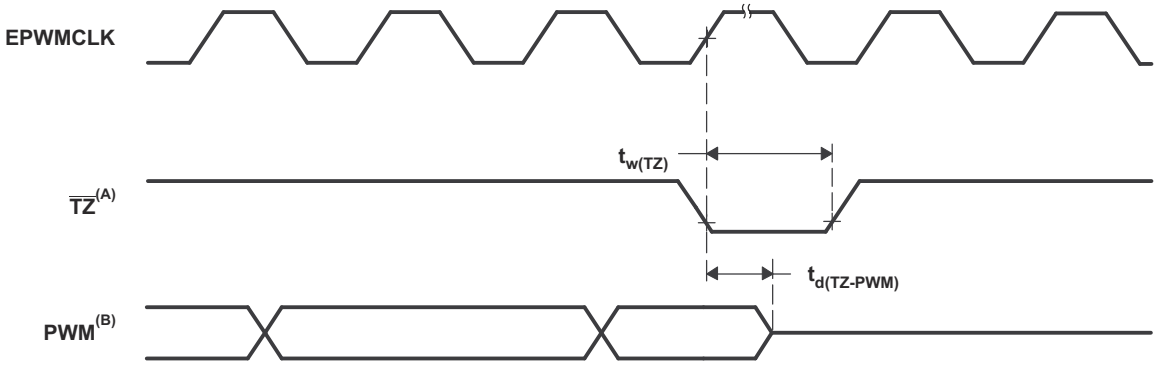
6.11.2.2.3 Trip-Zone Input Timing

Section 6.11.2.2.3.1 shows the trip-zone input timing requirements. Figure 6-53 shows the PWM Hi-Z characteristics.

6.11.2.2.3.1 Trip-Zone Input Timing Requirements

			MIN(1)	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(EPWMCLK)}$		cycles
		Synchronous	$2t_{c(EPWMCLK)}$		cycles
		With input qualifier	$1t_{c(EPWMCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12
B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-53. PWM Hi-Z Characteristics

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6.11.2.3 External ADC Start-of-Conversion Electrical Data and Timing

Section 6.11.2.3.1 shows the external ADC start-of-conversion switching characteristics. Figure 6-54 shows the $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ timing.

6.11.2.3.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{\text{ADCSOCxO}}$ low	$32t_{c(SYSCLK)}$		cycles

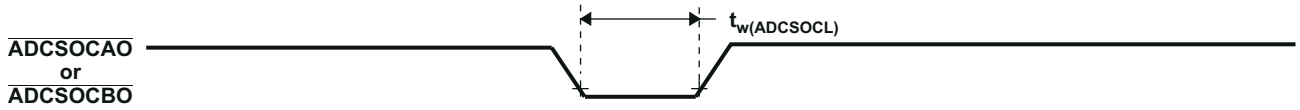


Figure 6-54. $\overline{\text{ADCSOCAO}}$ or $\overline{\text{ADCSOCBO}}$ Timing

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6.11.3 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position-control systems.

Each eQEP peripheral comprises five major functional blocks:

- Quadrature Capture Unit (QCAP)
- Position Counter/Control Unit (PCCU)
- Quadrature Decoder Unit (QDU)
- Unit Time Base for speed and frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)

The eQEP peripherals are clocked by PERx.SYSCLK. Figure 6-55 shows the eQEP block diagram.

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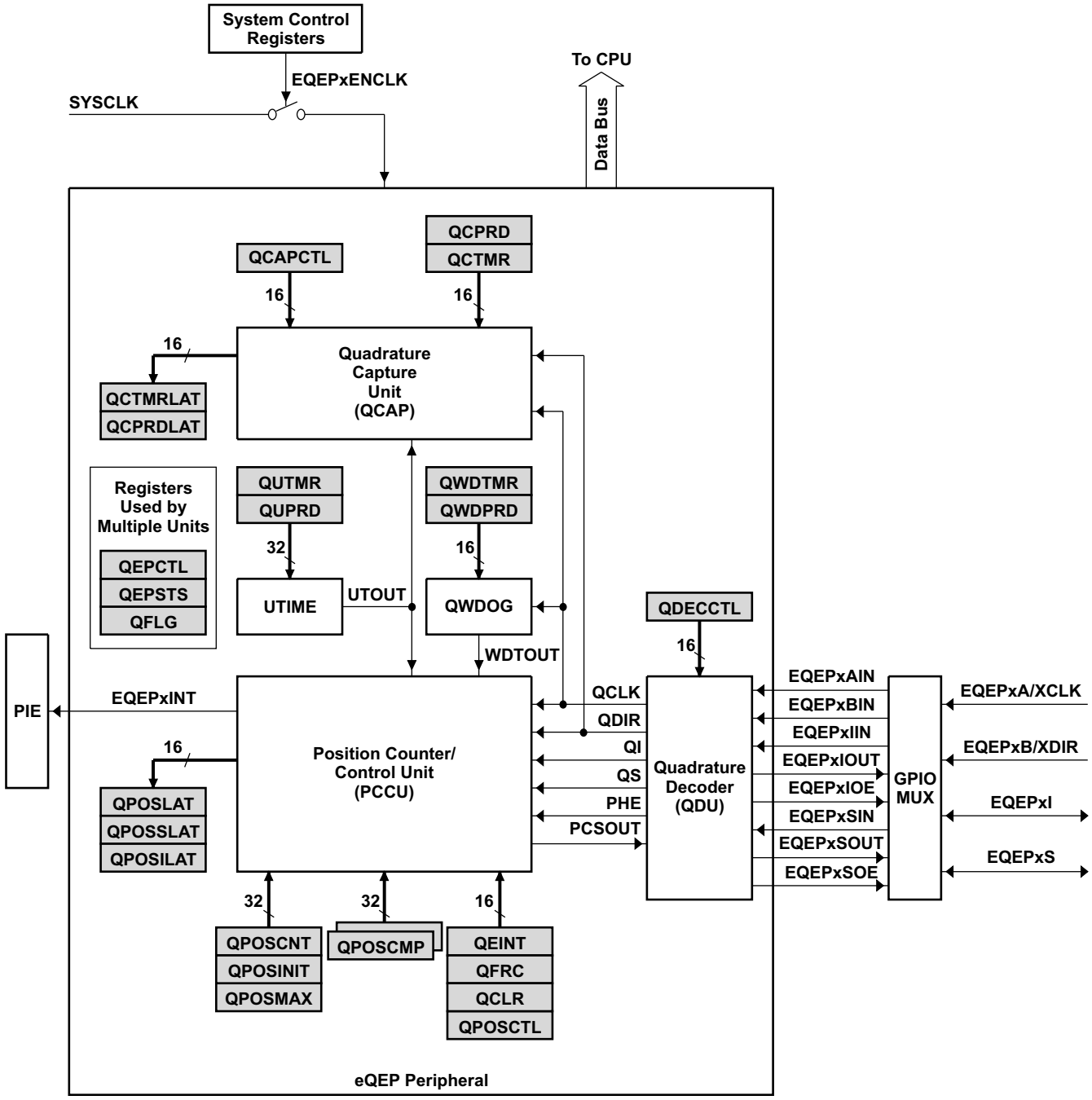


Figure 6-55. eQEP Block Diagram

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6.11.3.1 eQEP Electrical Data and Timing

Section 6.11.3.1.1 lists the eQEP timing requirement and Section 6.11.3.1.2 lists the eQEP switching characteristics.

6.11.3.1.1 eQEP Timing Requirements

			MIN(1)	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		cycles
$t_{w(INDEXH)}$	QEP Index Input High time	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(INDEXL)}$	QEP Index Input Low time	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBH)}$	QEP Strobe High time	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles
$t_{w(STROBL)}$	QEP Strobe Input Low time	Asynchronous(2)/Synchronous	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 6.9.8.2.1.
(2) See the *TMS320F2807x Real-Time MCUs Silicon Errata* for limitations in the asynchronous mode.

6.11.3.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$4t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$6t_{c(SYSCLK)}$	cycles

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6.11.4 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

Note

The minimum HRPWMCLK frequency allowed for HRPWM is 60 MHz.

6.11.4.1 HRPWM Electrical Data and Timing

Section 6.11.4.1.1 lists the high-resolution PWM timing requirements. Section 6.11.4.1.2 lists the high-resolution PWM switching characteristics.

6.11.4.1.1 High-Resolution PWM Timing Requirements

		MIN	MAX	UNIT
$f_{(EPWM)}$	Frequency, EPWMCLK(1)		100	MHz
$f_{(HRPWM)}$	Frequency, HRPWMCLK	60	100	MHz

(1) For SYSCLK above 100 MHz, the EPWMCLK must be half of SYSCLK.

6.11.4.1.2 High-Resolution PWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)		150	310	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

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6.11.5 Sigma-Delta Filter Module (SDFM)

The SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent sigma-delta (ΣΔ) modulated bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator for immediate digital threshold comparisons for overcurrent and undercurrent monitoring. Figure 6-56 shows a block diagram of the SDFMs.

SDFM features include:

- Eight external pins per SDFM module:
  - Four sigma-delta data input pins per SDFM module (SDx_Dy, where x = 1 to 2 and y = 1 to 4)
  - Four sigma-delta clock input pins per SDFM module (SDx_Cy, where x = 1 to 2 and y = 1 to 4)
- Four different configurable modulator clock modes:
  - Modulator clock rate equals modulator data rate
  - Modulator clock rate running at half the modulator data rate
  - Modulator data is Manchester encoded. Modulator clock not required.
  - Modulator clock rate is double that of modulator data rate
- Four independent configurable comparator units:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Ability to detect over-value and under-value conditions
  - Comparator Over-Sampling Ratio (COSR) value for comparator programmable from 1 to 32
- Four independent configurable data filter units:
  - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
  - Data filter Over-Sampling Ratio (DOSR) value for data filter unit programmable from 1 to 256
  - Ability to enable or disable individual filter module
  - Ability to synchronize all four independent filters of a SDFM module using the Master Filter Enable (MFE) bit or the PWM signals.
- Filter data can be 16-bit or 32-bit representation
- PWMs can be used to generate modulator clock for sigma-delta modulators

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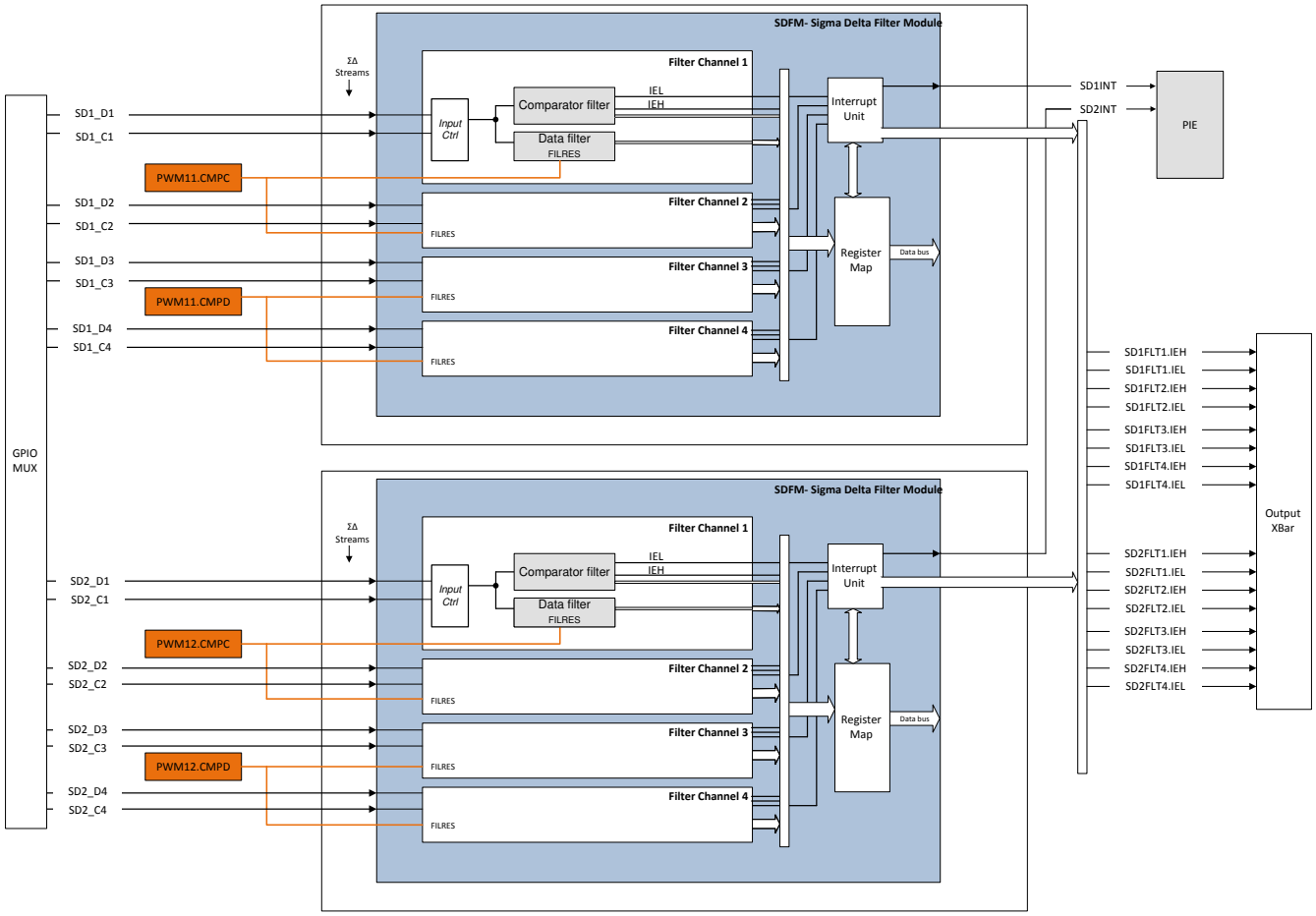


Figure 6-56. SDFM Block Diagram

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6.11.5.1 SDFM Electrical Data and Timing (Using ASYNC)

SDFM operation with asynchronous GPIO is defined by setting GPyQSELn = 0b11. Section 6.11.5.1.1 lists the SDFM timing requirements when using the asynchronous GPIO (ASYNC) option. Figure 6-57 through Figure 6-60 show the SDFM timing diagrams.

6.11.5.1.1 SDFM Timing Requirements When Using Asynchronous GPIO (ASYNC) Option

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	40	256 * SYSCLK period	ns
$t_{w(SDCH)M0}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M0}$ – 10	ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns
Mode 1				
$t_{c(SDC)M1}$	Cycle time, SDx_Cy	80	256 * SYSCLK period	ns
$t_{w(SDCH)M1}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M1}$ – 10	ns
$t_{su(SDDV-SDCL)M1}$	Setup time, SDx_Dy valid before SDx_Cy goes low	5		ns
$t_{su(SDDV-SDCH)M1}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCL-SDD)M1}$	Hold time, SDx_Dy wait after SDx_Cy goes low	5		ns
$t_{h(SDCH-SDD)M1}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns
Mode 2				
$t_{c(SDD)M2}$	Cycle time, SDx_Dy	8 * $t_{c(SYSCLK)}$	20 * $t_{c(SYSCLK)}$	ns
$t_{w(SDDH)M2}$	Pulse duration, SDx_Dy high	10		ns
$t_{w(SDD_LONG_KEEPOUT)M2}$	SDx_Dy long pulse duration keepout, where the long pulse must not fall within the MIN or MAX values listed. Long pulse is defined as the high or low pulse which is the full width of the Manchester bit-clock period. This requirement must be satisfied for any integer between 8 and 20.	(N * $t_{c(SYSCLK)}$) – 0.5	(N * $t_{c(SYSCLK)}$) + 0.5	ns
$t_{w(SDD_SHORT)M2}$	SDx_Dy Short pulse duration for a high or low pulse (SDD_SHORT_H or SDD_SHORT_L). Short pulse is defined as the high or low pulse which is half the width of the Manchester bit-clock period.	$t_{w(SDD_LONG)}$ / 2 – $t_{c(SYSCLK)}$	$t_{w(SDD_LONG)}$ / 2 + $t_{c(SYSCLK)}$	ns
$t_{w(SDD_LONG_DUTY)M2}$	SDx_Dy Long pulse variation (SDD_LONG_H – SDD_LONG_L)	– $t_{c(SYSCLK)}$	$t_{c(SYSCLK)}$	ns
$t_{w(SDD_SHORT_DUTY)M2}$	SDx_Dy Short pulse variation (SDD_SHORT_H – SDD_SHORT_L)	– $t_{c(SYSCLK)}$	$t_{c(SYSCLK)}$	ns
Mode 3				
$t_{c(SDC)M3}$	Cycle time, SDx_Cy	40	256 * SYSCLK period	ns
$t_{w(SDCH)M3}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M3}$ – 5	ns
$t_{su(SDDV-SDCH)M3}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCH-SDD)M3}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns

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WARNING

The SDFM clock inputs (SDx_Cy pins) directly clock the SDFM module when there is no GPIO input synchronization. Any glitches or ringing noise on these inputs can corrupt the SDFM module operation. Special precautions should be taken on these signals to ensure a clean and noise-free signal that meets SDFM timing requirements. Precautions such as series termination for ringing due to any impedance mismatch of the clock driver and spacing of traces from other noisy signals are recommended.

WARNING

See the "SDFM: Manchester Mode (Mode 2) Does Not Produce Correct Filter Results Under Several Conditions" advisory in the *TMS320F2807x Real-Time MCUs Silicon Errata*.

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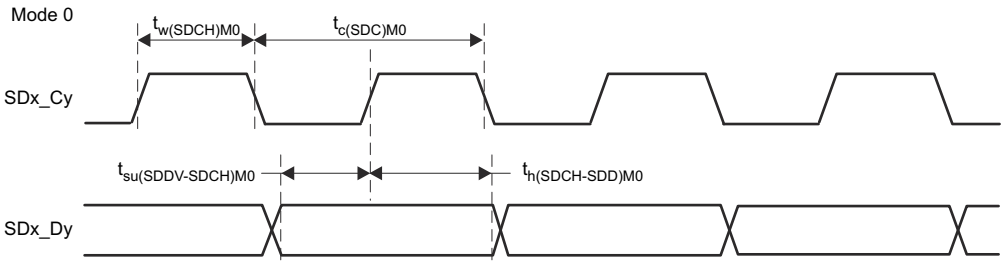


Figure 6-57. SDFM Timing Diagram – Mode 0

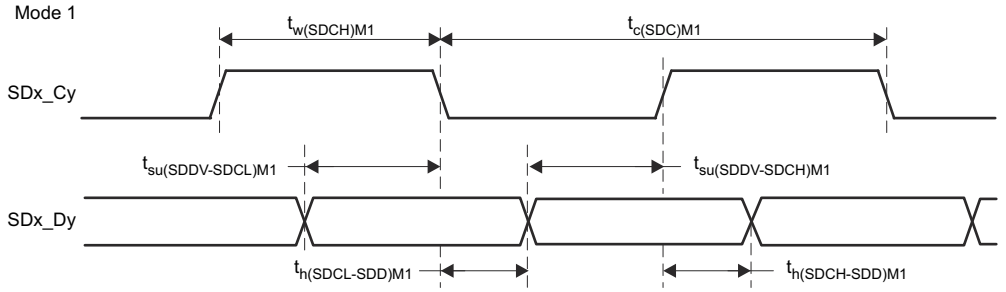


Figure 6-58. SDFM Timing Diagram – Mode 1

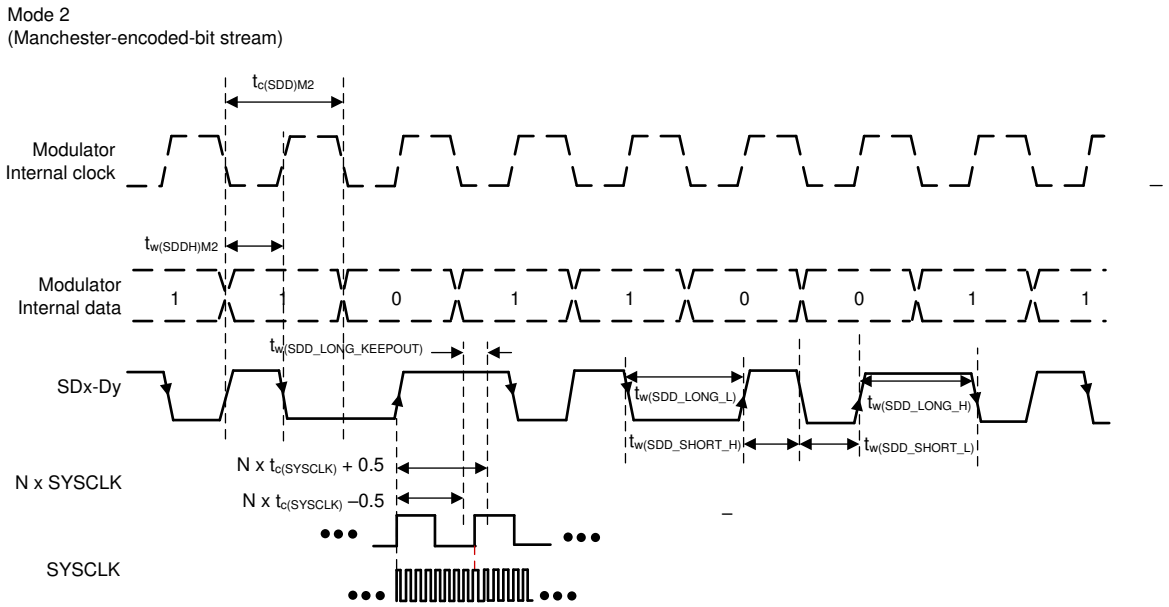


Figure 6-59. SDFM Timing Diagram – Mode 2

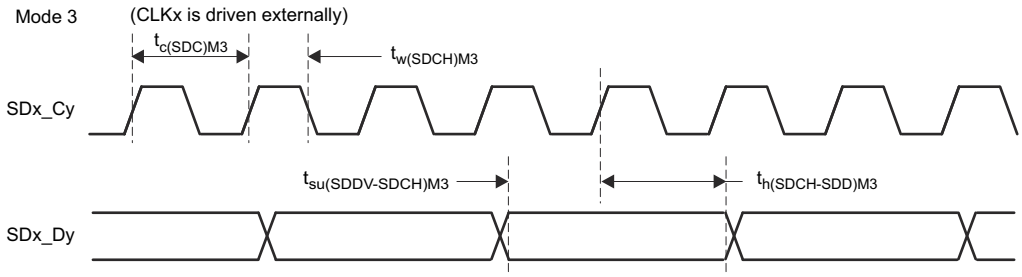


Figure 6-60. SDFM Timing Diagram – Mode 3

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6.11.5.2 SDFM Electrical Data and Timing (Using 3-Sample GPIO Input Qualification)

SDFM operation with qualified GPIO (3-sample window) is defined by setting GPyQSELn = 0b01. When using this qualified GPIO (3-sample window) mode, the timing requirement for the $t_{w(GPI)}$ pulse duration of $2t_{c(SYSCLK)}$ must be met. It is important for both SD-Cx and SD-Dx pairs to be configured with the same GPIO qualification option. Section 6.11.5.2.1 lists the SDFM timing requirements when using the GPIO input qualification (3-sample window) option. Figure 6-57 through Figure 6-60 show the SDFM timing diagrams.

6.11.5.2.1 SDFM Timing Requirements When Using GPIO Input Qualification (3-Sample Window) Option

		MIN(1)	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	10 * SYSCLK period	256 * SYSCLK period	ns
$t_{w(SDCHL)M0}$	Pulse duration, SDx_Cy high/low	4 * SYSCLK period	6 * SYSCLK period	ns
$t_{w(SDDHL)M0}$	Pulse duration, SDx_Dy high/low	4 * SYSCLK period		ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	2 * SYSCLK period		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	2 * SYSCLK period		ns
Mode 1				
$t_{c(SDC)M1}$	Cycle time, SDx_Cy	20 * SYSCLK period	256 * SYSCLK period	ns
$t_{w(SDCH)M1}$	Pulse duration, SDx_Cy high	4 * SYSCLK period	6 * SYSCLK period	ns
$t_{w(SDDHL)M1}$	Pulse duration, SDx_Dy high/low	4 * SYSCLK period		ns
$t_{su(SDDV-SDCL)M1}$	Setup time, SDx_Dy valid before SDx_Cy goes low	2 * SYSCLK period		ns
$t_{su(SDDV-SDCH)M1}$	Setup time, SDx_Dy valid before SDx_Cy goes high	2 * SYSCLK period		ns
$t_{h(SDCL-SDD)M1}$	Hold time, SDx_Dy wait after SDx_Cy goes low	2 * SYSCLK period		ns
$t_{h(SDCH-SDD)M1}$	Hold time, SDx_Dy wait after SDx_Cy goes high	2 * SYSCLK period		ns
Mode 2				
$t_{c(SDD)M2}$	Cycle time, SDx_Dy	Option unavailable		
$t_{w(SDDH)M2}$	Pulse duration, SDx_Dy high			
Mode 3				
$t_{c(SDC)M3}$	Cycle time, SDx_Cy	10 * SYSCLK period	256 * SYSCLK period	ns
$t_{w(SDCHL)M3}$	Pulse duration, SDx_Cy high	4 * SYSCLK period	6 * SYSCLK period	ns
$t_{w(SDDHL)M3}$	Pulse duration, SDx_Dy high/low	4 * SYSCLK period		ns
$t_{su(SDDV-SDCH)M3}$	Setup time, SDx_Dy valid before SDx_Cy goes high	2 * SYSCLK period		ns
$t_{h(SDCH-SDD)M3}$	Hold time, SDx_Dy wait after SDx_Cy goes high	2 * SYSCLK period		ns

(1) SDFM timing requirements apply only when the GPIO input qualification type is the 3-sample window (GPyQSELx = 1; QUALPRD = 0) option. It is important that both the SD-Cx and SD-Dx pairs be configured with the 3-sample window option.

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Note

The SDFM Qualified GPIO (3-sample) mode provides protection against SDFM module corruption due to occasional random noise glitches on the SDx_Cy pin that may result in a false comparator trip and filter output. For more details, refer to the "SDFM: Use Caution While Using SDFM Under Noisy Conditions" usage note in the *TMS320F2807x Real-Time MCUs Silicon Errata*.

The SDFM Qualified GPIO (3-sample) mode does not provide protection against persistent violations of the above timing requirements. Timing violations will result in data corruption proportional to the number of bits which violate the requirements.

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6.12 Communications Peripherals

Note

For the actual number of each peripheral on a specific device, see Table 4-1.

6.12.1 Controller Area Network (CAN)

The CAN module performs CAN protocol communication according to ISO 11898-1 (identical to Bosch® CAN protocol specification 2.0 A, B). The bit rate can be programmed to values up to 1 Mbps. A CAN transceiver chip is required for the connection to the physical layer (CAN bus).

For communication on a CAN network, individual message objects can be configured. The message objects and identifier masks are stored in the Message RAM.

All functions concerning the handling of messages are implemented in the message handler. These functions are: acceptance filtering; the transfer of messages between the CAN Core and the Message RAM; and the handling of transmission requests.

The register set of the CAN may be accessed directly by the CPU through the module interface. These registers are used to control and configure the CAN core and the message handler, and to access the message RAM.

The CAN module implements the following features:

- Complies with ISO11898-1 (Bosch® CAN protocol specification 2.0 A and B)
- Bit rates up to 1 Mbps
- Multiple clock sources
- 32 message objects (“message objects” are also referred to as “mailboxes” in this document; the two terms are used interchangeably), each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard (11-bit) or extended (29-bit) identifier
  - Supports programmable identifier receive mask
  - Supports data and remote frames
  - Holds 0 to 8 bytes of data
  - Parity-checked configuration and data RAM
- Individual identifier mask for each message object
- Programmable FIFO mode for message objects
- Programmable loop-back modes for self-test operation
- Suspend mode for debug support
- Software module reset
- Automatic bus-on, after bus-off state by a programmable 32-bit timer
- Message-RAM parity-check mechanism
- Two interrupt lines

Note

For a CAN bit clock of 200 MHz, the smallest bit rate possible is 7.8125 kbps.

Note

Depending on the timing settings used, the accuracy of the on-chip zero-pin oscillator (specified in the data manual) may not meet the requirements of the CAN protocol. In this situation, an external clock source must be used.

Figure 6-61 shows the CAN block diagram.

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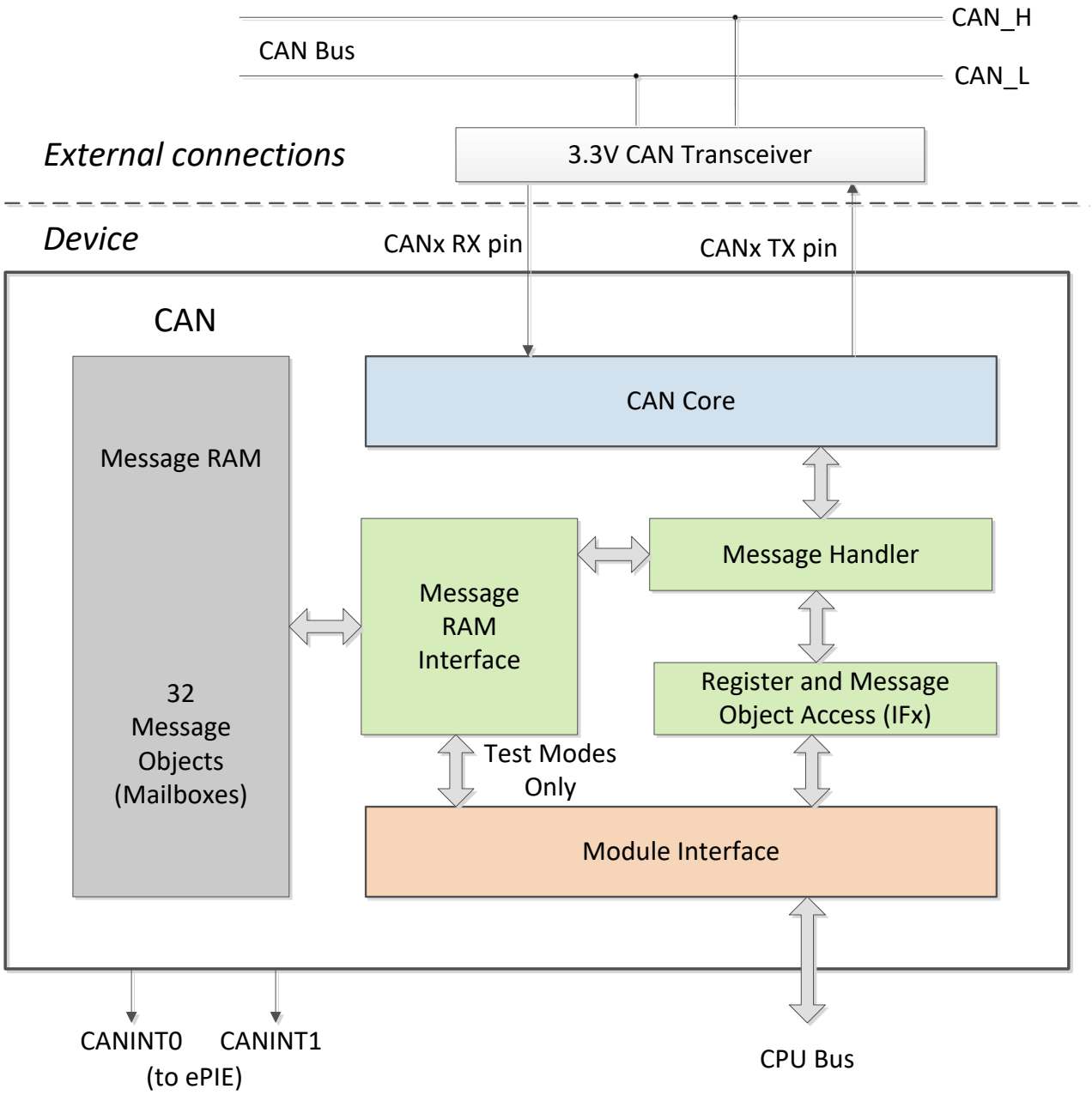


Figure 6-61. CAN Block Diagram

6.12.2 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the Philips Semiconductors I^2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

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Figure 6-62 shows how the I2C peripheral module interfaces within the device.

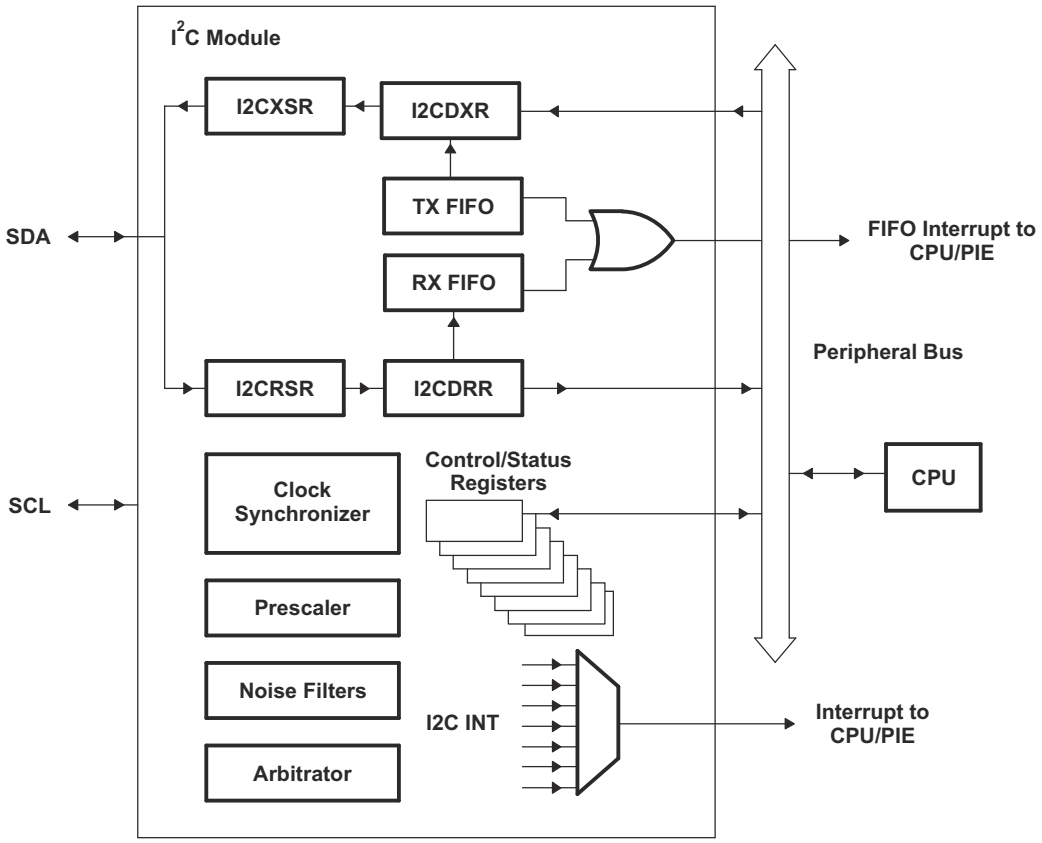


Figure 6-62. I2C Peripheral Module Interfaces

6.12.2.1 I2C Electrical Data and Timing

Section 6.12.2.1.1 lists the I2C timing requirements. Section 6.12.2.1.2 lists the I2C switching characteristics. Figure 6-63 shows the I2C timing diagram.

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

A pullup resistor must be chosen to meet the I2C standard timings. In most circumstances, 2.2 kΩ of total bus resistance to VDDIO is sufficient. For evaluating pullup resistor values for a particular design, see the *I2C Bus Pullup Resistor Calculation* Application Report.

6.12.2.1.1 I2C Timing Requirements

NO.			MIN	MAX	UNIT
Standard mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	4.0		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	4.7		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	250		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000(1)	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000(1)	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	4.0		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.6		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.6		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	100		ns
T5	$t_{r(SDA)}$	Rise time, SDA	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.6		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF

(1) In order to minimize the rise time, TI recommends using a strong pullup on both the SDA and SCL bus lines on the order of 2.2-kΩ net pullup resistance. It is also recommended that the value of the pullup resistance used on both SCL and SDA pins be matched.

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6.12.2.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Standard mode						
S1	f_{SCL}	SCL clock frequency		0	100	kHz
S2	T_{SCL}	SCL clock period		10		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		4.7		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		4.0		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		4.7		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			3.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			3.45	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA
Fast mode						
S1	f_{SCL}	SCL clock frequency		0	400	kHz
S2	T_{SCL}	SCL clock period		2.5		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
S8	I_I	Input current on pins	$0.1\ V_{bus} < V_i < 0.9\ V_{bus}$	–10	10	µA

6.12.2.1.3 I2C Timing Diagram

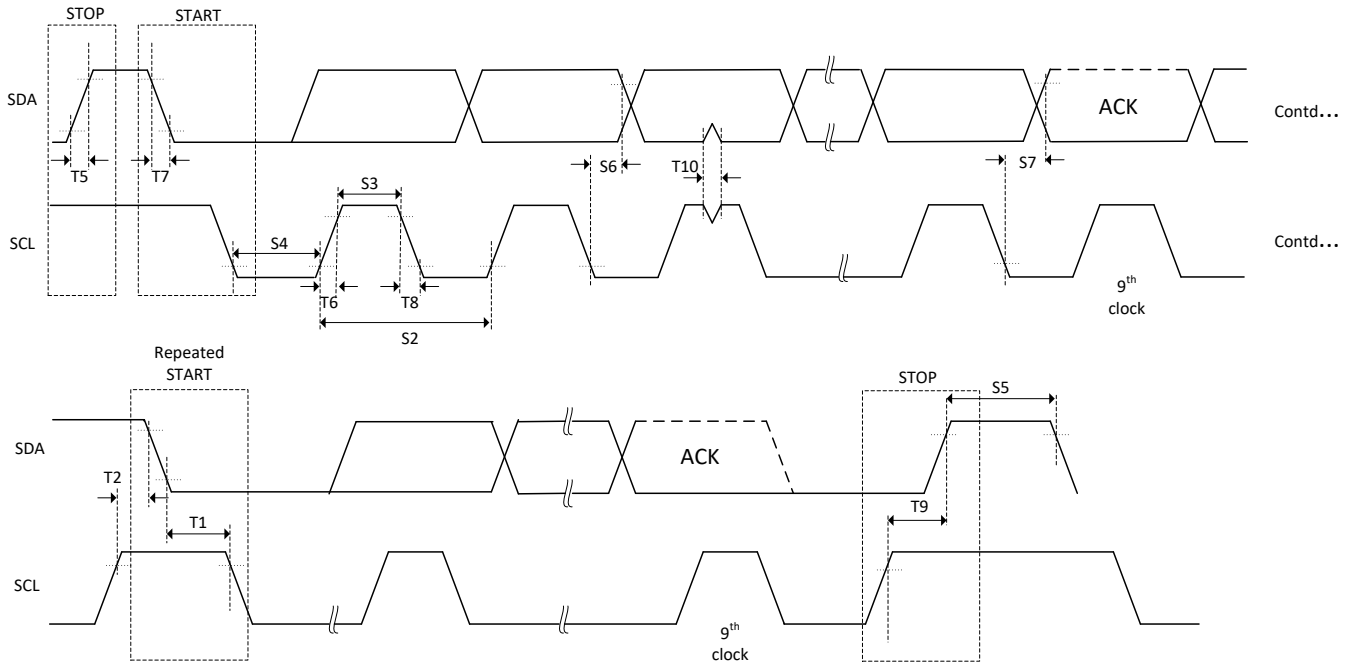


Figure 6-63. I2C Timing Diagram

6.12.3 Multichannel Buffered Serial Port (McBSP)

The McBSP module has the following features:

- Compatible with McBSP in TMS320C28x and TMS320F28x DSP devices
- Full-duplex communication
- Double-buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- 8-bit data transfer mode can be configured to transmit with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Supports AC97, I2S, and SPI protocols
- McBSP clock rate,

$$CLKG = \frac{CLKSRG}{(1 + CLKGDV)}$$

where CLKSRG source could be LSPCLK, CLKX, or CLKR.

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Figure 6-64 shows the block diagram of the McBSP module.

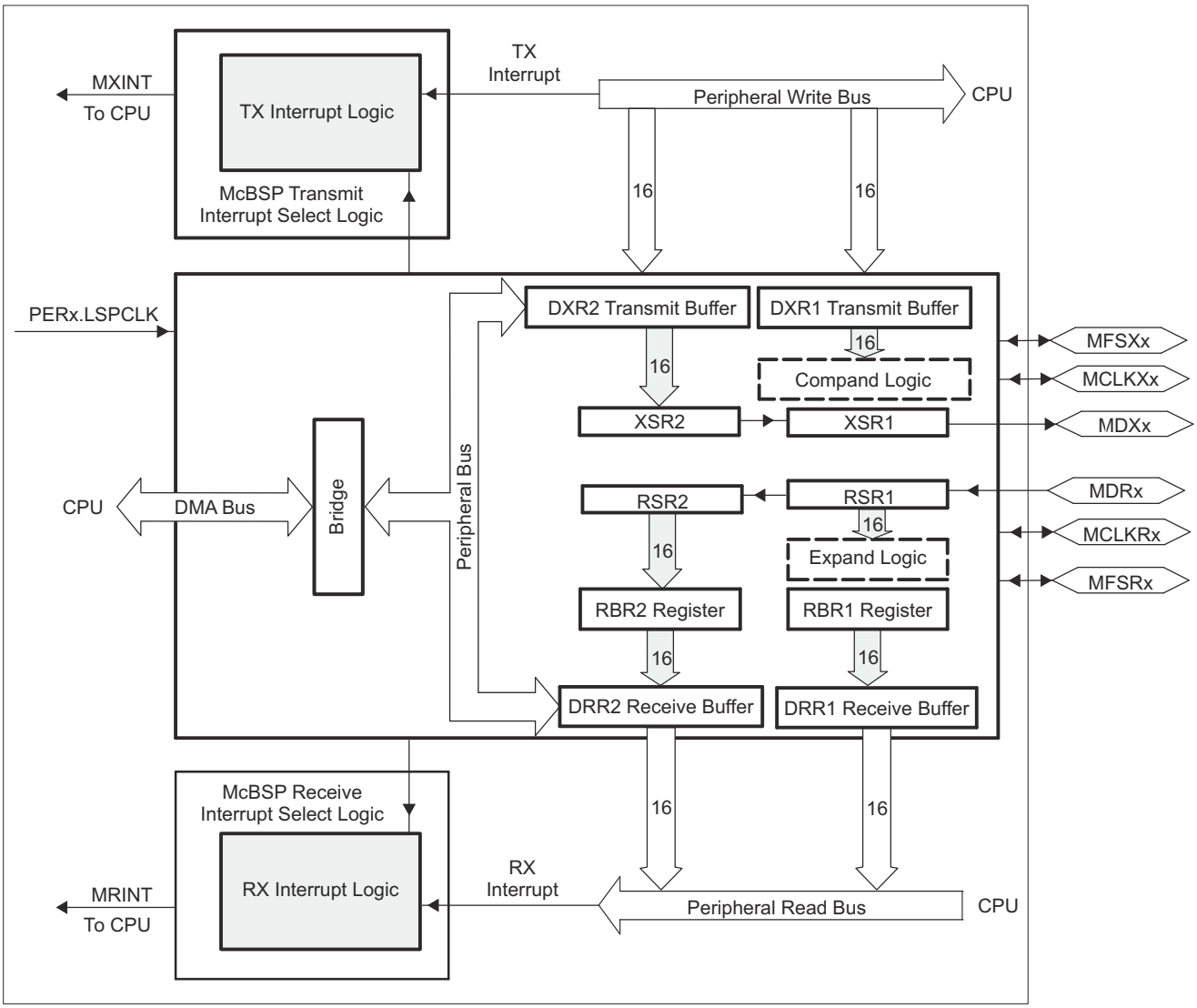


Figure 6-64. McBSP Block Diagram

6.12.3.1 McBSP Electrical Data and Timing

6.12.3.1.1 McBSP Transmit and Receive Timing

Section 6.12.3.1.1.1 shows the McBSP timing requirements. Section 6.12.3.1.1.2 shows the McBSP switching characteristics. Figure 6-65 and Figure 6-66 show the McBSP timing diagrams.

6.12.3.1.1.1 McBSP Timing Requirements

NO.(1) (2)				MIN	MAX	UNIT
		McBSP module clock (CLKG, CLKX, CLKR) range		1		kHz
					25	MHz
		McBSP module cycle time (CLKG, CLKX, CLKR) range		40		ns
					1	ms
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P – 7		ns
M13	$t_{r(CKRX)}$	Rise time, CLKR/X	CLKR/X ext		7	ns
M14	$t_{f(CKRX)}$	Fall time, CLKR/X	CLKR/X ext		7	ns
M15	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M16	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	18		ns
			CLKR ext	5		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	3		
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	18		ns
			CLKX ext	2		
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns. CLKG is the output of sample rate generator mux. CLKG = CLKSRG / (1 + CLKGDV). CLKSRG can be LSPCLK, CLKX, CLKR as source. CLKSRG ≤ (SYSCLK/2).

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6.12.3.1.1.2 McBSP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.(1) (2)	PARAMETER				MIN	MAX	UNIT
M1	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_{w(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	D – 5 (3)	D + 5 (3)	ns
M3	$t_{w(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	C – 5 (3)	C + 5 (3)	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid		CLKR int	-7	7.5	ns
				CLKR ext	3	27	
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid		CLKX int	-5	6	ns
				CLKX ext	3	27	
M6	$t_{dis(CKXH-DXHZ)}$	Disable time, CLKX high to DX high impedance following last data bit		CLKX int	–8	8	ns
				CLKX ext	3	15	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		CLKX int	–3	9	ns
				CLKX ext	5	25	
		Delay time, CLKX high to DX valid	DXENA = 0	CLKX int	–3	8	
				CLKX ext	5	20	
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int	P – 3	P + 8	
				CLKX ext	P + 5	P + 20	
M8	$t_{en(CKXH-DX)}$	Enable time, CLKX high to DX driven	DXENA = 0	CLKX int	-6		ns
				CLKX ext	4		
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int	P - 6		
				CLKX ext	P + 4		
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid	DXENA = 0	FSX int		8	ns
				FSX ext		17	
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode.	DXENA = 1	FSX int		P + 8	
				FSX ext		P + 17	
M10	$t_{en(FXH-DX)}$	Enable time, FSX high to DX driven	DXENA = 0	FSX int	-3		ns
				FSX ext	6		
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode	DXENA = 1	FSX int	P - 3		
				FSX ext	P + 6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns.
(3) C = CLKRX low pulse width = P
D = CLKRX high pulse width = P

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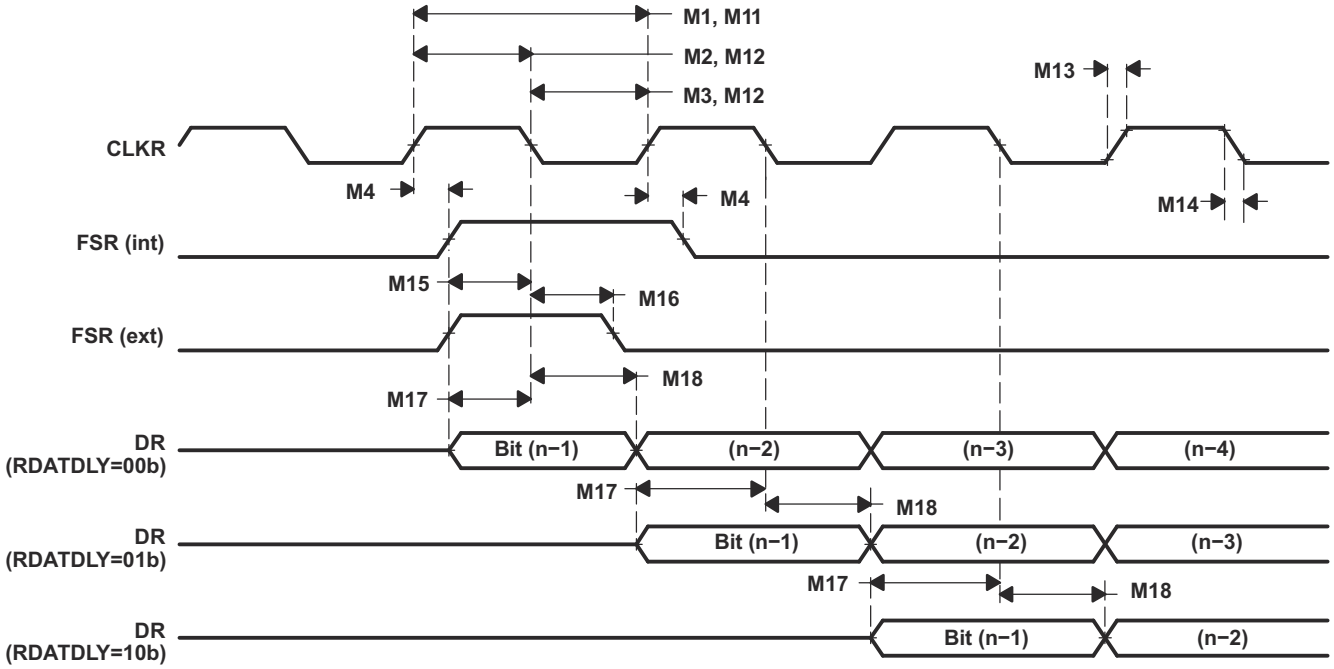


Figure 6-65. McBSP Receive Timing

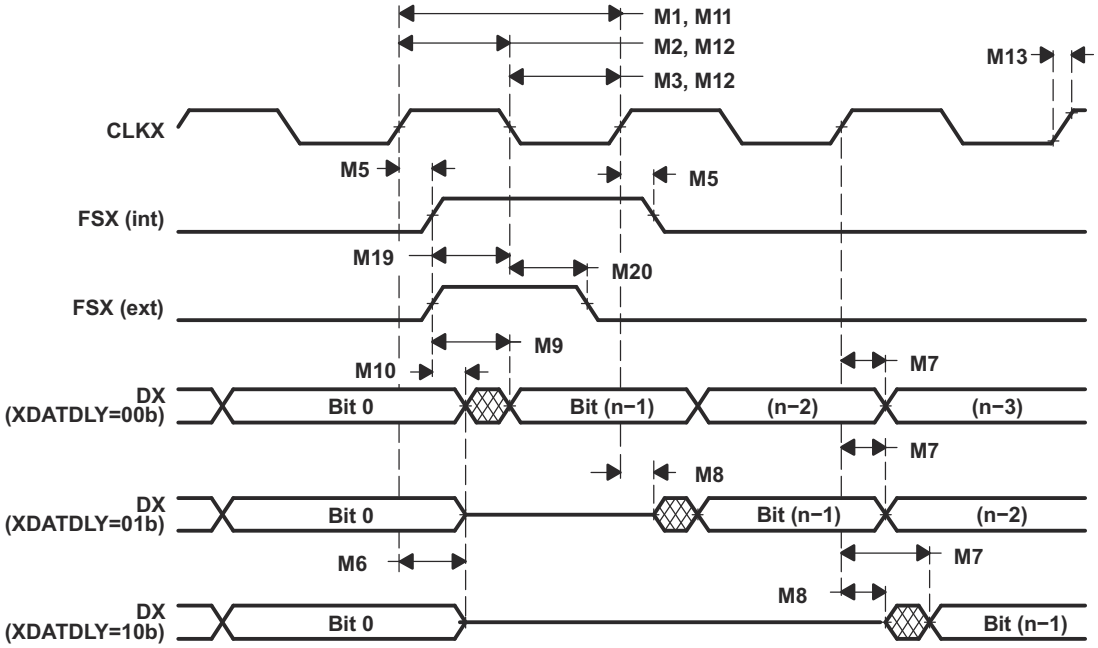


Figure 6-66. McBSP Transmit Timing

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6.12.3.1.2 McBSP as SPI Master or Slave Timing

Section 6.12.3.1.2.1 lists the McBSP as SPI master timing requirements. Section 6.12.3.1.2.2 lists the McBSP as SPI master switching characteristics. Section 6.12.3.1.2.3 lists the McBSP as SPI slave timing requirements. Section 6.12.3.1.2.4 lists the McBSP as SPI slave switching characteristics.

Figure 6-67 through Figure 6-70 show the McBSP as SPI master or slave timing diagrams.

6.12.3.1.2.1 McBSP as SPI Master Timing Requirements

NO.			MIN	MAX	UNIT
CLOCK					
	$t_{c(CLKG)}$	Cycle time, CLKG(1)	2 * $t_{c(LSPCLK)}$		ns
	P	Cycle time, LSPCLK(1)	$t_{c(LSPCLK)}$		ns
M33, M42, M52, M61	$t_{c(CKX)}$	Cycle time, CLKX	2P		ns
CLKSTP = 10b, CLKXP = 0					
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		ns
CLKSTP = 11b, CLKXP = 0					
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		ns
CLKSTP = 10b, CLKXP = 1					
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		ns
CLKSTP = 11b, CLKXP = 1					
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		ns

(1) CLKG should be configured to LSPCLK/2 by setting CLKSM = 1 and CLKGDV = 1

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6.12.3.1.2.2 McBSP as SPI Master Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
CLOCK						
M33	$t_{c(CLKG)}$	Cycle time, CLKG[1] (n * $t_{c(LSPCLK)}$)	40			ns
	P	Half CLKG cycle; 0.5 * $t_{c(CLKG)}$	20			ns
	n	LSPCLK to CLKG divider	2			ns
CLKSTP = 10b, CLKXP = 0						
M24	$t_{h(CKXL-FXL)}$	Hold time, FSX high after CLKX low	2P – 6			ns
M25	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	P – 6			ns
M26	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	–4		6	ns
M28	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P – 8			ns
M29	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	P – 3		P + 6	ns
CLKSTP = 11b, CLKXP = 0						
M34	$t_{h(CKXL-FXH)}$	Hold time, FSX high after CLKX low	P – 6			ns
M35	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	P – 6			ns
M36	$t_{d(CLKXL-DXV)}$	Delay time, CLKX low to DX valid	–4		6	ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P – 6			ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	–2		1	ns
CLKSTP = 10b, CLKXP = 1						
M43	$t_{h(CKXH-FXH)}$	Hold time, FSX high after CLKX high	2P – 6			ns
M44	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	P – 6			ns
M45	$t_{d(CLKXL-DXV)}$	Delay time, CLKX low to DX valid	–4		6	ns
M47	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P – 6			ns
M48	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	–2		1	ns
CLKSTP = 11b, CLKXP = 1						
M53	$t_{h(CKXH-FXH)}$	Hold time, FSX high after CLKX high	P – 6			ns
M54	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	2P – 6			ns
M55	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	–4		6	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	P – 8			ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	–2		1	ns

(1) CLKG should be configured to LSPCLK/2 by setting CLKSM = 1 and CLKGDV = 1.

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6.12.3.1.2.3 McBSP as SPI Slave Timing Requirements

NO.			MIN	MAX	UNIT
CLOCK					
	$t_{c(CLKG)}$	Cycle time, CLKG(1)	2 * $t_{c(LSPCLK)}$		ns
	P	Cycle time, LSPCLK(1)	$t_{c(LSPCLK)}$		ns
M33, M42, M52, M61	$t_{c(CKX)}$	Cycle time, CLKX(2)	16P		ns
CLKSTP = 10b, CLKXP = 0					
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	8P – 10		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	8P – 10		ns
M32	$t_{su(BFXL-CKXH)}$	Setup time, FSX low before CLKX high	8P+10		ns
CLKSTP = 11b, CLKXP = 0					
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	8P – 10		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	8P – 10		ns
M41	$t_{su(FXL-CKXH)}$	Setup time, FSX low before CLKX high	16P+10		ns
CLKSTP = 10b, CLKXP = 1					
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	8P – 10		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	8P – 10		ns
M51	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low	8P+10		ns
CLKSTP = 11b, CLKXP = 1					
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	8P – 10		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	8P – 10		ns
M60	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low	16P+10		ns

(1) CLKG should be configured to LSPCLK/2 by setting CLKSM = 1 and CLKGDV = 1
(2) For SPI slave modes CLKX must be a minimum of 8 CLKG cycles

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6.12.3.1.2.4 McBSP as SPI Slave Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

NO.	PARAMETER		MIN	TYP	MAX	UNIT
CLOCK						
	2P	Cycle time, CLKG				ns
CLKSTP = 10b, CLKXP = 0						
M26	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	3P + 6		5P + 20	ns
M28	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6P + 6			ns
M29	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	4P + 6			ns
CLKSTP = 11b, CLKXP = 0						
M36	$t_{d(CLKXL-DXV)}$	Delay time, CLKX low to DX valid	3P + 6		5P + 20	ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	7P + 6			ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	4P + 6			ns
CLKSTP = 10b, CLKXP = 1						
M45	$t_{d(CLKXL-DXV)}$	Delay time, CLKX low to DX valid	3P + 6		5P + 20	ns
M47	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6P + 6			ns
M48	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	4P + 6			ns
CLKSTP = 11b, CLKXP = 1						
M55	$t_{d(CLKXH-DXV)}$	Delay time, CLKX high to DX valid	3P + 6		5P + 20	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	7P + 6			ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	4P + 6			ns

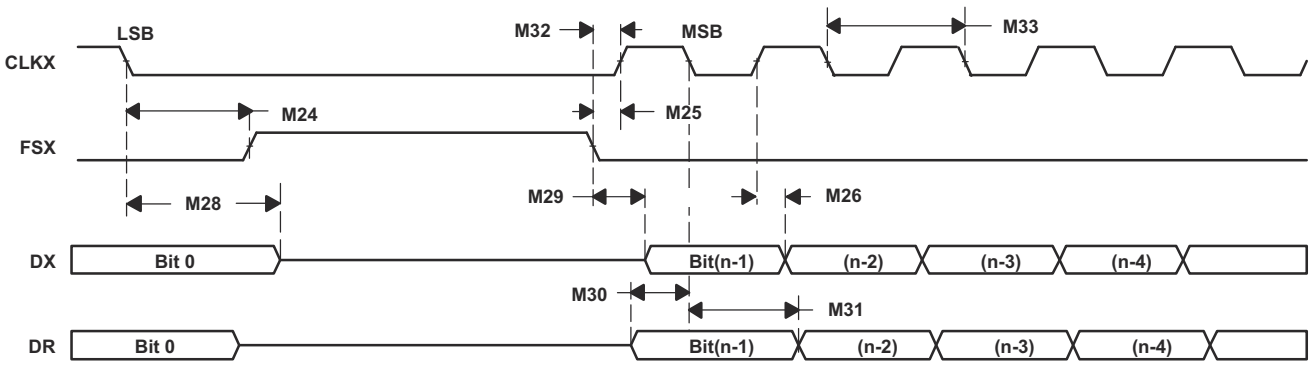


Figure 6-67. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

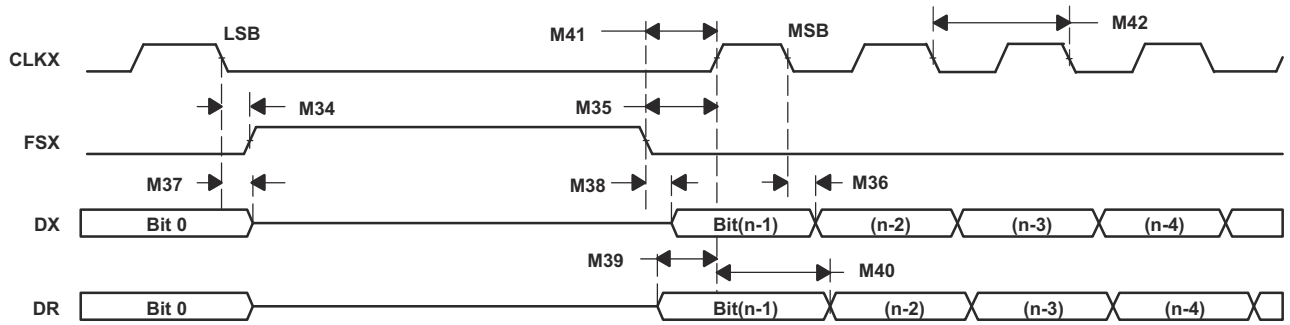


Figure 6-68. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

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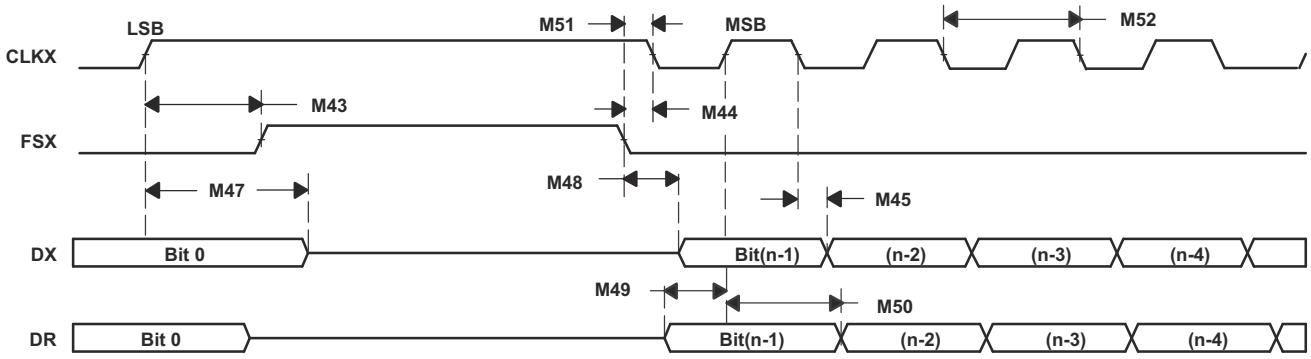


Figure 6-69. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

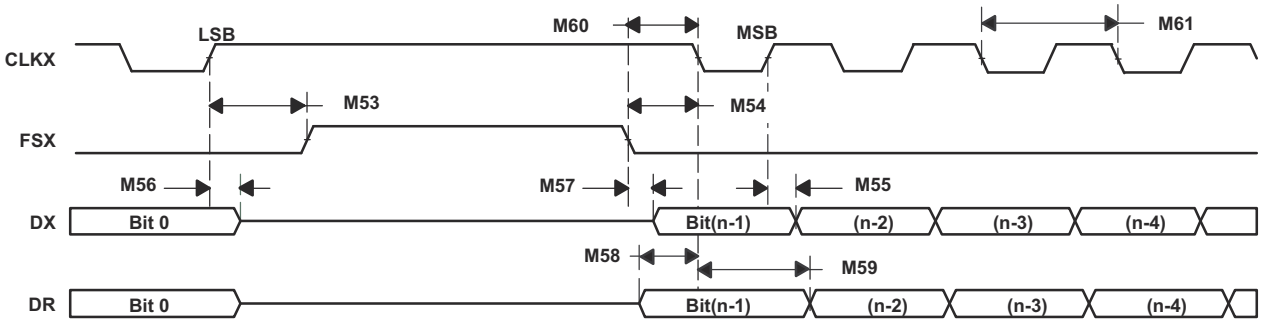


Figure 6-70. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

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6.12.4 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register. Figure 6-71 shows the SCI block diagram.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

Note

NOTE: Both pins can be used as GPIO if not used for SCI.

  - Baud rate programmable to 64K different rates
- Data-word format
  - One start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wakeup multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Note

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

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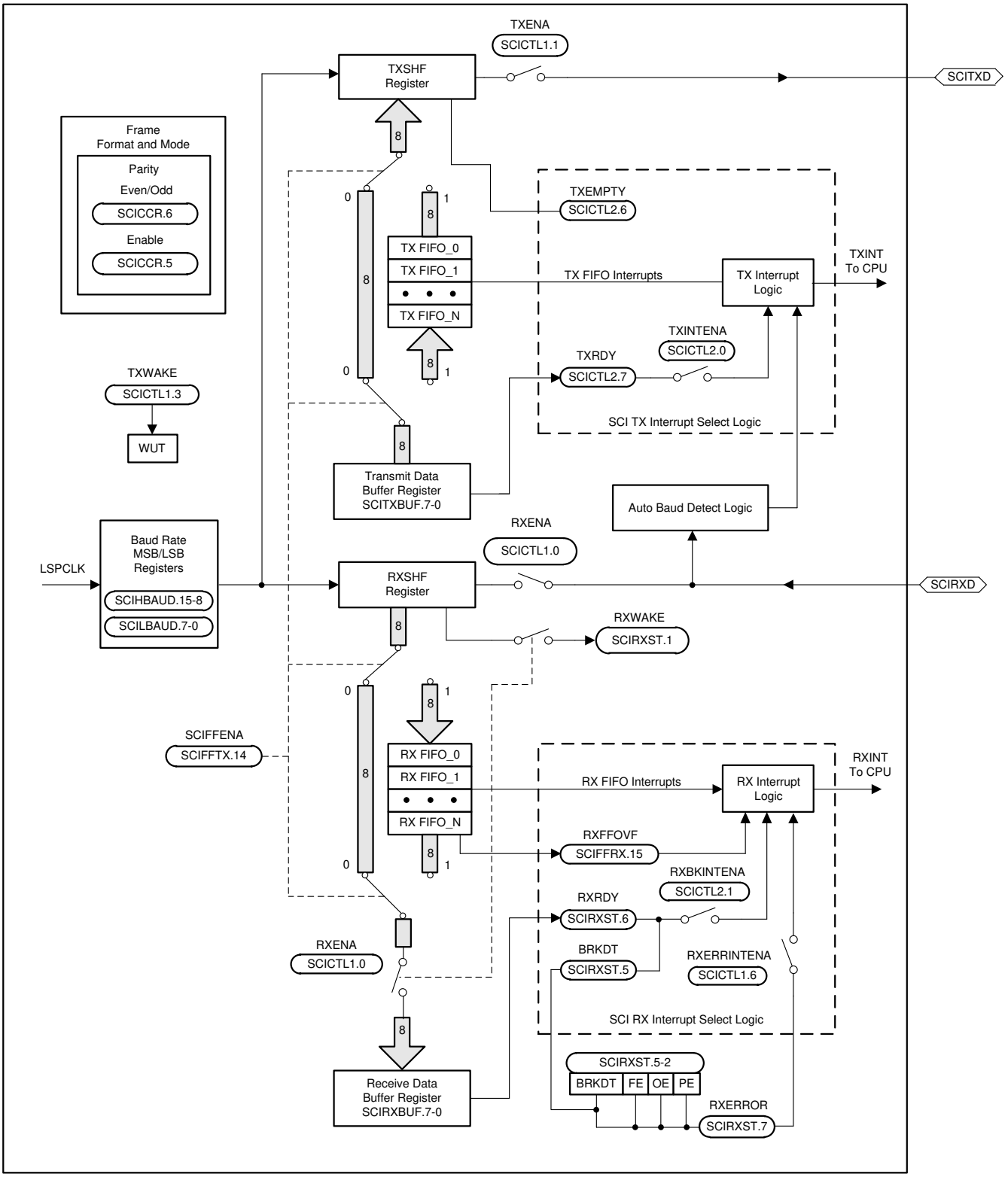


Figure 6-71. SCI Block Diagram

The major elements used in full-duplex operation include:

- A transmitter (TX) and its major registers:
  - SCITXBUF register – Transmitter Data Buffer register. Contains data (loaded by the CPU) to be transmitted
  - TXSHF register – Transmitter Shift register. Accepts data from the SCITXBUF register and shifts data onto the SCITXD pin, 1 bit at a time
- A receiver (RX) and its major registers:
  - RXSHF register – Receiver Shift register. Shifts data in from the SCIRXD pin, 1 bit at a time
  - SCIRXBUF register – Receiver Data Buffer register. Contains data to be read by the CPU. Data from a remote processor is loaded into the RXSHF register and then into the SCIRXBUF and SCIRXEMU registers
- A programmable baud generator
- Data-memory-mapped control and status registers enable the CPU to access the I2C module registers and FIFOs.

The SCI receiver and transmitter operate independently.

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6.12.5 Serial Peripheral Interface (SPI)

The SPI is a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI. The port supports 16-level receive and transmit FIFOs for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive-and-transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- 16-level transmit and receive FIFO
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules
- DMA support
- High-speed mode for up to 30-MHz full-duplex communication

The SPI operates in master or slave mode. The master initiates data transfer by sending the SPICLK signal. For both the slave and the master, data is shifted out of the shift registers on one edge of the SPICLK and latched into the shift register on the opposite SPICLK clock edge. If the CLOCK PHASE bit (SPICTL.3) is high, data is transmitted and received a half-cycle before the SPICLK transition. As a result, both controllers send and receive data simultaneously. The application software determines whether the data is meaningful or dummy data. There are three possible methods for data transmission:

- Master sends data; slave sends dummy data
- Master sends data; slave sends data
- Master sends dummy data; slave sends data

The master can initiate a data transfer at any time because it controls the SPICLK signal. The software, however, determines how the master detects when the slave is ready to broadcast data.

Figure 6-72 shows the SPI CPU Interface.

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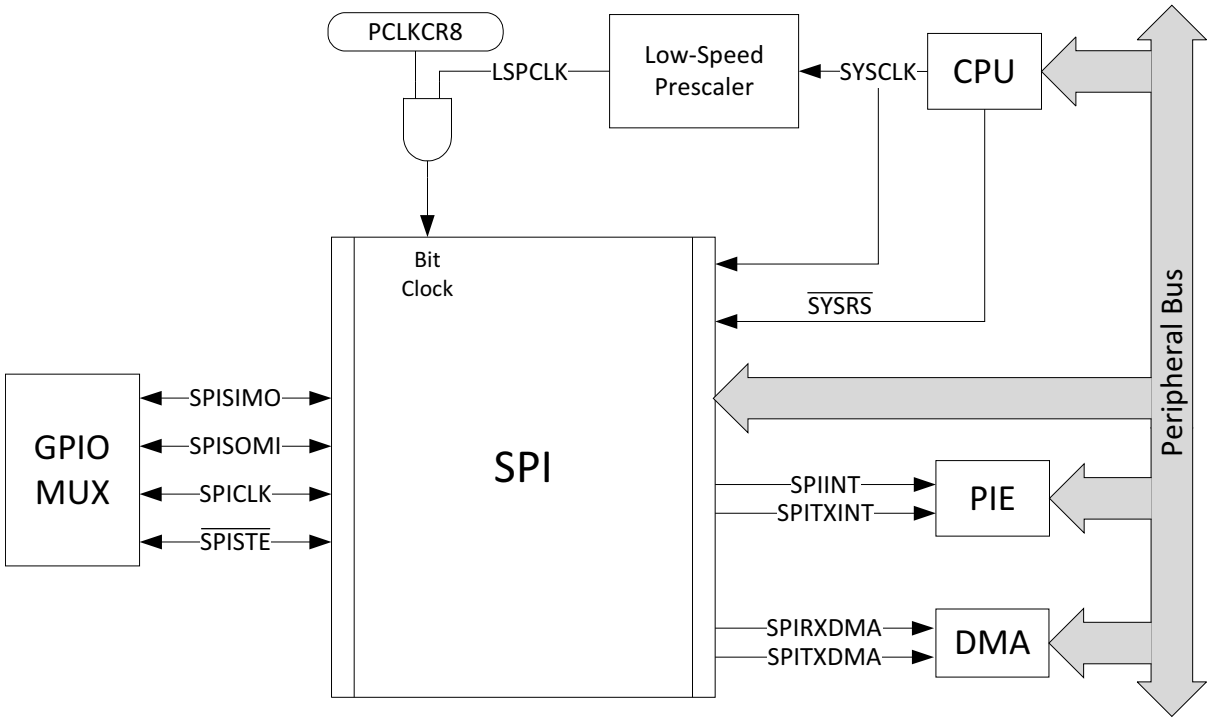


Figure 6-72. SPI CPU Interface

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6.12.5.1 SPI Electrical Data and Timing

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPISIMO, and SPISOMI.

For more information about the SPI in High-Speed mode, see the Serial Peripheral Interface (SPI) chapter of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

To use the SPI in High-Speed mode, the application must use the high-speed enabled GPIOs (see Section 5.4.5).

6.12.5.1.1 SPI Master Mode Timings

Section 6.12.5.1.1.1 lists the SPI master mode timing requirements. Section 6.12.5.1.1.2 lists the SPI master mode switching characteristics (clock phase = 0). Section 6.12.5.1.1.3 lists the SPI master mode switching characteristics (clock phase = 1). Figure 6-73 shows the SPI master mode external timing where the clock phase = 0. Figure 6-74 shows the SPI master mode external timing where the clock phase = 1.

6.12.5.1.1.1 SPI Master Mode Timing Requirements

NO.			(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
High Speed Mode						
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	1		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	5		ns
Normal Mode						
8	$t_{su(SOMI)M}$	Setup time, SPISOMI valid before SPICLK	Even, Odd	20		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	Even, Odd	0		ns

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

6.12.5.1.1.2 SPI Master Mode Switching Characteristics (Clock Phase = 0)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{SPISTE}$ active to SPICLK	Even	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 7$	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 5$	ns
			Odd	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 7$	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 5$	

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6.12.5.1.1.2 SPI Master Mode Switching Characteristics (Clock Phase = 0) (continued)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
24	$t_{v(STE)M}$	Valid time, SPICLK to $\overline{SPISTE}$ inactive	Even	$0.5t_{c(SPC)M} - 7$	$0.5t_{c(SPC)M} + 5$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 7$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 5$	
High Speed Mode						
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		1	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 2$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 2$		
Normal Mode						
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid	Even, Odd		6	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 5$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 5$		

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

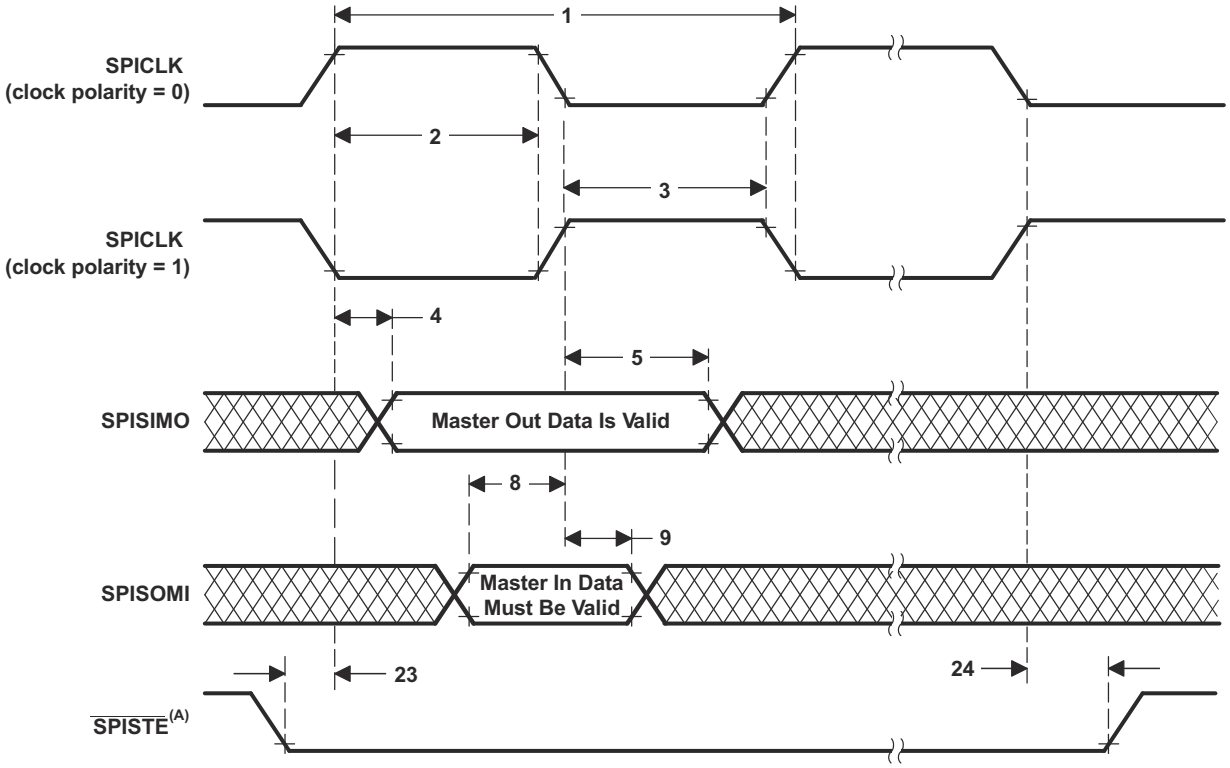
6.12.5.1.1.3 SPI Master Mode Switching Characteristics (Clock Phase = 1)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		(BRR + 1) CONDITION(1)	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{SPISTE}$ valid to SPICLK	Even, Odd	2tc(SPC)M – 3tc(SYSCLK) – 7	2tc(SPC)M – 3tc(SYSCLK) + 5	ns
24	$t_{v(STE)M}$	Valid time, SPICLK to $\overline{SPISTE}$ invalid	Even	– 7	+5	ns
			Odd	– 7	+5	
High Speed Mode						
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 1$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 2$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 2$		
Normal Mode						
4	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 5$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 5$		
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 5$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 5$		

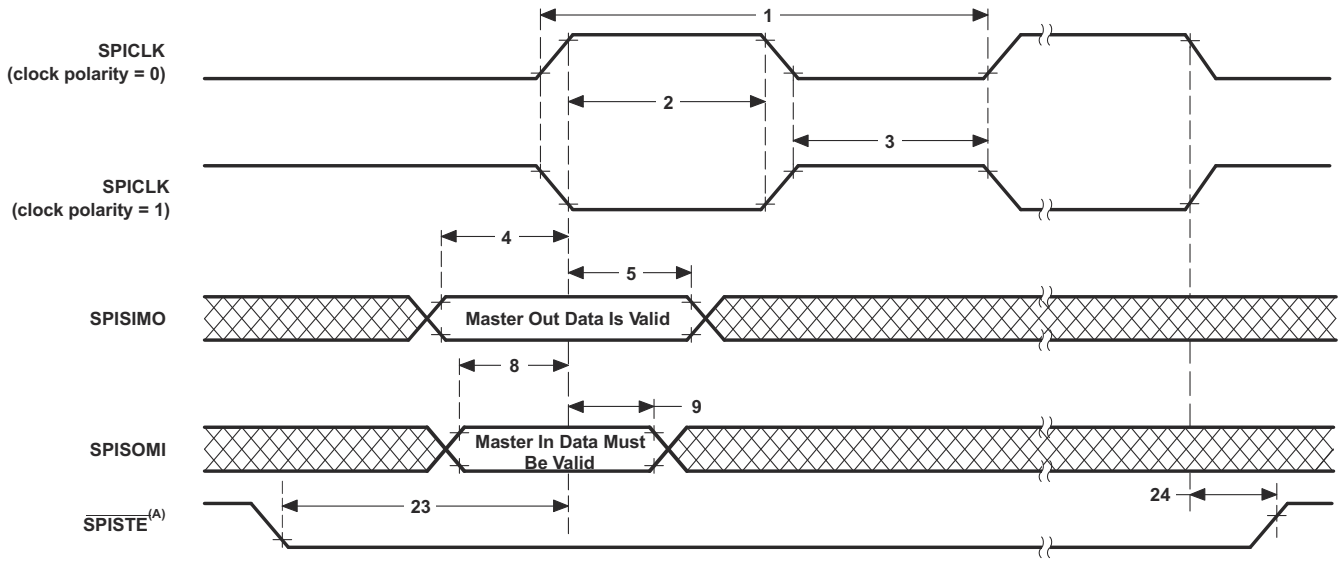
(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-73. SPI Master Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, $\overline{\text{SPISTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-74. SPI Master Mode External Timing (Clock Phase = 1)

6.12.5.1.2 SPI Slave Mode Timings

Section 6.12.5.1.2.1 lists the SPI slave mode timing requirements. Section 6.12.5.1.2.2 lists the SPI slave mode switching characteristics. Figure 6-75 shows the SPI slave mode external timing where the clock phase = 0. Figure 6-76 shows the SPI slave mode external timing where the clock phase = 1.

6.12.5.1.2.1 SPI Slave Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} – 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} – 1$		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 0)	$2t_{c(SYSCLK)} + 4$		ns
		Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 1)	$2t_{c(SYSCLK)} + 14$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK	$1.5t_{c(SYSCLK)}$		ns

6.12.5.1.2.2 SPI Slave Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
High Speed Mode					
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		9	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI valid after SPICLK	0		ns
Normal Mode					
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		20	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI valid after SPICLK	0		ns

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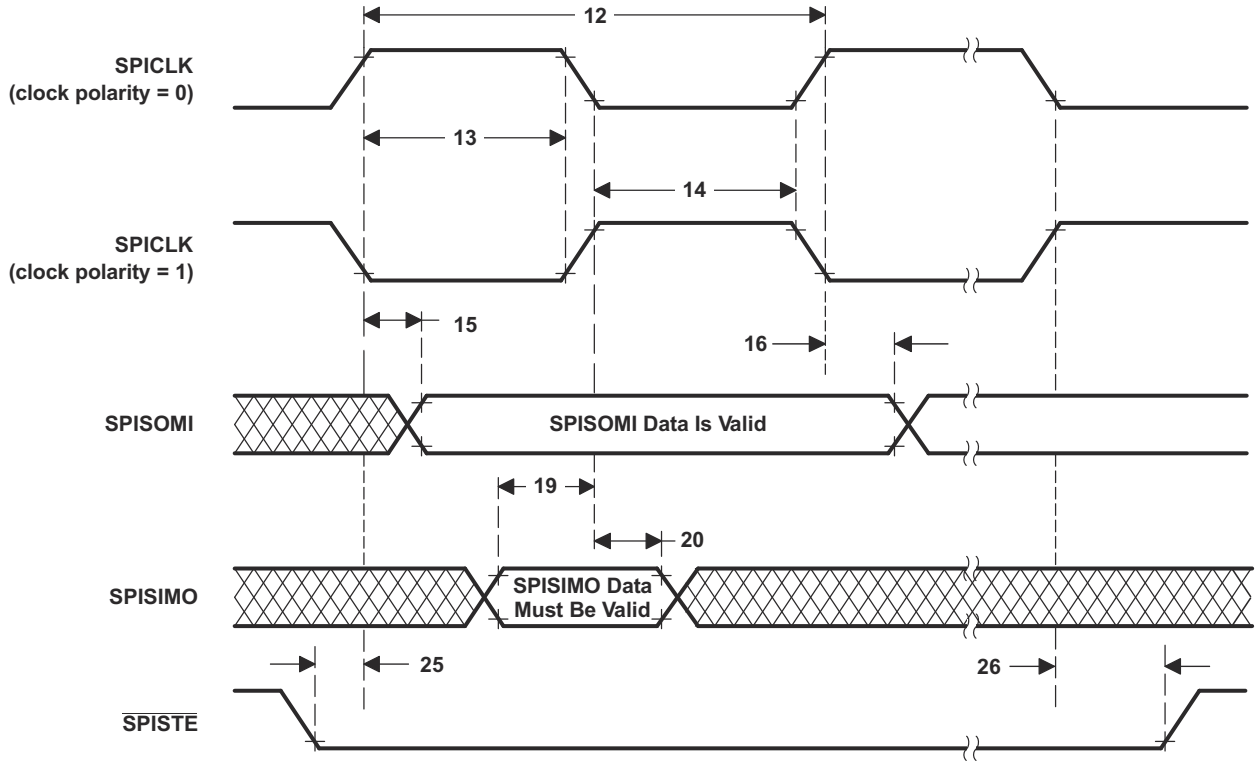


Figure 6-75. SPI Slave Mode External Timing (Clock Phase = 0)

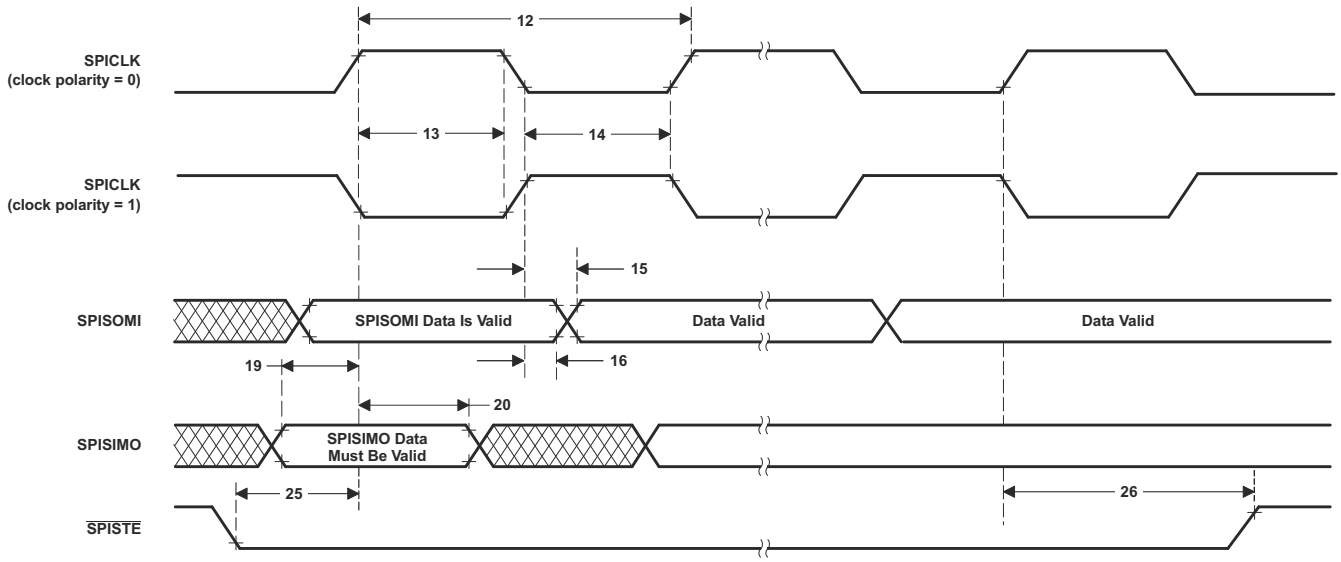


Figure 6-76. SPI Slave Mode External Timing (Clock Phase = 1)

6.12.6 Universal Serial Bus (USB) Controller

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host or device functions.

The USB module has the following features:

- USB 2.0 full-speed and low-speed operation
- Integrated PHY
- Three transfer types: control, interrupt, and bulk
- 32 endpoints
  - One dedicated control IN endpoint and one dedicated control OUT endpoint
  - 15 configurable IN endpoints and 15 configurable OUT endpoints
- 4KB of dedicated endpoint memory

Figure 6-77 shows the USB block diagram.

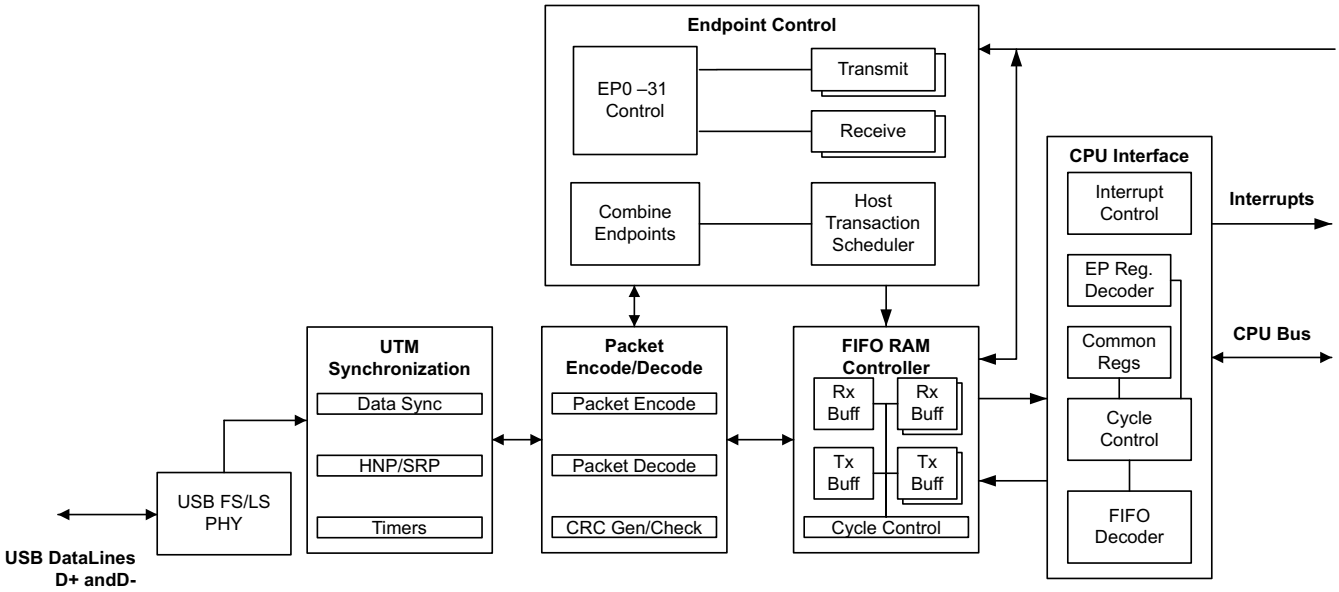


Figure 6-77. USB Block Diagram

Note

The accuracy of the on-chip zero-pin oscillator (Section 6.9.3.5.1, Internal Oscillator Electrical Characteristics) will not meet the accuracy requirements of the USB protocol. An external clock source must be used for applications using USB. For applications using the USB boot mode, see Section 7.9 (Boot ROM and Peripheral Booting) for clock frequency requirements.

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6.12.6.1 USB Electrical Data and Timing

Section 6.12.6.1.1 shows the USB input ports DP and DM timing requirements. Section 6.12.6.1.2 shows the USB output ports DP and DM switching characteristics.

6.12.6.1.1 USB Input Ports DP and DM Timing Requirements

		MIN	MAX	UNIT
V(CM)	Differential input common mode range	0.8	2.5	V
Z(IN)	Input impedance	300		kΩ
VCRS	Crossover voltage	1.3	2.0	V
V_{IL}	Static SE input logic-low level	0.8		V
V_{IH}	Static SE input logic-high level		2.0	V
VDI	Differential input voltage		0.2	V

6.12.6.1.2 USB Output Ports DP and DM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	D+, D– single-ended	USB 2.0 load conditions	2.8	3.6	V
V_{OL}	D+, D– single-ended	USB 2.0 load conditions	0	0.3	V
Z(DRV)	D+, D– impedance		28	44	Ω
t_r	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns
t_f	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns

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7 Detailed Description

7.1 Overview

The TMS320F2807x microcontroller family is suited for advanced closed-loop control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; and sensing and signal processing. Complete development packages for digital power and industrial drives are available as part of the powerSUITE and DesignDRIVE initiatives.

The F2807x is a 32-bit floating-point microcontroller based on TI's industry-leading C28x core. This core is boosted by the trigonometric hardware accelerator which improves performance of trigonometric-based algorithms with CPU instructions such as sine, cosine, and arctangent functions, which are common in torque-loop and position calculations.

The F2807x microcontroller family features a CLA real-time control coprocessor. The CLA is an independent 32-bit floating-point processor that runs at the same speed as the main CPU. The CLA responds to peripheral triggers and executes code concurrently with the main C28x CPU. This parallel processing capability can effectively double the computational performance of a real-time control system. By using the CLA to service time-critical functions, the main C28x CPU is free to perform other tasks, such as communications and diagnostics.

The F2807x device supports up to 512KB (256KW) of ECC-protected onboard flash memory and up to 100KB (50KW) of SRAM with parity. Two independent security zones are also available for 128-bit code protection of the main C28x.

The analog subsystem boasts up to three 12-bit ADCs, which enable simultaneous management of three independent power phases, and up to eight windowed comparator subsystems (CMPSSs), allowing very fast, direct trip of the PWMs in overvoltage or overcurrent conditions. In addition, the device has three 12-bit DACs, and precision control peripherals such as enhanced pulse width modulators (ePWMs) with fault protection, eQEP peripherals, and eCAP units.

Connectivity peripherals such as dual Controller Area Network (CAN) modules (ISO 11898-1/CAN 2.0B-compliant) and a USB 2.0 port with MAC and full-speed PHY let users add universal serial bus (USB) connectivity to their application.

Want to learn more about features that make C2000 Real-Time MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000™ real-time control MCUs page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the TMDSCNCD28379D or LAUNCHXL-F28379D evaluation boards and download C2000Ware.

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7.2 Functional Block Diagram

Figure 7-1 shows the CPU system and associated peripherals.

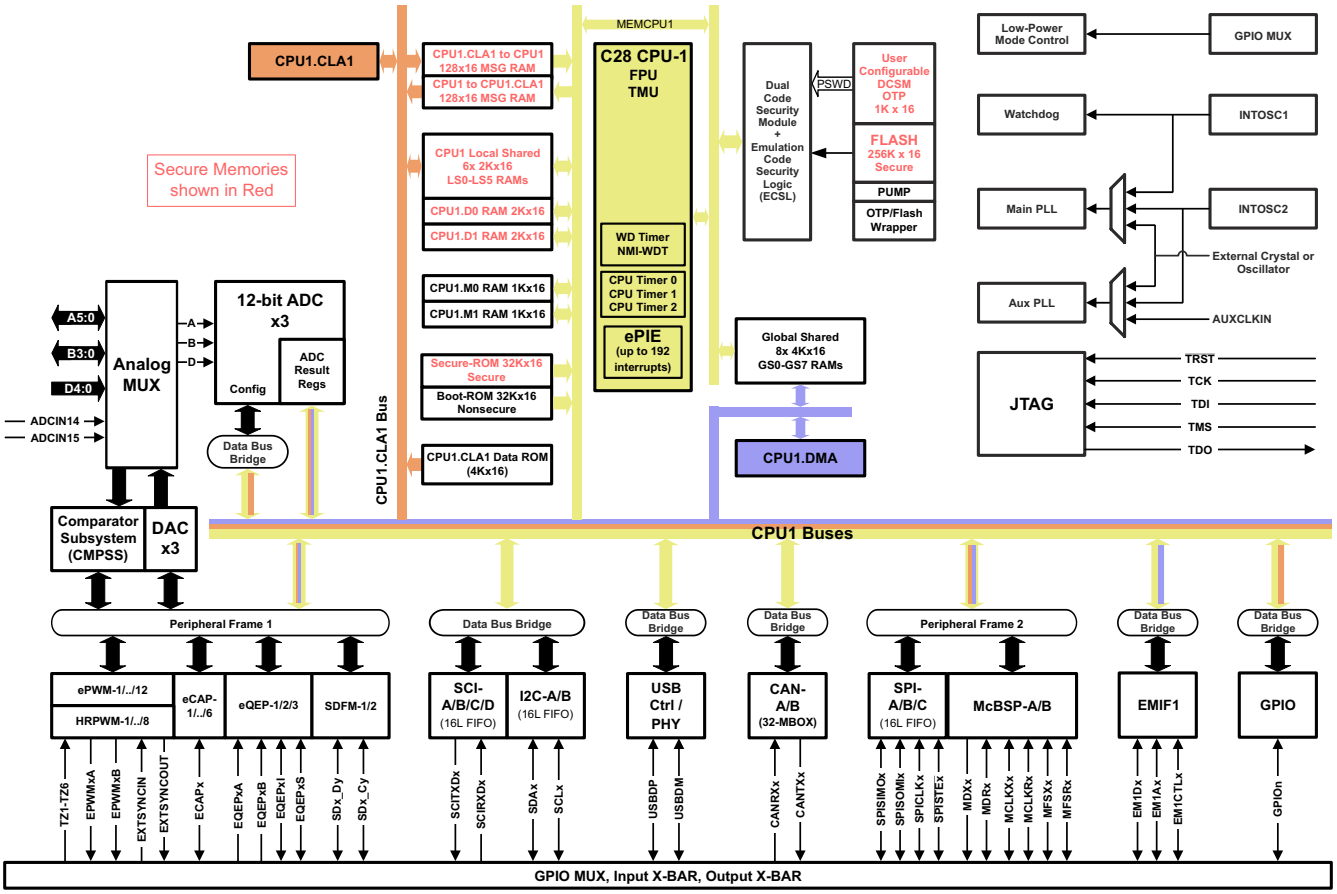


Figure 7-1. Functional Block Diagram

7.3 Memory

7.3.1 C28x Memory Map

The C28x memory map is described in Table 7-1. Memories accessible by the CLA or DMA (direct memory access) are noted as well.

Table 7-1. C28x Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
M0 RAM	1K × 16	0x0000 0000	0x0000 03FF		
M1 RAM	1K × 16	0x0000 0400	0x0000 07FF		
PieVectTable	512 × 16	0x0000 0D00	0x0000 0EFF		
CLA to CPU MSGRAM	128 × 16	0x0000 1480	0x0000 14FF	Yes	
CPU to CLA MSGRAM	128 × 16	0x0000 1500	0x0000 157F	Yes	
LS0 RAM	2K × 16	0x0000 8000	0x0000 87FF	Yes	
LS1 RAM	2K × 16	0x0000 8800	0x0000 8FFF	Yes	
LS2 RAM	2K × 16	0x0000 9000	0x0000 97FF	Yes	
LS3 RAM	2K × 16	0x0000 9800	0x0000 9FFF	Yes	
LS4 RAM	2K × 16	0x0000 A000	0x0000 A7FF	Yes	
LS5 RAM	2K × 16	0x0000 A800	0x0000 AFFF	Yes	
D0 RAM	2K × 16	0x0000 B000	0x0000 B7FF		
D1 RAM	2K × 16	0x0000 B800	0x0000 BFFF		
GS0 RAM	4K × 16	0x0000 C000	0x0000 CFFF		Yes
GS1 RAM	4K × 16	0x0000 D000	0x0000 DFFF		Yes
GS2 RAM	4K × 16	0x0000 E000	0x0000 EFFF		Yes
GS3 RAM	4K × 16	0x0000 F000	0x0000 FFFF		Yes
GS4 RAM	4K × 16	0x0001 0000	0x0001 0FFF		Yes
GS5 RAM	4K × 16	0x0001 1000	0x0001 1FFF		Yes
GS6 RAM	4K × 16	0x0001 2000	0x0001 2FFF		Yes
GS7 RAM	4K × 16	0x0001 3000	0x0001 3FFF		Yes
CAN A Message RAM	2K × 16	0x0004 9000	0x0004 97FF		
CAN B Message RAM	2K × 16	0x0004 B000	0x0004 B7FF		
Flash Bank 0	256K × 16	0x0008 0000	0x000B FFFF		
Secure ROM	32K × 16	0x003F 0000	0x003F 7FFF		
Boot ROM	32K × 16	0x003F 8000	0x003F FFBF		
Vectors	64 × 16	0x003F FFC0	0x003F FFFF		

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7.3.2 Flash Memory Map

The F28076 and F28075 devices have one flash bank of 512KB (256KW). See Section 6.9.4 for details on flash wait-states. The following table shows the addresses of flash sectors on F28076 and F28075.

Table 7-2. Addresses of Flash Sectors on F28076 and F28075

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP Bank 0	1K x 16	0x0007 0000	0x0007 03FF
User configurable DCSM OTP Bank 0	1K x 16	0x0007 8000	0x0007 83FF
Sectors			
Sector 0	8K x 16	0x0008 0000	0x0008 1FFF
Sector 1	8K x 16	0x0008 2000	0x0008 3FFF
Sector 2	8K x 16	0x0008 4000	0x0008 5FFF
Sector 3	8K x 16	0x0008 6000	0x0008 7FFF
Sector 4	32K x 16	0x0008 8000	0x0008 FFFF
Sector 5	32K x 16	0x0009 0000	0x0009 7FFF
Sector 6	32K x 16	0x0009 8000	0x0009 FFFF
Sector 7	32K x 16	0x000A 0000	0x000A 7FFF
Sector 8	32K x 16	0x000A 8000	0x000A FFFF
Sector 9	32K x 16	0x000B 0000	0x000B 7FFF
Sector 10	8K x 16	0x000B 8000	0x000B 9FFF
Sector 11	8K x 16	0x000B A000	0x000B BFFF
Sector 12	8K x 16	0x000B C000	0x000B DFFF
Sector 13	8K x 16	0x000B E000	0x000B FFFF
Flash ECC Locations			
TI OTP ECC Bank 0	128 x 16	0x0107 0000	0x0107 007F
User-configurable DCSM OTP ECC Bank 0	128 x 16	0x0107 1000	0x0107 107F
Flash ECC (Sector 0)	1K x 16	0x0108 0000	0x0108 03FF
Flash ECC (Sector 1)	1K x 16	0x0108 0400	0x0108 07FF
Flash ECC (Sector 2)	1K x 16	0x0108 0800	0x0108 0BFF
Flash ECC (Sector 3)	1K x 16	0x0108 0C00	0x0108 0FFF
Flash ECC (Sector 4)	4K x 16	0x0108 1000	0x0108 1FFF
Flash ECC (Sector 5)	4K x 16	0x0108 2000	0x0108 2FFF
Flash ECC (Sector 6)	4K x 16	0x0108 3000	0x0108 3FFF
Flash ECC (Sector 7)	4K x 16	0x0108 4000	0x0108 4FFF
Flash ECC (Sector 8)	4K x 16	0x0108 5000	0x0108 5FFF
Flash ECC (Sector 9)	4K x 16	0x0108 6000	0x0108 6FFF
Flash ECC (Sector 10)	1K x 16	0x0108 7000	0x0108 73FF
Flash ECC (Sector 11)	1K x 16	0x0108 7400	0x0108 77FF
Flash ECC (Sector 12)	1K x 16	0x0108 7800	0x0108 7BFF

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Table 7-2. Addresses of Flash Sectors on F28076 and F28075 (continued)

SECTOR	SIZE	START ADDRESS	END ADDRESS
Flash ECC (Sector 13)	1K x 16	0x0108 7C00	0x0108 7FFF

7.3.3 EMIF Chip Select Memory Map

The EMIF memory map is shown in Table 7-3.

Table 7-3. EMIF Chip Select Memory Map

EMIF CHIP SELECT	SIZE(1)	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
EMIF1_CS0n - Data	256M × 16	0x8000 0000	0x8FFF FFFF		Yes
EMIF1_CS2n - Program + Data(2)	2M × 16	0x0010 0000	0x002F FFFF		Yes
EMIF1_CS3n - Program + Data	512K × 16	0x0030 0000	0x0037 FFFF		Yes
EMIF1_CS4n - Program + Data	393K × 16	0x0038 0000	0x003D FFFF		Yes

(1) Available memory size listed in this table is the maximum possible size assuming 32-bit memory. This may not apply to other memory sizes because of pin mux setting. See Section 5.4.1 to find the available address lines for your use case.
(2) The 2M × 16 size is for a 32-bit interface with the assumption that 16-bit accesses are not performed; hence, byte enables are not used (tied to active value on board). If byte enables are used, then the maximum size is smaller because byte enables are muxed with address pins (see Section 5.4.1) . If 16-bit memory is used, then the maximum size is 1M × 16.

7.3.4 Peripheral Registers Memory Map

The peripheral registers memory map can be found in Table 7-4. Registers in the peripheral frames share a secondary master (CLA or DMA) selection with all other registers within the same peripheral frame. See the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual* for details on the CPU subsystem and secondary master selection.

Note

None of the device peripherals have program bus access.

Table 7-4. Peripheral Registers Memory Map

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	PROTECTED(1)	CLA ACCESS	DMA ACCESS
AdcaResultRegs	ADC_RESULT_REGS	0x0000 0B00	0x0000 0B1F		Yes	Yes
AdcbResultRegs	ADC_RESULT_REGS	0x0000 0B20	0x0000 0B3F		Yes	Yes
AdcdResultRegs	ADC_RESULT_REGS	0x0000 0B60	0x0000 0B7F		Yes	Yes
CpuTimer0Regs	CPUTIMER_REGS	0x0000 0C00	0x0000 0C07			
CpuTimer1Regs	CPUTIMER_REGS	0x0000 0C08	0x0000 0C0F			
CpuTimer2Regs	CPUTIMER_REGS	0x0000 0C10	0x0000 0C17			
PieCtrlRegs (2)	PIE_CTRL_REGS	0x0000 0CE0	0x0000 0CFF			
Cla1SoftIntRegs(2)	CLA_SOFTINT_REGS	0x0000 0CE0	0x0000 0CFF		Yes – CLA only, no CPU access	
DmaRegs	DMA_REGS	0x0000 1000	0x0000 11FF			
Cla1Regs	CLA_REGS	0x0000 1400	0x0000 147F			
Clb1LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	0x0000 3000	0x0000 30FF	Yes	Yes	
Clb1LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	0x0000 3100	0x0000 31FF	Yes	Yes	
Clb1DataExchRegs	CLB_DATA_EXCHANGE_REGS	0x0000 3200	0x0000 33FF	Yes	Yes	
Clb2LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	0x0000 3400	0x0000 34FF	Yes	Yes	
Clb2LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	0x0000 3500	0x0000 35FF	Yes	Yes	
Clb2DataExchRegs	CLB_DATA_EXCHANGE_REGS	0x0000 3600	0x0000 37FF	Yes	Yes	
Clb3LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	0x0000 3800	0x0000 38FF	Yes	Yes	
Clb3LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	0x0000 3900	0x0000 39FF	Yes	Yes	
Clb3DataExchRegs	CLB_DATA_EXCHANGE_REGS	0x0000 3A00	0x0000 3BFF	Yes	Yes	

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Table 7-4. Peripheral Registers Memory Map (continued)

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	PROTECTED[1]	CLA ACCESS	DMA ACCESS
Clb4LogicCfgRegs	CLB_LOGIC_CONFIG_REGS	0x0000 3C00	0x0000 3CFF	Yes	Yes	
Clb4LogicCtrlRegs	CLB_LOGIC_CONTROL_REGS	0x0000 3D00	0x0000 3DFF	Yes	Yes	
Clb4DataExchRegs	CLB_DATA_EXCHANGE_REGS	0x0000 3E00	0x0000 3FFF	Yes	Yes	
Peripheral Frame 1						
EPwm1Regs	EPWM_REGS	0x0000 4000	0x0000 40FF	Yes	Yes	Yes
EPwm2Regs	EPWM_REGS	0x0000 4100	0x0000 41FF	Yes	Yes	Yes
EPwm3Regs	EPWM_REGS	0x0000 4200	0x0000 42FF	Yes	Yes	Yes
EPwm4Regs	EPWM_REGS	0x0000 4300	0x0000 43FF	Yes	Yes	Yes
EPwm5Regs	EPWM_REGS	0x0000 4400	0x0000 44FF	Yes	Yes	Yes
EPwm6Regs	EPWM_REGS	0x0000 4500	0x0000 45FF	Yes	Yes	Yes
EPwm7Regs	EPWM_REGS	0x0000 4600	0x0000 46FF	Yes	Yes	Yes
EPwm8Regs	EPWM_REGS	0x0000 4700	0x0000 47FF	Yes	Yes	Yes
EPwm9Regs	EPWM_REGS	0x0000 4800	0x0000 48FF	Yes	Yes	Yes
EPwm10Regs	EPWM_REGS	0x0000 4900	0x0000 49FF	Yes	Yes	Yes
EPwm11Regs	EPWM_REGS	0x0000 4A00	0x0000 4AFF	Yes	Yes	Yes
EPwm12Regs	EPWM_REGS	0x0000 4B00	0x0000 4BFF	Yes	Yes	Yes
ECap1Regs	ECAP_REGS	0x0000 5000	0x0000 501F	Yes	Yes	Yes
ECap2Regs	ECAP_REGS	0x0000 5020	0x0000 503F	Yes	Yes	Yes
ECap3Regs	ECAP_REGS	0x0000 5040	0x0000 505F	Yes	Yes	Yes
ECap4Regs	ECAP_REGS	0x0000 5060	0x0000 507F	Yes	Yes	Yes
ECap5Regs	ECAP_REGS	0x0000 5080	0x0000 509F	Yes	Yes	Yes
ECap6Regs	ECAP_REGS	0x0000 50A0	0x0000 50BF	Yes	Yes	Yes
EQep1Regs	EQEP_REGS	0x0000 5100	0x0000 513F	Yes	Yes	Yes
EQep2Regs	EQEP_REGS	0x0000 5140	0x0000 517F	Yes	Yes	Yes
EQep3Regs	EQEP_REGS	0x0000 5180	0x0000 51BF	Yes	Yes	Yes
DacaRegs	DAC_REGS	0x0000 5C00	0x0000 5C0F	Yes	Yes	Yes
DacbRegs	DAC_REGS	0x0000 5C10	0x0000 5C1F	Yes	Yes	Yes
DaccRegs	DAC_REGS	0x0000 5C20	0x0000 5C2F	Yes	Yes	Yes
Cmpss1Regs	CMPSS_REGS	0x0000 5C80	0x0000 5C9F	Yes	Yes	Yes
Cmpss2Regs	CMPSS_REGS	0x0000 5CA0	0x0000 5CBF	Yes	Yes	Yes
Cmpss3Regs	CMPSS_REGS	0x0000 5CC0	0x0000 5CDF	Yes	Yes	Yes
Cmpss4Regs	CMPSS_REGS	0x0000 5CE0	0x0000 5CFF	Yes	Yes	Yes
Cmpss5Regs	CMPSS_REGS	0x0000 5D00	0x0000 5D1F	Yes	Yes	Yes
Cmpss6Regs	CMPSS_REGS	0x0000 5D20	0x0000 5D3F	Yes	Yes	Yes
Cmpss7Regs	CMPSS_REGS	0x0000 5D40	0x0000 5D5F	Yes	Yes	Yes
Cmpss8Regs	CMPSS_REGS	0x0000 5D60	0x0000 5D7F	Yes	Yes	Yes
Sdfm1Regs	SDFM_REGS	0x0000 5E00	0x0000 5E7F	Yes	Yes	Yes
Sdfm2Regs	SDFM_REGS	0x0000 5E80	0x0000 5EFF	Yes	Yes	Yes
Peripheral Frame 2						
McbspaRegs	MCBSP_REGS	0x0000 6000	0x0000 603F	Yes	Yes	Yes
McbspbRegs	MCBSP_REGS	0x0000 6040	0x0000 607F	Yes	Yes	Yes
SpiaRegs	SPI_REGS	0x0000 6100	0x0000 610F	Yes	Yes	Yes
SpibRegs	SPI_REGS	0x0000 6110	0x0000 611F	Yes	Yes	Yes
SpicRegs	SPI_REGS	0x0000 6120	0x0000 612F	Yes	Yes	Yes
WdRegs	WD_REGS	0x0000 7000	0x0000 703F	Yes		
NmiIntruptRegs	NMI_INTRUPT_REGS	0x0000 7060	0x0000 706F	Yes		
XintRegs	XINT_REGS	0x0000 7070	0x0000 707F	Yes		
SciaRegs	SCI_REGS	0x0000 7200	0x0000 720F	Yes		

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Table 7-4. Peripheral Registers Memory Map (continued)

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	PROTECTED(1)	CLA ACCESS	DMA ACCESS
ScibRegs	SCI_REGS	0x0000 7210	0x0000 721F	Yes		
ScicRegs	SCI_REGS	0x0000 7220	0x0000 722F	Yes		
ScidRegs	SCI_REGS	0x0000 7230	0x0000 723F	Yes		
I2caRegs	I2C_REGS	0x0000 7300	0x0000 733F	Yes		
I2cbRegs	I2C_REGS	0x0000 7340	0x0000 737F	Yes		
AdcaRegs	ADC_REGS	0x0000 7400	0x0000 747F	Yes	Yes	
AdcbRegs	ADC_REGS	0x0000 7480	0x0000 74FF	Yes	Yes	
AdcdRegs	ADC_REGS	0x0000 7580	0x0000 75FF	Yes	Yes	
InputXbarRegs	INPUT_XBAR_REGS	0x0000 7900	0x0000 791F	Yes		
XbarRegs	XBAR_REGS	0x0000 7920	0x0000 793F	Yes		
TrigRegs	TRIG_REGS	0x0000 7940	0x0000 794F	Yes		
DmaClaSrcSelRegs	DMA_CLA_SRC_SEL_REGS	0x0000 7980	0x0000 798F	Yes		
EPwmXbarRegs	EPWM_XBAR_REGS	0x0000 7A00	0x0000 7A3F	Yes		
OutputXbarRegs	OUTPUT_XBAR_REGS	0x0000 7A80	0x0000 7ABF	Yes		
GpioCtrlRegs	GPIO_CTRL_REGS	0x0000 7C00	0x0000 7D7F	Yes		
GpioDataRegs	GPIO_DATA_REGS	0x0000 7F00	0x0000 7F2F	Yes	Yes	
UsbaRegs	USB_REGS	0x0004 0000	0x0004 0FFF	Yes		
Emif1Regs	EMIF_REGS	0x0004 7000	0x0004 77FF	Yes		
CanaRegs	CAN_REGS	0x0004 8000	0x0004 87FF	Yes		
CanbRegs	CAN_REGS	0x0004 A000	0x0004 A7FF	Yes		
FlashPumpSemaphoreRegs	FLASH_PUMP_SEMAPHORE_REGS	0x0005 0024	0x0005 0025	Yes		
DevCfgRegs	DEV_CFG_REGS	0x0005 D000	0x0005 D17F	Yes		
AnalogSubsysRegs	ANALOG_SUBSYS_REGS	0x0005 D180	0x0005 D1FF	Yes		
ClkCfgRegs	CLK_CFG_REGS	0x0005 D200	0x0005 D2FF	Yes		
CpuSysRegs	CPU_SYS_REGS	0x0005 D300	0x0005 D3FF	Yes		
RomPrefetchRegs	ROM_PREFETCH_REGS	0x0005 E608	0x0005 E60B	Yes		
DcsmZ1Regs	DCSM_Z1_REGS	0x0005 F000	0x0005 F02F	Yes		
DcsmZ2Regs	DCSM_Z2_REGS	0x0005 F040	0x0005 F05F	Yes		
DcsmCommonRegs	DCSM_COMMON_REGS	0x0005 F070	0x0005 F07F	Yes		
MemCfgRegs	MEM_CFG_REGS	0x0005 F400	0x0005 F47F	Yes		
Emif1ConfigRegs	EMIF1_CONFIG_REGS	0x0005 F480	0x0005 F49F	Yes		
AccessProtectionRegs	ACCESS_PROTECTION_REGS	0x0005 F4C0	0x0005 F4FF	Yes		
MemoryErrorRegs	MEMORY_ERROR_REGS	0x0005 F500	0x0005 F53F	Yes		
RomWaitStateRegs	ROM_WAIT_STATE_REGS	0x0005 F540	0x0005 F541	Yes		
Flash0CtrlRegs	FLASH_CTRL_REGS	0x0005 F800	0x0005 FAFF	Yes		
Flash0EccRegs	FLASH_ECC_REGS	0x0005 FB00	0x0005 FB3F	Yes		

(1) The CPU (not applicable for CLA or DMA) contains a write followed by read protection mode to ensure that any read operation that follows a write operation within a protected address range is executed as written by delaying the read operation until the write is initiated.

(2) The address overlap of PieCtrlRegs and Cla1SoftIntRegs is correct. Each CPU, C28x and CLA, only has access to one of the register sets.

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7.3.5 Memory Types

Table 7-5 provides more information about each memory type.

Table 7-5. Memory Types

MEMORY TYPE	ECC-CAPABLE	PARITY	SECURITY	HIBERNATE RETENTION	ACCESS PROTECTION
M0, M1	Yes	–	–	Yes	–
D0, D1	Yes	–	Yes	–	Yes
LSx	–	Yes	Yes	–	Yes
GSx	–	Yes	–	–	Yes
CPU/CLA MSGRAM	–	Yes	Yes	–	Yes
Boot ROM	–	–	–	N/A	–
Secure ROM	–	–	Yes	N/A	–
Flash	Yes	–	Yes	N/A	N/A
User-configurable DCSM OTP	Yes	–	Yes	N/A	N/A

7.3.5.1 Dedicated RAM (Mx and Dx RAM)

The CPU subsystem has four dedicated ECC-capable RAM blocks: M0, M1, D0, and D1. M0/M1 memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them). D0/D1 memories are secure blocks and also have the access-protection feature (CPU write/CPU fetch protection).

7.3.5.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have parity. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default, these memories are dedicated to the CPU only, and the user could choose to share these memories with the CLA by configuring the MSEL_LSx bit field in the LSxMSEL registers appropriately.

Table 7-6 shows the master access for the LSx RAM.

Table 7-6. Master Access for LSx RAM
(With Assumption That all Other Access Protections are Disabled)

MSEL_LSx	CLAPGM_LSx	CPU ALLOWED ACCESS	CLA ALLOWED ACCESS	COMMENT
00	X	All	–	LSx memory is configured as CPU dedicated RAM.
01	0	All	Data Read Data Write	LSx memory is shared between CPU and CLA1.
01	1	Emulation Read Emulation Write	Fetch Only	LSx memory is CLA1 program memory.

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7.3.5.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Both the CPU and DMA have full read and write access to these memories.

All GSx RAM blocks have parity.

The GSx RAMs have access protection (CPU write/CPU fetch/DMA write).

7.3.5.4 CLA Message RAM (CLA MSGRAM)

These RAM blocks can be used to share data between the CPU and CLA. The CLA has read and write access to the "CLA to CPU MSGRAM." The CPU has read and write access to the "CPU to CLA MSGRAM." The CPU and CLA both have read access to both MSGRAMs.

This RAM has parity.

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7.4 Identification

Table 7-7 shows the Device Identification Registers.

Table 7-7. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION	
PARTIDH	0x0005 D00A	2	Device part identification number(1)	
			TMS320F28076	0x**FC 0500
			TMS320F28075	0x**FF 0500
REVID	0x0005 D00C	2	Silicon revision number	
			Revision B	0x0000 0002
			Revision C	0x0000 0003
UID_UNIQUE	0x0007 03CC	2	Unique identification number. This number is different on each individual device with the same PARTIDH. This can be used as a serial number in the application. This number is present only on TMS Revision C devices.	
JTAG ID	N/A	N/A	JTAG Device ID	0x0B99 C02F

(1) PARTIDH may have one of two values for each part number, with the eight most significant bits identified with '**' above being 0x00 or 0x02.

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7.5 Bus Architecture – Peripheral Connectivity

Table 7-8 shows a broad view of the peripheral and configuration register accessibility from each bus master. Peripherals within peripheral frames 1 or 2 will all be mapped to the respective secondary master as a group (if SPI is assigned to CPU1.DMA, then McBSP is also assigned to CPU1.DMA).

Table 7-8. Bus Master Peripheral Access

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1
Peripheral Frame 1: • ePWM/HRPWM • SDFM • eCAP(1) • eQEP(1) • CMPSS(1) • DAC(1)	Y	Y	Y
Peripheral Frame 2: • SPI • McBSP	Y	Y	Y
SCI			Y
I2C			Y
CAN			Y
ADC Configuration		Y	Y
EMIF1	Y		Y
USB			Y
Device Capability, Peripheral Reset, Peripheral CPU Select			Y
GPIO Pin Mapping and Configuration			Y
Analog System Control			Y
Reset Configuration			Y
Clock and PLL Configuration			Y
System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating)			Y
Flash Configuration			Y
CPU Timers			Y
DMA and CLA Trigger Source Select			Y
GPIO Data(2)		Y	Y
ADC Results	Y	Y	Y

(1) These modules are on a Peripheral Frame with DMA access; however, they cannot trigger a DMA transfer.
(2) The GPIO Data Registers are unique for each CPU1 and CPU1.CLAx. When the GPIO Pin Mapping Register is configured to assign a GPIO to a particular master, the respective GPIO Data Register will control the GPIO. See the General-Purpose Input/Output (GPIO) chapter of the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual* for more details.

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7.6 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide*.

7.6.1 Floating-Point Unit

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the repeat block register, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information, see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

7.6.2 Trigonometric Math Unit

The TMU extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in Table 7-9.

Table 7-9. TMU Supported Instructions

INSTRUCTIONS	C EQUIVALENT OPERATION	PIPELINE CYCLES
MPY2PIF32 RaH,RbH	a = b * 2pi	2/3
DIV2PIF32 RaH,RbH	a = b / 2pi	2/3
DIVF32 RaH,RbH,RcH	a = b/c	5
SQRTF32 RaH,RbH	a = sqrt(b)	5
SINPUF32 RaH,RbH	a = sin(b*2pi)	4
COSPUF32 RaH,RbH	a = cos(b*2pi)	4
ATANPUF32 RaH,RbH	a = atan(b)/2pi	4
QUADF32 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2	5

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations. A detailed explanation of the workings of the FPU can be found in the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

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7.7 Control Law Accelerator

The CLA is an independent single-precision (32-bit) FPU processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks can be specified. Each task is started by software or a peripheral such as the ADC, ePWM, eCAP, eQEP, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes, the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers, ePWM, eCAP, eQEP, Comparator and DAC registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

Figure 7-2 shows the CLA block diagram.

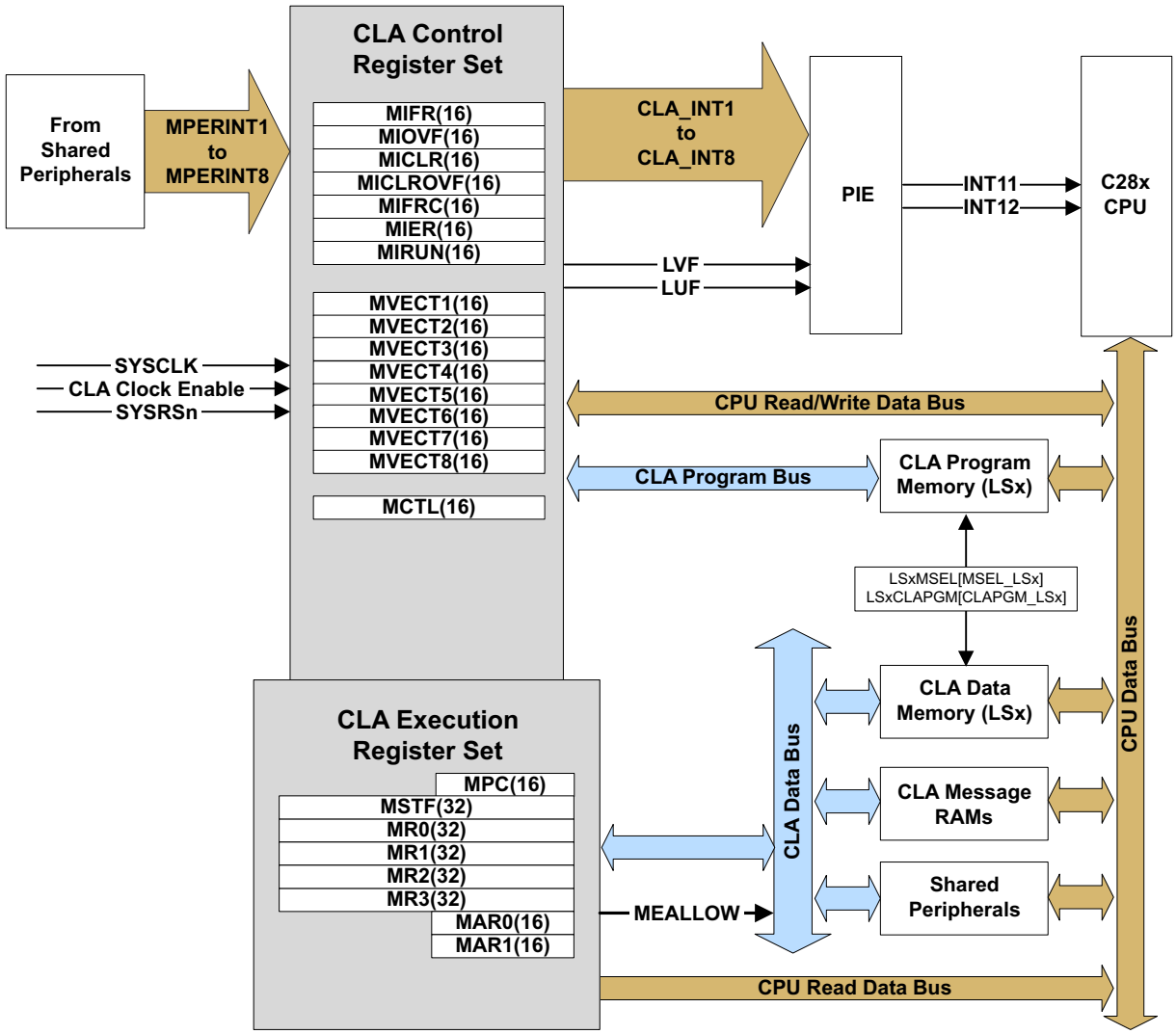


Figure 7-2. CLA Block Diagram

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7.8 Direct Memory Access

The CPU has its own 6-channel DMA module. The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

The DMA module is an event-based machine, meaning it requires a peripheral or software trigger to start a DMA transfer. Although it can be made into a periodic time-driven machine by configuring a timer as the interrupt trigger source, there is no mechanism within the module itself to start memory transfers periodically. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has the ability to be configured at a higher priority than the others.

DMA features include:

- Six channels with independent PIE interrupts
- Peripheral interrupt trigger sources
  - ADC interrupts and EVT signals
  - Multichannel buffered serial port transmit and receive
  - External interrupts
  - CPU timers
  - EPWMxSOC signals
  - SPIx transmit and receive
  - SDFM
  - Software trigger
- Data sources and destinations:
  - GSx RAM
  - ADC result registers
  - ePWMx
  - SPI
  - McBSP
  - EMIF
- Word Size: 16-bit or 32-bit (SPI and McBSP limited to 16-bit)
- Throughput: four cycles/word (without arbitration)

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Figure 7-3 shows a device-level block diagram of the DMA.

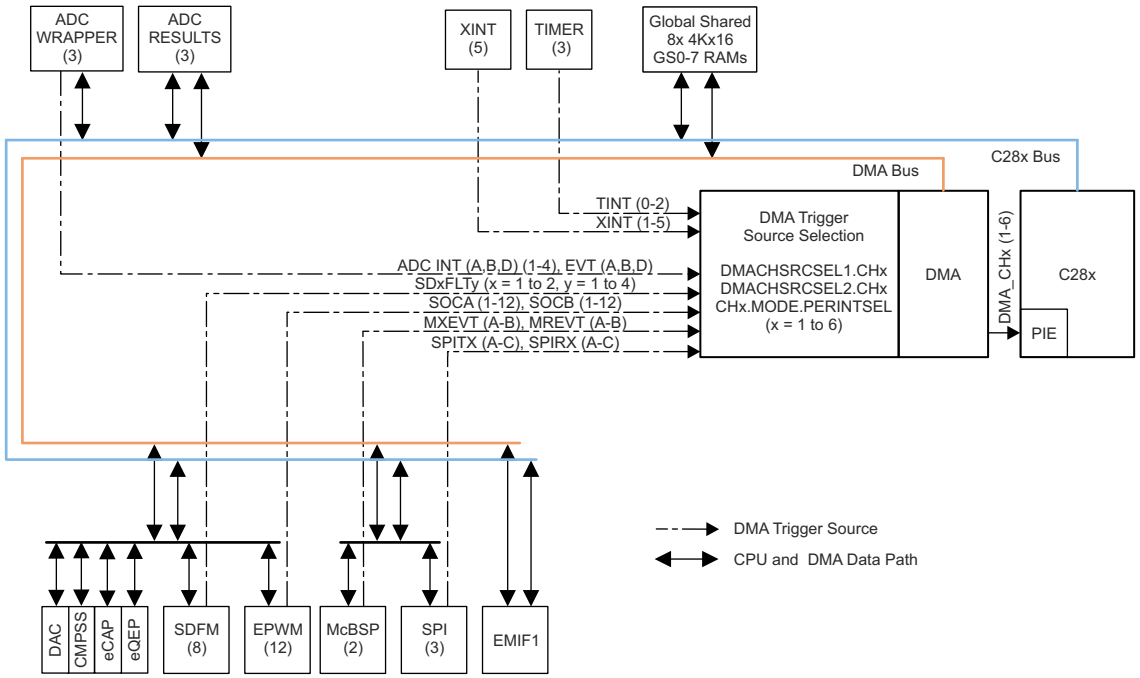


Figure 7-3. DMA Block Diagram

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7.9 Boot ROM and Peripheral Booting

The device boot ROM contains bootloading software. The device boot ROM is executed each time the device comes out of reset. Users can configure the device to boot to flash (using GET mode) or choose to boot the device through one of the bootable peripherals by configuring the boot mode GPIO pins.

Table 7-10 shows the possible boot modes supported on the device. The default boot mode pins are GPIO72 (boot mode pin 1) and GPIO 84 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming OTP locations. This is recommended only for cases in which the factory default boot mode pins do not fit into the customer design. More details on the locations to be programmed is available in the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-10. Device Boot Mode

MODE NO.	CPU1 BOOT MODE	$\overline{\text{TRST}}$	GPIO72 (BOOT MODE PIN 1)	GPIO84 (BOOT MODE PIN 0)
0	Parallel I/O	0	0	0
1	SCI Mode	0	0	1
2	Wait Boot Mode	0	1	0
3	Get Mode	0	1	1
4-7	EMU Boot Mode (JTAG debug probe connected)	1	X	X

Note

The default behavior of Get mode is boot-to-flash. On unprogrammed devices, using Get mode will result in repeated watchdog resets, which may prevent proper JTAG connection and device initialization. Use Wait mode or another boot mode for unprogrammed devices.

CAUTION

Some reset sources are internally driven by the device. The user must ensure the pins used for boot mode are not actively driven by other devices in the system for these cases. The boot configuration has a provision for changing the boot pins in OTP. For more details, see the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

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7.9.1 EMU Boot or Emulation Boot

The CPU enters this boot when it detects that $\overline{\text{TRST}}$ is HIGH (that is, when a JTAG debug probe/debugger is connected). In this mode, the user can program the EMU_BOOTCTRL control-word (at location 0xD00) to instruct the device on how to boot. If the contents of the EMU_BOOTCTRL location are invalid, then the device would default to WAIT Boot mode. The emulation boot allows users to verify the device boot before programming the boot mode into OTP. Note that EMU_BOOTCTRL is not actually a register, but refers to a location in RAM (PIE RAM). PIE RAM starts at 0xD00, but the first few locations are reserved (when initializing the PIE vector table in application code) for these boot ROM variables.

7.9.2 WAIT Boot Mode

The device in this boot mode loops in the boot ROM. This mode is useful if users want to connect a debugger on a secure device or if users do not want the device to execute an application in flash yet.

7.9.3 Get Mode

The default behavior of Get mode is boot-to-flash. This behavior can be changed by programming the Zx-OTPBOOTCTRL locations in user configurable DCSM OTP. The user configurable DCSM OTP on this device is divided in to two secure zones: Z1 and Z2. The Get mode function in boot ROM first checks if a valid OTPBOOTCTRL value is programmed in Z1. If the answer is yes, then the device boots as per the Z1-OTPBOOTCTRL location. The Z2-OTPBOOTCTRL location is read and decodes only if Z1-OTPBOOTCTRL is invalid or not programmed. If either Zx-OTPBOOTCTRL location is not programmed, then the device defaults to factory default operation, which is to use factory default boot mode pins to boot to flash if the boot mode pins are set to GET MODE. Users can choose the device through which to boot—SPI, I2C, CAN, and USB—by programming proper values into the user configurable DCSM OTP. More details on this can be found in the *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*.

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7.9.4 Peripheral Pins Used by Bootloaders

Table 7-11 shows the GPIO pins used by each peripheral bootloader. This device supports two sets of GPIOs for each mode, as shown in Table 7-11.

Table 7-11. GPIO Pins Used by Each Peripheral Bootloader

BOOTLOADER	GPIO PINS	NOTES
SCI-Boot0	SCITXDA: GPIO84 SCIRXDA: GPIO85	SCIA Boot I/O option 1 (default SCI option when chosen through Boot Mode GPIOs)
SCI-Boot1	SCIRXDA: GPIO28 SCITXDA: GPIO29	SCIA Boot option 2 – with alternate I/Os.
Parallel Boot	D0 – GPIO65 D1 – GPIO64 D2 – GPIO58 D3 – GPIO59 D4 – GPIO60 D5 – GPIO61 D6 – GPIO62 D7 – GPIO63 HOST_CTRL – GPIO70 DSP_CTRL – GPIO69	
CAN-Boot0	CANRXA: GPIO70 CANTXA: GPIO71	CAN-A Boot – I/O option 1
CAN-Boot1	CANRXA: GPIO62 CANTXA: GPIO63	CAN-A Boot – I/O option 2
I2C-Boot0	SDAA: GPIO91 SCLA: GPIO92	I2CA Boot – I/O option 1
I2C-Boot1	SDAA: GPIO32 SCLA: GPIO33	I2CA Boot – I/O option 2
SPI-Boot0	SPISIMOA - GPIO58 SPISOMIA - GPIO59 SPICLKA - GPIO60 $\overline{\text{SPISTEA}}$ - GPIO61	SPIA Boot – I/O option 1
SPI-Boot1	SPISIMOA – GPIO16 SPISOMIA – GPIO17 SPICLKA – GPIO18 $\overline{\text{SPISTEA}}$ – GPIO19	SPIA Boot – I/O option 2
USB Boot	USB0DM - GPIO42 USB0DP - GPIO43	The USB Bootloader will switch the clock source to the external crystal oscillator (X1 and X2 pins). A 20-MHz crystal should be present on the board if this boot mode is selected.

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7.10 Dual Code Security Module

The dual code security module (DCSM) prevents access to on-chip secure memories. The term “secure” means access to secure memories and resources is blocked. The term “unsecure” means access is allowed; for example, through a debugging tool such as Code Composer Studio™ (CSS).

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both the zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (CLA, LSx RAM, and flash sectors).

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in an OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP.

Note

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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7.11 Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- X1 (XTAL)
- AUXPLLCLK

7.12 Nonmaskable Interrupt With Watchdog Timer (NMIWD)

The NMIWD module is used to handle system-level errors. The conditions monitored are:

- Missing system clock due to oscillator failure
- Uncorrectable ECC error on CPU access to flash memory
- Uncorrectable ECC error on CPU, CLA, or DMA access to RAM

If the CPU does not respond to the latched error condition, then the NMI watchdog will trigger a reset after a programmable time interval. The default time is 65536 SYSCLK cycles.

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7.13 Watchdog

The watchdog module is the same as the one on previous TMS320C2000™ MCUs, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backwards-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-4 shows the various functional blocks within the watchdog module.

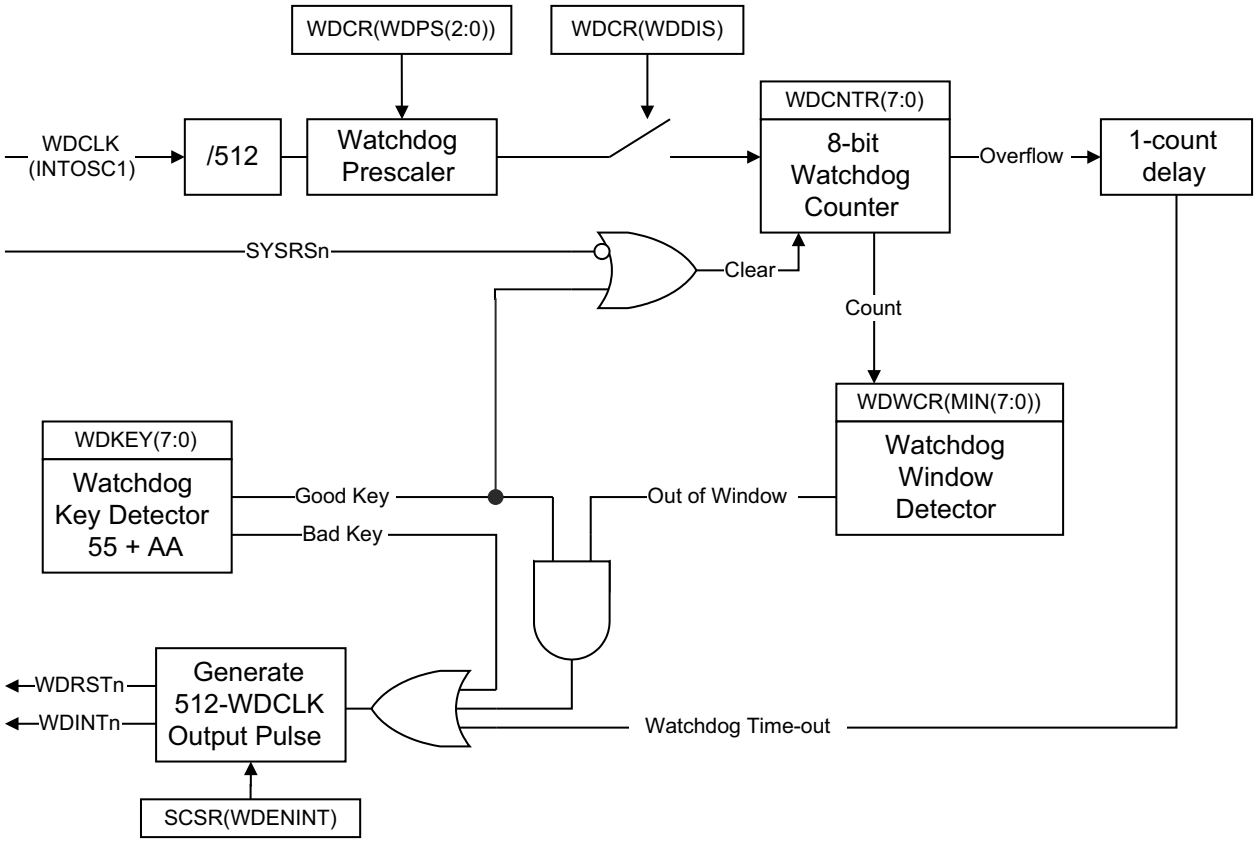


Figure 7-4. Windowed Watchdog

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7.14 Configurable Logic Block (CLB)

The C2000 configurable logic block (CLB) is a collection of blocks that can be interconnected using software to implement custom digital logic functions or enhance existing on-chip peripherals. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as comparators, or to implement custom serial data exchange protocols. Through the CLB, functions that would otherwise be accomplished using external logic devices can now be implemented inside the MCU.

The CLB peripheral is configured through the CLB tool. For more information on the CLB tool, available examples, application reports and users guide, please refer to the following location in your C2000Ware package (C2000Ware_2_00_00_03 and higher):

- **C2000WARE_INSTALL_LOCATION\utilities\clb_tool\clb_syscfg\doc**
- *CLB Tool User's Guide*
- *Designing With the C2000™ Configurable Logic Block (CLB) Application Report*
- *How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers Application Report*

The CLB module and its interconnects are shown in Figure 7-5.

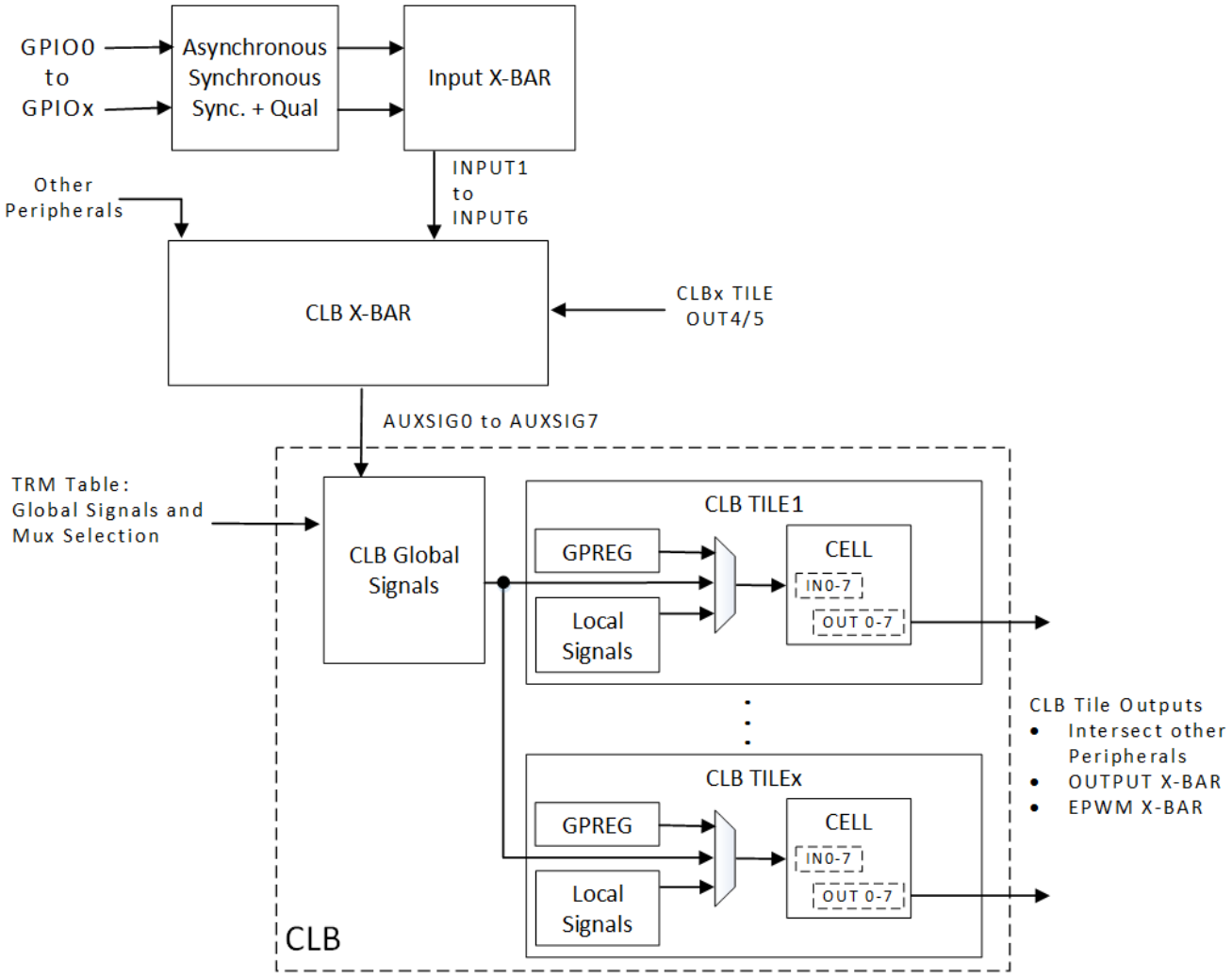


Figure 7-5. CLB Overview

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Absolute encoder protocol interfaces are now provided as Position Manager solutions in the C2000Ware MotorControl SDK. Configuration files, application programmer interface (API), and use examples for such solutions are provided with C2000Ware MotorControl SDK. In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality. See Table 4-1 for the devices that support the CLB feature.

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7.15 Functional Safety

TMS320C2000™ MCUs are equipped with a TI release validation-based C28x and CLA Compiler Qualification Kit (CQ-Kit), which is available for free and may be requested at the Compiler Qualification Kit web page.

Additionally, C2000™ MCUs are supported by the TI C2000 Support from Embedded Coder from MathWorks® to generate C2000-optimized code from a Simulink® model. Simulink® enables Model-Based Design to ease the systematic compliance process with certified tools, including Embedded Coder®, Simulink® model verification tools, Polyspace® code verification tools, and the IEC Certification Kit for ISO 26262 and IEC 61508 compliance. For more information, see the How to Use Simulink for ISO 26262 Projects article.

The *Error Detection in SRAM Application Report* provides technical information about the nature of the SRAM bit cell and bit array, as well as the sources of SRAM failures. It then presents methods for managing memory failures in electronic systems. This discussion is intended for electronic system developers or integrators who are interested in improving the robustness of the embedded SRAM.

Functional Safety-Compliant products are developed using an ISO 26262/IEC 61508-compliant hardware development process that is independently assessed and certified to meet ASIL D/SIL 3 systematic capability (see certificate). The TMS320F2837D, TMS320F2837xS, and TMS320F2807x MCUs have been certified to meet a component-level random hardware capability of ASIL B/SIL 2 (see certificate).

The Functional Safety-Compliant enablers include:

- A Functional Safety Manual
- A detailed, tunable, quantitative Failure Modes, Effects, and Diagnostics Analysis (FMEDA)
- A software diagnostic library that will help shorten the time to implement various software safety mechanisms
- A collection of application reports to help in the development of functionally safe systems.

A functional safety manual that describes all of the hardware and software functional safety mechanisms is available. See the *Safety Manual for TMS320F2837xD, TMS320F2837xS, and TMS320F2807x*.

A detailed, tunable, fault-injected, quantitative FMEDA that enables the calculation of random hardware metrics—as outlined in the International Organization for Standardization ISO 26262 and the International Electrotechnical Commission IEC 61508 for automotive and industrial applications, respectively—is also available. This tunable FMEDA must be requested; see the *C2000™ Package for Automotive and Industrial MCUs User's Guide*.

- A white paper outlining the value (or benefit) of a tunable FMEDA is available. See the *Functional Safety: A tunable FMEDA for C2000™ MCUs* publication.
- Parts 1 and 2 of a five-part FMEDA tuning training are available. See the C2000™ Tunable FMEDA Training page.
  Parts 3, 4, and 5 are packaged with the tunable FMEDA, and must be requested.

The C2000 Diagnostic Software Library is a collection of different safety mechanisms designed to detect faults. These safety mechanisms target different device components, including the C28x core, the control law accelerator (CLA), system control, static random access memory (SRAM), flash, and communications and control peripherals. The software safety mechanisms leverage available hardware safety features such as the C28x hardware built-in self-test (HWBIST); error detection and correction functionality on memories; parallel signature analysis circuitry; missing clock detection logic; watchdog counters; and hardware redundancy.

Also included are software functional safety manual, user guides, example projects, and source code to help users shorten system integration time. The library package includes a compliance support package (CSP), a series of documents that TI used to develop and test the diagnostic software library. The CSP provides the necessary documentation and reports to assist users with compliance to functional safety standards: software safety requirements specifications; a software architecture document; software module design documents; software module unit test plans; software module unit test documents; static analysis reports; unit test reports; dynamic analysis reports; functional test reports; and traceability documents. Users can use these documents to comply with route 1s (as described in IEC 61508-3, section 7.4.2.12) to reuse a preexisting software element to implement all or part of a safety function. The contents of the CSP could also help users make important decisions for overall system safety compliance.

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Two application reports offer details about how to develop functionally safe systems with C2000 real-time control devices:

- *C2000™ Hardware Built-In Self-Test* discusses the HWBIST safety mechanism, along with its functions and features, in the F2807x/F2837xS/F2837xD series of C2000 devices. The report also addresses some system-level considerations when using the HWBIST feature and explains how customers can use the diagnostic library on their system.
- *C2000™ CPU Memory Built-In Self-Test* describes embedded memory validation using the C28x central processing unit (CPU) during an active control loop. It discusses system challenges to memory validation as well as the different solutions provided by C2000 devices and software. Finally, it presents the Diagnostic Library implementations for memory testing.

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8 Applications, Implementation, and Layout

8.1 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.2 Key Device Features

Table 8-1. Key Device Features

MODULE	FEATURE	SYSTEM BENEFIT
C28x PROCESSING		
Real-time control CPUs	Up to 240 MIPS One C28x core: 120 MIPS (1 x 120 MIPS) Two CLA cores: 120 MIPS (1 x 120 MIPS) Flash: Up to 512 KB RAM : Up to 100 KB 64-bit Floating Point Unit (FPU64) Trigonometric Math Unit (TMU) CRC engine and instructions (VCRC)	TI's 32-bit C28x DSP cores, provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM Provides 120 MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. **CLA:** Allows user to execute time-critical control loops concurrently with main CPU **FPU64:** Native hardware support for IEEE-754 double-precision floating-point operations **TMU:** Accelerators used to speed up execution of trigonometric and arithmetic operations for faster computation (such as PLL and DQ transform) optimized for control applications. Helps in achieving faster control loops, resulting in higher efficiency and better component sizing. Special instructions to support nonlinear PID control algorithms **VCRC:** Provides a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. See Real-time Benchmarks Showcasing C2000™ControlMCU's Optimized Signal Chain.
SENSING		
Analog-to-Digital Converter (ADC) (configurable 12-bit or 16-bit)	Three ADC modules 12-bit mode: (3.5 MSPS) Single-ended mode: Up to 17 channels	ADC provides precise and concurrent sampling of all three-phase currents and DC bus with zero jitter. ADC post-processing – On-chip hardware reduces ADC ISR complexity and shortens current loop cycles. More ADCs help in multiphase applications. Provide better effective MSPS (oversampling) and typical ENOB for better control-loop performance.

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Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
Comparator Subsystem (CMPSS)	**CMPSS** 8 windowed comparators Three 12-bit DACs 60-ns detection to trip time DAC ramp generation Low DAC output on external pin Digital filters Slope compensation	**System protection without false alarms:** Comparator Subsystem (CMPSS) modules are useful for applications such as peak-current mode control, switched-mode power, power factor correction, and voltage trip monitoring. PWM trip-triggering and removal of unwanted noise are easy with blanking window and filtering features provided with the analog comparator subsystems. Provides better control accuracy. No need for further CPU configuration to control the PWM with the comparator and 12-bit DAC (CMPSS). Enables protection and control using the same pin.
Sigma Delta Filter Module (SDFM)	Up to 8 independently configurable digital comparator filter channels Up to 8 independently configurable digital data filter channels	Enables galvanic isolation with reinforced delta sigma modulators. SDFMs interface with external delta sigma modulator ADCs, which is ideal for signals that may require isolation. Comparator filter supports overcurrent and undercurrent protection but tripping the PWM without CPU intervention Digital data filter provides higher ENOBs for better control-loop performance
Enhanced Quadrature Encoder Pulse (eQEP)	3 eQEP modules	Used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine used in a high-performance motion and position-control system. Also can be used in other applications to count input pulses from an external device (such as a sensor).
Enhanced Capture (eCAP)	6 eCAP modules Measures elapsed time between events (up to 4 time-stamped events). Connects to any GPIO through the input X-BAR. When not used in capture mode, the eCAP module can be configured as a single-channel PWM output (APWM).	**Applications for eCAP include:** Speed measurements of rotating machinery (for example, toothed sprockets sensed through Hall sensors) Elapsed time measurements between position sensor pulses Period and duty-cycle measurements of pulse train signals Decoding current or voltage amplitude derived from duty-cycle encoded current/voltage sensors

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Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
ACTUATION		
Enhanced Pulse Width Modulation (ePWM)/High-Resolution Pulse Width Modulation (HRPWM)	Up to 24 ePWM channels Ability to generate high-side/low-side PWMs with deadband Supports Valley switching (ability to switch PWM output at valley point) and features like blanking window	Flexible PWM waveform generation with best power topology coverage. Shadowed Dead band itself and shadowed action qualifier enable adaptive PWM generation and protection for improved control accuracy and reduced power loss. Enables improvement in Power Factor (PF) and Total Harmonic Distortion (THD), which is especially relevant in Power Factor Correction (PFC) applications. Improves light load efficiency.
	HRPWM capability: 16 channels provide high-resolution capability (150 ps) Provides 150-ps steps for duty cycle, period, deadband, and phase offsets for 99% greater precision	Beneficial for accurate control and enables better-performance high-frequency power conversion. Achieves cleaner waveforms and avoids oscillations/limit cycle at output.
	One-shot and global reload feature	Critical for variable-frequency and multiphase DC-DC applications and helps in attaining high-frequency control loops (>2 MHz). En*ables control of interleaved LLC topologies at high frequencies*
	Independent PWM action on a Cycle-by-Cycle (CBC) trip event and an One-Shot Trip (OST) trip event	Provides cycle-by-cycle protection and complete shutoff of PWM under fault condition. Helps implement multiphase PFC or DC-DC control.
	Load on SYNC (support for shadow-to-active load on a SYNC event)	Enables variable-frequency applications (allows LLC control in power conversion).
	Ability to shut down the PWMs without software intervention (no ISR latency)	Fast protection under fault condition
	Delayed Trip Functionality	Helps implement the deadband with Peak Current Mode Control (PCMC) Phase-Shifted Full Bride (PSFB) DC-DC easily without occupying much CPU resources (even on trigger events based on comparator, trip, or sync-in events).
	Dead band Generator (DB) submodule	Prevents simultaneous ON conditions of High- and Low-side gates by adding programmable delay to rising (RED) and falling (FED) PWM signal edges.
	Flexible PWM Phase Relationships and Timer Synchronization	Each ePWM module can be synchronized with other ePWM modules or other peripherals. Keeps PWM edges perfectly in synchronization with certain events. Supports flexible ADC scheduling with specific sampling window in synchronization with power device switching.
CONNECTIVITY		
Serial Peripheral Interface (SPI)	3 high-speed SPI port	Supports 50 MHz
Serial Communication Interface (SCI)	4 SCI (UART) modules	Interfaces with controllers
Controller Area Network (CAN/DCAN)	2 DCAN module (can be assigned to Connectivity Manager (M4))	Provides compatibility with classic CAN modules
Inter-Integrated Circuit (I2C)	2 I2C modules	Interfaces with external EEPROMs, sensors, or controllers
Multichannel Buffered Serial Port (McBSP)	Up to 2 McBSP modules	Interface to high-speed external ADC or additional SPI peripheral

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Table 8-1. Key Device Features (continued)

MODULE	FEATURE	SYSTEM BENEFIT
External Memory Interfaces (EMIFs) with ASRAM and SDRAM support	One EMIF module	Interface with External ASRAM and SDRAM
OTHER SYSTEM FEATURES		
Configurable Logic Block (CLB)	Collection of configurable blocks that can be inter-connected using software to implement custom digital logic functions	User customized PWM protection features, custom logic to off-load complex algorithms/state machines, custom peripherals, and used to implement absolute encoders used in servo drives User also used for protection of multilevel inverter/PFC or multilevel DC-DC Provides the ability to build logic around existing IPs like ETPWM, ECAP, QEP and GPIOs. Enables development of unique IP such as PWM Safety modules, Encoder engines, etc.
Security enhancers	Dual-zone Code Security Module (DCSM) Secure Boot JTAGLOCK BackGround CRC (BGCRC) Generic CRC (GCRC) Watchdog Write Protection on Register Missing Clock Detection Logic (MCD) Error Correction Code (ECC) and parity	**DCSM:** Prevents duplication and reverse-engineering of proprietary code **Secure Boot:** Uses AES128 CMAC algorithm to ensure code that runs on the device is authentic **JTAGLOCK:** Ability to block emulation of the device **BGCRC:** Checks memory integrity with no CPU overhead or system performance impact **GCRC:** Designated Connectivity Manager module for computing the CRC value on a configurable block of memory **Watchdog:** Generates reset if CPU gets stuck in endless loops of execution **Write Protection on Registers:** LOCK protection on system configuration registers Protection against spurious CPU writes **MCD:** Automatic clock failure detection **ECC and parity:** Single-bit error correction and double-bit error detection
Crossbars (XBARs)	Provides flexibility to connect device inputs, outputs, and internal resources in a variety of configurations. • Input X-BAR • Output X-BAR • ePWM X-BAR • CLB Input X-BAR • CLB Output X-BAR • CLB X-BAR	**Enhances hardware design versatility:** **Input X-BAR:** Routes signals from any GPIO to multiple IP blocks within the chip **Output XBAR:** Routes internal signals onto designated GPIO pins **ePWM X-BAR:** Routes internal signals from various IP blocks to ePWM **CLB Input X-BAR:** Allows user to route signals directly from any GPIO to Configurable Logic Block (CLB) **CLB Output X-BAR:** Allows user to bring signals from CLB tiles to designated GPIO pins **CLB X-BAR:** Allows user to bring signals from various IP blocks to CLB
Direct Memory Access (DMA) controller	6-channels	The direct memory access (DMA) module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up CPU bandwidth for other system functions.
USB		Useful for system datalogging and boot to USB for updating on-chip flash

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8.3 Application Information

8.3.1 Typical Application

The *Typical Applications* section details *some* applications of this device. For a more extensive list of applications, see the *Applications* section of this data sheet.

8.3.1.1 Servo Drive Control Module

Servo drives require high precision current and voltage sensing for accurate torque control and often supports interfaces for multiple encoder types along with communication interfaces. This C2000 device can be used either as single chip solution for standalone servo drive (shown in Figure 8-1) or can be used in decentralized systems (shown in Figure 8-2). In the later case, the F2838x C2000 device functions as the controller which samples all the voltage and current inputs and generates the correct PWM signals for inverter. Each C2000 device serves as real-time controller for a target axis, running motor current control loop. Using the Fast Serial Interface (FSI) peripheral, up to 16 axes can be managed with one C2000 device. As an outer loop controller, the C2000 device executes main axis motor control, controls data exchange with all secondary axis over FSI and communicates with a host or PLC through EtherCAT.

8.3.1.1.1 System Block Diagram

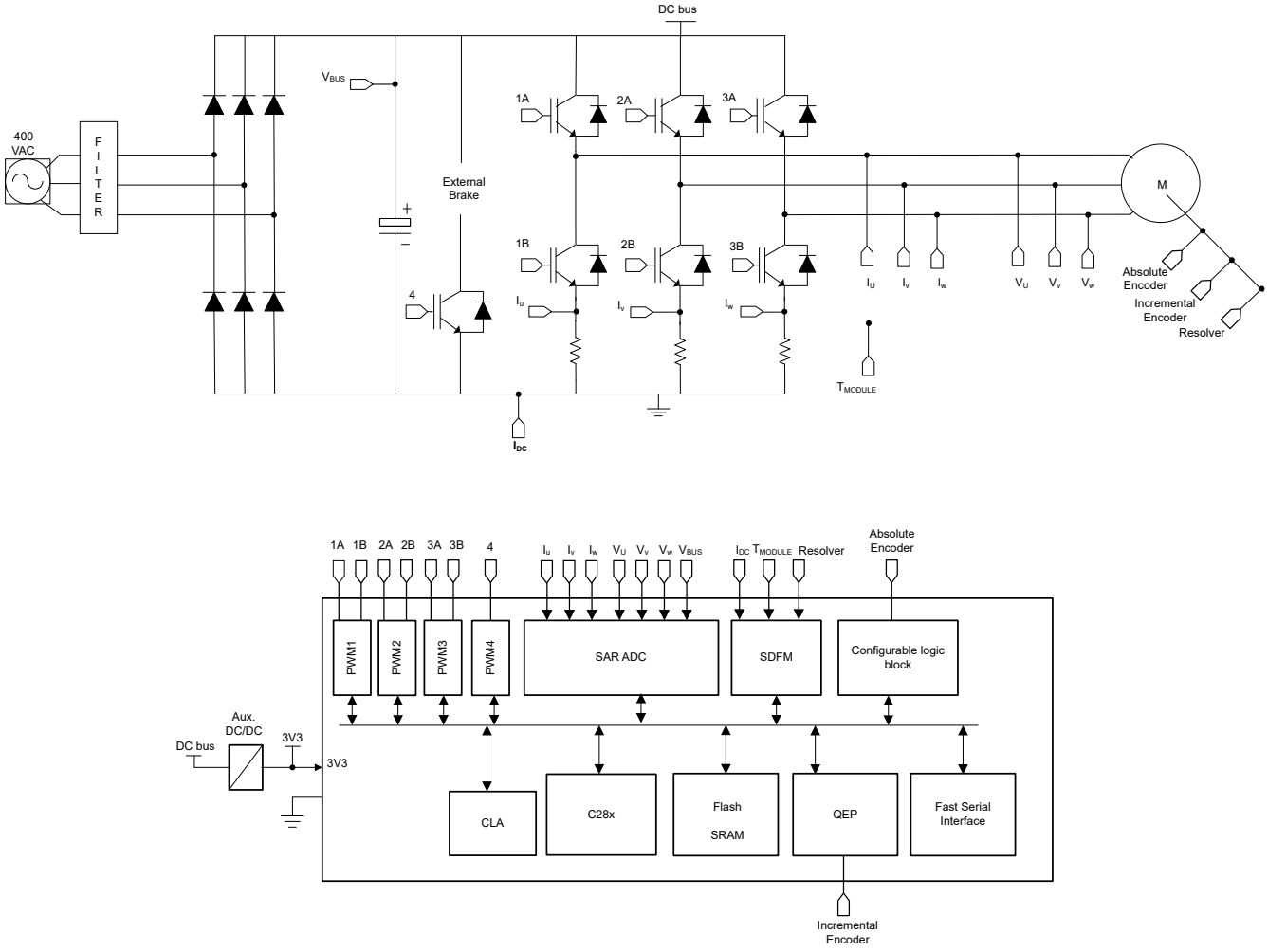


Figure 8-1. Servo Drive Control Module

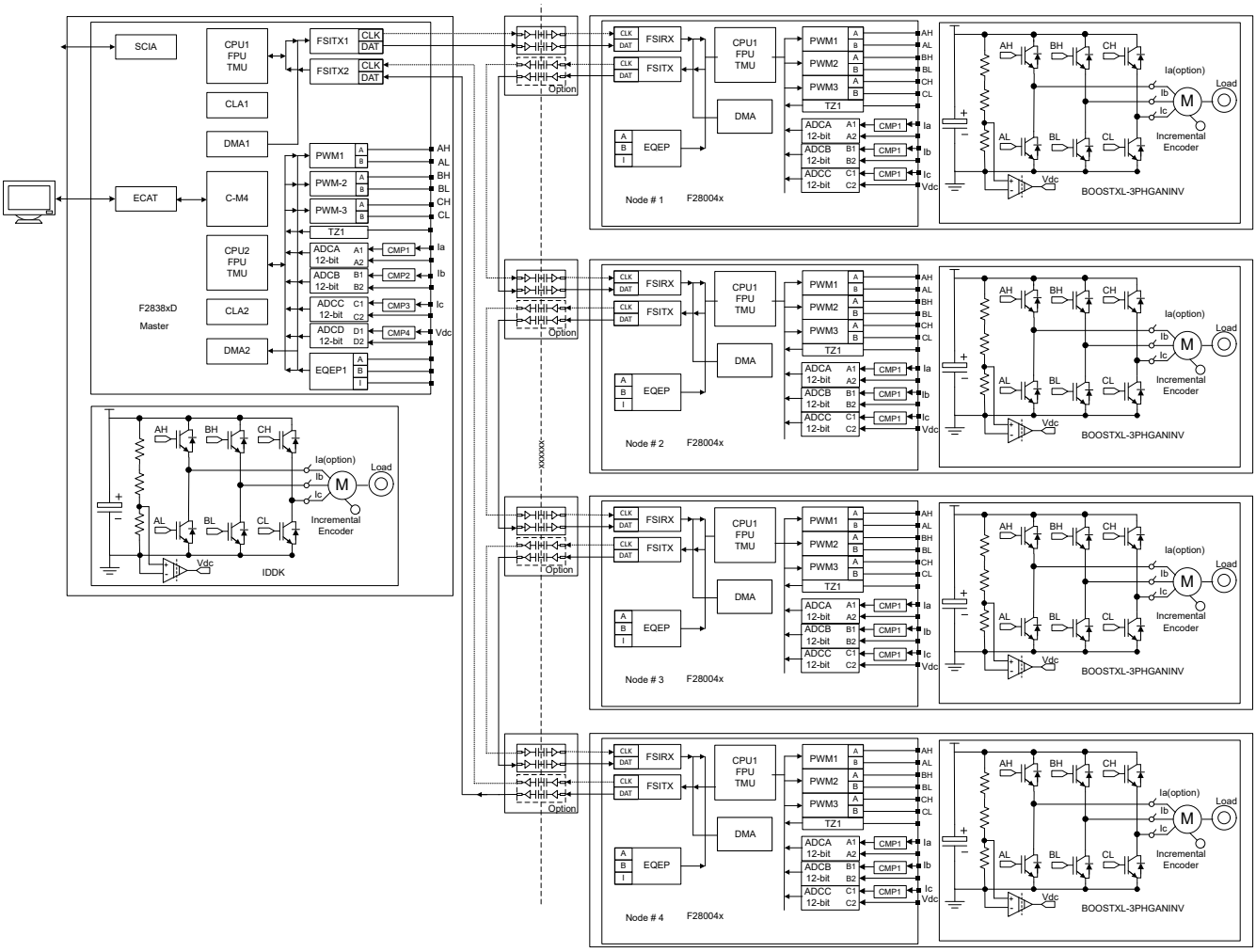


Figure 8-2. Distributed Multi-Axis Servo Drive

8.3.1.1.2 Servo Drive Control Module Resources

Reference Designs and Associated Training Videos

48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Evaluation Module

The BOOSTXL-3PHGANINV evaluation module features a 48-V/10-A three-phase GaN inverter with precision in-line shunt-based phase current sensing for accurate control of precision drives such as servo drives.

C2000 DesignDRIVE position manager BoosterPack™ plug-in module

The PositionManager BoosterPack is a flexible low voltage platform intended for evaluating interfaces to absolute encoders and analog sensors like resolvers and SinCos transducers. When combined with the DesignDRIVE Position Manager software solutions this low-cost evaluation module becomes a powerful tool for interfacing many popular position encoder types such as EnDat, BiSS and T-format with C2000 Real-Time Control devices. C2000 Position Manager technology integrates interfaces to the most popular digital and analog position sensors onto C2000 Real-Time Controller, thus eliminating the need for external FPGAs for these functions.

C2000Ware MotorControl SDK

MotorControl SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 real-time controller based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs) which are targeted for industrial drives, robotics,

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appliances, and automotive applications. MotorControl SDK provides all the needed resources at every stage of development and evaluation for high performance motor control applications.

TIDM-02006 Distributed multi-axis servo drive over fast serial interface (FSI) reference design
This reference design presents an example distributed or decentralized multi-axis servo drive over Fast Serial Interface (FSI) using C2000™ real-time controllers. Multi-axis servo drives are used in many applications such as factory automation and robots. The cost per axis, performance and ease of use are always high concerns for such systems. FSI is a cost-optimized and reliable high speed communication interface with low jitter that can daisy-chain multiple C2000 microcontrollers. In this design, each TMS320F280049 or TMS320F280025 real-time controller serves as a real-time controller for a distributed axis, running motor current control loop. A single TMS320F28388D runs position and speed control loops for all axes. The same F2838x also executes a centralized motor control axis plus EtherCAT communication, leveraging its multiple cores. The design uses our existing EVM kits, the software is released within C2000WARE MotorControl SDK.

TIDM-02007 Dual-axis motor drive using fast current loop (FCL) and SFRA on a single MCU reference design
This reference design presents a dual-axis motor drive using fast current loop (FCL) and software frequency response analyzer (SFRA) technologies on a single C2000 controller. The FCL utilizes dual core (CPU, CLA) parallel processing techniques to achieve a substantial improvement in control bandwidth and phase margin, to reduce the latency between feedback sampling and PWM update, to achieve higher control bandwidth and maximum modulation index, to improve DC bus utilization by the drive and to increase speed range of the motor. The integrated SFRA tool enables developers to quickly measure the frequency response of the application to tune speed and current controllers. Given the system-level integration and performance of C2000 series, MCUs have the ability to support dual-axis motor drive requirements simultaneously that delivers very robust position control with higher performance. The software is released within C2000Ware MotorControl SDK.

8.3.1.2 Solar Micro Inverter

A Solar Micro Inverter consists of a DC-AC inverter power stage and one or more Maximum Power Point Tracking (MPPT) DC-DC power stages. Typical switching frequency for the inverter (DC-AC) is between 20kHz-50kHz and for DC-DC side can be in the range 100kHz-200kHz. A variety of power stage topologies can be used to achieve this and the diagram only depicts a typical power stage and the control & communication requirements. A C2000 microcontroller has on-chip EPWM, ADC and analog comparator modules to implement complete digital control of such micro inverter system.

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8.3.1.2.1 System Block Diagram

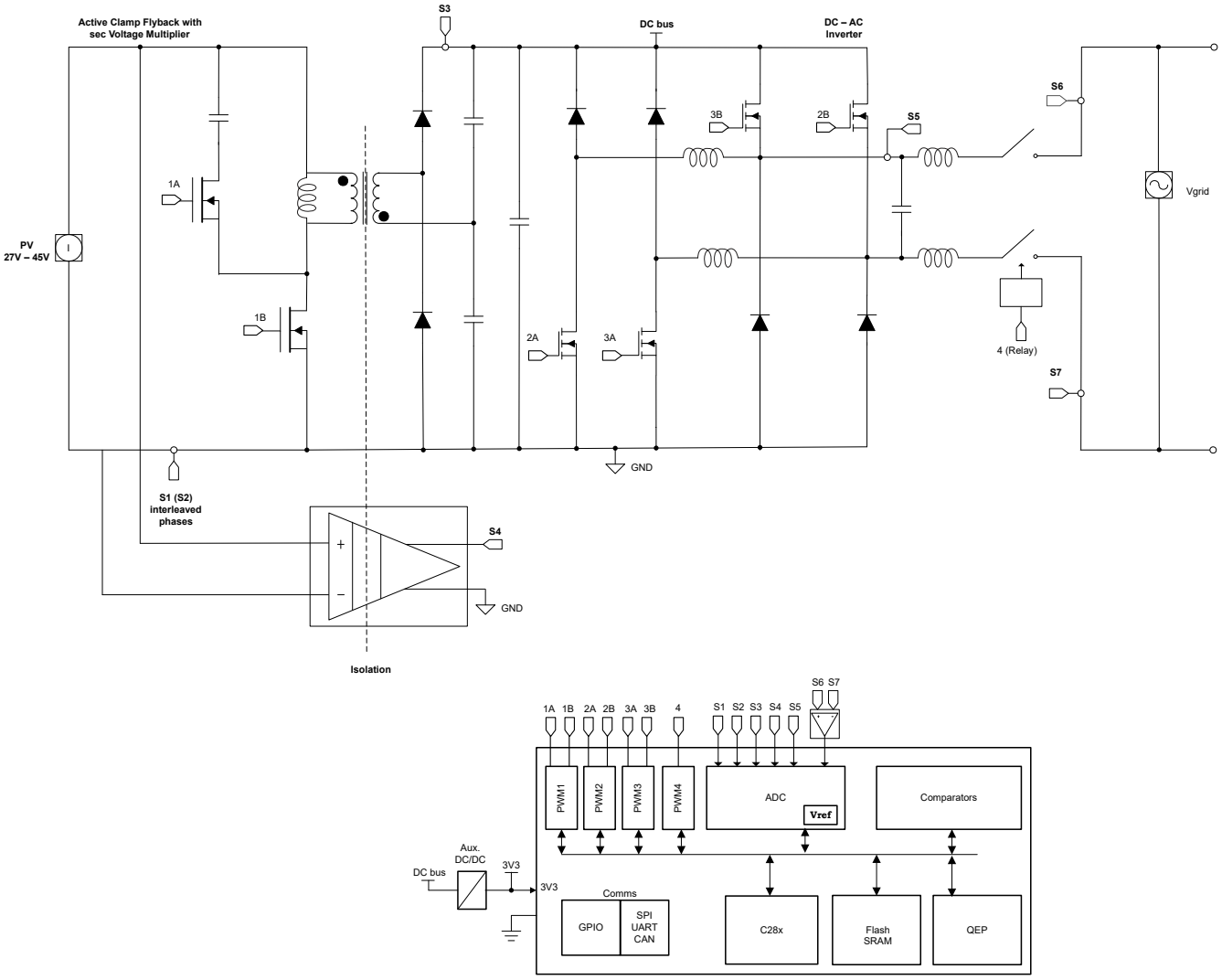


Figure 8-3. Solar Micro Inverter

8.3.1.2.2 Solar Micro Inverter Resources

Reference Designs and Associated Training Videos

C2000™ MCUs - Digital Power (Video)
This training series covers the basics of digital power control and how to implement it on C2000 microcontrollers.

Four Key Design Considerations When Adding Energy Storage to Solar Power Grids
This white paper explores the design considerations in a grid-connected storage-integrated solar installation system

C2000WARE-DIGITALPOWER-SDK
DigitalPower SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs) which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power application

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Digitally Controlled Solar Micro Inverter Design using C2000™ Piccolo Microcontroller
This document presents the implementation details of a digitally-controlled solar micro inverter using the C2000 microcontroller. A 250-W isolated micro inverter design presents all the necessary PV inverter functions using the Piccolo-B (F28035) control card. This document describes the power stages on the micro inverter board, as well as an incremental build level system that builds the software by verifying open loop operation and closed loop operation. This guide describes control structures and algorithms for controlling power flow, maximizing power from the PV panel (MPPT), and locking to the grid using phase locked loop (PLL), along with hardware details of Texas Instruments Solar Micro Inverter Kit (TMDSOLARUINVKIT)

TIDU405B Grid-tied Solar Micro Inverter with MPPT
This C2000 Solar Micro Inverter EVM hardware consists of two stages. These are: (1) an active clamp fly-back DC/DC converter with secondary voltage multiplier and, (2) a DC-AC inverter. A block diagram of this system is shown in Figure 1b. The DC-DC converter draws dc current from the PV panel such that the panel operates at its maximum power transfer point. This requires maintaining the panel output, that is, the DC-DC converter input at a level determined by the MPPT algorithm. The MPPT algorithm determines the panel output current (reference current) for maximum power transfer. Then a current control loop for the fly-back converter ensures that the converter input current tracks the MPPT reference current. The fly-back converter also provides high frequency isolation for the DC-DC stage. The output of the fly-back stage is a high voltage DC bus which drives the DC-AC inverter. The inverter stage maintains the DC bus at a desired set point and injects controlled sine wave current into the grid. The inverter also implements grid synchronization in order to maintain its current waveform locked to phase and frequency of the grid voltage. A C2000 piccolo microcontroller with its on-chip PWM, ADC and analog comparator modules is able to implement complete digital control of such micro inverter system.

Software Phase Locked Loop Design Using C2000™ Microcontrollers for Single Phase Grid Connected Inverter Application Report
Grid connected applications require an accurate estimate of the grid angle to feed power synchronously to the grid. This is achieved using a software phase locked loop (PLL). This application report discusses different challenges in the design of software phase locked loops and presents a methodology to design phase locked loops using C2000 controllers for single phase grid connection applications.

8.3.1.3 On-Board Charger (OBC)

An On-Board Charger (OBC) consists of two power stages: an AC-DC power converter and a subsequent DC-DC power converter stage. The OBC can be implemented by using a single MCU to control both the AC-DC and DC-DC power converters. For example: an 11-kW OBC can be implemented by using three 3.7-kW single-phase OBC modules, as shown in Figure 8-4. This approach allows us to easily support both single-phase 240 AC (North America) and 3-phase AC (rest of the world).

OBC-charging design requirements are as follows:

- High-performance and fast digital control loops enabling highly efficient power conversion and increased power density.
- Enabling precise control and fast shutdown in an overcurrent scenario by high bandwidth and fast response current sensing.
- Safely and efficiently controlling and protecting the power switch [insulated-gate bipolar transistor/silicon carbide (IGBT/SiC)].

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8.3.1.3.1 System Block Diagram

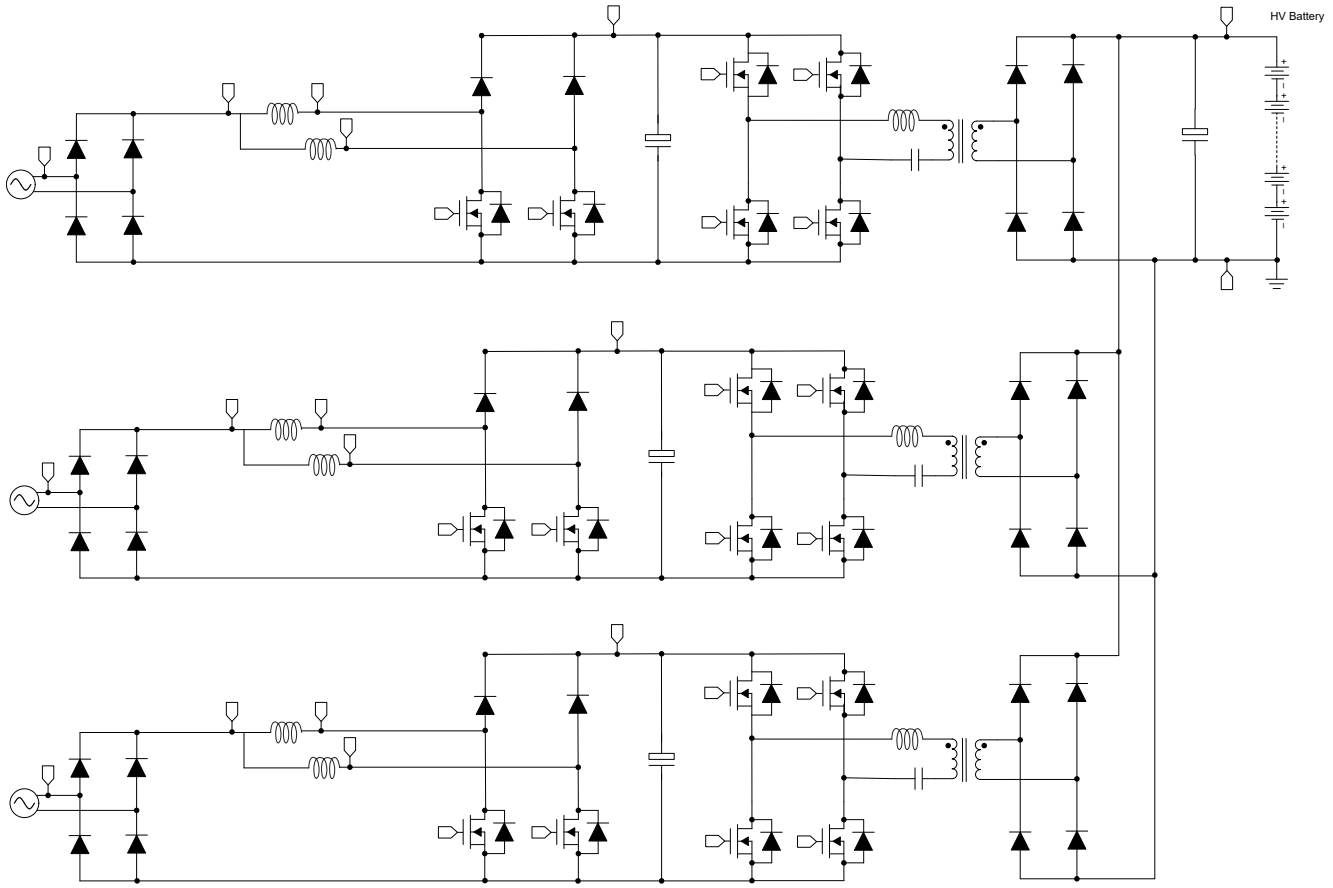


Figure 8-4. 11 kW Modular OBC Power Topology (Unidirectional, bridge PFC)

8.3.1.3.2 OBC Resources

Reference Designs and Associated Training Videos

C2000 Digital Power Training videos
This power topology is capable of bidirectional power flow (PFC and grid-tied inverter) and uses GaN devices, which enables higher efficiency and reduction in size of the power supply. The hardware and software available with this reference design accelerates time to market.

C2000™ MCUs - Electric vehicle (EV) training videos (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

PMP22650 GaN-based, 6.6-kW, bidirectional, onboard charger reference design
The PMP22650 reference design is a 6.6-kW, bidirectional, onboard charger. The design employs a two-phase totem pole PFC and a full-bridge CLLLC converter with synchronous rectification. The CLLLC utilizes both frequency and phase modulation to regulate the output across the required regulation range. The design uses a single processing core inside a TMS320F28388D microcontroller to control both the PFC and CLLLC. Synchronous rectification is implemented via the same microcontroller with Rogowski coil current sensors. High density is achieved through the use of high-speed GaN switches (LMG3522). The PFC is operating at 120 kHz and the CLLLC runs with a variable frequency from 200 kHz to 800 kHz. A peak system efficiency of 96.5% was achieved with an open-frame power density of 3.8 kW/L. While the design calculations were done for a 6.6-kW output power, the design represents a suitable starting point for a 7.x-kW (for example, 7.2-kW to 7.4-kW) rated OBC operating from a 240-V input with a 32-A breaker.

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TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger
The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

TIDUEG3A TIDM-1022 Valley switching boost power factor correction (PFC) reference design
This reference design illustrates a digital control method to significantly improve Boost Power Factor Correction (PFC) converter performance such as the efficiency and Total Harmonic Distortion (THD) under light load condition where efficiency and THD standards are difficult to meet. This is achieved using the integrated digital control feature of the C2000™ microcontroller (MCU). The design supports phase-shedding, valley-switching, valley-skipping, and Zero Voltage Switching (ZVS) for different load and instantaneous input voltage conditions. The software available with this reference design accelerates time to market.

8.3.1.4 EV Charging Station Power Module

The power module in a DC charging station consists of AC/DC power stage and DC/DC power stage. Each converter associated with its power stage comprises of power switches and gate driver, current and voltage sensing, and a real-time micro-controller. On the input side it has three-phase AC mains which are connected to the AC/DC power stage. This block converts the incoming AC voltage into a fixed DC voltage of around 800 V. This voltage serves as input to the DC/DC power stage which processes power and interfaces directly with the battery on the electric vehicle. Each power stage has a separate real-time micro-controller which is responsible for the processing of analog signals and providing fast control action.

The AC/DC stage (also known as the PFC stage) is the first level of power conversion in an EV charging station. It converts the incoming AC power from the grid (380–415 VAC) into a stable DC link voltage of around 800 V. The PFC stage maintains sinusoidal input currents, with typically a THD < 5%, and provides controlled DC output voltage higher than the amplitude of the line-to-line input voltage. The DC/DC stage is the second level of power conversion in an EV charging station. It converts the incoming DC link voltage of 800 V (in case of three-phase systems) to a lower DC voltage to charge the battery of an electric vehicle. The DC/DC converter must be capable of delivering rated power to the battery over a wide range with the capability of charging the battery at constant current or at constant voltage modes, depending on the State Of Charge (SOC) of the battery.

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8.3.1.4.1 System Block Diagram

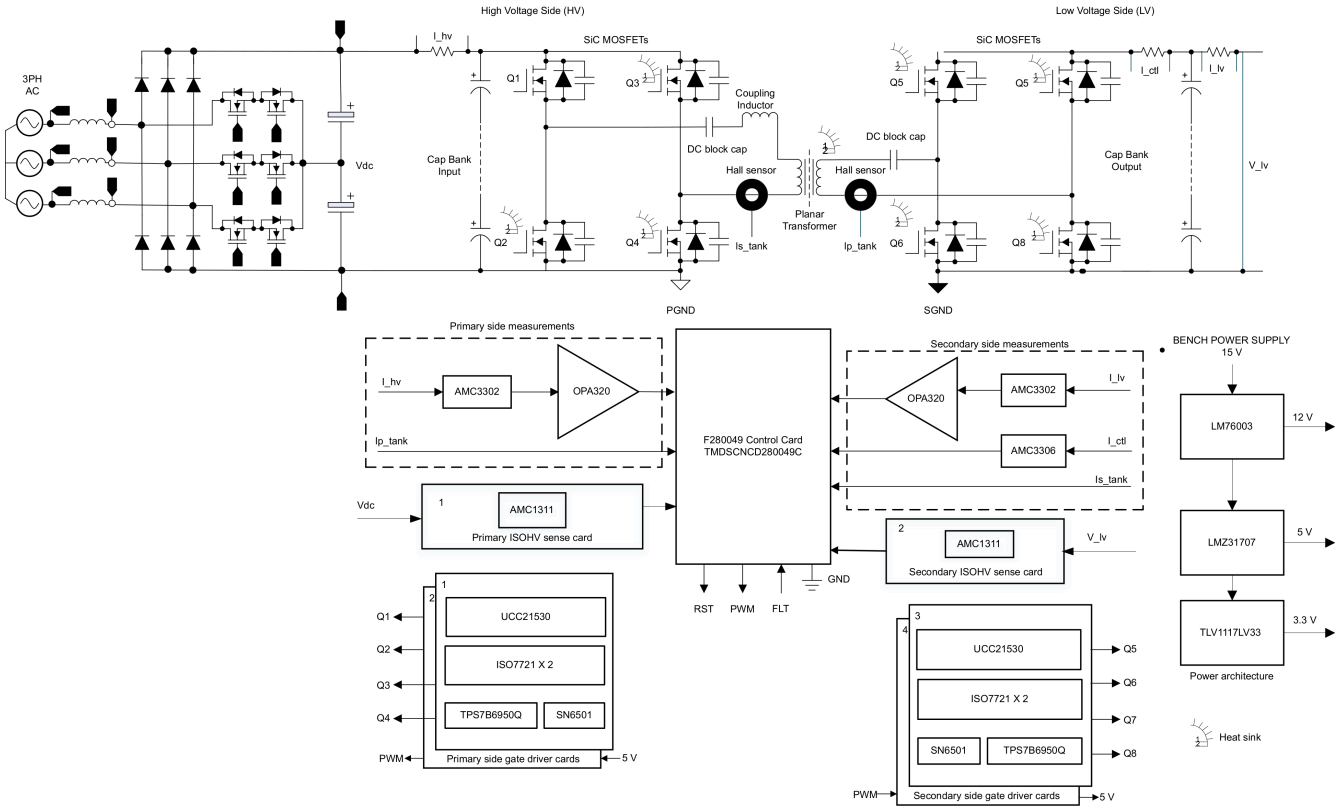


Figure 8-5. Dual-active-bridge DC/DC converter

8.3.1.4.2 EV Charging Station Power Module Resources

Reference Designs and Associated Training Videos

TIDM-02002 CLLLC resonant dual active bridge for HEV/EV onboard charger (Video)
The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

TIDA-01606 10-kW, bidirectional three-phase three-level (T-type) inverter and PFC reference design
This reference design provides an overview on how to implement a bidirectional three-level, three-phase, SiC-based active front end (AFE) inverter and PFC stage. The design uses a switching frequency of 50 kHz and a LCL output filter to reduce the size of the magnetics. A peak efficiency of 99% is achieved. The design shows how to implement a complete three phase AFE control in the DQ domain. The control and software is validated on the actual hardware and on hardware in the loop (HIL) setup.

TIDA-010210 11-kW, bidirectional, three-phase ANPC based on GaN reference design
This reference design provides a design template for implementing a three-level, three-phase, gallium nitride (GaN) based ANPC inverter power stage. The use of fast switching power devices makes it possible to switch at a higher frequency of 100 kHz, reducing the size of magnetics for the filter and increasing the power density of the power stage. The multilevel topology allows the use of 600-V rated power devices at higher DC bus voltages of up to 1000 V. The lower switching voltage stress reduces switching losses, resulting in a peak efficiency of 98.5%

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TIDA-010054 Bi-directional, dual active bridge reference design for level 3 electric vehicle charging stations
This reference design provides an overview on the implementation of a single-phase Dual Active Bridge (DAB) DC/DC converter. DAB topology offers advantages like soft-switching commutations, a decreased number of devices and high efficiency. The design is beneficial where power density, cost, weight, galvanic isolation, high-voltage conversion ratio, and reliability are critical factors, making it ideal for EV charging stations and energy storage applications. Modularity and symmetrical structure in the DAB allow for stacking converters to achieve high power throughput and facilitate a bidirectional mode of operation to support battery charging and discharging applications.

C2000™ MCUs - Electric vehicle (EV) training videos (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

Maximizing power for Level 3 EV charging stations
This explains how C2000's rich portfolio provide optimal solutions that help engineers solve design challenges and implement advanced power topologies.

Power Topology Considerations for Electric Vehicle Charging Stations Application Report
This Application Report discusses the topology consideration for designing power modules that acts as a building block for design of these fast DC Charging Station.

TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger
The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

TIDM-1000 Vienna Rectifier-Based Three Phase Power Factor Correction Reference Design Using C2000 MCU
The Vienna rectifier power topology is used in high-power, three-phase power factor correction applications such as off-board electric vehicle charging and telecom rectifiers. This design illustrates how to control a Vienna rectifier using a C2000 MCU.

8.3.1.5 High-Voltage Traction Inverter

The traction drive subsystem is designed to drive an AC induction motor or some combination of interior permanent magnet synchronous motor (IPMSM) and synchronous reluctance motor (SynRM). A high-bandwidth, field-oriented control (FOC) scheme with dynamic decoupling is implemented with a C2000 real-time control MCU together with field-weakening and over-modulation techniques to driver motor to industry-leading high speed up to 20,000 RPM, which can enable cost and weight reduction to the traction motor.

A traction drive system normally uses a variable reluctance (VR) resolver, which matches the pole count of the motor, to directly measure the electric angle of the rotor. Resolver-to-digital conversion (RDC) is required to measure position and speed using the resolver signal. RDC is traditionally handled by a separate IC, such as PGA411-Q1. With a C2000 MCU, RDC for a high-speed traction inverter can be integrated into the main control MCU, where the excitation generation can be handled with the DMA without CPU involvement, and feedback is read through the ADC and decoded with the CPU.

A Phase-Shifted Full Bride (PSFB) topology allows the switching devices to switch with zero-voltage switching (ZVS), resulting in lower switching losses and higher efficiency. Peak Current Mode Control (PCMC) is a highly desired control scheme for power converters because of its inherent voltage feed forward, automatic cycle-by-cycle current limiting, flux balancing, and other advantages, which require generating complex PWM drive waveforms along with fast and efficient control loop calculations. This is made possible on C2000 microcontrollers by advanced on-chip control peripherals like PWM modules, analog comparators with DAC and slope compensation hardware, and 12-bit high-speed ADCs coupled with an efficient 32-bit CPU.

Figure 8-6 shows a high-level block diagram of a single C2000™ real-time MCU controlling both an HEV/EV traction inverter and a bidirectional DC-DC converter.

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8.3.1.5.1 System Block Diagram

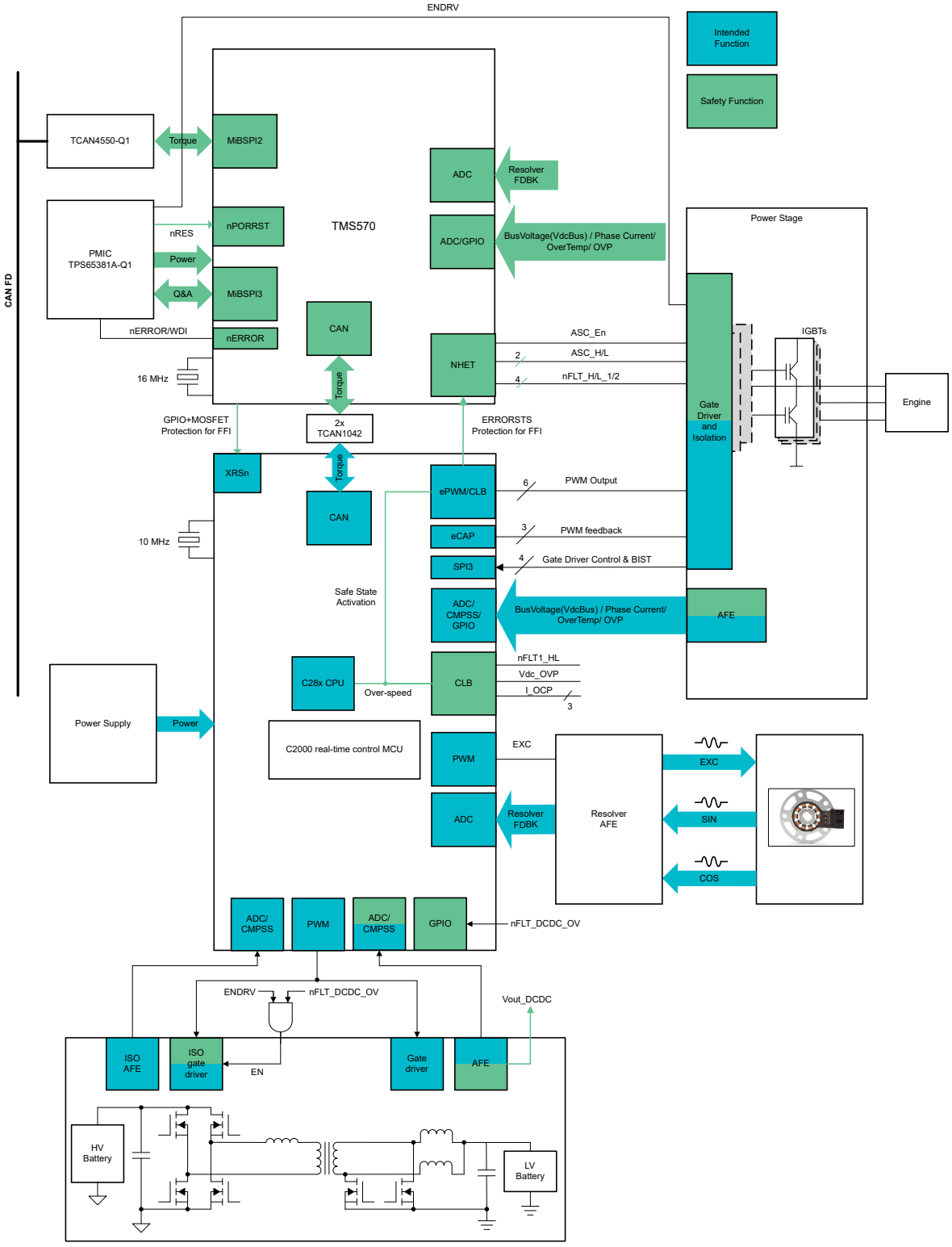


Figure 8-6. Traction Inverter High Voltage

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8.3.1.5.2 High-Voltage Traction Inverter Resources

Reference Designs and Associated Training Videos

TIDM-02009 ASIL D Safety Concept-Assessed High-Speed Traction, Bi-directional DC/DC Conversion Reference Design
This reference design demonstrates control of HEV/EV traction inverter and bi-directional DC-DC converter by a single TMS320F28388D real-time C2000™ MCU. The traction control uses a software-based resolver to digital converter (RDC) driving the motor to a high speed up to 20,000 RPM. The DC-DC converter uses peak current mode control (PCMC) technique with phase-shifted full-bridge (PSFB) topology and synchronous rectification (SR) scheme. The traction inverter stage uses silicon carbide (SiC) power stage, driven by UCC5870-Q1 smart gate driver. PCMC waveform is generated using state-of-the-art PWM module and built-in slope compensation in the comparator sub-system (CMPSS). An ASIL decomposition based functional safety concept for the system has been assessed with TÜV SÜD to demonstrate system level safety integrity level up to ISO 26262 ASIL D for representative safety goals.

C2000™ MCUs - Electric vehicle (EV) | TI.com Training Series (Video)
This collection of C2000™ MCU videos covers electric vehicle (EV)-specific training in both English and Chinese.

PSFB Control Using C2000 Microcontrollers Application Report
This application report presents the implementation details of a digitally controlled PSFB system implemented on the high voltage phase shifted full bridge (HVPSFB) kit from Texas Instruments. This kit converts a 400 V DC input to a regulated 12 V DC output and is rated for operations up to 600W. Both peak current mode control (PCMC) and voltage mode control (VMC) implementations are described.

***TIDA-BIDIR-400-12** Bidirectional DC-DC Converter*
This document presents the details of this microcontroller-based implementation of an isolated bidirectional DC-DC converter. A phase-shifted full-bridge (PSFB) with synchronous rectification controls power flow from a 400-V bus or battery to the 12-V battery in step-down mode, while a push-pull stage controls the reverse power flow from the low-voltage battery to the high-voltage bus or battery in boost mode. This design is rated for up to 300 W of output power in either mode.

TIDM-02014 High-power, high-performance automotive SiC traction inverter reference design
TIDM-02014 is a 800-V, 300kW SiC-based traction inverter system reference design developed by Texas Instruments and Wolfspeed provides a foundation for design engineers to create high-performance, high-efficiency traction inverter systems and get to market faster. This solution demonstrates how the traction inverter system technology from TI and Wolfspeed improves system efficiency by reducing the overshoot in available voltages with a high-performance isolated gate driver and real-time variable gate drive strength driving the Wolfspeed SiC power module. TI's high-control performance MCUs featuring tightly-integrated, innovative real-time peripherals enable effective traction motor control even at speeds greater than 20,000 RPM. Fast current loop implementation helps minimize motor torque ripple and provides smooth speed-torque profiles. The mechanical and thermal design of the system is provided by Wolfspeed.

8.3.1.6 Single-Phase Online UPS

Uninterruptible power supplies (UPS) play an important role in interfacing critical loads such as computers, communication systems, medical/life support systems, and industrial controls to the utility power grid. They are designed to provide clean and continuous power to the load under essentially any normal or abnormal utility power condition. Among the various UPS topologies or configurations, on-line UPS, also known as inverter-preferred UPS, offers the best line-conditioning performance and the most protection to the load against any utility power problems. It provides regulated sinusoidal output voltage under any input line condition. When powered from the utility power lines, it draws sinusoidal input current at a high input power factor. These improved input/output characteristics make on-line UPS the ideal solution in many applications.

A triple conversion on-line UPS system is shown in Figure 8-7. The power factor correction (PFC) input stage is an ac-to-dc converter, which rectifies the input Vac and creates the dc bus voltage while maintaining sinusoidal input current at a high input power factor. The PFC stage also regulates the dc bus voltage against variation in

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input Vac. The dc bus voltage is inverted through the output dc-to-ac inverter stage to generate the output Vac of appropriate frequency. A dc-to-dc buck converter stage implements the battery charger. The battery charger stage steps down the high dc bus voltage (up to 400 V) to allow a smaller battery to be charged. A dc-to-dc boost converter raises the battery voltage up to the bus voltage when the system is operating in battery backup mode.

8.3.1.6.1 System Block Diagram

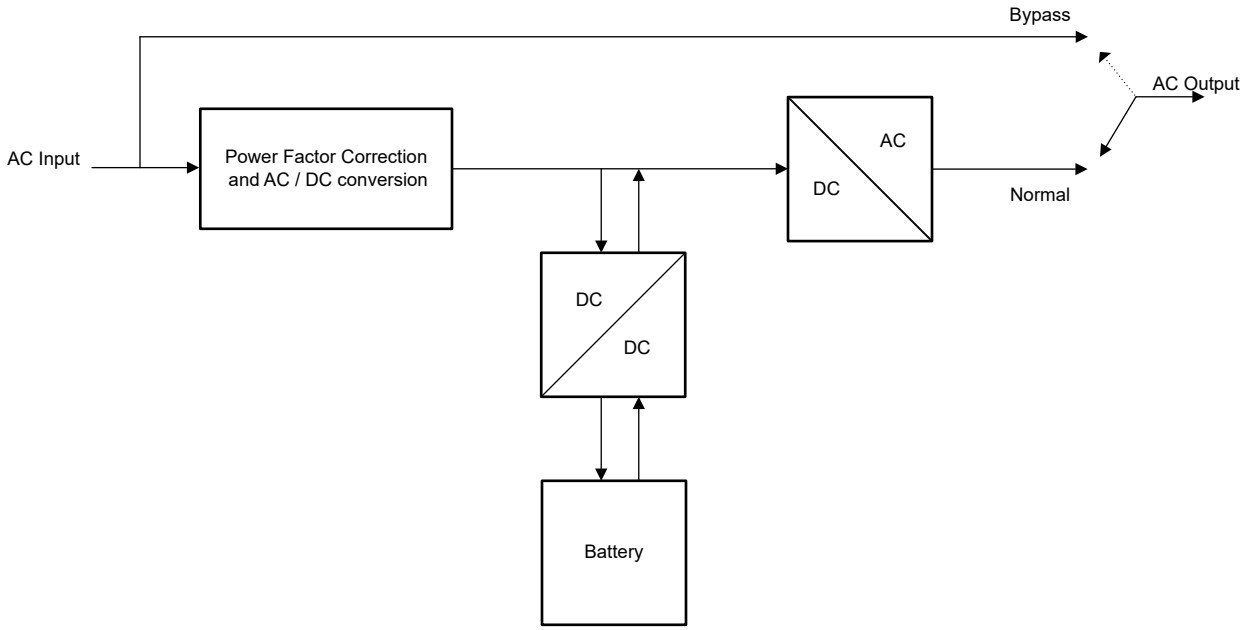


Figure 8-7. Triple Conversion Online UPS System

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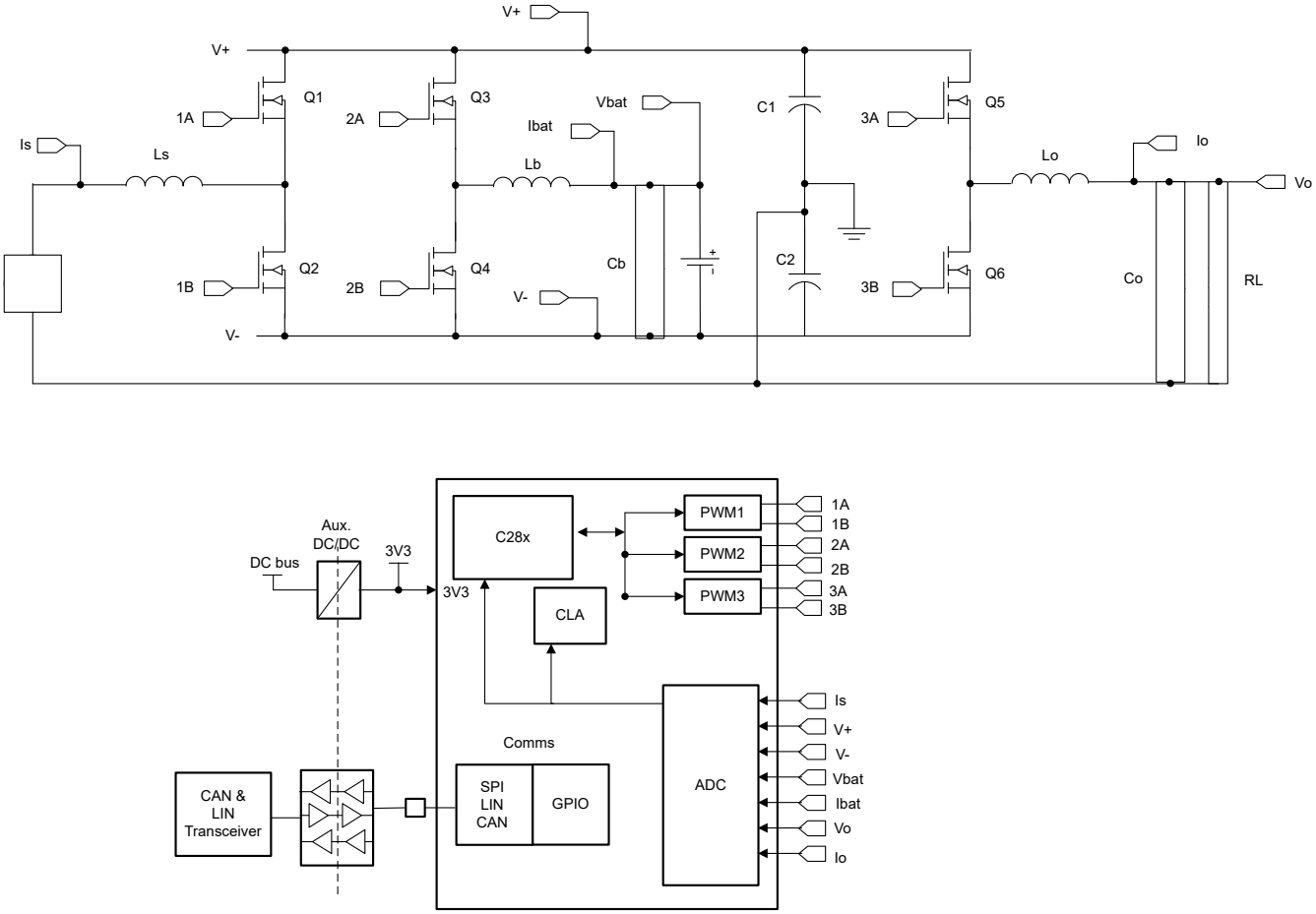


Figure 8-8. Single Phase Online UPS

8.3.1.6.2 Single-Phase Online UPS Resources

Reference Designs and Associated Training Videos

PMP23069 3.6-kW single-phase totem-pole bridgeless PFC reference design with a > 180-W/in³ power density
This reference design is a GaN-based 3.6-kW single-phase continuous conduction mode (CCM) totem-pole power factor correction (PFC) converter targeting maximum power density. The power stage is followed by a small boost converter, which helps to reduce the size of the bulk capacitor. The LMG3522 top-side cooled GaN with integrated driver and protection enables higher efficiency and reduces power supply size and complexity. The F28004x or F28002x C2000™ controller is used for all the advanced controls that includes fast relay control; baby boost operation during AC dropout event; reverse-current-flow protection; and communication between the PFC and the housekeeping controller. The PFC operates at a switching frequency of 65 kHz and achieves peak efficiency of 98.7%.

TIDM-HV-1PH-DCAC Single-Phase Inverter Reference Design With Voltage Source and Grid Connected Modes
This reference design implements single-phase inverter (DC-AC) control using the C2000™ F2837xD and F28004x microcontrollers. Design supports two modes of operation for the inverter. First is the voltage source mode using an output LC filter. This control mode is typically used in uninterruptible power supplies (UPS). Second is grid connected mode with an output LCL filter, which is typically used in solar inverters. Firmware for the design is supported under the powerSUITE framework which enables adaptation using the Solution Adapter and enables tuning of the control loop using the Compensation Designer and SFRA. High-efficiency, low THD and intuitive software make this design attractive for engineers working on inverter design for UPS and alternative energy applications such as PV inverters, grid storage and micro grids.

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TIDUEG2C TIDM-02002 Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger

The CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate your time to market.

TIDM-02008 Bidirectional high density GaN CCM totem pole PFC using C2000™ MCU

This reference design is a 3.-kW bidirectional interleaved continuous conduction mode (CCM) totem-pole (TTPL) bridgeless power factor correction (PFC) power stage using a C2000™ real-time controller and LMG3410R070 gallium nitride (GaN) with integrated driver and protection. This power topology is capable of bidirectional power flow (PFC and grid-tied inverter) and it uses LMG341x GaN devices, which enables higher efficiency and reduction in size of the power supply. The design supports phase shedding and adaptive dead time for efficiency improvements, input cap compensation scheme for improved power factor at light loads, and non-linear voltage loop to reduce voltage spikes under transient in PFC mode. The hardware and software available with this reference design accelerates time to market.

TIDUAI7 TIDM-BIDIR-400-12: Bidirectional 400-V/12-V DC/DC Converter Reference Design

The Bidirectional 400V-12V DC/DC Converter Reference Design is a microcontroller-based implementation of an isolated bidirectional DC-DC converter. A phase-shifted full-bridge (PSFB) with synchronous rectification controls power flow from a 400-V bus/battery to the 12-V battery in step-down mode, while a push-pull stage controls the reverse power flow from the low-voltage battery to the high-voltage bus/battery in boost mode. In this implementation, closed-loop control for both directions of power flow is implemented using a Texas Instruments TMS320F28035 32-bit microcontroller, which is placed on the LV side. This digital controller system can implement advanced control strategies to optimally control the power stage under different conditions and also provide system-level intelligence to make safe and seamless transitions between operation modes and PWM switching patterns.

TIDU638 TIDM-BUCKBOOST-BIDIR Bi-Directional Non-Isolated Buck Boost Converter

This design implements a bi-directional, non-isolated buck boost power converter, ideal for solar microconverters, hybrid electric vehicles (HEV) including Regeneration (Regen or Recuperation), and battery charging applications.

Variable-frequency, ZVS, 5-kW, GaN-based, two-phase totem-pole PFC reference design

This reference design is a high-density and high-efficiency 5-kW totem-pole power factor correction (PFC) design. The design uses a two-phase totem-pole PFC operating with variable frequency and zero voltage switching (ZVS). The control uses a new topology and improved triangular current mode (iTCM) to achieve both small size and high efficiency. The design uses a high performance processing core inside a TMS320F280049C microcontroller to maintain efficiency over a wide operating range. The PFC operates with variable frequency between 100 kHz and 800 kHz. A peak system efficiency of 99% was achieved with an open-frame power density of 120 W/in3.

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9 Device and Documentation Support

9.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320 MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F28075). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

TMX	Experimental device that is not necessarily representative of the final device's electrical specifications
TMP	Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
TMS	Fully qualified production device

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing
TMDS	Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer: "Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PTP) and temperature range (for example, T). Figure 9-1 provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F2807x Real-Time MCUs Silicon Errata*.

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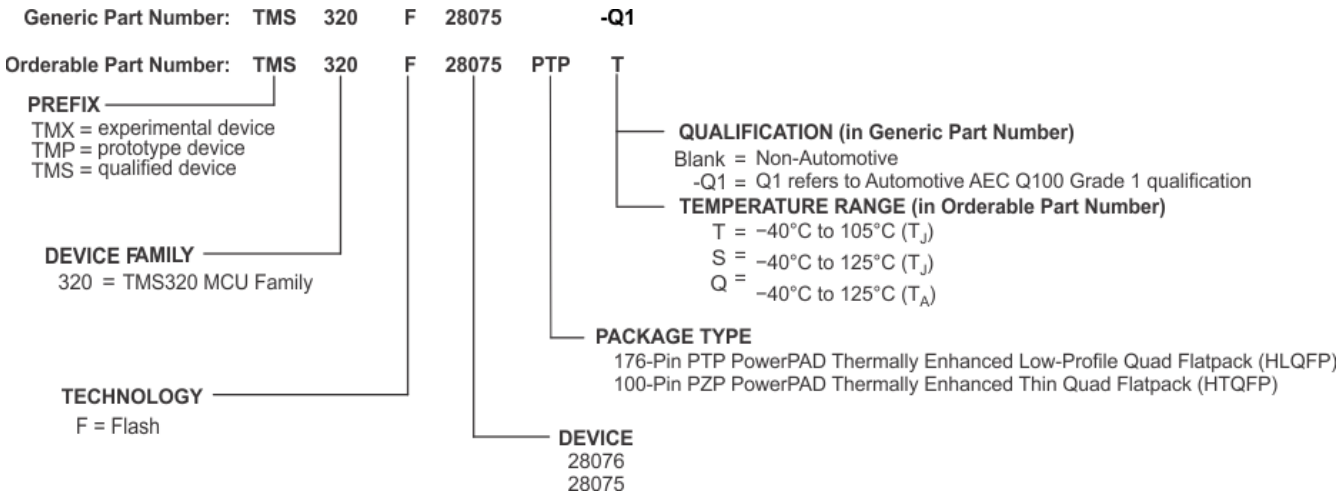


Figure 9-1. Device Nomenclature

9.2 Markings

Figure 9-2 provides an example of the 2807x device markings and defines each of the markings. The device revision can be determined by the symbols marked on the top of the package as shown in Figure 9-2. Some prototype devices may have markings different from those illustrated.

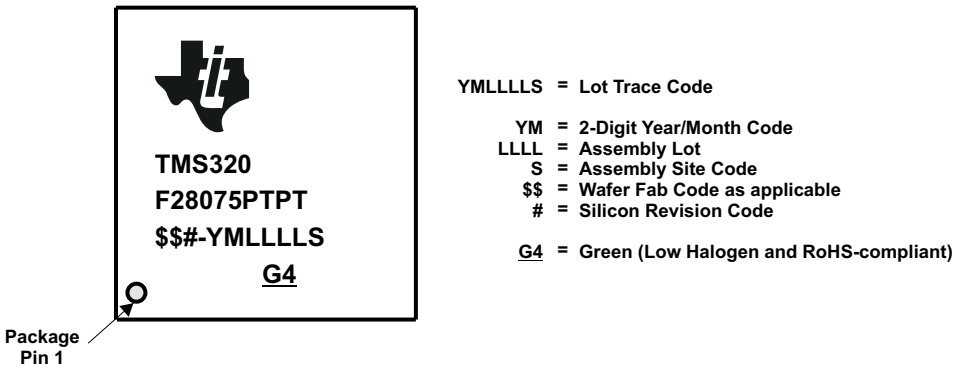


Figure 9-2. Example of Device Markings

Table 9-1. Determining Silicon Revision From Lot Trace Code

SILICON REVISION CODE	SILICON REVISION	REVID(1) Address: 0x5D00C	COMMENTS
B	B	0x0002	This silicon revision is available as TMX.
C	C	0x0003	This silicon revision is available as TMS.

(1) Silicon Revision ID

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9.3 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time control MCUs – Design & development page.

Development Tools

F28379D controlCARD for C2000 Real time control development kits
The F28379D controlCARD from Texas Instruments is Position Manager-ready and an ideal product for initial software development and short run builds for system prototypes, test stands, and many other projects that require easy access to high-performance controllers. All C2000 controlCARDs are complete board-level modules that utilize a HSEC180 or DIMM100 form factor to provide a low-profile single-board controller solution. The host system needs to provide only a single 5V power rail to the controlCARD for it to be fully functional.

F28379D Experimenter Kit
C2000™ MCU Experimenter Kits provide a robust hardware prototyping platform for real-time, closed loop control development with Texas Instruments C2000 32-bit microcontroller family. This platform is a great tool to customize and prove-out solutions for many common power electronics applications, including motor control, digital power supplies, solar inverters, digital LED lighting, precision sensing, and more.

Software Tools

C2000Ware for C2000 MCUs
C2000Ware for C2000 microcontrollers is a cohesive set of development software and documentation designed to minimize software development time. From device-specific drivers and libraries to device peripheral examples, C2000Ware provides a solid foundation to begin development and evaluation. C2000Ware is now the recommended content delivery tool versus controlSUITE™.

Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for C2000 Microcontrollers
Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

Pin Mux Tool
The Pin Mux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs.

F021 Flash Application Programming Interface (API)
The F021 Flash Application Programming Interface (API) provides a software library of functions to program, erase, and verify F021 on-chip Flash memory.

UniFlash Standalone Flash Tool
UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

C2000 Third-party search tool
TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

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Models

Various models are available for download from the product Tools & Software pages. These include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Models section of the Tools & Software page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000™ real-time microcontrollers design & development – Educational resources site.

Specific F2837xD/F2837xS/F2807x hands-on training resources can be found within the C2000 Academy on TI Resource Explorer.

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9.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

Errata

TMS320F2807x Real-Time MCUs Silicon Errata describes known advisories on silicon and provides workarounds.

Technical Reference Manual

TMS320F2807x Real-Time Microcontrollers Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the 2807x microcontrollers.

CPU User's Guides

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

TMS320C28x Extended Instruction Sets Technical Reference Manual describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

C2000 Real-Time Control Peripherals Reference Guide describes the peripheral reference guides of the 28x DSPs.

Tools Guides

TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures and future trends.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

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9.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.6 Trademarks

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MathWorks®, Simulink®, Embedded Coder®, and Polyspace® are registered trademarks of The MathWorks, Inc.
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9.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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10 Revision History

Changes from January 16, 2021 to February 21, 2024 (from Revision J (January 2021) to Revision K (February 2024)) **Page**

- Changed document title from *TMS320F2807x Microcontrollers* to *TMS320F2807x Real-Time Microcontrollers*... 1
- **Global:** Changed the title of the errata from *TMS320F2807x MCUs Silicon Errata* to *TMS320F2807x Real-Time MCUs Silicon Errata*. Changed the title of the Technical Reference Manual from *TMS320F2807x Microcontrollers Technical Reference Manual* to *TMS320F2807x Real-Time Microcontrollers Technical Reference Manual*... 1
- *Description* section: Updated section... 2
- *Package Information* table: Changed title of *Device Information* table to *Package Information*. Updated table and footnotes... 2
- *Device Comparison* table: Updated Serial Communications Interface (SCI) – Type 0 with (UART Compatible)... 6
- *Device Comparison* table: Updated part numbers... 6
- *Pin Configuration and Functions* section: Changed section title from *Terminal Configuration and Functions* to *Pin Configuration and Functions*... 8
- *Signal Descriptions* table: Updated **DESCRIPTION** column of $\overline{\text{TRST}}$, VREGENZ, and VDD. Updated **PTP PIN NO.** column and **PZP PIN NO.** column of VSS... 11
- *Input X-BAR* figure: Updated figure... 31
- *ESD Ratings – Commercial* table: Updated part numbers... 36
- *Device Current Consumption at 120-MHz SYSCLK* table: Added values for RESET MODE... 37
- *Electrical Characteristics* table: Moved parametric value of $V_{HYSTERESIS}$ (150 mV) from TYP column to MIN column... 43
- *Internal 1.2-V VREG* section: Updated section... 46
- *Power-on Reset* figure: Updated figure... 48
- *Clocking System* figure: Updated figure... 50
- *XTAL Oscillator Characteristics* section: Added section... 52
- *XTAL Oscillator* section: Changed section title from *Crystal Oscillator* to *XTAL Oscillator*. Updated section... 54
- *Crystal Oscillator Electrical Characteristics* table: Updated table... 59
- *Negative Resistance Variation at 10 MHz* figure: Added figure... 59
- *Negative Resistance Variation at 20 MHz* figure: Added figure... 59
- *Flash Parameters* table: Updated table... 62
- *RAM Specifications* section: Added section... 63
- *ROM Specifications* section: Added section... 63
- *EMIF Asynchronous Memory Switching Characteristics* table: Updated Parameters 3, 10, 15, and 24. Added "Maximum wait time-out condition" footnote... 82
- *ADC Characteristics* table: Updated TYP values of SNR, THD, SFDR, SINAD, and ENOB... 95
- *Single-Ended Input Model Parameters* section: Updated "This input model should be used along with actual signal source impedance ..." paragraph... 97
- *ADC Timings for 12-Bit Mode* figure: Updated figure... 100
- *Comparator Electrical Characteristics* table: Added MIN and MAX Hysteresis values. Added Power Supply Rejection Ratio (PSRR)... 105
- *CMPSS DAC Static Electrical Characteristics* section: Added "Figures not drawn to scale" Note. ... 106
- *CMPSS DAC Dynamic Error* section: Added section... 113
- *Synchronization Chain Architecture* figure: Updated figure... 120
- *SDFM Timing Requirements When Using Asynchronous GPIO (ASYNC) Option* section: Updated WARNING about SDFM Manchester Mode (Mode 2)... 129
- *I2C Electrical Data and Timing* section: Added "To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz ..." Note. ... 138
- *I2C Timing Requirements* table: Added footnote. ... 138

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- *I2C Timing Diagram* section: Added section title. 139
- *I2C Timing Diagram* section: Removed duplicate "To meet all of the I2C protocol timing specifications, the I2C module clock (Fmod) must be configured from 7 MHz to 12 MHz." Note. This Note is now in the *I2C Electrical Data and Timing* section..... 139
- *Overview* section: Updated section..... 162
- *Peripheral Registers Memory Map* section: Added "None of the device peripherals have program bus access" Note..... 166
- *Peripheral Registers Memory Map* table: Added CLB registers..... 166
- *Applications, Implementation, and Layout* section: Updated section..... 187
- *Tools and Software* section: Added C2000 Third-party search tool. Updated Training section..... 207

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11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

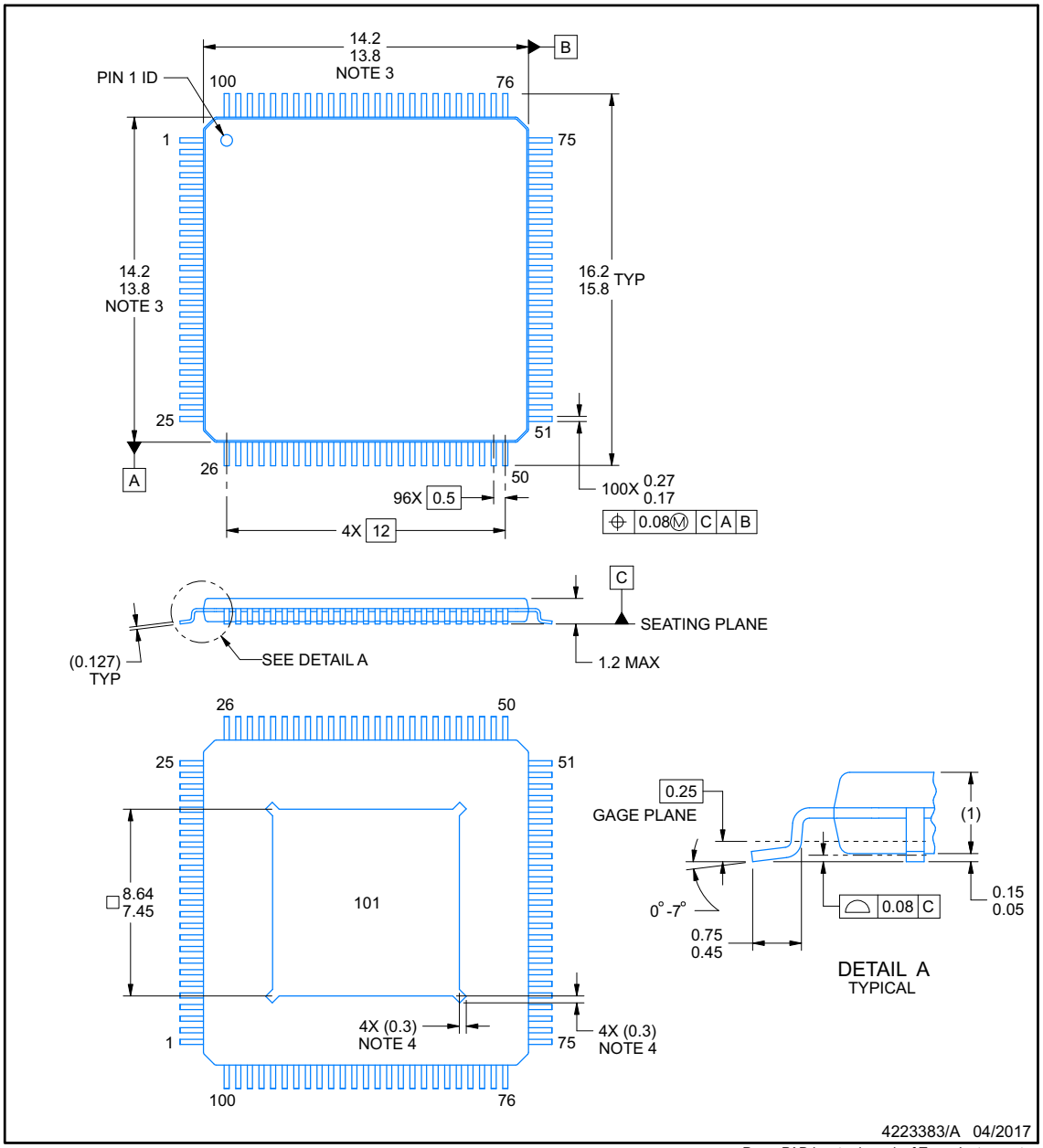
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PACKAGE OUTLINE

PZP0100N

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

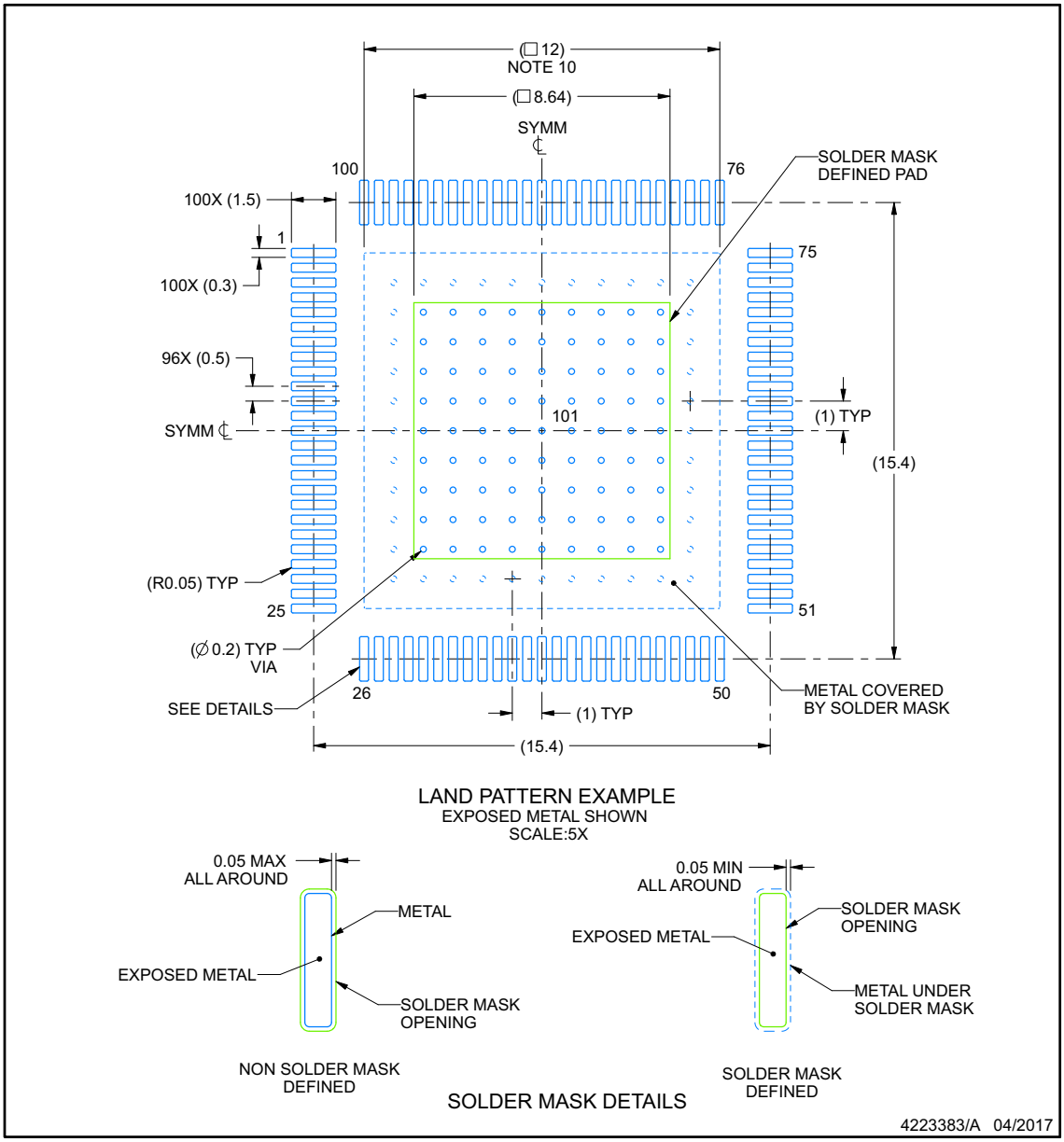
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EXAMPLE BOARD LAYOUT

PZP0100N

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

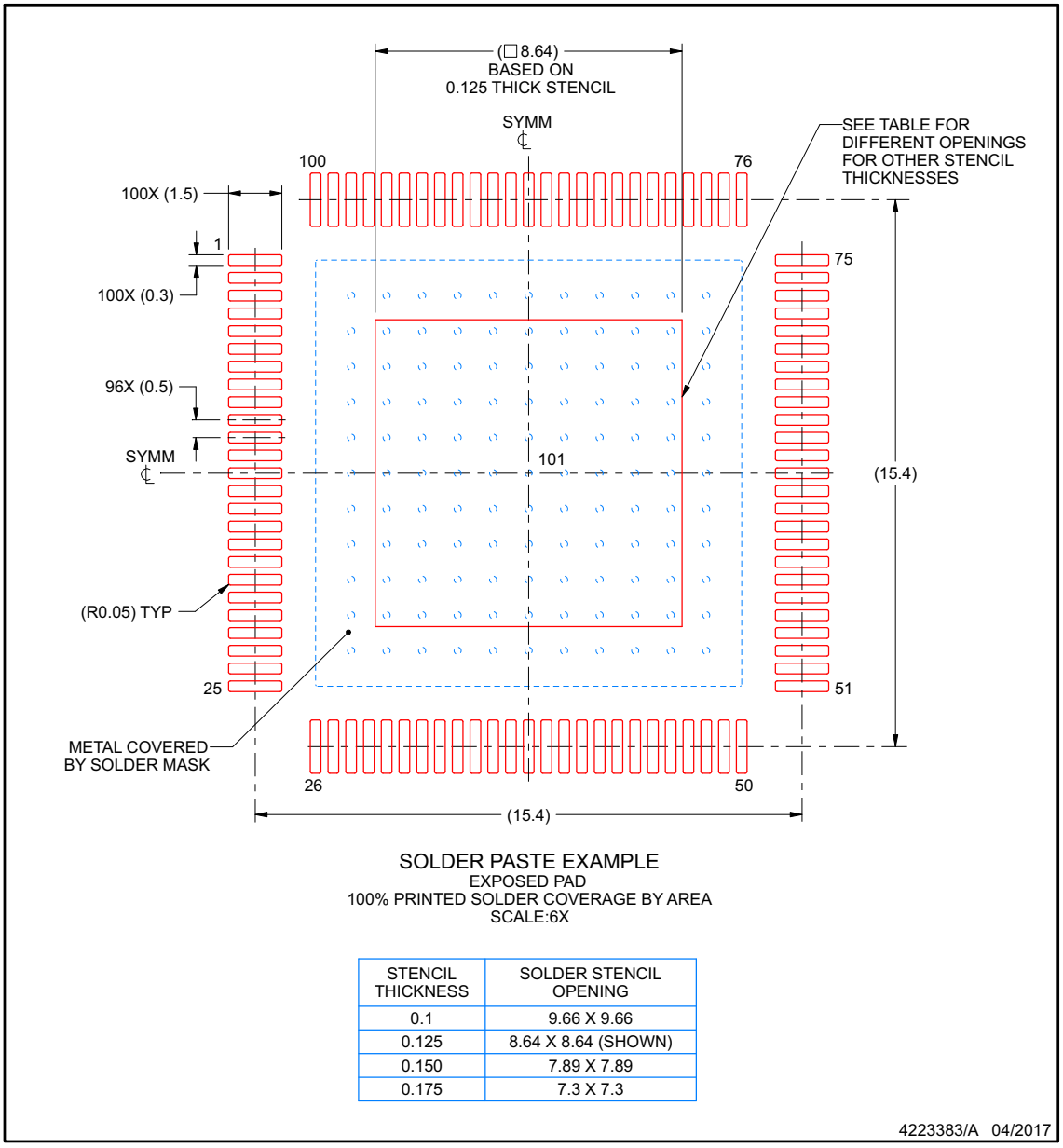
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

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EXAMPLE STENCIL DESIGN

PZP0100N — **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	9.66 X 9.66
0.125	8.64 X 8.64 (SHOWN)
0.150	7.89 X 7.89
0.175	7.3 X 7.3

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

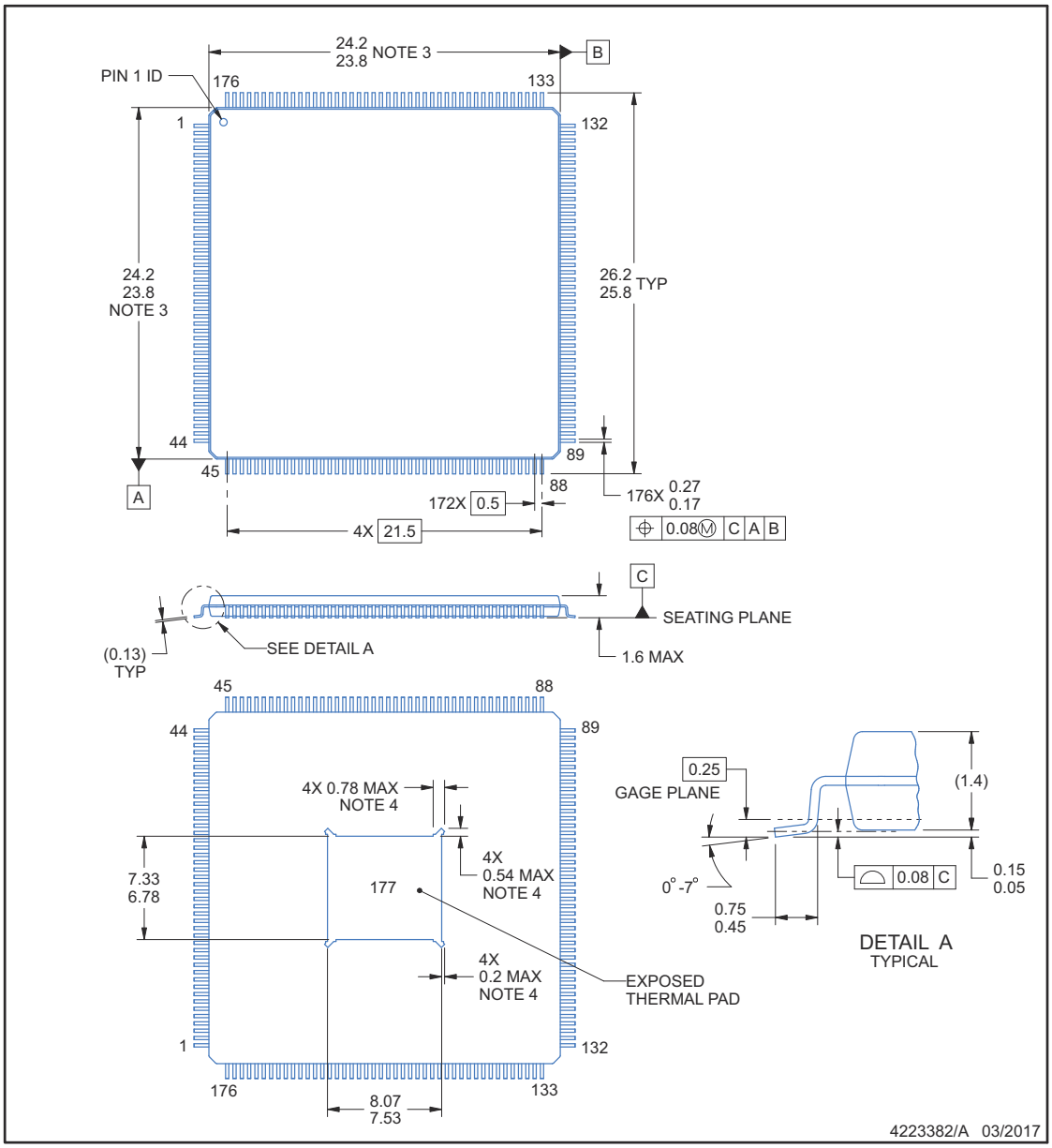
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PACKAGE OUTLINE

PTP0176F

PowerPAD™ HLQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features my not present.
5. Reference JEDEC registration MS-026.

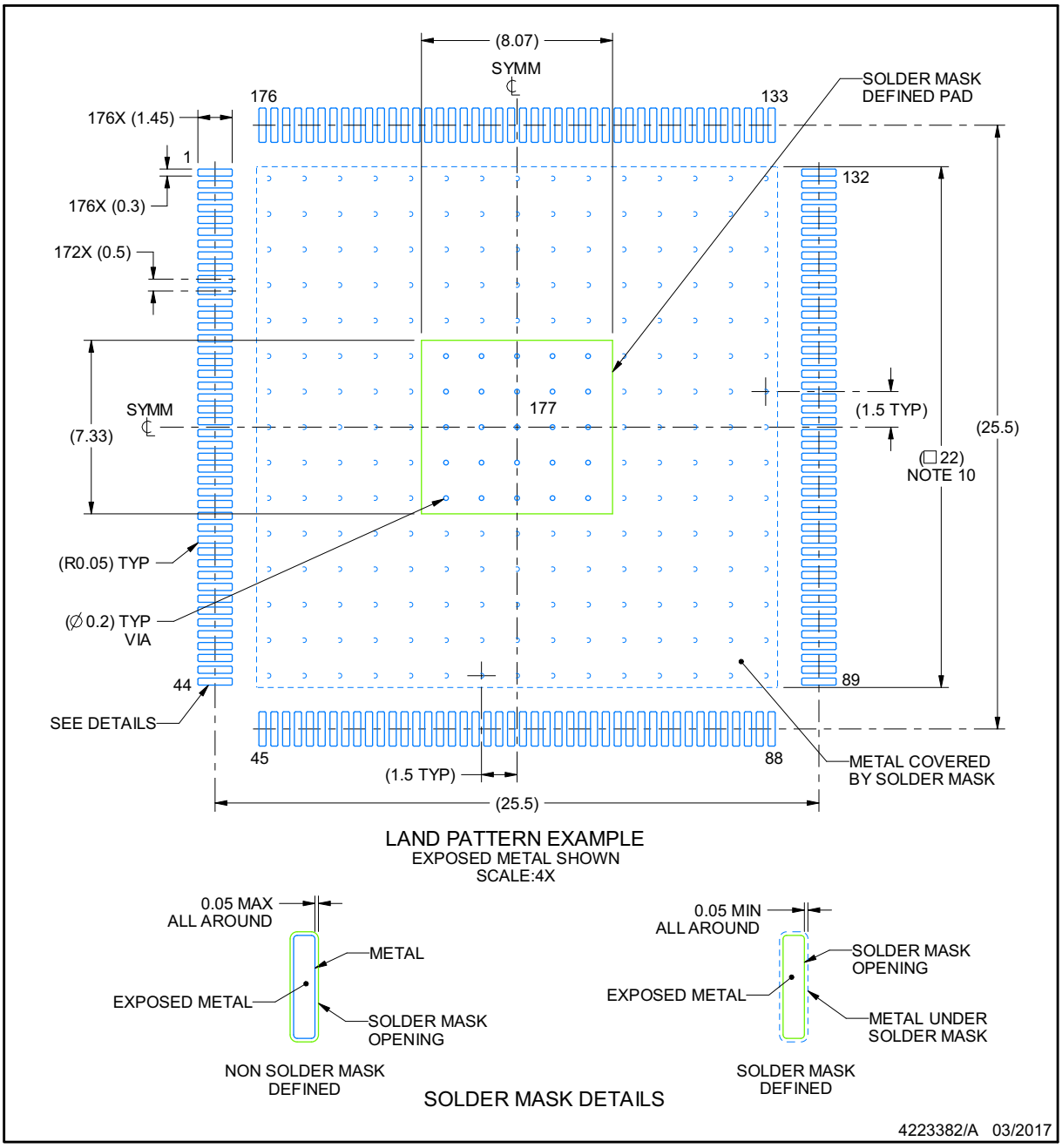
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EXAMPLE BOARD LAYOUT

PTP0176F

PowerPAD™ HLQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

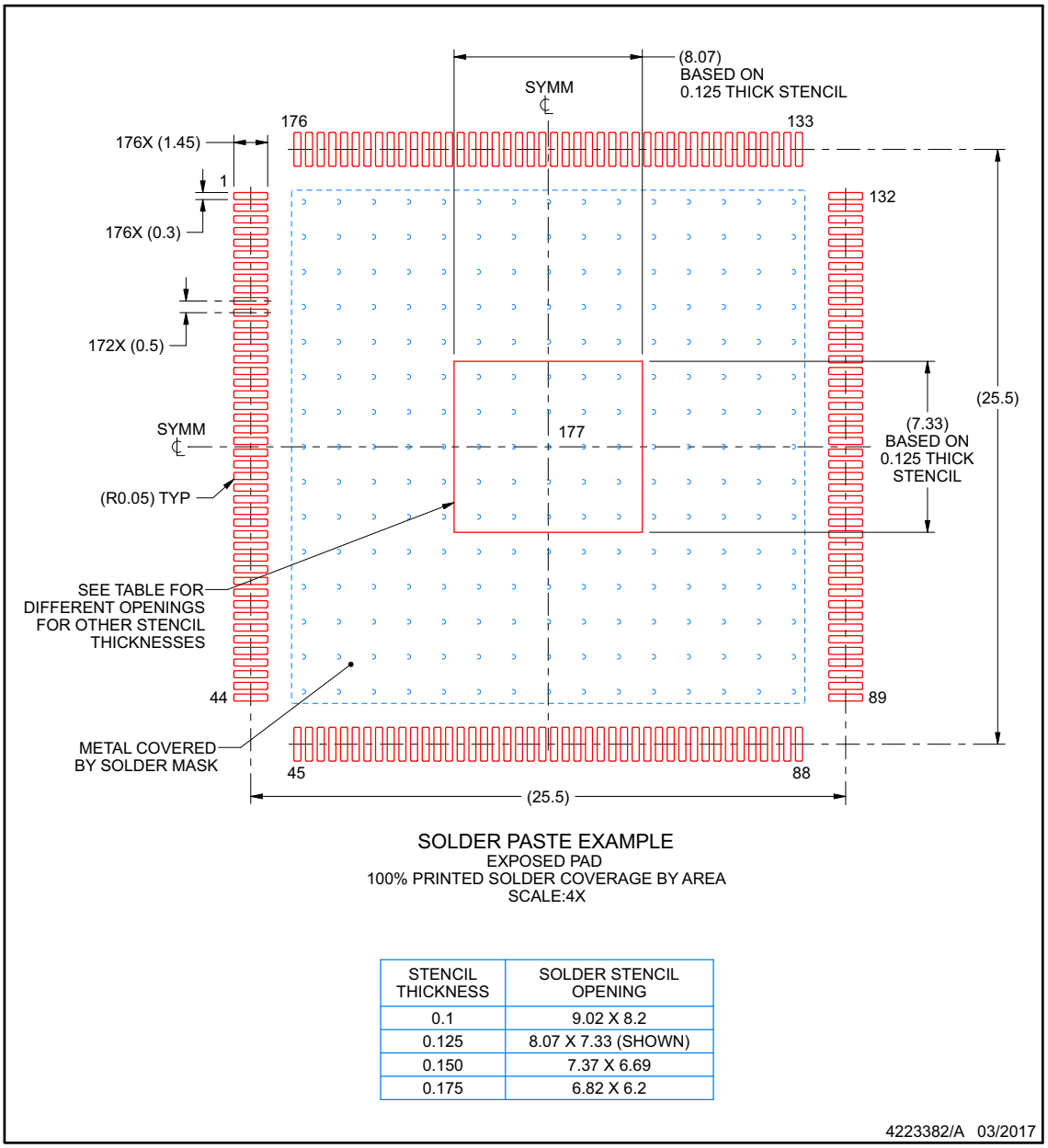
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

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EXAMPLE STENCIL DESIGN

PTP0176F — **PowerPAD™ HLQFP - 1.6 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:4X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	9.02 X 8.2
0.125	8.07 X 7.33 (SHOWN)
0.150	7.37 X 6.69
0.175	6.82 X 6.2

4223382/A 03/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS320F28075PTPQ	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPQ
TMS320F28075PTPQ.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPQ
TMS320F28075PTPQ.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPQ
TMS320F28075PTPQR	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPQ
TMS320F28075PTPQR.A	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPQ
TMS320F28075PTPQR.B	Active	Production	HLQFP (PTP) | 176	200 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPQ
TMS320F28075PTPS	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPS
TMS320F28075PTPS.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPS
TMS320F28075PTPS.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPS
TMS320F28075PTPT	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TMS320 F28075PTPT
TMS320F28075PTPT.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPT
TMS320F28075PTPT.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PTPT
TMS320F28075PZPQ	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PZPQ
TMS320F28075PZPQ.A	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PZPQ
TMS320F28075PZPQ.B	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PZPQ
TMS320F28075PZPS	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PZPS

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS320F28075PZPS.A	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PZPS
TMS320F28075PZPS.B	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PZPS
TMS320F28075PZPT	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	TMS320 F28075PZPT
TMS320F28075PZPT.A	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PZPT
TMS320F28075PZPT.B	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28075PZPT
TMS320F28076PTPS	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28076PTPS
TMS320F28076PTPS.A	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28076PTPS
TMS320F28076PTPS.B	Active	Production	HLQFP (PTP) | 176	40 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28076PTPS
TMS320F28076PZPS	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28076PZPS
TMS320F28076PZPS.A	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28076PZPS
TMS320F28076PZPS.B	Active	Production	HTQFP (PZP) | 100	90 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TMS320 F28076PZPS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TMS320F28075, TMS320F28075-Q1 :

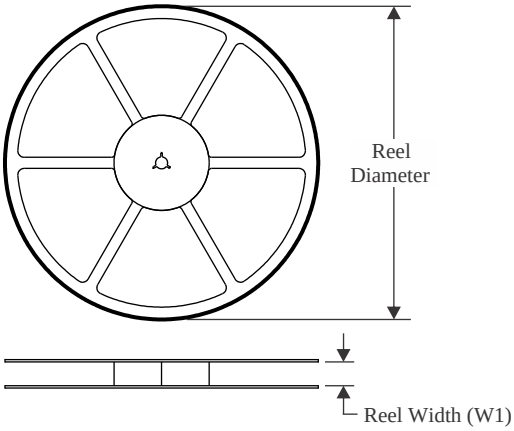
- Catalog : TMS320F28075
- Automotive : TMS320F28075-Q1

NOTE: Qualified Version Definitions:

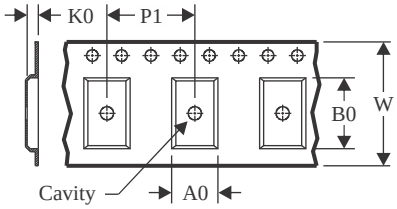
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

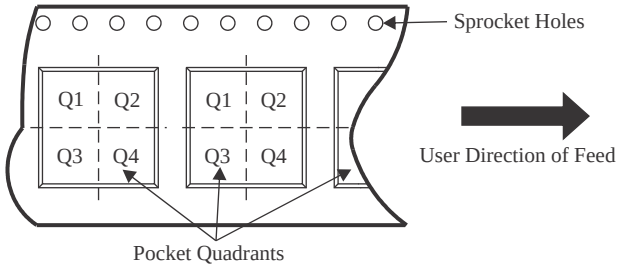


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

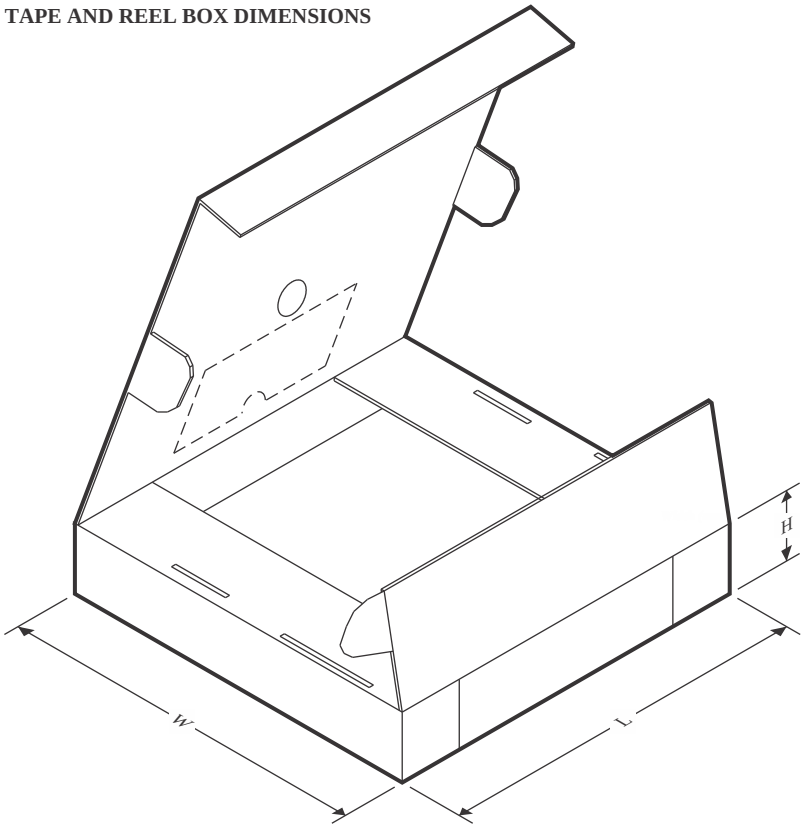
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMS320F28075PTPQR	HLQFP	PTP	176	200	330.0	44.4	26.6	26.6	2.2	36.0	44.0	Q2

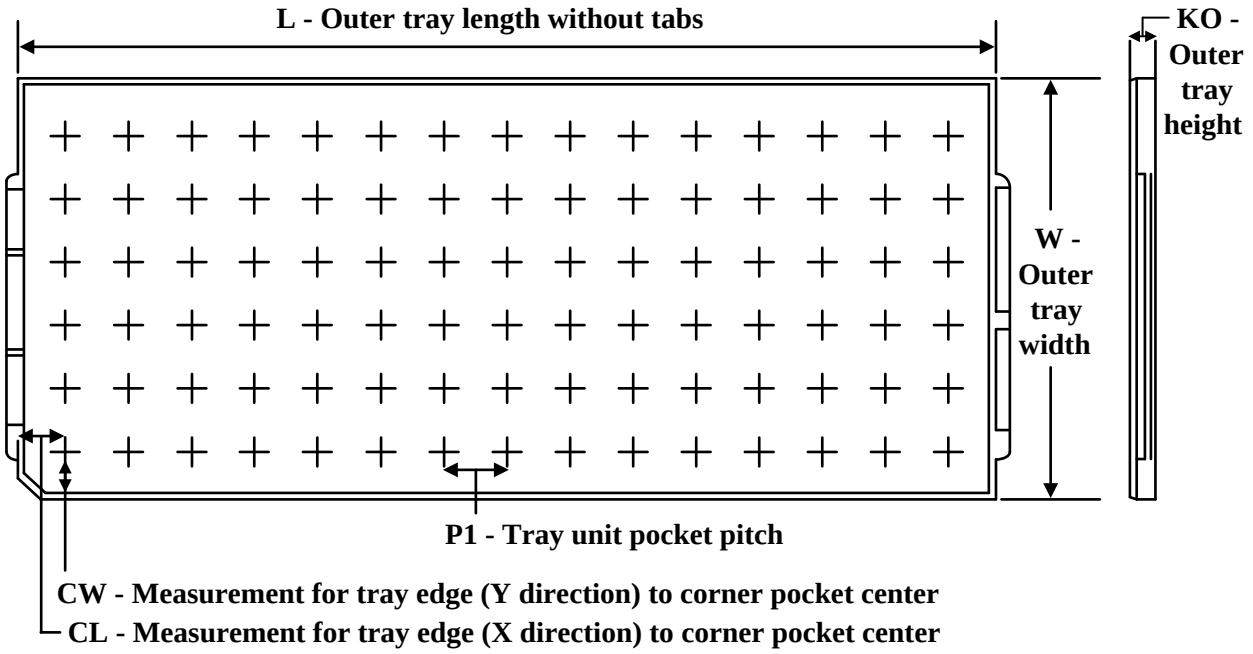
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMS320F28075PTPQR	HLQFP	PTP	176	200	367.0	367.0	67.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320F28075PTPQ	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PTPQ.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PTPQ.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PTPS	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PTPS.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PTPS.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PTPT	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PTPT.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PTPT.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28075PZPQ	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28075PZPQ.A	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28075PZPQ.B	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28075PZPS	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28075PZPS.A	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28075PZPS.B	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28075PZPT	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28075PZPT.A	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320F28075PZPT.B	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28076PTPS	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28076PTPS.A	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28076PTPS.B	PTP	HLQFP	176	40	4x10	150	315	135.9	7620	20.7	30.4	20.7
TMS320F28076PZPS	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28076PZPS.A	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28076PZPS.B	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21

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