TPA3112D1-Q1 25-W Filter-Free Mono Class-D Audio Power Amplifier With SpeakerGuard™

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C2
- 25-W into an 8-Ω Load at < 0.1% THD+N From a 24-V Supply
- 20-W into an 4-Ω Load at 10% THD+N From a 12-V Supply
- 94% Efficient Class-D Operation into 8-Ω Load Eliminates Need for Heat Sinks
- Wide Supply Voltage Range Allows Operation from 8 to 26 V
- Filter-Free Operation
- SpeakerGuard Protection Circuitry Includes Adjustable Power Limiter Plus DC Protection
- Flow Through Pin Out Facilitates Easy Board Layout
- Robust Pin-to-Pin Short Circuit Protection and Thermal Protection with Auto-Recovery Option
- Excellent THD+N and Pop Free Performance
- Four Selectable, Fixed Gain Settings
- Differential Inputs

2 Applications

- Automotive Noise Generation for HEV/EV
- Automotive Emergency Call Systems (eCall)
- Automotive Infotainment Systems (i.e. Head Unit, Connectivity Gateway, Cluster, Telematics, Navigation)
- ADAS Noise Generation for Blind Spot Detection, Security and Alarm Systems
- Professional Audio Equipment (i.e. PA Speakers, Studio Headphones, Performance Amplifiers, Premium Microphones)
- Aerospace and Aviation Audio Systems

3 Description

The TPA3112D1-Q1 is a 25-W efficient, Class-D audio power amplifier for driving a bridge tied speaker. Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ protection circuitry system includes an adjustable power limiter and a DC detection circuit. The adjustable power limiter allows the user to set a virtual voltage rail lower than the chip supply to limit the amount of current through the speaker. The DC detect circuit measures the frequency and amplitude of the PWM signal and shuts off the output stage if the input capacitors are damaged or shorts exist on the inputs.

The TPA3112D1-Q1 can drive a mono speaker as low as 4 Ω. The high efficiency of the device, > 90%, eliminates the need for an external heat sink when playing music.

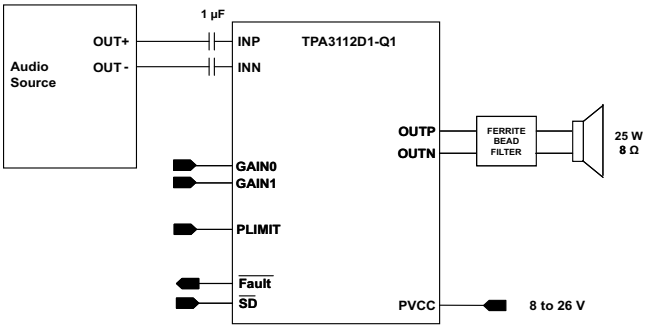
The outputs are fully protected against shorts to GND, V_{CC}, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA3112D1-Q1	HTSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 DC Characteristics ... 5
6.6 DC Characteristics ... 5
6.7 AC Characteristics ... 6
6.8 AC Characteristics ... 6
6.9 Typical Characteristics ... 7
7 Detailed Description ... 10
7.1 Overview ... 10
7.2 Functional Block Diagram ... 11
7.3 Feature Description ... 11
7.4 Device Functional Modes ... 12
8 Application and Implementation ... 15
8.1 Application Information ... 15
8.2 Typical Application ... 15
9 Power Supply Recommendations ... 21
10 Layout ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 23
11 Device and Documentation Support ... 24
11.1 Device Support ... 24
11.2 Documentation Support ... 24
11.3 Community Resources ... 24
11.4 Trademarks ... 24
11.5 Electrostatic Discharge Caution ... 24
11.6 Glossary ... 24
12 Mechanical, Packaging, and Orderable Information ... 24

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2012) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

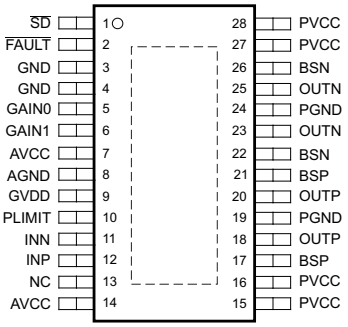
Changes from Original (September 2012) to Revision A **Page**

- Changed AEC-Q100-003 to per JESD22-A115 in Abs Max table. ... 4
- Changed conditition statement for DC and AC characteristics sections from T_A from 25°C to –40°C to 125°C ... 5

Copyright © 2012–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP With PowerPAD™ IC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{SD}$	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
2	$\overline{FAULT}$	O	Open drain output used to display short circuit or DC detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise both the short circuit faults and DC detect faults must be reset by cycling PVCC.
3	GND	—	Connect to local ground.
4	GND	—	Connect to local ground.
5	GAIN0	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
6	GAIN1	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
7	AVCC	P	Analog supply
8	AGND	—	Analog supply ground. Connect to the thermal pad.
9	GVDD	O	High-side FET gate drive supply. Nominal voltage is 7 V. May also be used as supply for PLIMIT divider. Add a 1-μF cap to ground at this pin.
10	PLIMIT	I	Power limit level adjust. Connect directly to GVDD pin for no power limiting. Add a 1-μF cap to ground at this pin.
11	INN	I	Negative audio input. Biased at 3 V.
12	INP	I	Positive audio input. Biased at 3 V.
13	NC	—	Not connected
14	AVCC	P	Connect AVCC supply to this pin.
15	PVCC	P	Power supply for H-bridge. PVCC pins are also connected internally.
16	PVCC	P	Power supply for H-bridge. PVCC pins are also connected internally.
17	BSP	I	Bootstrap I/O for positive high-side FET.
18	OUTP	O	Class-D H-bridge positive output.
19	PGND	—	Power ground for the H-bridges.
20	OUTP	O	Class-D H-bridge positive output.
21	BSP	I	Bootstrap I/O for positive high-side FET.
22	BSN	I	Bootstrap I/O for negative high-side FET.
23	OUTN	O	Class-D H-bridge negative output.
24	PGND	—	Power ground for the H-bridges.
25	OUTN	O	Class-D H-bridge negative output.
26	BSN	I	Bootstrap I/O for negative high-side FET.
27	PVCC	P	Power supply for H-bridge. PVCC pins are also connected internally.
28	PVCC	P	Power supply for H-bridge. PVCC pins are also connected internally.

Copyright © 2012–2015, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	AVCC, PVCC	–0.3	30	V
V_I	Interface pin voltage	$\overline{SD}$, $\overline{FAULT}$,GAIN0, GAIN1, AVCC (Pin 14) (2)	–0.3	V_{CC} + 0.3	V
				< 10	V/ms
		PLIMIT	–0.3	GVDD + 0.3	V
		INN, INP	–0.3	6.3	V
R_L	Minimum Load Resistance	BTL		3.2	
	Continuous total power dissipation		See *Thermal Information* Table		
T_A	Operating free-air temperature range		–40	125	°C
T_J	Operating junction temperature range(3)		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage slew rate of these pins must be restricted to no more than 10 V/ms. For higher slew rates, use a 100 kΩ resister in series with the pins, per application note SLUA626.
(3) The TPA3112D1-Q1 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SCBA017 and SLUA271 for more information about using the QFN thermal pad. See TI Technical Brief SLMA002 for more information about using the HTQFP thermal pad.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±250	
		Machine model (MM) per JESD22-A115	±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	8	26	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1		0.8	V
V_{OL}	Low-level output voltage	$\overline{FAULT}$, R_{PULLUP} = 100 kΩ, V_{CC} = 26 V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$, GAIN0, GAIN1, V_I = 2, V_{CC} = 18 V		50	µA
I_{IL}	Low-level input current	$\overline{SD}$, GAIN0, GAIN1, V_I = 0.8 V, V_{CC} = 18 V		5	µA
T_A	Operating free-air temperature		–40	125	°C

Copyright © 2012–2015, Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1][2]		TPA3112D1-Q1 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator

6.5 DC Characteristics

T_A = –40°C to 125°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PVCC = 21 V			40		mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PVCC = 21 V			400		µA
$r_{DS(on)}$	Drain-source on-state resistance	I_O = 500 mA, T_J = 25°C	High side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ = 2 V			10		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate Drive Supply	I_{GVDD} = 2 mA		6.5	6.9	7.3	V

6.6 DC Characteristics

T_A = –40°C to 125°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, PVCC = 12 V			20		mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load, PVCC = 12 V			200		µA
$r_{DS(on)}$	Drain-source on-state resistance	I_O = 500 mA, T_J = 25°C	High side		240		mΩ
			Low side		240		
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	dB
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	$\overline{SD}$ = 2 V			10		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2		µs
GVDD	Gate Drive Supply	I_{GVDD} = 2 mA		6.5	6.9	7.3	V
PLIMIT	Output Voltage maximum under PLIMIT control	V_{PLIMIT} = 2.0 V; V_I = 6-V differential		6.75	7.90	8.75	V

Copyright © 2012–2015, Texas Instruments Incorporated

6.7 AC Characteristics

T_A = –40°C to 125°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Power Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, inputs AC-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N ≤ 0.1%, f = 1 kHz, V_{CC} = 24 V		25		W
THD+N	Total harmonic distortion + noise	V_{CC} = 24 V, f = 1 kHz, P_O = 12 W (half-power)		<0.05 %		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 20 dB, f = 1 kHz		–70		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

6.8 AC Characteristics

T_A = –40°C to 125°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, inputs AC-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N ≤ 10%, f = 1 kHz , R_L = 8 Ω		10		W
P_O	Continuous output power	THD+N ≤ 10%, f = 1 kHz , R_L = 4 Ω		20		W
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 5 W (half-power)		<0.06 %		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	P_o = 1 W, Gain = 20 dB, f = 1 kHz		–70		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			150		°C
	Thermal hysteresis			15		°C

Copyright © 2012–2015, Texas Instruments Incorporated

6.9 Typical Characteristics

All measurements taken at 1 kHz, unless otherwise noted. The TPA3112D2 EVM (which is available at ti.com) made these measurements.

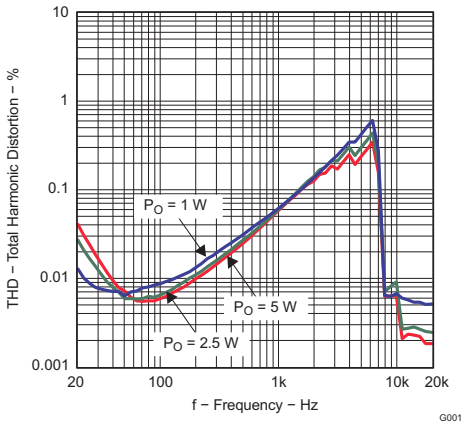


Figure 1. Total Harmonic Distortion vs Frequency

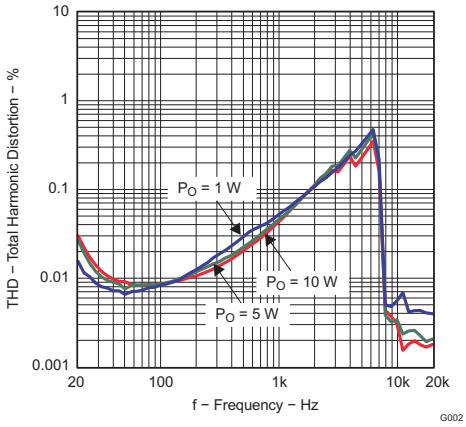


Figure 2. Total Harmonic Distortion vs Frequency

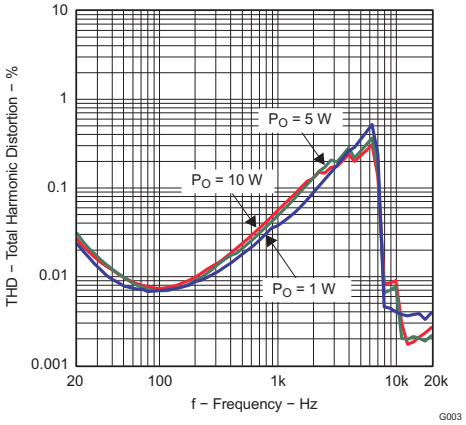


Figure 3. Total Harmonic Distortion vs Frequency

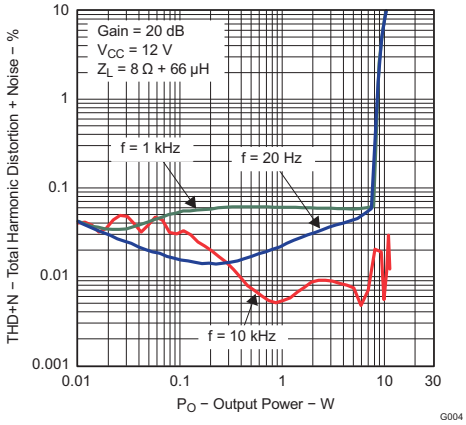
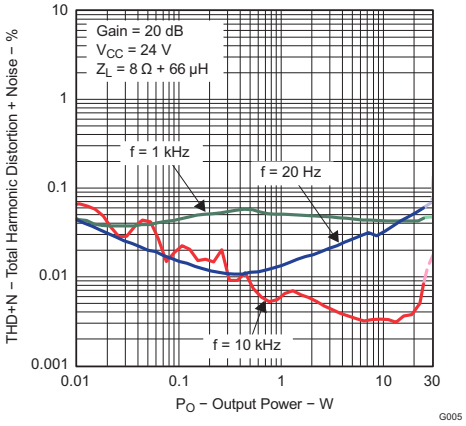


Figure 4. Total Harmonic Distortion + Noise vs Output Power



Note: Lighter colored lines represent thermally limited region.

Figure 5. Total Harmonic Distortion + Noise vs Output Power

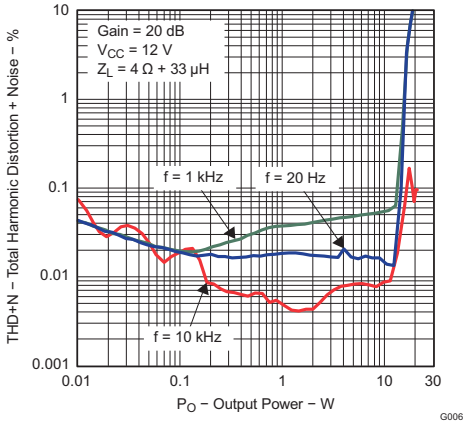
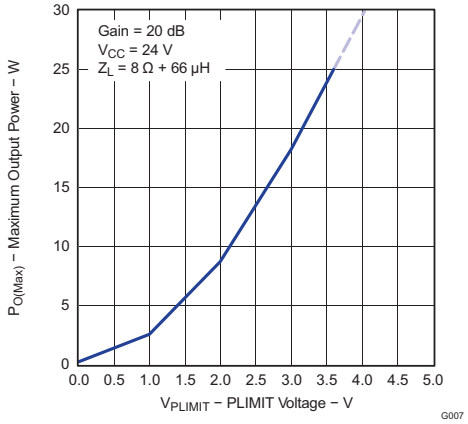


Figure 6. Total Harmonic Distortion + Noise vs Output Power

Copyright © 2012–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3112D2 EVM (which is available at ti.com) made these measurements.



Note: Lighter color represents thermally limited region.

Figure 7. Maximum Output Power vs Plimit Voltage

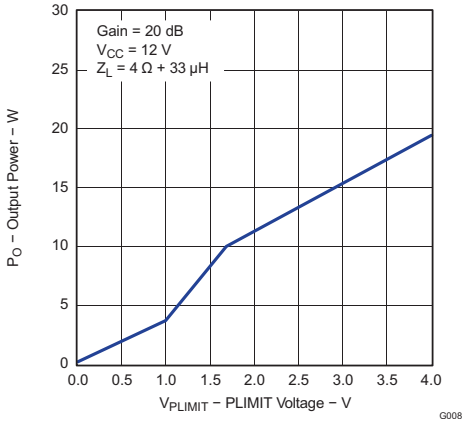


Figure 8. Output Power vs Plimit Voltage

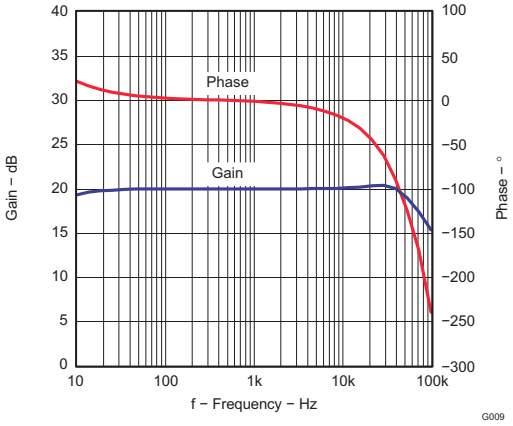
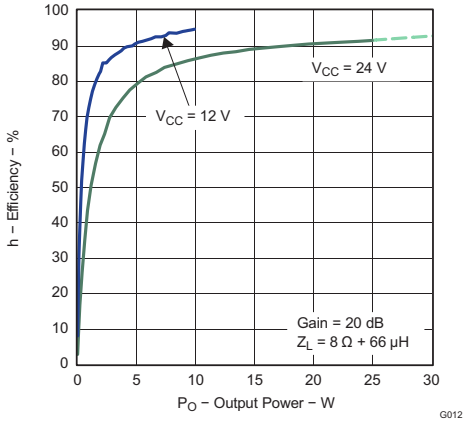
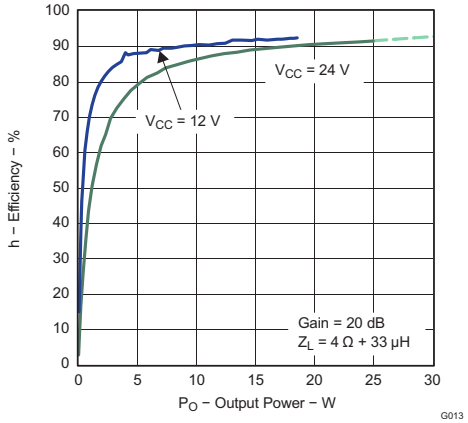


Figure 9. Gain/Phase vs Frequency



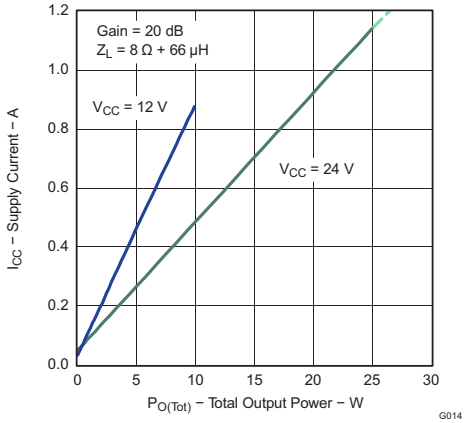
Note: Lighter color represents thermally limited region.

Figure 10. Efficiency vs Output Power



Note: Lighter color represents thermally limited region.

Figure 11. Efficiency vs Output Power



Note: Lighter color represents thermally limited region.

Figure 12. Supply Current vs Total Output Power

Copyright © 2012–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

All measurements taken at 1 kHz, unless otherwise noted. The TPA3112D2 EVM (which is available at ti.com) made these measurements.

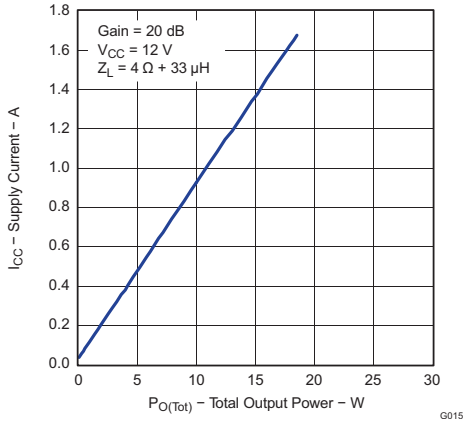


Figure 13. Supply Current vs Total Output Power

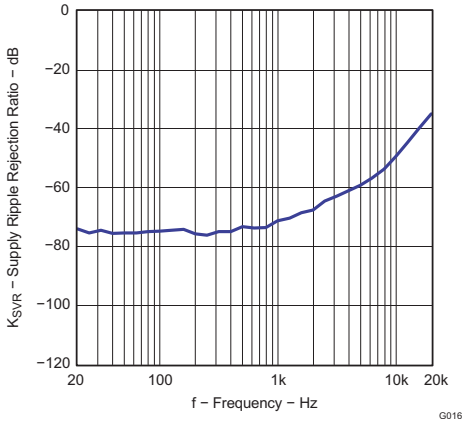


Figure 14. Supply Ripple Rejection Ratio vs Frequency

7 Detailed Description

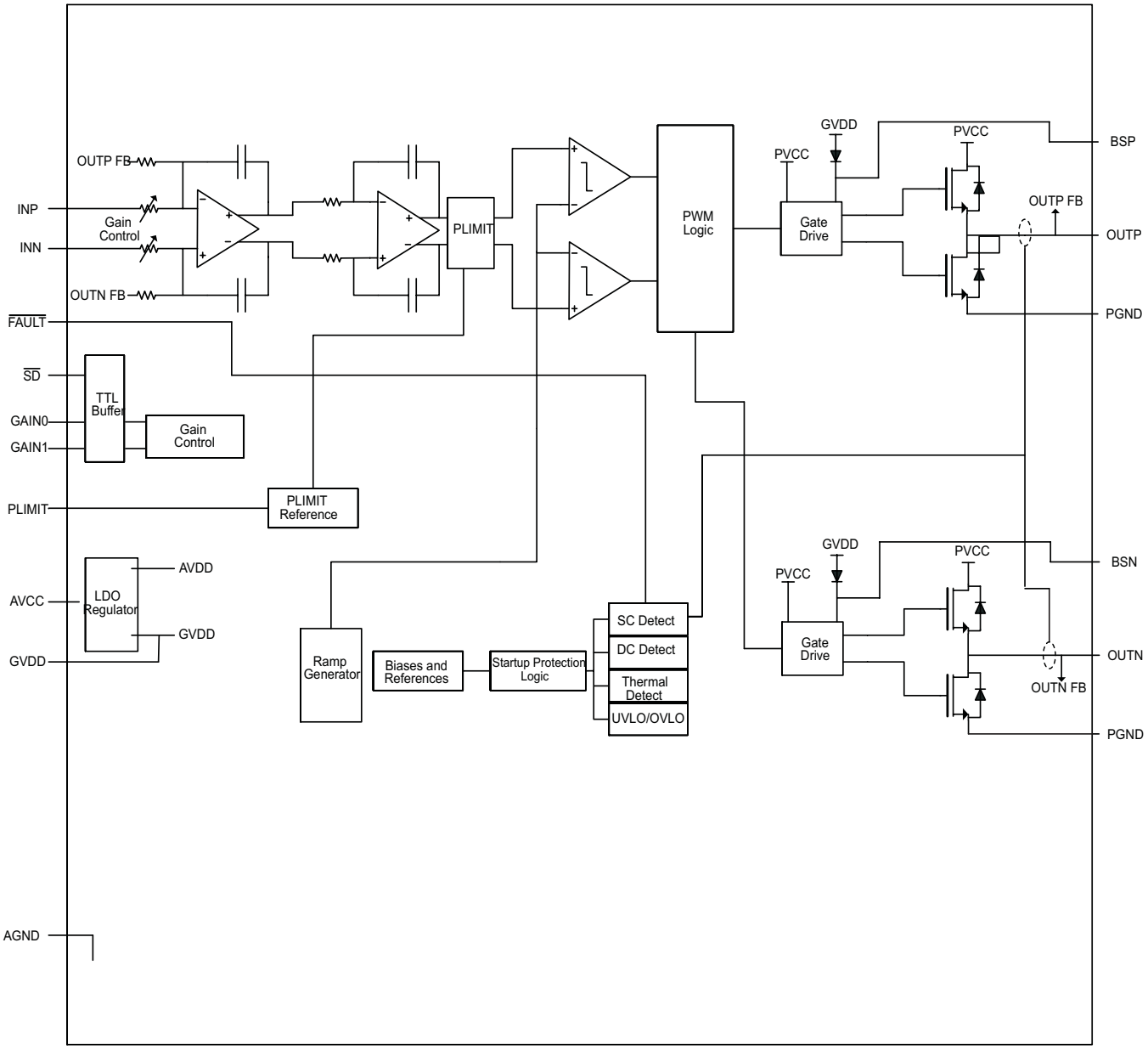
7.1 Overview

The TPA3112D1-Q1 is AEC-Q100 qualified with a temperature grade 1 (-40°C to 125°C), HBM ESD classification level H2, and CDM ESD classification level C2. This automotive audio amplifier also features several protection mechanisms.

- DC Current Detection
  - The TPA3112D1-Q1 protects speakers from DC current by reporting a fault on the $\overline{\text{FAULT}}$ pin and turning the amplifier outputs to a Hi-Z state when a DC current is detected. The PVCC supply must be cycled to clear this fault.
- Short-Circuit Protection and Automatic Recovery
  - The TPA3112D1-Q1 has short circuit protection from the output pins to VCC, GND, or to each other. If a short circuit is detected, it will be reported on the $\overline{\text{FAULT}}$ pin and the amplifier outputs will be switched to a Hi-Z state. The fault can be cleared by cycling the $\overline{\text{SD}}$ pin.
- Thermal Protection
  - When the die temperature exceeds 150°C (±15°C) the device enters the shutdown state and the amplifier outputs are disabled. The TPA3112D1-Q1 recovers automatically when the temperature decreases by 15°C.

Copyright © 2012–2015, Texas Instruments Incorporated

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DC Detect

The TPA3112D1-Q1 has circuitry that protects the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault is reported on the FAULT pin as a low state. The DC detect fault also causes the amplifier to shut down by changing the state of the outputs to Hi-Z. To clear the DC detect it is necessary to cycle the PVCC supply. Cycling SD does NOT clear a DC detect fault.

A DC detect fault is issued when the output differential duty-cycle exceeds 14% (for example, 57%, –43%) for more than 420 ms at the same polarity. This feature protects the speaker from large DC currents or AC currents, less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative input to avoid nuisance DC detect faults.

Copyright © 2012–2015, Texas Instruments Incorporated

Feature Description (continued)

The minimum differential input voltages required to trigger the DC detect are shown in Table Table 1. The inputs must remain at or above the voltage listed in the table for more than 420 ms to trigger the DC detect.

Table 1. DC Detect Threshold

AV (dB)	V_{IN} (mV, Differential)
20	112
26	56
32	28
36	17

7.3.2 Short-Circuit Protection and Automatic Recovery Feature

TPA3112D2 has protection from overcurrent conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{\text{SD}}$ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which clears the short circuit protection latch.

7.3.3 Thermal Protection

Thermal protection on the TPA3112D1-Q1 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ terminal.

7.3.4 GVDD Supply

The GVDD supply is used to power the gates of the output full bridge transistors. It can also used to supply the PLIMIT voltage divider circuit. Add a 1-μF capacitor to ground at this pin.

7.4 Device Functional Modes

7.4.1 Gain Setting Through GAIN0 and GAIN1 Inputs

The gain of the TPA3112D1-Q1 is set to one of four options by the state of the GAIN0 and GAIN1 pins. Changing the gain setting also changes the input impedance of the TPA3112D1-Q1.

Refer to Table 2 for a list of the gain settings.

Table 2. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

Copyright © 2012–2015, Texas Instruments Incorporated

7.4.2 $\overline{\text{SD}}$ Operation

The $\overline{\text{SD}}$ pin can be used to enter the shutdown mode which mutes the amplifier and causes the TPA3112D1-Q1 to enter a low-current state. This mode can also be triggered to improve power-off pop performance.

7.4.3 PLIMIT

The PLIMIT pin limits the output peak-to-peak voltage based on the voltage supplied to the PLIMIT pin. The peak output voltage is limited to four times the voltage at the PLIMIT pin.

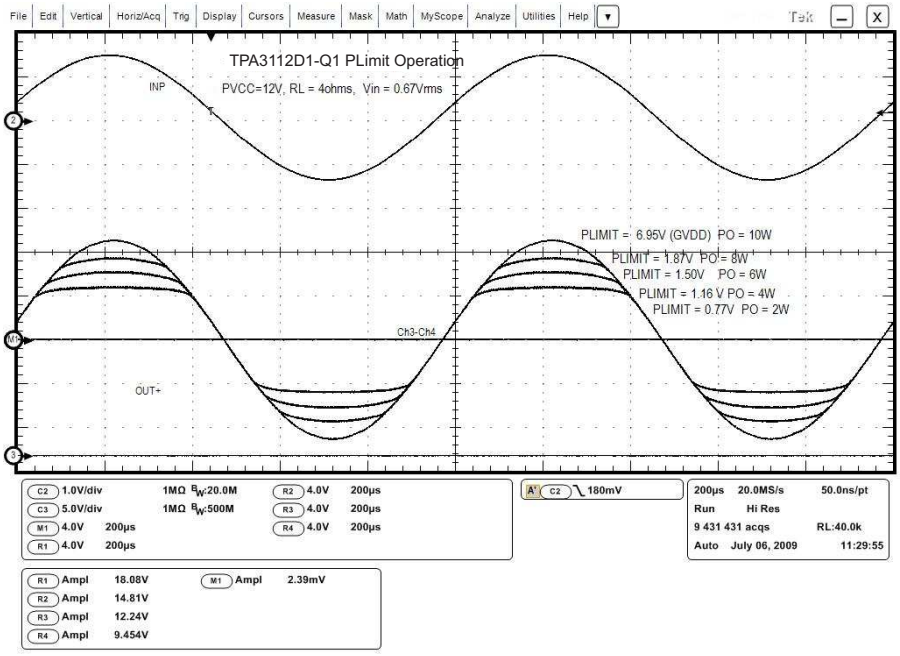


Figure 15. Plimit Circuit Operation

The PLIMIT circuits sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a virtual voltage rail which is lower than the supply connected to PVCC. This virtual rail is four times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

Copyright © 2012–2015, Texas Instruments Incorporated

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power} \tag{1}$$

Where:

R_S is the total series resistance including $R_{DS(on)}$, and any resistance in the output filter.

R_L is the load resistance.

V_P is the peak amplitude of the output possible within the supply rail.

V_P = 4 × PLIMIT voltage if PLIMIT < 4 × V_P

P_{OUT}(10%THD) = 1.25 × P_{OUT}(unclipped)

Table 3. PLIMIT Typical Operation

TEST CONDITIONS	PLIMIT VOLTAGE (V)	OUTPUT POWER (W)	OUTPUT VOLTAGE AMPLITUDE (V_{P-P})
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 4 Ω, Gain = 20 dB	6.97	22.1	26.9
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 4 Ω, Gain = 20 dB	1.92	10	15
PVCC = 24 V, V_{IN} = 1 V_{RMS}, R_L = 4 Ω, Gain = 20 dB	1.24	5	10
PVCC = 12 V, V_{IN} = 1 V_{RMS}, R_L = 4 Ω, Gain = 20 dB	6.95	17.2	20.9
PVCC = 12 V, V_{IN} = 1 V_{RMS}, R_L = 4 Ω, Gain = 20 dB	1.75	10	15.3
PVCC = 12 V, V_{IN} = 1 V_{RMS}, R_L = 4 Ω, Gain = 20 dB	1.2	5	10.3

Copyright © 2012–2015, Texas Instruments Incorporated

8 Application and Implementation

NOTE

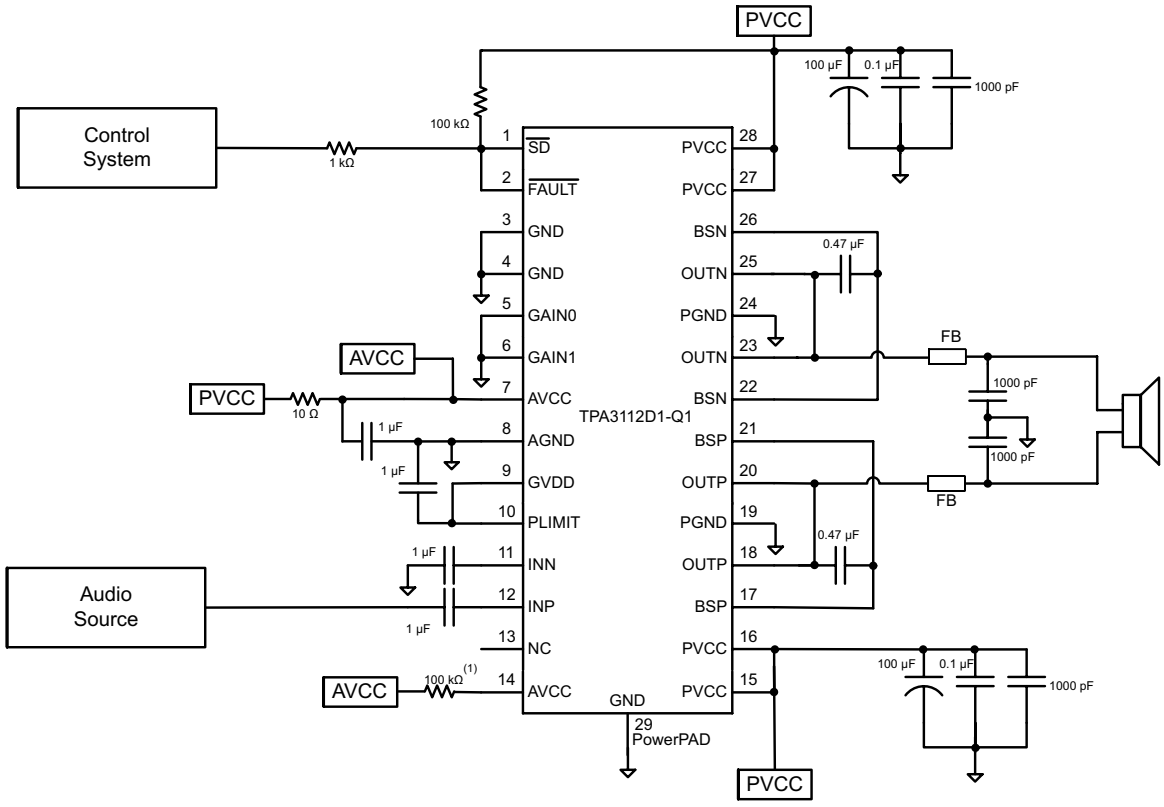
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPA3112D1-Q1 device is an automotive class-D audio amplifier. It accepts either a single ended or differential analog input, amplifies the signal, and drives up to 25-W across a bridge tied load, usually a speaker. Because an analog input is needed, this device is often paired with a codec or audio DAC if the audio source is digital.

The four digital input/output pins, GAIN0, GAIN1, $\overline{SD}$, and $\overline{FAULT}$, can be pulled up to PVCC. When connecting these terminals to PVCC, a 100 kΩ-resistor must be put in series to limit the slew rate. One of four gain settings is used depending on the configuration of GAIN0 and GAIN1. The $\overline{SD}$ pin is used to put the device in shutdown or normal mode. The $\overline{FAULT}$ pin is used to indicate if a DC detect or short circuit fault was detected. The next few sections explains design considerations and how to choose the external components.

8.2 Typical Application



(1) 100 kΩ resistor is needed if the PVCC slew rate is more than 10 V/ms.

Figure 16. Mono Class-D Amplifier With BTL Output

Typical Application (continued)

8.2.1 Design Requirements

The typical requirements for designing the external components around the TPA3112D1-Q1 include efficiency and EMI/EMC performance. For most applications, only a ferrite bead is needed to filter unwanted emissions. The ripple current is low enough that an LC filter is typically not needed. As the output power increases, causing the ripple current to increase, an LC filter can be added to improve efficiency. An LC filter can also be added in cases where additional EMI suppression is needed.

In addition to discussing how to choose a ferrite bead and when to use an LC filter, the following sections also discuss the input filter and power supply decoupling. The input filter must be chosen with the input impedance of the amplifier in mind. The cut-off frequency should be chosen so that bass performance is not impacted. Power supply decoupling is important to ensure that noise from the power line does not impact the audio quality of the amplifier output.

8.2.2 Detailed Design Procedure

8.2.2.1 Class-D Operation

This section focuses on the Class-D operation of the TPA3112D1-Q1.

8.2.2.2 TPA3112D1-Q1 Modulation Scheme

The TPA3112D1-Q1 uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

Please see Figure 20 for a plot of the output waveforms.

8.2.2.3 Ferrite Bead Filter Considerations

Using the advanced emissions suppression technology in the TPA3112D1-Q1 amplifier, it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. it is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10- to 100-MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead and capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at very low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3112D2 include the 28L0138-80R-10 and HI1812V101R-10 from Steward and the 742792510 from Wurth Electronics.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics works best.

Copyright © 2012–2015, Texas Instruments Incorporated

Typical Application (continued)

Additional EMC improvements may be obtained by adding snubber networks from each of the Class-D outputs to ground. Suggested values for a simple RC series snubber network would be 10 Ω in series with a 330-pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the PGND or the PowerPAD™ integrated circuit package beneath the chip.

8.2.2.4 Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional Class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 x V_{CC}, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3112D1-Q1 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of 2 x V_{CC}. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the Class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

8.2.2.5 When to Use an Output Filter for EMI Suppression

The TPA3112D1-Q1 has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The TPA3112D1-Q1 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are circuits near which are sensitive to noise. Therefore, a classic second order Butterworth filter similar to those shown in Figure 17 through Figure 19 can be used.

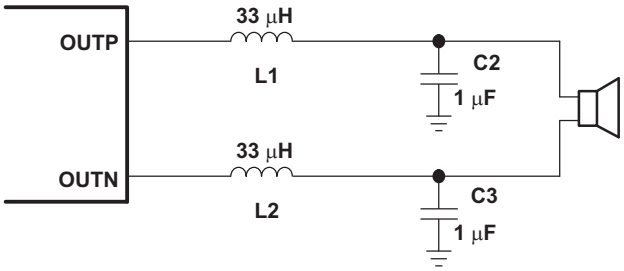


Figure 17. Typical LC Output Filter, Cutoff Frequency Of 27 Khz, Speaker Impedance = 8 Ω

Typical Application (continued)

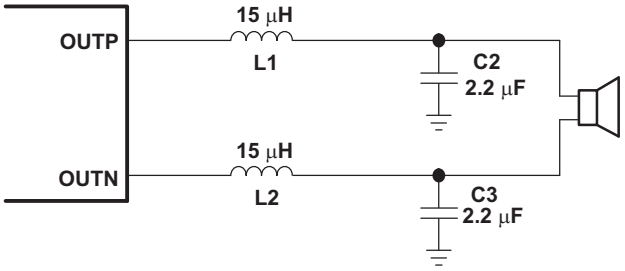


Figure 18. Typical LC Output Filter, Cutoff Frequency Of 27 Khz, Speaker Impedance = 4 Ω

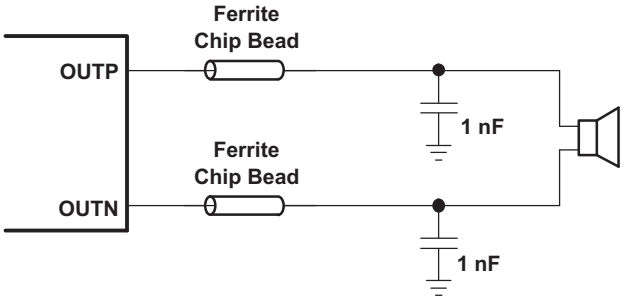
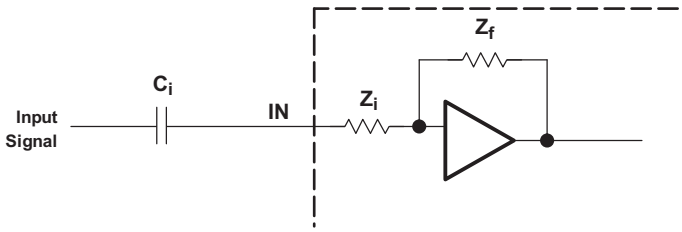


Figure 19. Typical Ferrite Chip Bead Filter (Chip Bead Example: Steward Hi0805r800r-10)

8.2.2.6 Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency may change when changing gain steps.



The –3–dB frequency can be calculated using Equation 2. Use the Z_I values given in Table 2.

$$f = \frac{1}{2\pi Z_i C_i} \quad (2)$$

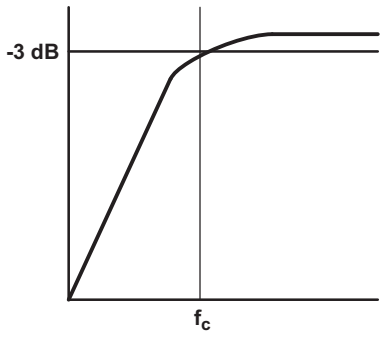
8.2.2.7 Input Capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 3.

Copyright © 2012–2015, Texas Instruments Incorporated

Typical Application (continued)

$$f_c = \frac{1}{2\pi Z_i C_i}$$



(3)

The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (4)$$

In this example, C_I is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 2 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network C_I) and the feedback network to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. If using a ceramic capacitor, choose a high quality capacitor with good temperature and voltage coefficient. An X7R type works well and if possible use a higher voltage rating than required. This gives a better C versus voltage characteristic. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at 3 V, which is likely higher than the source DC level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create DC offset voltages and it is important to ensure that boards are cleaned properly.

8.2.2.8 BSN and BSP Capacitors

The full H-bridge output stage uses only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 470-nF ceramic capacitor, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 470-nF capacitor must be connected from OUTP to BSP, and one 470-nF capacitor must be connected from OUTN to BSN.

The bootstrap capacitors connected between the BSx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

8.2.2.9 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3112D1-Q1 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3112D1-Q1 with a single-ended source, AC-ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be AC-grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input DC blocking capacitors to become completely charged during the 14 msec power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

Copyright © 2012–2015, Texas Instruments Incorporated

Typical Application (continued)

8.2.2.10 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

8.2.3 Application Curves

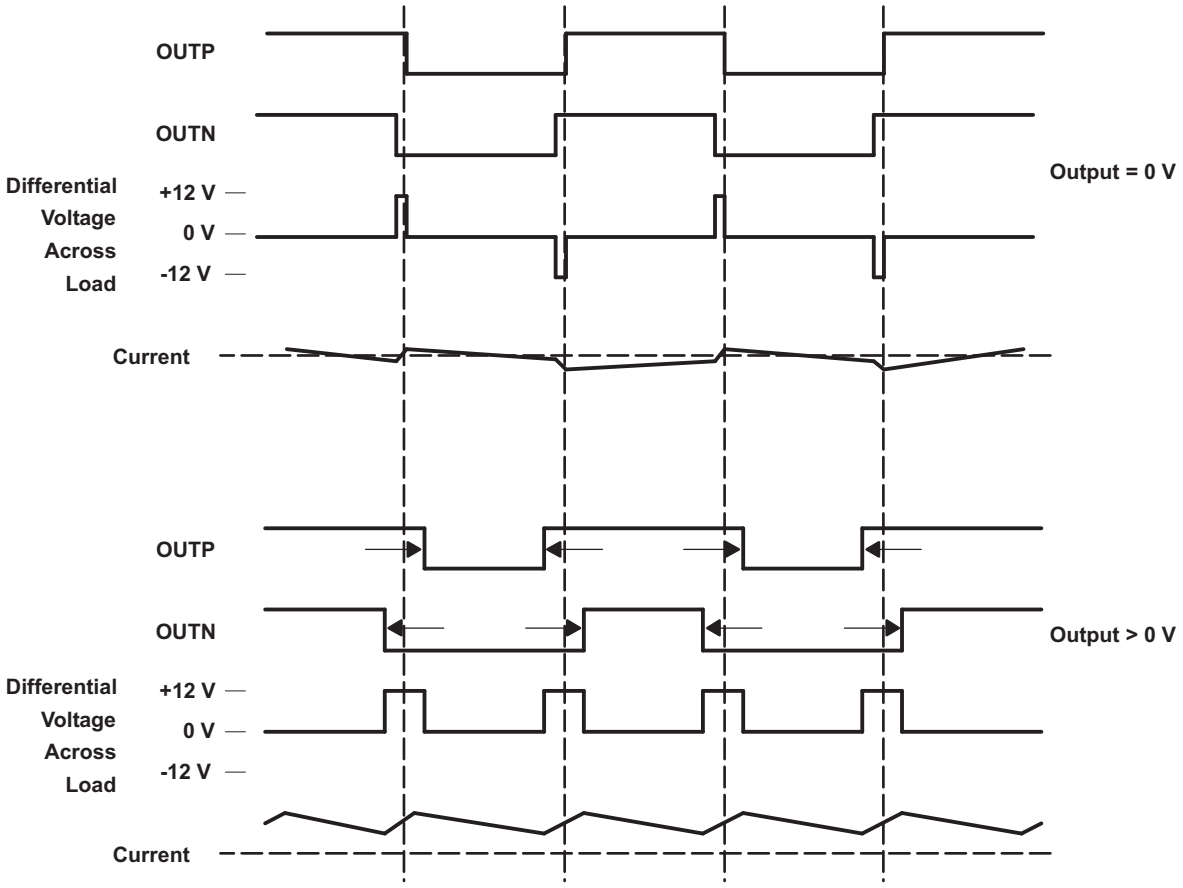


Figure 20. The TPA3112D1-Q1 Output Voltage and Current Waveforms into an Inductive Load

Copyright © 2012–2015, Texas Instruments Incorporated

9 Power Supply Recommendations

The TPA3112D1-Q1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker.

Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPAD™ integrated circuit package) as possible.

For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 mF to 1 μF placed as close as possible to the device PVCC leads works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 mF or greater placed near the audio power amplifier is recommended. The 220-mF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220-μF or larger capacitor should be placed on each PVCC terminal. A 10-μF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency Class-D noise from entering the linear input amplifiers.

Copyright © 2012–2015, Texas Instruments Incorporated

10 Layout

10.1 Layout Guidelines

The TPA3112D1-Q1 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are very fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220-μF or greater) bulk power supply decoupling capacitors should be placed near the TPA3112D1-Q1 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1 mF and 1 mF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Output filter—The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46 mm by 2.35 mm. Seven rows of solid vias (three vias per row, 0.33 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See the TI Application Report SLMA002 for more information about using the TSSOP thermal pad.

For an example layout, see the TPA3112D1-Q1 Evaluation Module User's Guide, SLOU272. Both the EVM user's guide and the thermal pad application note are available on the TI website at http://www.ti.com.

Copyright © 2012–2015, Texas Instruments Incorporated

10.2 Layout Example

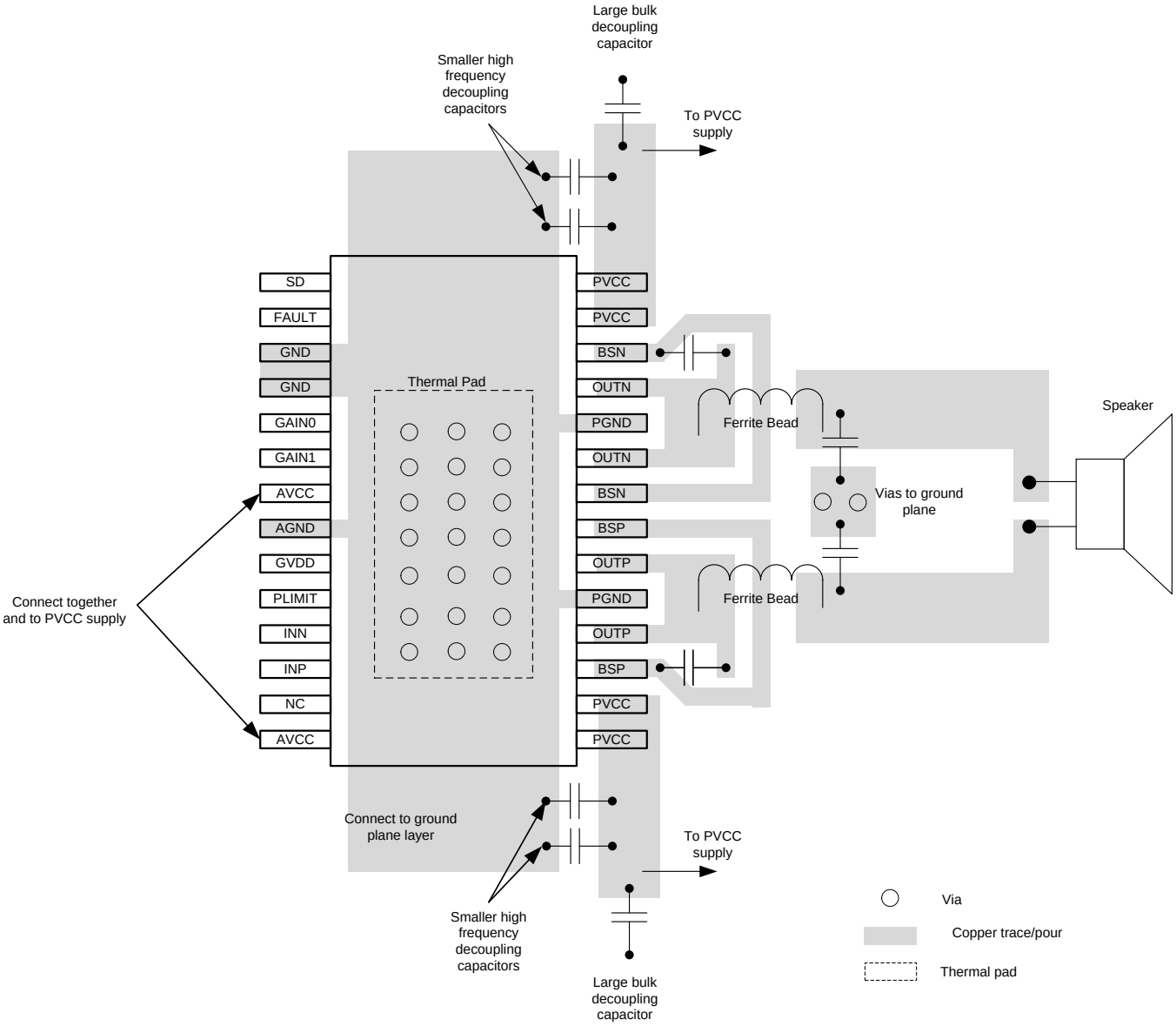


Figure 21. TPA3112D1-Q1 Layout Example for BTL Output

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

TI PCB Thermal Calculator

11.2 Documentation Support

11.2.1 Related Documentation

Maximum Slew Rate on High-Voltage Pins for TPA3111D1, SLUA626

Quad Flatpack No-Lead Logic Packages, SCBA017

QFN/SON PCB Attachment, SLUA217

PowerPAD ™ Thermally Enhanced Package, SLMA002

Semiconductor and IC Package Thermal Metrics, SPRA953

TPA3112D1EVM Audio Amplifier Evaluation Board, SLOU272

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

SpeakerGuard, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2012–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3112D1QPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA3112Q1
TPA3112D1QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA3112Q1
TPA3112D1QPWPRQ1.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA3112Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPA3112D1-Q1 :

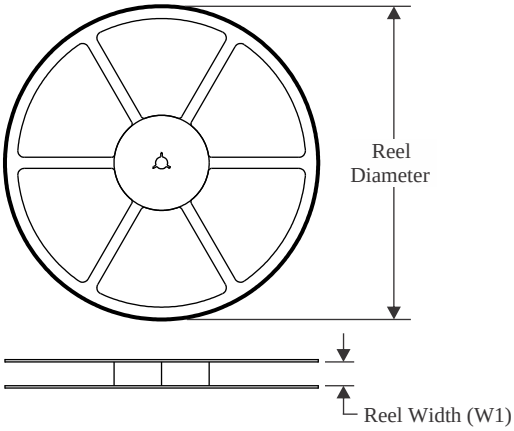
- Catalog : TPA3112D1

NOTE: Qualified Version Definitions:

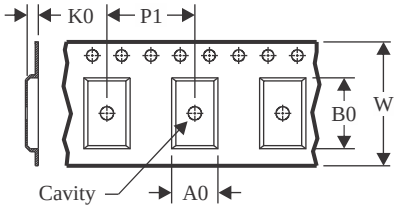
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

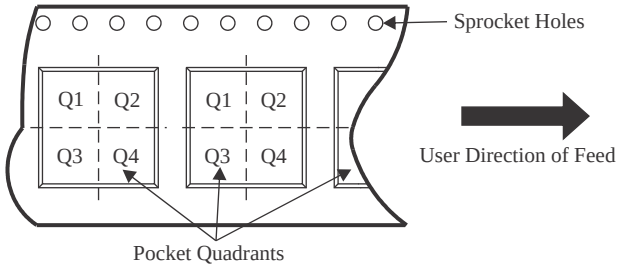


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

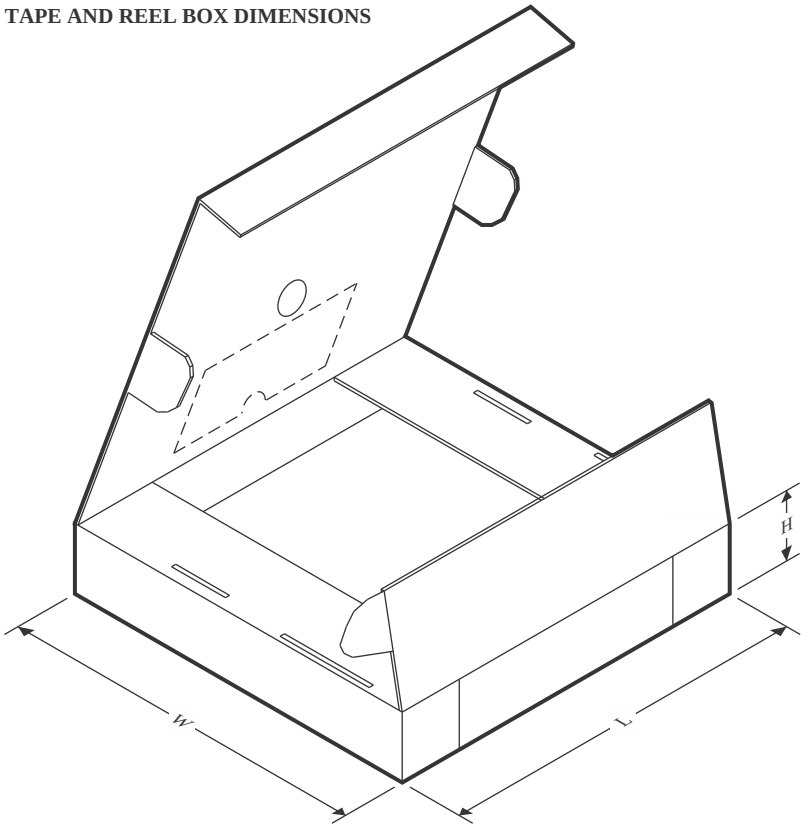
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3112D1QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3112D1QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

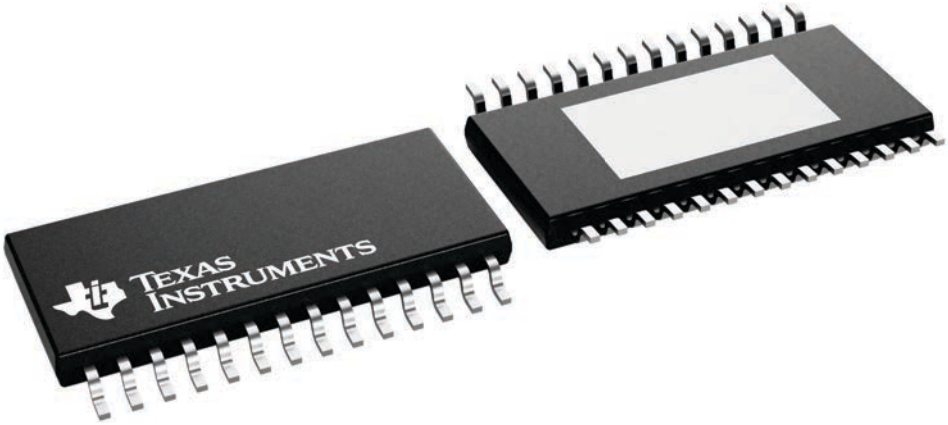
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

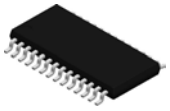
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

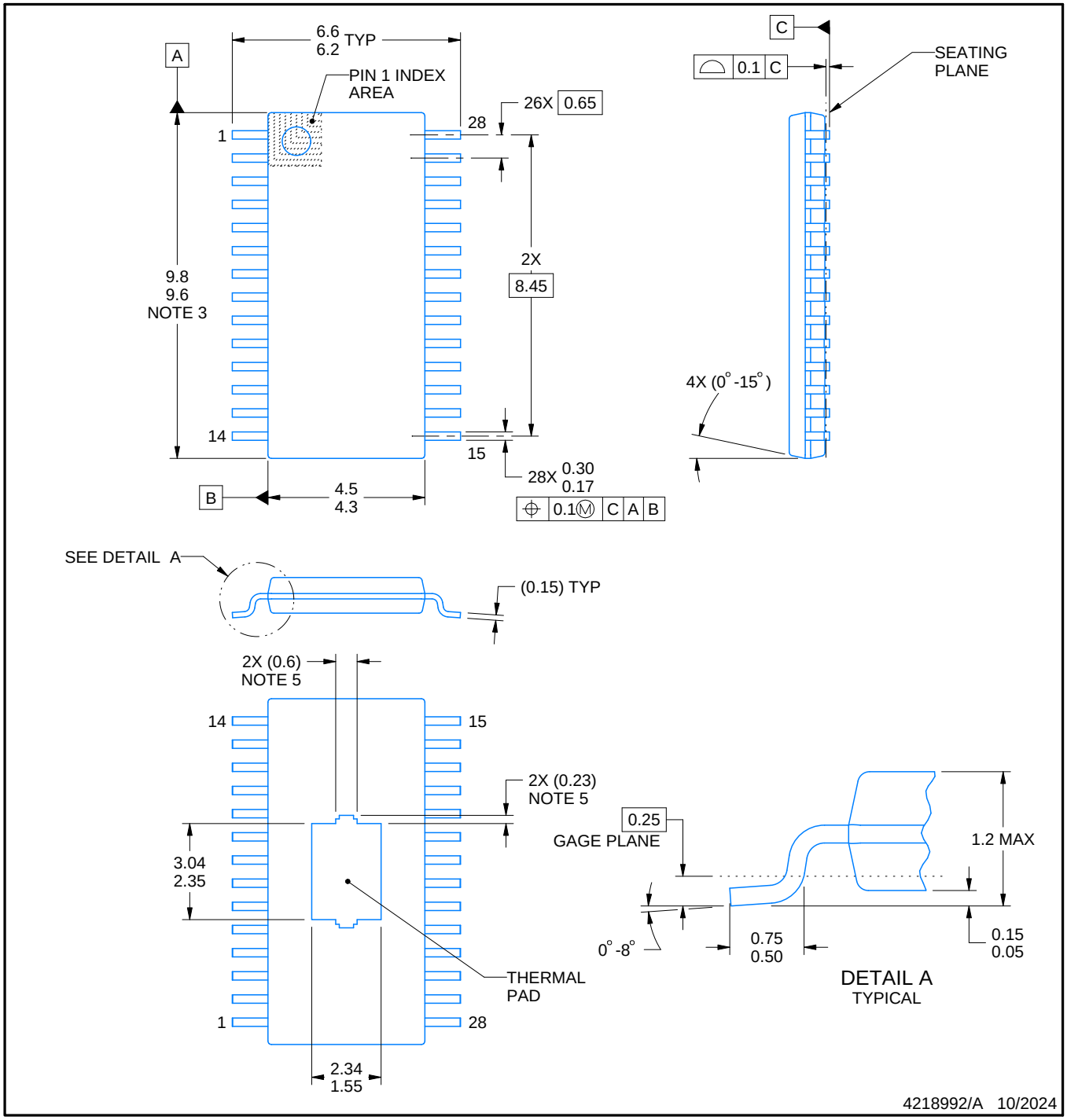
PACKAGE OUTLINE

PWP0028H



PowerPAD™ TSSOP - 1.2 mm max height

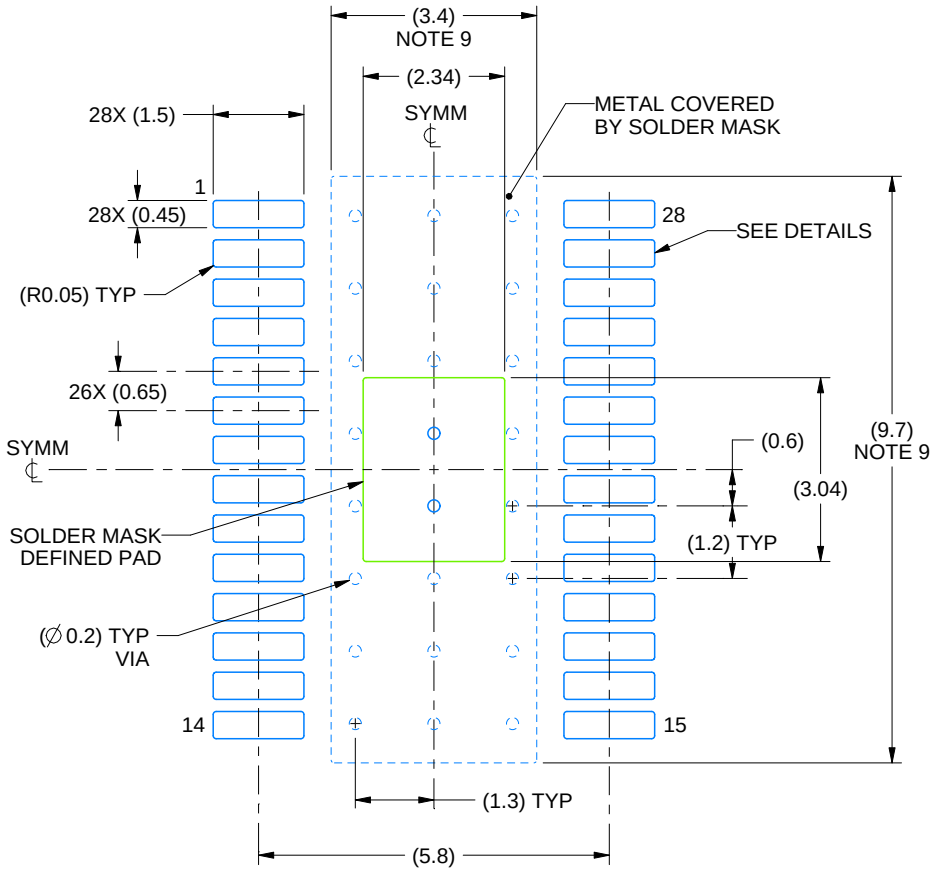
SMALL OUTLINE PACKAGE



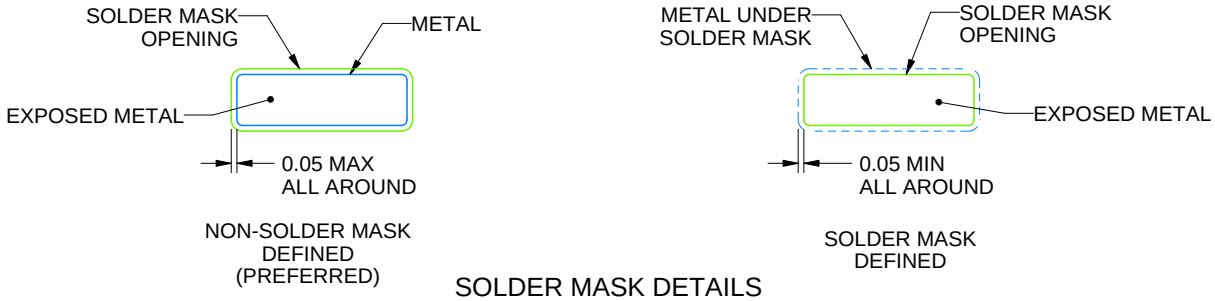
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

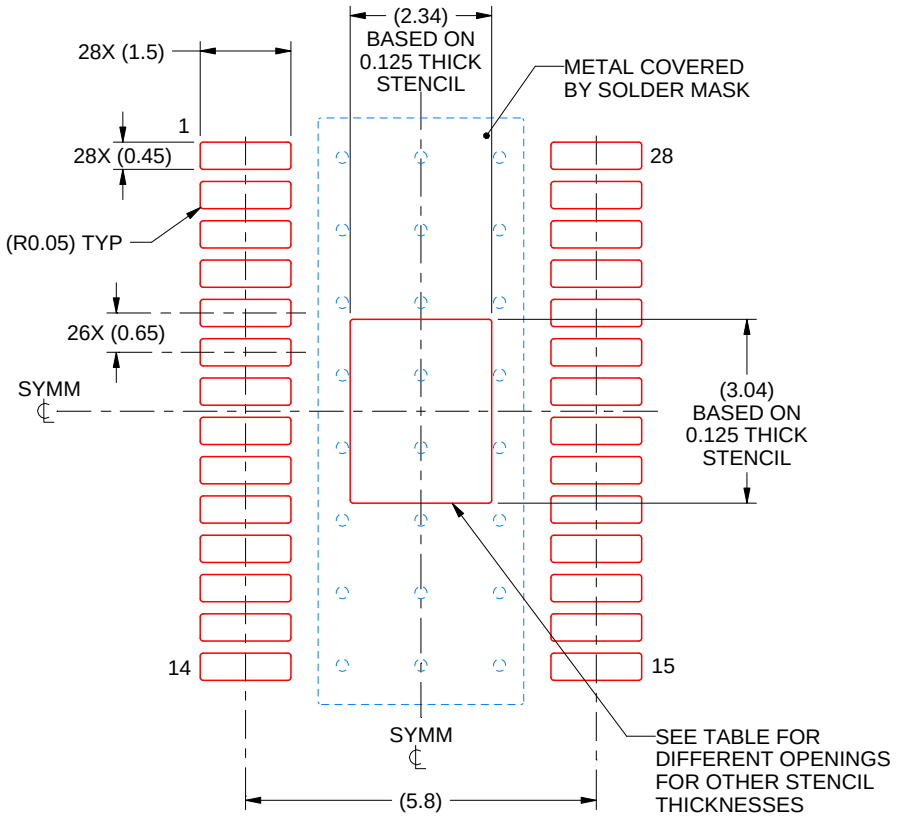


SOLDER MASK DETAILS

4218992/A 10/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 3.40
0.125	2.34 X 3.04 (SHOWN)
0.15	2.14 X 2.78
0.175	1.98 X 2.57

4218992/A 10/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025