TPA3128D2, TPA3129D2 2x30-W, 2x15-W Class-D Amplifier With Low Idle Power Dissipation

1 Features

- Supports Multiple Output Configurations
  - 2 × 30 W Into a 8-Ω BTL Load at 24 V (TPA3128D2)
  - 2 × 15 W Into a 8-Ω BTL Load at 15 V (TPA3129D2)
- Wide Voltage Range: 4.5 V to 26 V
- Efficient Class-D Operation
  - Very Low Idle Current: <23 mA for recommended LC filter configurations
  - Greater than 90% Power Efficiency Combined With Low Idle Loss Greatly Eliminates Need for Heat Sink
  - Adaptive Modulation Schemes based on Output Power
  - Smart Amplifier Drivers to Reduce the Requirement for RC Snubbers
- Multiple Switching Frequencies
  - AM Avoidance
  - Master and Slave Synchronization
  - 300-KHz to 1.2-MHz Switching Frequency
- Feedback Power-Stage Architecture With High PSRR Reduces PSU Requirements
- Programmable Power Limit
- Parallel BTL Mode and Mono-Channel Mode Support
- Supports Both Single and Dual Power Supply Modes
- Integrated Self-Protection Circuits Including Overvoltage, Undervoltage, Overtemperature, DC-Detect, and Short Circuit With Error Reporting
- Thermally Enhanced Packages
  - DAP (32-Pin HTSSOP Pad Down for TPA3128D2 and TPA3129D2)

2 Applications

- Bluetooth/Wireless Speakers
- Soundbars
- Mini-Micro Component, Docks
- LCD/LED TVs
- Home Theaters

3 Description

The TPA3128D2 and TPA3129D2 have low idle power loss and helps to extend the battery life of Bluetooth/Wireless speakers and other battery-powered audio systems. The high efficiency of the TPA3128D2 device allows it to do 2 × 30 W without external heat sink on a dual layer PCB. The high efficiency of the TPA3129D2 device allows it to do 2 × 15 W without external heat sink on a dual layer PCB. This device proposed an efficiency boost Mode, which can dynamically reduced the current ripple of the external LC filter and the idle current .

The TPA31xxD2 advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM interferences, which is achieved together with an option of either master or slave option, making it possible to synchronize multiple devices.

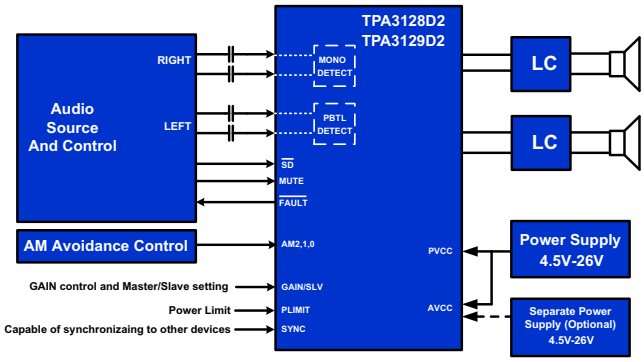
The TPA31xxD2 devices are fully protected against faults with short-circuit protection and thermal protection as well as overvoltage, undervoltage, and DC protection. Faults are reported back to the processor to prevent devices from being damaged during overload conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA3128D2	DAP (32)	11.00 mm × 6.20 mm
TPA3129D2	DAP (32)	11.00 mm × 6.20 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2017) to Revision C	Page
• Added mA to the Unit value for I_{CC} in the *DC Electrical Characteristics* table	6

Changes from Revision A (December 2016) to Revision B	Page
• Added TPA3129D2 device to data sheet	1
• Added Output power capability value for TPA3129D2 device	1
• Changed GVDD max value for both devices to 6.3 V	6
• Changed over current trip point value for TPA3129D2 device to 5.5 A	7

Changes from Original (May 2016) to Revision A	Page
• Released full datasheet as Production Data	1

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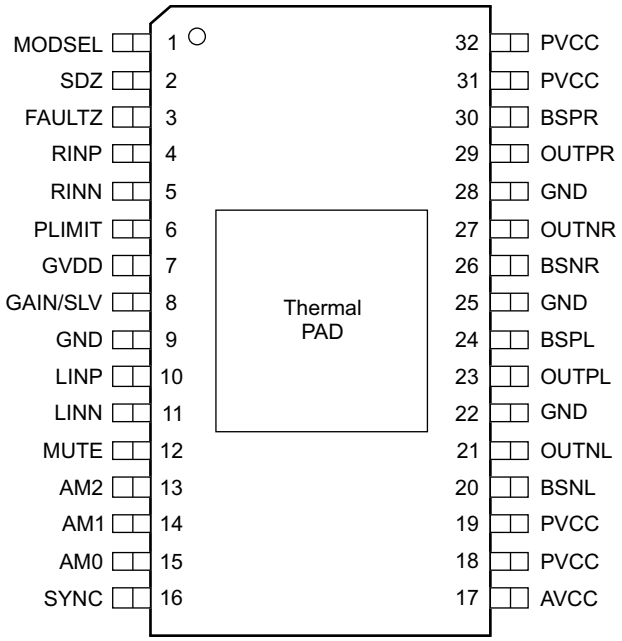
5 Pin Configuration and Functions

DAP Package
32-Pin HTSSOP With PowerPAD Down
TPA3128D2, TPA3129D2, Top View



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	MODSEL	I	Mode selection logic input (LOW = Ultra Low Idle Loss Mode, HIGH = BD Mode). TTL logic levels with compliance to AVCC.
2	SDZ	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
3	FAULTZ	DO	General fault reporting including Over-temp, DC Detect. Open drain. FAULTZ = High, normal operation FAULTZ = Low, fault condition
4	RINP	I	Positive audio input for right channel. Connect to GND for MONO mode.
5	RINN	I	Negative audio input for right channel. Connect to GND for MONO mode.
6	PLIMIT	I	Power limit level adjust. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
7	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the PLIMIT and GAIN/SLV resistor dividers.
8	GAIN/SLV	I	Selects Gain and selects between Master and Slave mode depending on pin voltage divider.
9	GND	G	Ground
10	LINP	I	Positive audio input for left channel. Connect to GND for PBTL mode.
11	LINN	I	Negative audio input for left channel. Connect to GND for PBTL mode.
12	MUTE	I	Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
13	AM2	I	AM Avoidance Frequency Selection
14	AM1	I	AM Avoidance Frequency Selection
15	AM0	I	AM Avoidance Frequency Selection
16	SYNC	DIO	Clock input/output for synchronizing multiple class-D devices. Direction determined by GAIN/SLV terminal.
17	AVCC	P	Analog Supply

(1) **TYPE**: DO = Digital Output, I = Analog Input, G = General Ground, PO = Power Output, BST = Boot Strap.

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Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
18	PVCC	P	Power supply
19	PVCC	P	Power supply
20	BSNL	BST	Boot strap for negative left channel output, connect to 220 nF X5R, or better ceramic cap to OUTPL
21	OUTNL	PO	Negative left channel output
22	GND	G	Ground
23	OUTPL	PO	Positive left channel output
24	BSPL	BST	Boot strap for positive left channel output, connect to 220 nF X5R, or better ceramic cap to OUTNL
25	GND	G	Ground
26	BSNR	BST	Boot strap for negative right channel output, connect to 220 nF X5R, or better ceramic cap to OUTNR
27	OUTNR	PO	Negative right channel output
28	GND	G	Ground
29	OUTPR	PO	Positive right channel output
30	BSPR	BST	Boot strap for positive right channel output, connect to 220 nF X5R or better ceramic cap to OUTPR
31	PVCC	P	Power supply
32	PVCC	P	Power supply
33	PowerPAD	G	Connect to GND for best system performance. If not connected to GND, leave floating.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	–0.3	30	V
Input voltage, V_I	INPL, INNL, INPR, INNR	–0.3	6.3	V
	PLIMIT, GAIN / SLV, SYNC	–0.3	GVDD+0.3	V
	AM0, AM1, AM2, MUTE, SDZ, MODSEL	–0.3	PVCC+0.3	V
Slew rate, maximum[2]	AM0, AM1, AM2, MUTE, SDZ, MODSEL		10	V/ms
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature , T_J		–40	150	°C
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under absolute maximum ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) 100-kΩ series resistor is required if maximum slew rate is exceeded.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. .

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}		4.5		26	V
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL		2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL				0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 kΩ, PV_{CC} = 26 V				0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, SDZ, MODSEL (V_I = 2 V, V_{CC} = 18 V)				50	µA
R_L(BTL)	Minimum load Impedance	Output filter: L = 10 µH, C = 680 nF	TPA3128D2	3.2	4		Ω
			TPA3129D2	5.6	8		
R_L(PBTL)		Output filter: L = 10 µH, C = 1 µF	TPA3128D2	1.6	2		
			TPA3129D2	3.2	4		
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition		1			µH

6.4 Thermal Information

THERMAL METRIC[1]		TPA3128D2, TPA3129D2 DAP[2] 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) For the PCB layout, see the TPS3128D2EVM user guide.

6.5 DC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω, f_s = 400 kHz, low idle-loss mode(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V		1.5	5	mV
I_{CC}	Quiescent supply current	SDZ = 2 V, With load and filter, PV_{CC} = 12 V		17		mA
		SDZ = 2 V, With load and filter, PV_{CC} = 24 V		23		mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ = 0.8 V, With load and filter, PV_{CC} = 12 V		20		µA
		SDZ = 0.8 V, With load and filter, PV_{CC} = 24 V		30		
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PV_{CC} = 21 V, I_{out} = 500 mA, T_J = 25°C		90		mΩ
G	Gain (BTL)	R1 = 5.6 kΩ, R2 = Open	19	20	21	dB
		R1 = 20 kΩ, R2 = 100 kΩ	25	26	27	
		R1 = 39 kΩ, R2 = 100 kΩ	31	32	33	dB
		R1 = 47 kΩ, R2 = 75 kΩ	35	36	37	
G	Gain (SLV)	R1 = 51 kΩ, R2 = 51 kΩ	19	20	21	dB
		R1 = 75 kΩ, R2 = 47 kΩ	25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ	31	32	33	dB
		R1 = 100 kΩ, R2 = 16 kΩ	35	36	37	
t_{on}	Turn-on time	SDZ = 2 V		40		ms
t_{OFF}	Turn-off time	SDZ = 0.8 V		2		µs
GVDD	Gate drive supply	IGVDD < 200 µA	5.1	5.6	6.3	V
V_O	Output voltage maximum under PLIMIT control	V(PLIMIT) = 2 V; V_I = 1 V_{rms}	6.75	8.2	8.75	V

6.6 AC Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 20 dB, Inputs AC-coupled to GND		–70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, PV_{CC} = 14.4 V		25		W
		THD+N = 10%, f = 1 kHz, PV_{CC} = 21 V		30		
THD+N	Total harmonic distortion + noise	V_{CC} = 21 V, f = 1 kHz, P_O = 15 W (half-power)		0.1%		
Vn	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		µV
				–80		dBV
	Crosstalk	V_O = 1 V_{rms}, Gain = 20 dB, f = 1 kHz		–100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB

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AC Electrical Characteristics (continued)

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	AM2=0, AM1=0, AM0=0	376	400	424	kHz
		AM2=0, AM1=0, AM0=1	470	500	530	
		AM2=0, AM1=1, AM0=0	564	600	636	
		AM2=0, AM1=1, AM0=1	940	1000	1060	
		AM2=1, AM1=0, AM0=0	1128	1200	1278	
		AM2=1, AM1=0, AM0=1	282	300	318	
		AM2=1, AM1=1, AM0=0	Reserved			
		AM2=1, AM1=1, AM0=1				
	Thermal trip point			≥150		°C
	Thermal hysteresis			15		°C
	Over current trip point	TPA3128D2		7.5		A
		TPA3129D2		5.5		

6.7 Typical Characteristics

f_s = 400 kHz, Ultra Low Idle Loss Mode, TPA3128D2EVM Tested With AP2722. (unless otherwise noted)

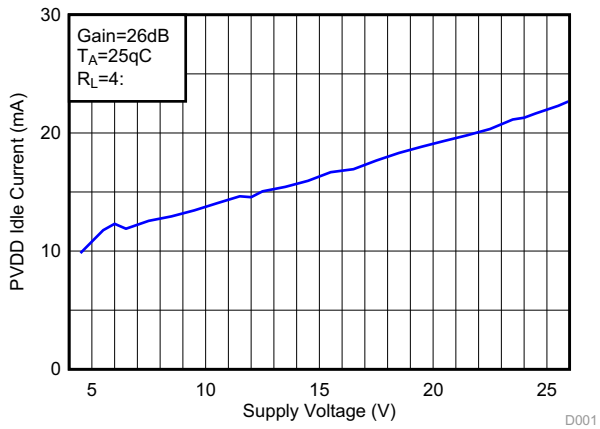

Figure 1. Idle Current vs PVCC

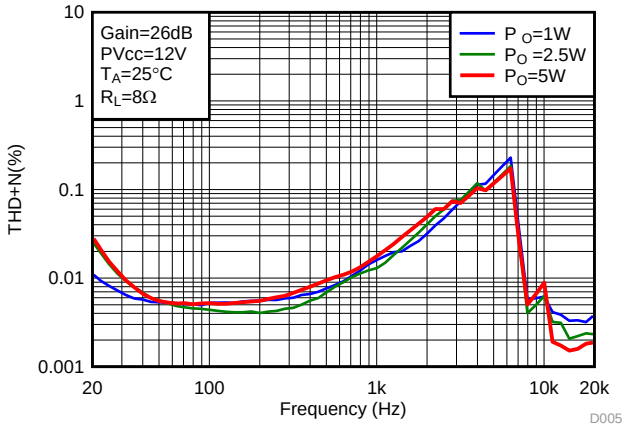

Figure 2. Total Harmonic Distortion + Noise (BTL) vs Frequency

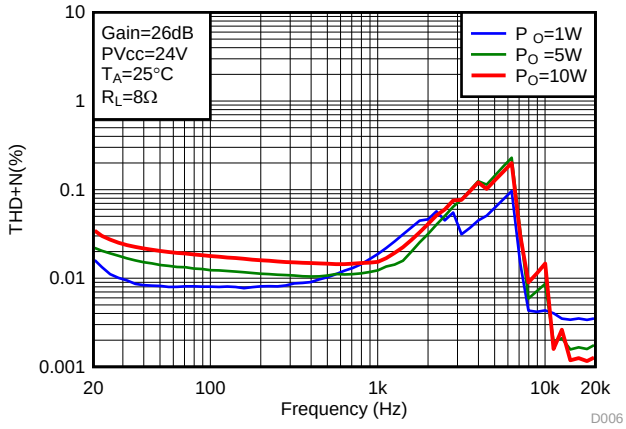

Figure 3. Total Harmonic Distortion + Noise (BTL) vs Frequency

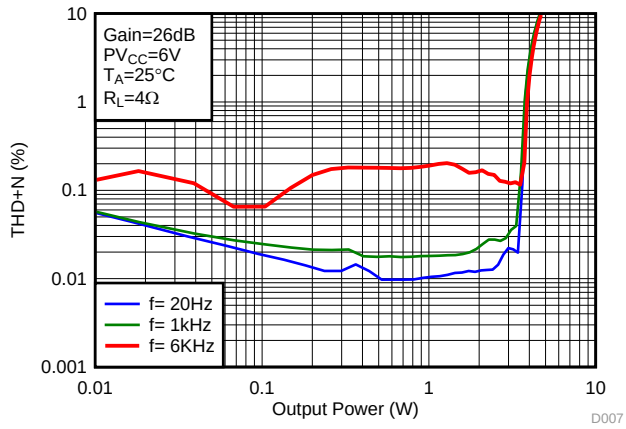

Figure 4. Total Harmonic Distortion + Noise (BTL) vs Output Power

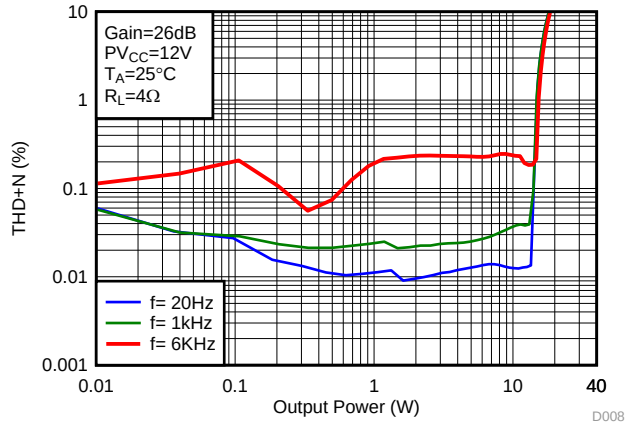

Figure 5. Total Harmonic Distortion + Noise (BTL) vs Output Power

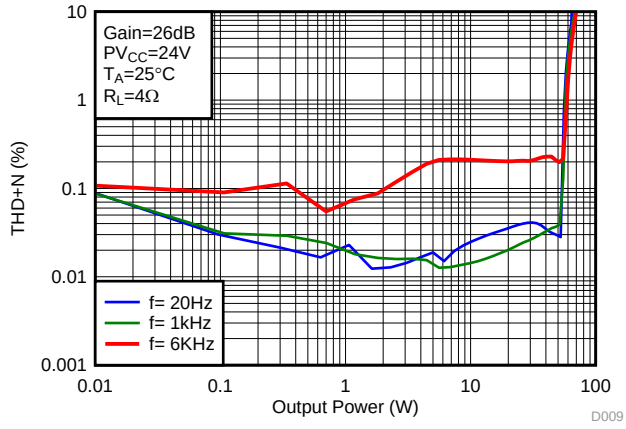

Figure 6. Total Harmonic Distortion + Noise (BTL) vs Output Power

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Typical Characteristics (continued)

f_s = 400 kHz, Ultra Low Idle Loss Mode, TPA3128D2EVM Tested With AP2722. (unless otherwise noted)

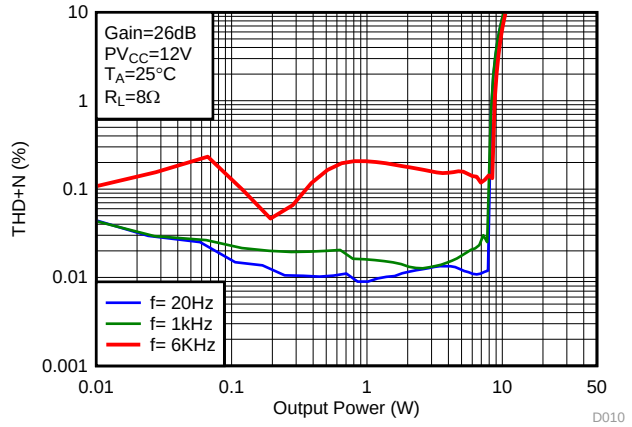

Figure 7. Total Harmonic Distortion + Noise (BTL) vs Output Power

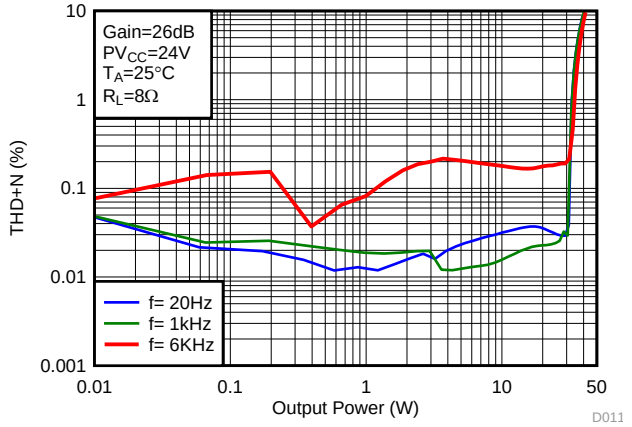

Figure 8. Total Harmonic Distortion + Noise (BTL) vs Output Power

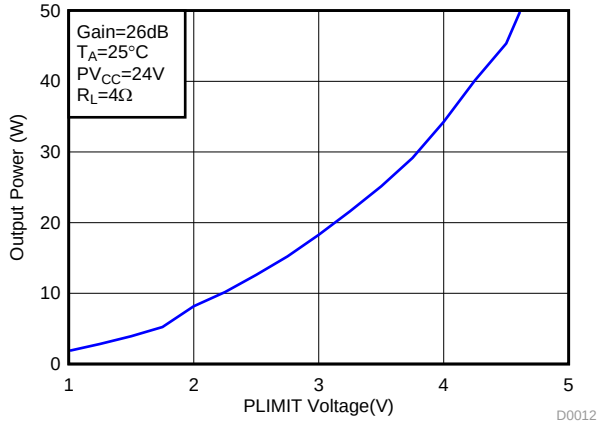

Figure 9. Output Power (BTL) vs Plimit Voltage

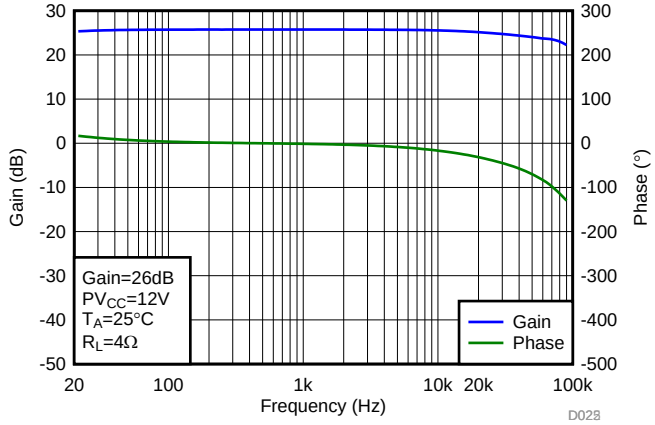

Figure 10. Gain/Phase (BTL) vs Frequency

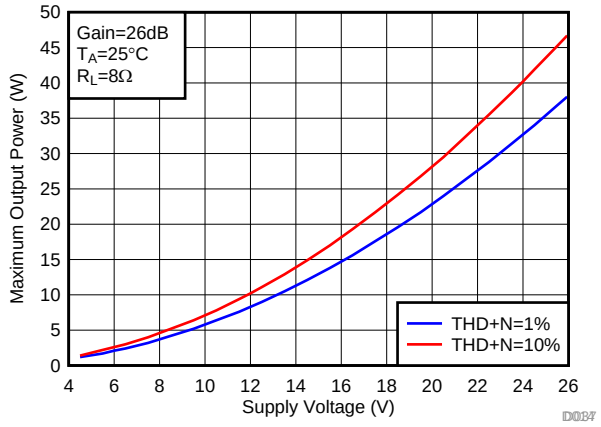

Figure 11. Maximum Output Power (BTL) vs Supply Voltage

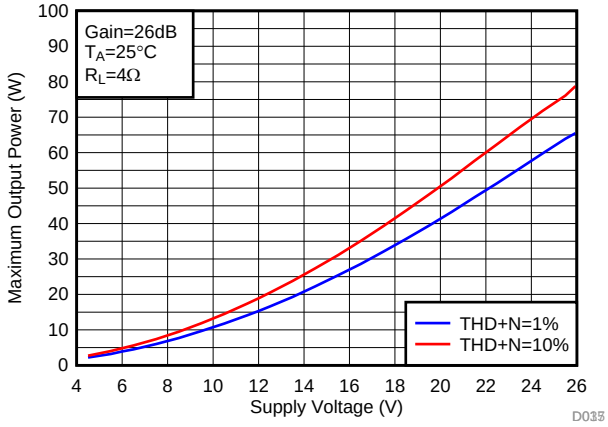

Figure 12. Maximum Output Power (BTL) vs Supply Voltage

Typical Characteristics (continued)

f_s = 400 kHz, Ultra Low Idle Loss Mode, TPA3128D2EVM Tested With AP2722. (unless otherwise noted)

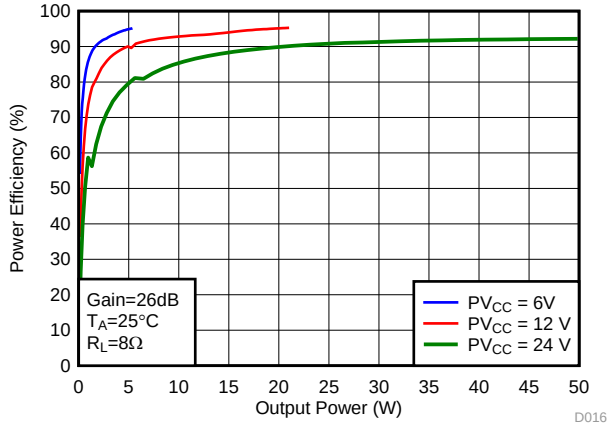

Figure 13. Power Efficiency (BTL) vs Output Power

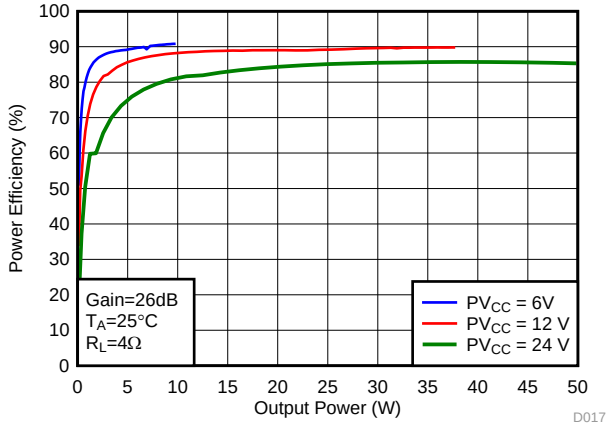

Figure 14. Power Efficiency (BTL) vs Output Power

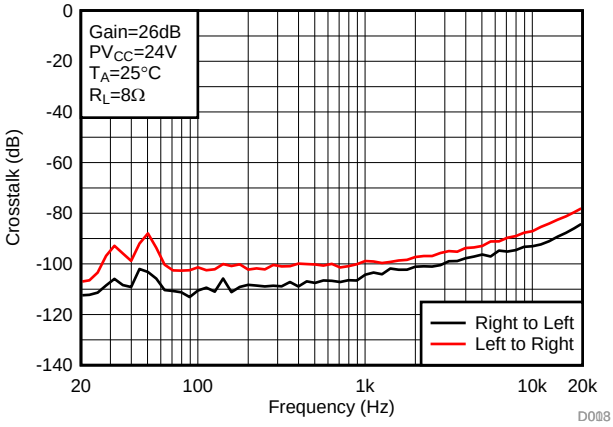

Figure 15. Crosstalk vs Frequency

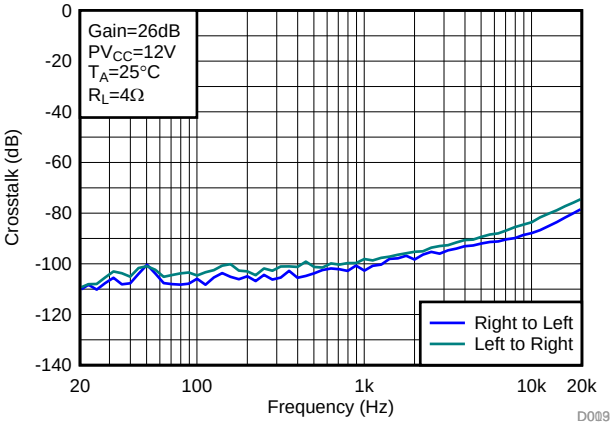

Figure 16. Crosstalk vs Frequency

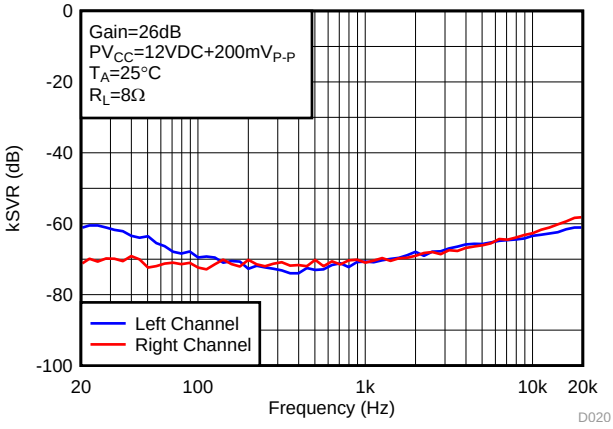

Figure 17. Supply Ripple Rejection Ratio (BTL) vs Frequency

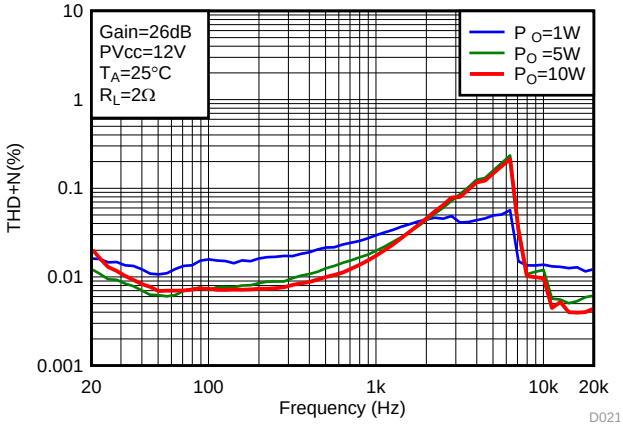

Figure 18. Total Harmonic Distortion + Noise (PBTL) vs Frequency

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Typical Characteristics (continued)

f_s = 400 kHz, Ultra Low Idle Loss Mode, TPA3128D2EVM Tested With AP2722. (unless otherwise noted)

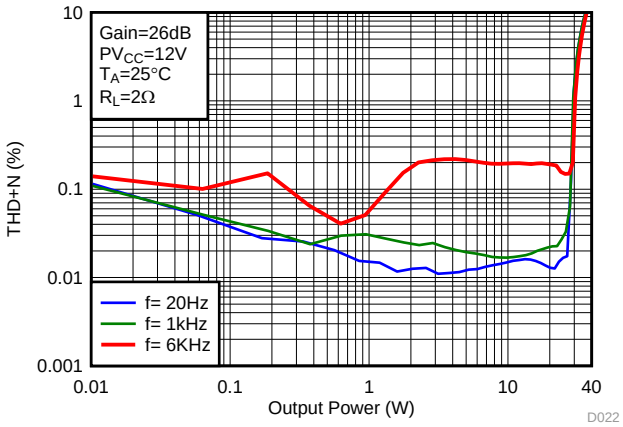


Figure 19. Total Harmonic Distortion + Noise (PBTL) vs Output Power

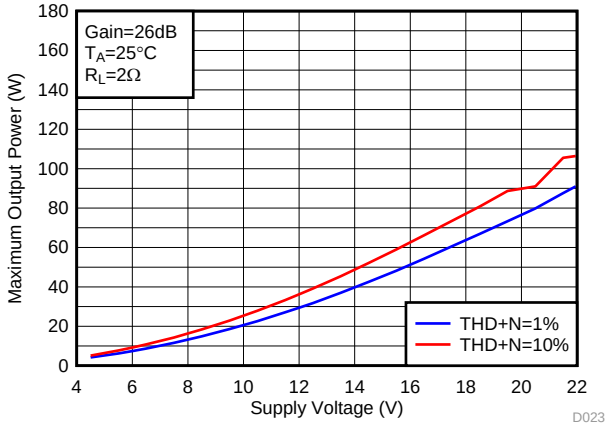


Figure 20. Maximum Output Power (PBTL) vs Supply Voltage

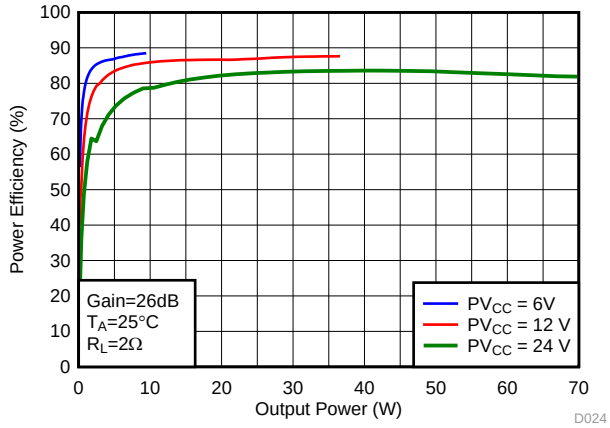


Figure 21. Power Efficiency (PBTL) vs Output Power

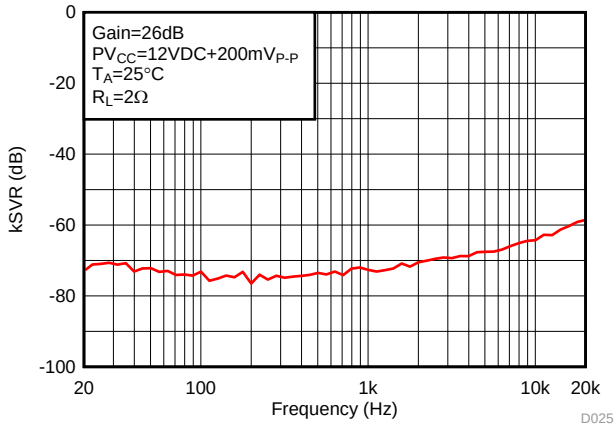


Figure 22. Supply Ripple Rejection Ratio (PBTL) vs Frequency

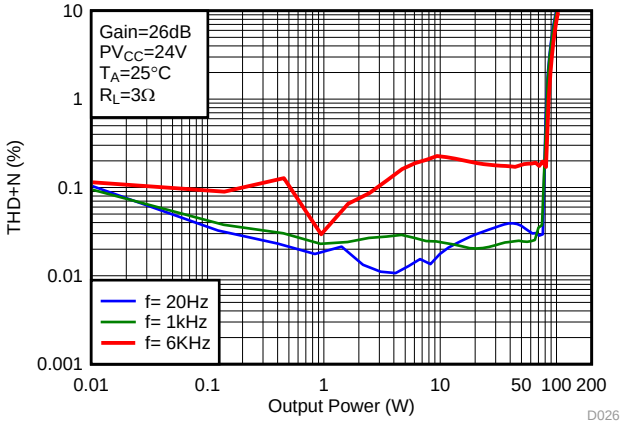


Figure 23. Total Harmonic Distortion + Noise (PBTL) vs Output Power

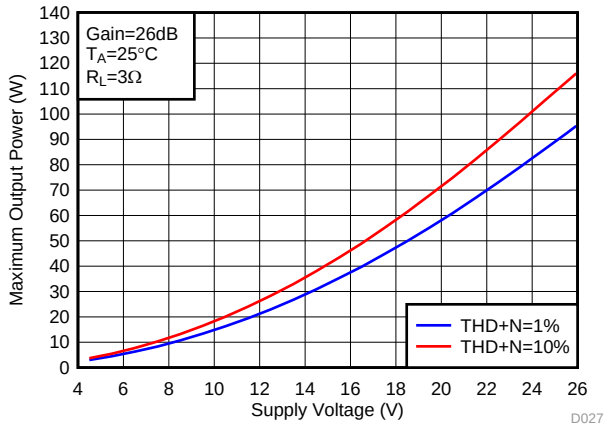


Figure 24. Maximum Output Power (PBTL) vs Supply Voltage

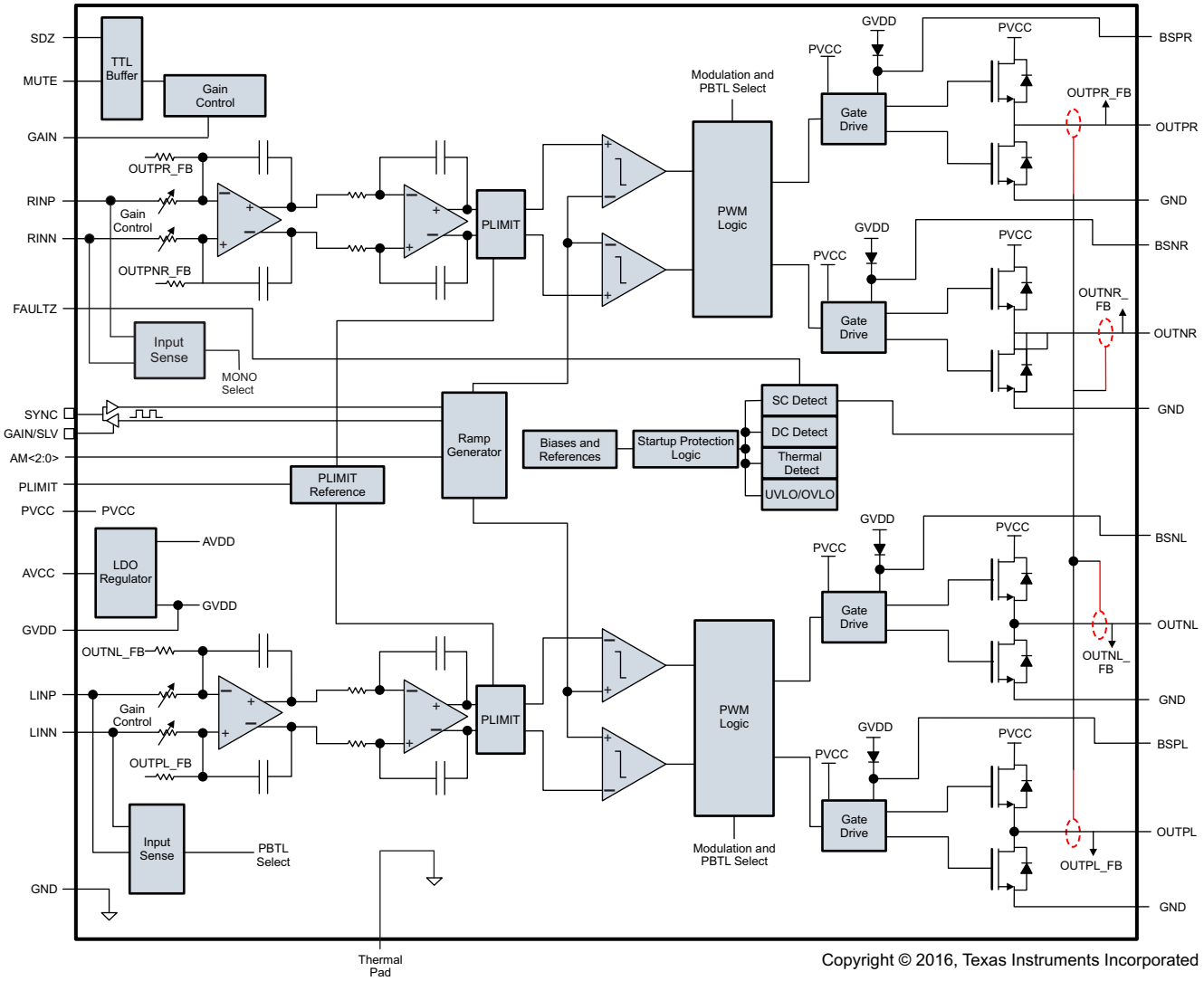
7 Detailed Description

7.1 Overview

The TPA3128D2and TPA3129D2 devices are a highly efficient Class D audio amplifier with extreme low idle power dissipation. It can support as low as 23-mA idle loss current using standard LC filter configurations. It is integrated with 90-mΩ MOSFET that allows output currents up to 7.5 A for TPA3128D2 and 5.5 A for TPA3129D2. The high efficiency allows the amplifier to provide an excellent audio performance without the requirement for a bulky heat sink.

The device can be configured for either master or slave operation by using the SYNC pin. Configuring using the SYNC pin helps to prevent audible beats noise.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Gain Setting and Master and Slave

The gain of the TPA312xD2 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN in Master mode in gains of 20, 26, 32, 36 dB respectively, while the next four stages sets the GAIN in Slave mode in gains of 20, 26, 32, 36 dB respectively. The gain setting is latched during power-up and cannot be changed while device is powered. Table 1 lists the recommended resistor values and the state and gain:

Table 1. Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	26 dB	20 kΩ	100 kΩ	30 kΩ
Master	32 dB	39 kΩ	100 kΩ	15 kΩ
Master	36 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	75 kΩ	47 kΩ	30 kΩ
Slave	32 dB	100 kΩ	39 kΩ	15 kΩ
Slave	36 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

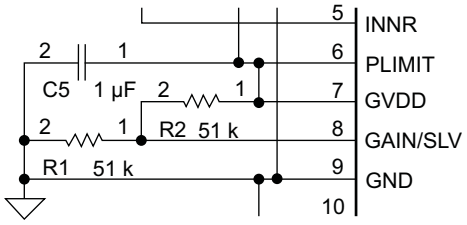

Figure 25. Gain, Master/Slave

In Master mode, SYNC terminal is an output, in Slave mode, SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD.

7.3.2 Input Impedance

The TPA31xxD2 input stage is a fully differential input stage and the input impedance changes with the gain setting from 9 kΩ at 36 dB gain to 60 kΩ at 20 dB gain. Table 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so the minimum value will be higher than 7.2 kΩ. The inputs must be AC-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

$$f = \frac{1}{2\pi Z_i C_i} \tag{1}$$

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. Table 2 lists the recommended ac-couplings capacitors for each gain step. If a –3-dB capacitor is accepted at 20 Hz 10 times lower capacitors can used – for example, a 1-µF capacitor can be used.

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 µF	1.8 Hz
26 dB	30 kΩ	3.3 µF	1.6 Hz
32 dB	15 kΩ	5.6 µF	2.3 Hz
36 dB	9 kΩ	10 µF	1.8 Hz

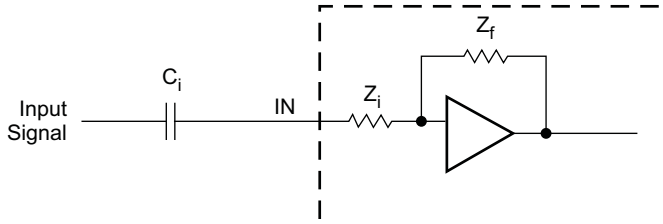

Figure 26. Input Impedance

The input capacitors used should be a type with low leakage, such as quality electrolytic, tantalum, or ceramic capacitors. If a polarized type is used the positive connection should face the input pins which are biased to 3 Vdc.

7.3.3 Startup and Shutdown Operation

The TPA31xxD2 employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to mute and the amplifier to enter a low-current state. Do not leave SDZ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle. At the end of the start-up cycle, the gain is selected and cannot be changed until the next power-up.

7.3.4 PLIMIT Operation

The TPA31xxD2 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail, the amplifier operates as if it was powered by a lower supply voltage, and thereby limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1-µF capacitor from pin PLIMIT to ground to ensure stability.

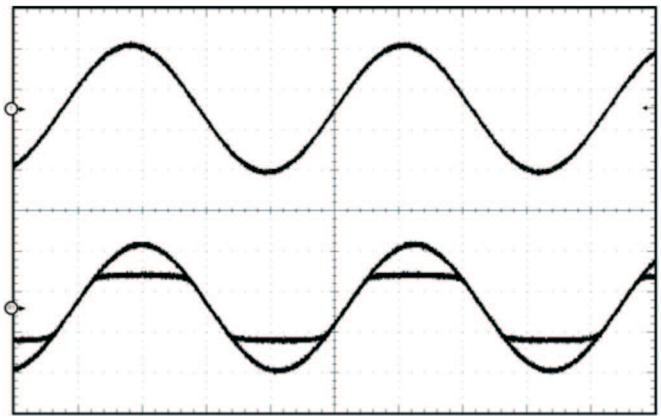

Figure 27. Power Limit Example

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The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. The limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is approximately four times the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

where

- P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)
- R_L is the load resistance.
- R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
- V_P is the peak amplitude, which is limited by "virtual" voltage rail. (2)

Table 3. Power Limit Example

PV_{CC} (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
24 V	GVDD	Open	Short	17.9
24 V	3.3	45 kΩ	51 kΩ	12.67
24 V	2.25	24 kΩ	51 kΩ	9
12 V	GVDD	Open	Short	10.33
12 V	2.25	24 kΩ	51 kΩ	9
12 V	1.5	18 kΩ	68 kΩ	6.3

(1) PLIMIT measurements taken with EVM gain set to 26 dB and input voltage set to 1 V_{rms}.

7.3.5 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. The GVDD Supply can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. Decouple GVDD with a X5R ceramic 1-µF capacitor to GND. The GVDD supply is not intended to be used for external supply. The current consumption should be limited by using resistor voltage dividers for GAIN/SLV and PLIMIT of 100 kΩ or more.

7.3.6 BSPx AND BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input. (See the application circuit diagram in Figure 36.) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

7.3.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA31xxD2 with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input. To use the TPA31xxD2 with a single-ended source, ac ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible to allow the input dc blocking capacitors to become completely charged during the 40-ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

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7.3.8 Device Protection System

The TPA31xxD2 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin will signal if an error is detected according to Table 4:

Table 4. Fault Reporting

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	LATCHED/SELF-CLEARING
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	T_j > 150°C	Low	Output high impedance	Latched
Too High DC Offset	DC output voltage	Low	Output high impedance	Latched
Under Voltage on PVCC	PVCC < 4.5V	–	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 27V	–	Output high impedance	Self-clearing

7.3.9 DC Detect Protection

The TPA31xxD2 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. Connecting the FAULTZ and SDZ pins allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the DC Detect protection latch.

A DC Detect Fault is issued when the output differential voltage of either channel exceeds DC protection threshold level for more than 640 ms at the same polarity. Table 5 below shows some examples of the typical DC Detect Protection threshold for several values of the supply voltage. The Detect Protection Threshold feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

Table 5 lists the minimum output offset voltages required to trigger the DC detect. The outputs must remain at or above the voltage listed in the table for more than 640 ms to trigger the DC detect.

Table 5. DC Detect Threshold

PV_{CC} (V)	V_{OS} - OUTPUT OFFSET VOLTAGE (V)
4.5	1.35
6	1.8
12	3.6
18	5.4

7.3.10 Short-Circuit Protection and Automatic Recovery Feature

The TPA31xxD2 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. Connecting the FAULTZ and SDZ pins allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

In systems where a possibility of a permanent short from the output to PVDD or to a high voltage battery like a car battery can occur, pull the MUTE pin low with the FAULTZ signal with a inverting transistor to ensure a high-Z restart, like shown in the Figure 28 below:

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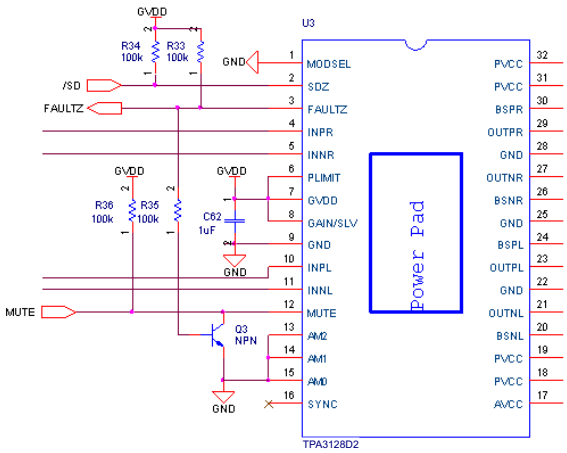

Figure 28. MUTE Driven by Inverted FAULTZ

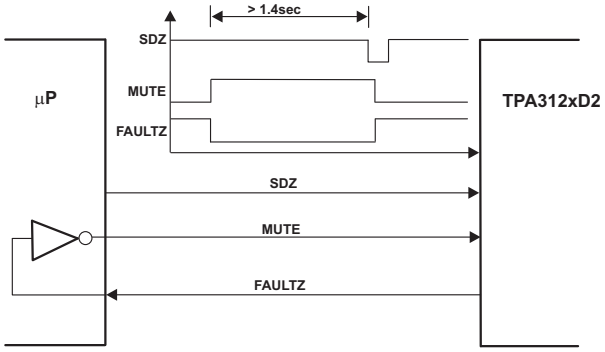

Figure 29. Timing Requirement for SDZ

7.3.11 Thermal Protection

Thermal protection on the TPA31xxD2 prevents damage to the device when the internal die temperature exceeds 150°C. This trip point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state.

If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

7.3.12 Device Modulation Scheme

The TPA3128D2 and TPA3129D2 have the option of running in either BD modulation or low idle-loss mode.

7.3.12.1 BD-Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

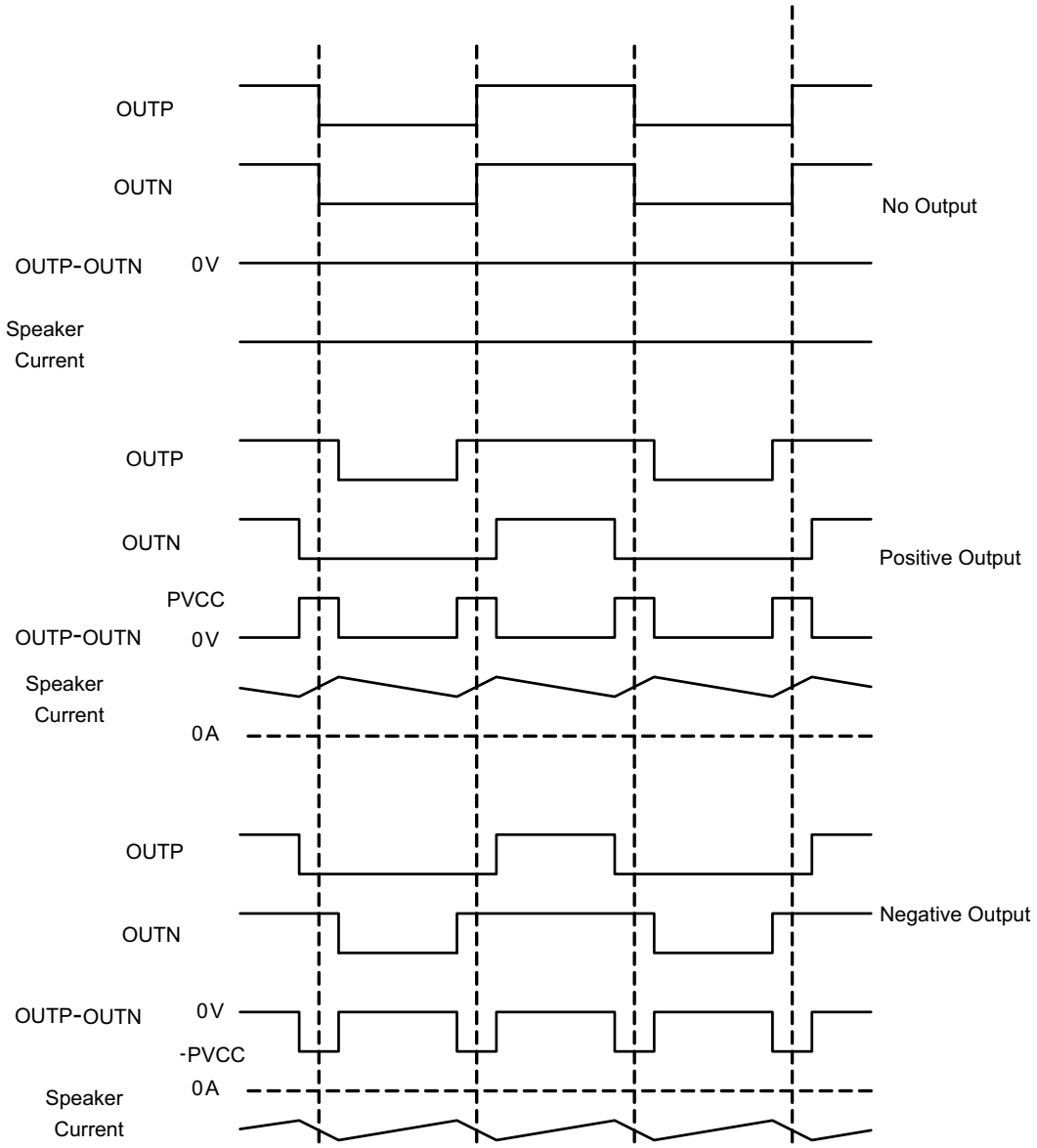

Figure 30. BD Mode Modulation

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7.3.13 Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier-based on AD modulation requires an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × VCC, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is required to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3128D2 and TPA3129D2 modulation schemes have little loss in the load without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not required.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

7.3.14 Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3128D2 and TPA3129D2 amplifiers, a high efficiency class-D audio amplifier can be designed while minimizing interference to surrounding circuits. Designing the amplifier can also be accomplished with only a low-cost ferrite bead filter. In this case the user must carefully select the ferrite bead used in the filter. One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, therefore the user must select a material that is effective in the 10-MHz to 100-MHz range which is key to the operation of the class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. The ferrite bead filter should be used to block radiation in the 30-MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, the ferrite bead must be large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case the user can make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, the device can also estimate the bead current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3136D2 can be seen in the TPA3136D2EVM user guide SLOU444.

A high quality ceramic capacitor is also required for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network would be 18 Ω in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND pins on the IC.

Figure 31 and Figure 32 are TPA3128D2 EN55022 Radiated Emissions results uses TPA3128D2EVM with 8-Ω speakers.

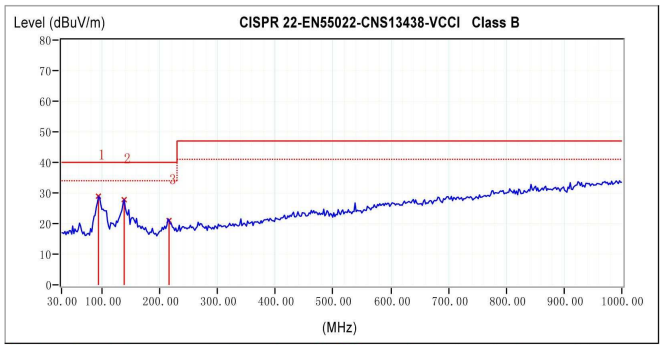

Figure 31. TPA3128D2 Radiated Emissions-Horizontal (PVCC=12V, P_O=1W)

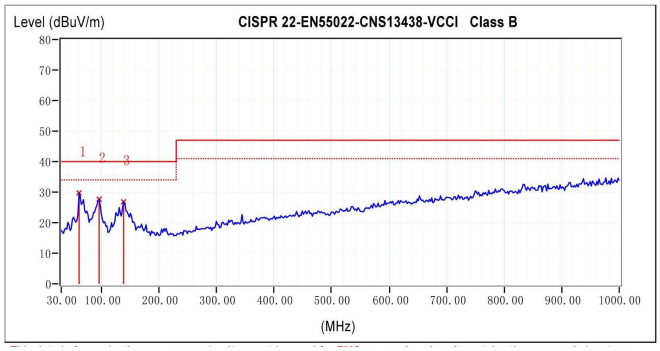

Figure 32. TPA3128D2 Radiated Emissions-Vertical (PVCC=12V, P_O=1W)

7.3.15 When to Use an Output Filter for EMI Suppression

A complete LC reconstruction filter should be added in some circuit instances. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

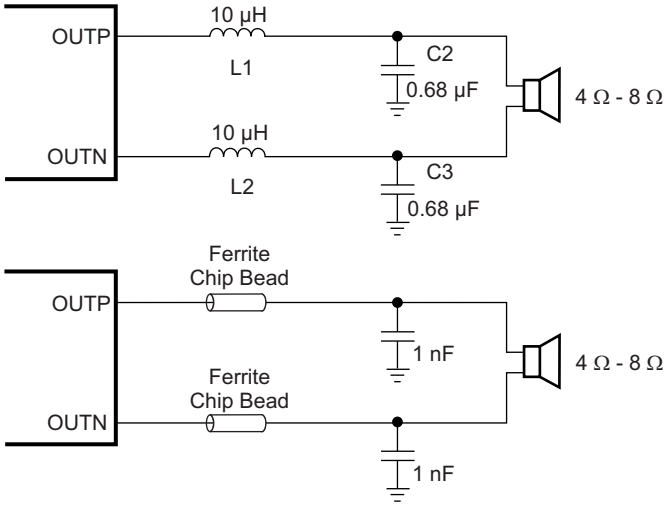

Figure 33. TPA31xxD2 Output Filters

7.3.16 AM Avoidance EMI Reduction

Table 6. AM Frequencies

US	EUROPEAN	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
AM FREQUENCY (kHz)	AM FREQUENCY (kHz)				
	522-540				
540-917	540-914	500	0	0	1
917-1125	914-1122	600 (or 400)	0 0	1 0	0 0
1125-1375	1122-1373	500	0	0	1
1375-1547	1373-1548	600 (or 400)	0 0	1 0	0 0

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Table 6. AM Frequencies (continued)

US	EUROPEAN	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
AM FREQUENCY (kHz)	AM FREQUENCY (kHz)				
1547-1700	1548-1701	600 (or 500)	0 0	1 0	0 1

7.4 Device Functional Modes

7.4.1 PBTL Mode

The TPA3128D2 can be connected in PBTL mode enabling up to 60W output power. This is done by:

- Connect INPL and INNL directly to Ground (without capacitors) this sets the device in Mono mode during power up.
- Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative pin.
- Analog input signal is applied to INPR and INNR.

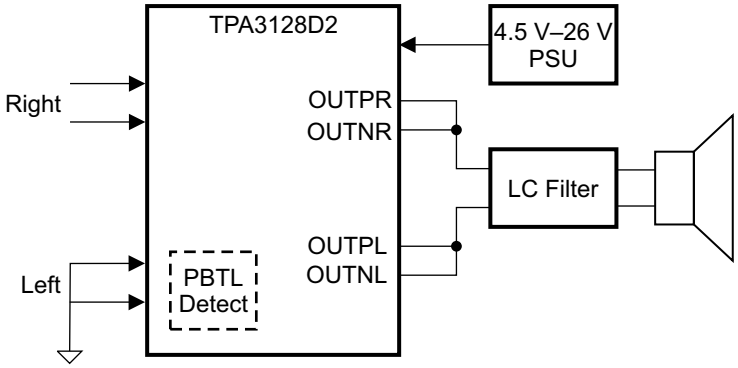

Figure 34. PBTL Mode

7.4.2 Mono Mode (Single Channel Mode)

The and TPA3129D2 can be connected in MONO mode to cut the idle power-loss nearly by half. This is done by:

- Connect INPR and INNR directly to Ground (without capacitors) this sets the device in Mono mode during power up.
- Connect OUTPL and OUTNL to speaker just like normal BTL mode.
- Analog input signal is applied to INPL and INNL.

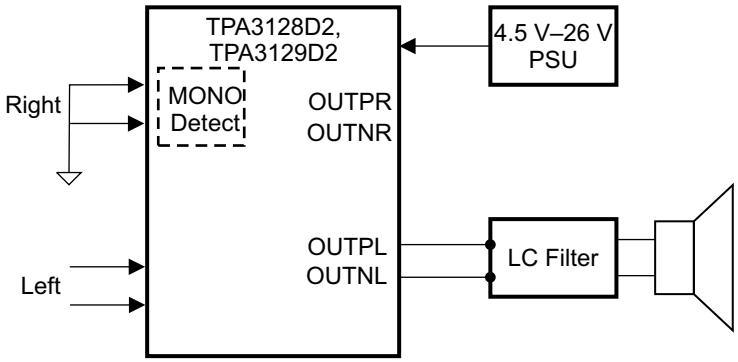

Figure 35. MONO Mode

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section describes a 2.1 Master and Slave application. The Master is configured as stereo outputs and the Slave is configured as mono PBTL output.

8.2 Typical Application

A 2.1 solution, U1 TPA312xD2 in Master mode 400 kHz, BTL, gain if 20 dB, power limit not implemented. U2 in Slave, PBTL mode gain of 20dB. Inputs are connected for differential inputs.

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Typical Application (continued)

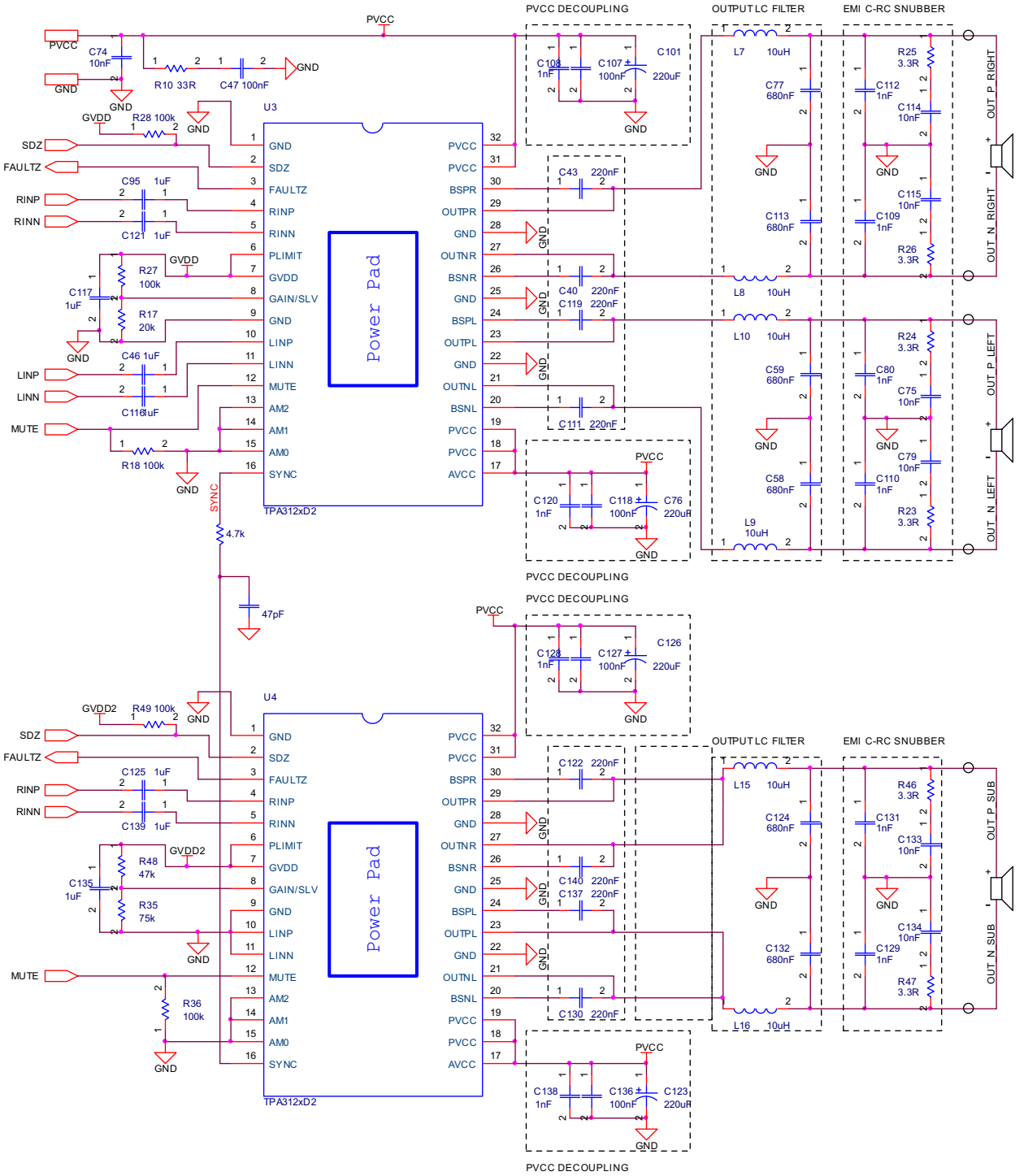

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Figure 36. TPA312xD2 Schematic

Typical Application (continued)

8.2.1 Design Requriements

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range PVCC	4.5 V to 26 V
PWM output frequencies	300kHz, 400 kHz, 500 kHz, 600 kHz, 1 MHz or 1.2 MHz
Maximum output power	50 W

8.2.2 Detailed Design Procedure

The TPA31xxD2 devices are very flexible and easy to use Class D amplifier; therefore the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

- PVCC rail planned for the design
- Speaker or load impedance
- Maximum output power requirement
- Desired PWM frequency

8.2.2.1 Select the PWM Frequency

Set the PWM frequency by using AM0, AM1 and AM2 pins.

8.2.2.2 Select the Amplifier Gain and Master/Slave Mode

In order to select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once these parameters have been determined, calculate the required output voltage swing which delivers the maximum output power.

Choose the lowest analog gain setting that corresponds to produce an output voltage swing greater than the required output swing for maximum power. The analog gain and master/slave mode can be set by selecting the voltage divider resistors (R1 and R2) on the Gain/SLV pin.

8.2.2.3 Select Input Capacitance

Select the bulk capacitors at the PVCC inputs for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed power supply, two 100-μF, 50-V capacitors should be sufficient. One capacitor should be placed near the PVCC inputs at each side of the device. PVCC capacitors should be a low ESR type because they are being used in a high-speed switching application.

8.2.2.4 Select Decoupling Capacitors

Good quality decoupling capacitors must be added at each of the PVCC inputs to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances.

8.2.2.5 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.22-μF, 25-V capacitors of X5R quality or better.

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8.2.3 Application Curves

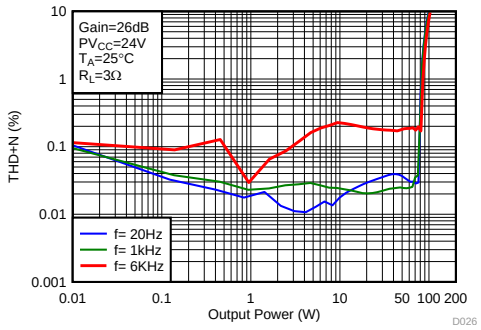

Figure 37. Total Harmonic Distortion + Noise (PBTL) vs Output Power

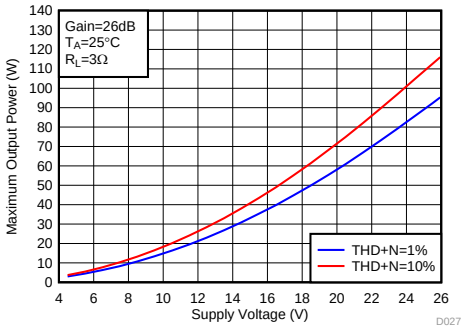

Figure 38. Maximum Output Power (PBTL) vs Supply Voltage

9 Power Supply Recommendations

The power supply requirements for the TPA312xD2 consist of one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the TPA312xD2 to generate the voltages necessary for the internal circuitry of the audio path. The voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The high voltage supply, between 4.5 V and 26 V, supplies the analog circuitry (AVCC) and the power stage (PVCC). The AVCC supply feeds internal LDO including GVDD. This LDO output are connected to external pins for filtering purposes, but should not be connected to external circuits. GVDD LDO output have been sized to provide current necessary for internal functions but not for external loading.

9.1 Power Supply Mode

The TPA3128D2 and TPA3129D2 devices support both single and dual power supply modes. Dual power supply mode is benefit for low PVCC power consumption. For dual power supply mode application, when AVCC is supplied with 4.5V power, PVCC is recommended to be lower than 20V. When PVCC is supplied with power greater than 20V, AVCC is recommended to be higher than 6V.

10 Layout

10.1 Layout Guidelines

The TPA312xD2 can be used with a small, inexpensive ferrite bead output filter for most applications. However, because the class-D switching edges are fast, the layout of the printed circuit board must be planned carefully. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (100 µF or greater) bulk power supply decoupling capacitors should be placed near the TPA312xD2 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1 nF and a larger mid-frequency cap of value between 100 nF and 1 µF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the TPA312xD2.
- Output filter — The ferrite EMI filter (see Figure 33) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.

Layout Guidelines (continued)

For an example layout, see the TPA3128D2 Evaluation Module (TPA3128D2EVM) User Guide (SLOU336). Both the EVM user manual and the thermal pad application reports, SLMA002 and SLMA004, are available on the TI Web site at http://www.ti.com.

10.2 Layout Example

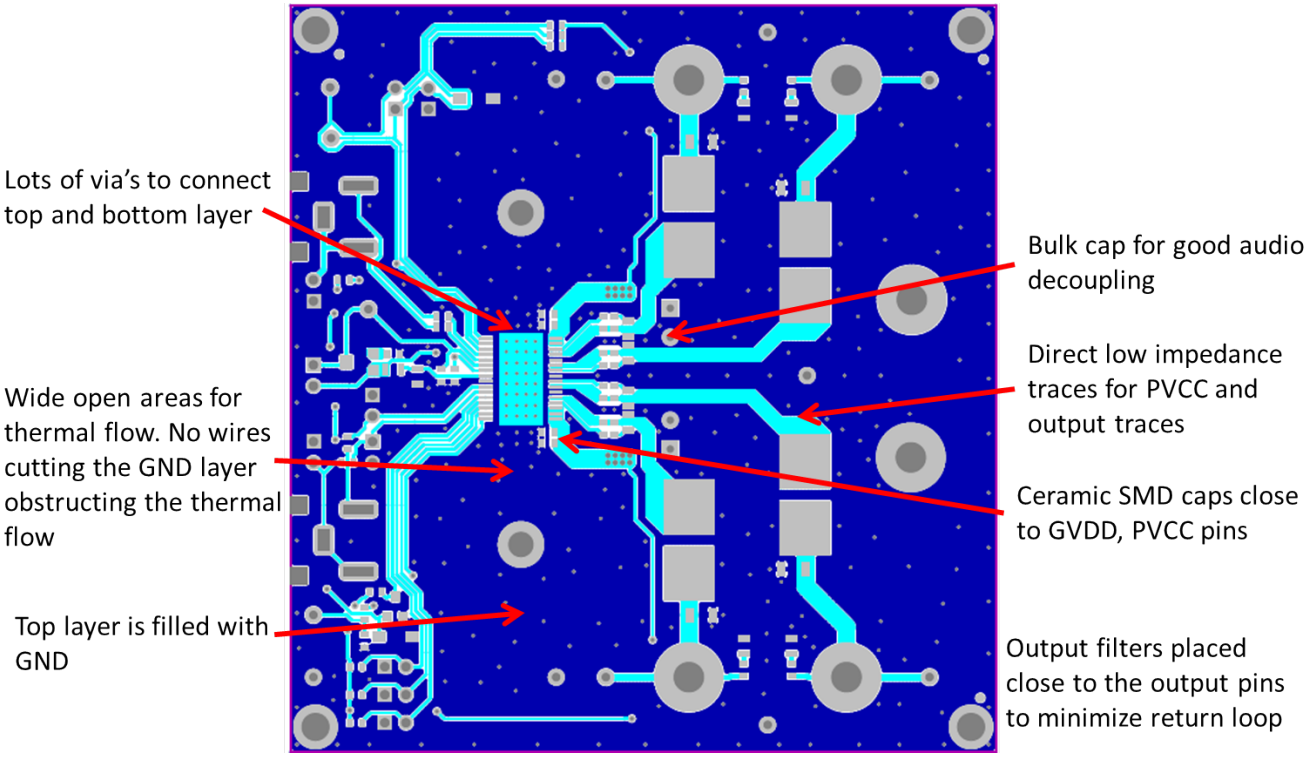

Figure 39. Layout Example Top

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Layout Example (continued)

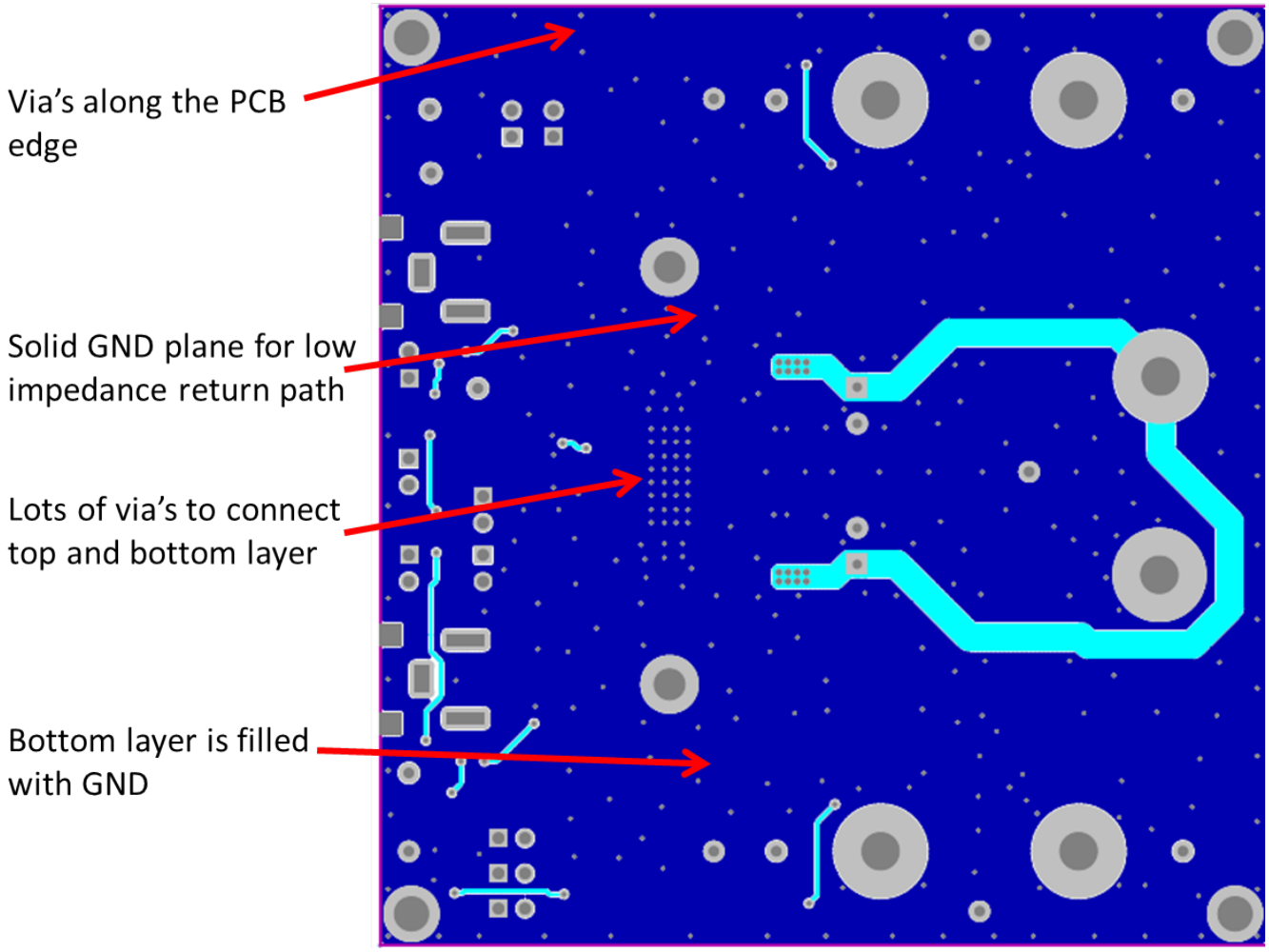

Figure 40. Layout Example Bottom

11 Device and Documentation Support

11.1 Documentation Support

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3128D2DAP	Active	Production	HTSSOP (DAP) | 32	46 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3128D2
TPA3128D2DAP.A	Active	Production	HTSSOP (DAP) | 32	46 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3128D2
TPA3128D2DAPR	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3128D2
TPA3128D2DAPR.A	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3128D2
TPA3128D2DAPRG4	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3128D2
TPA3128D2DAPRG4.A	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3128D2
TPA3129D2DAP	Active	Production	HTSSOP (DAP) | 32	46 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3129D2
TPA3129D2DAP.A	Active	Production	HTSSOP (DAP) | 32	46 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3129D2
TPA3129D2DAPR	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3129D2
TPA3129D2DAPR.A	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3129D2
TPA3129D2DAPRG4	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3129D2
TPA3129D2DAPRG4.A	Active	Production	HTSSOP (DAP) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3129D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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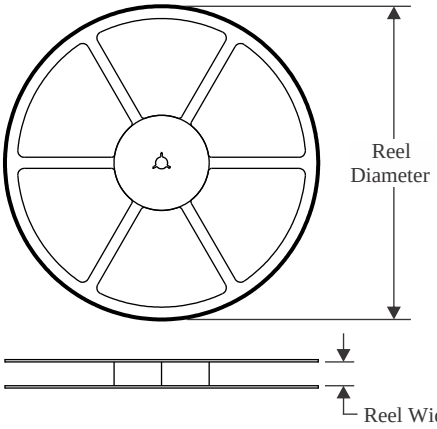
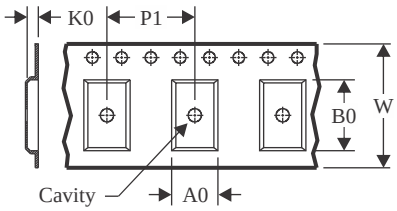
TAPE AND REEL INFORMATION

REEL DIMENSIONS

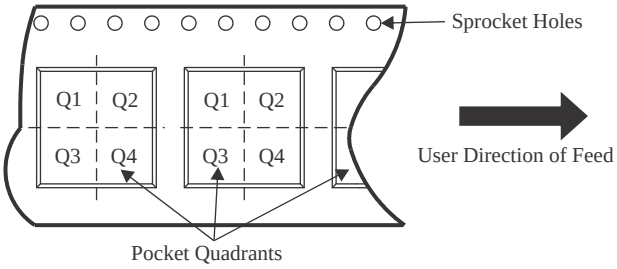


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

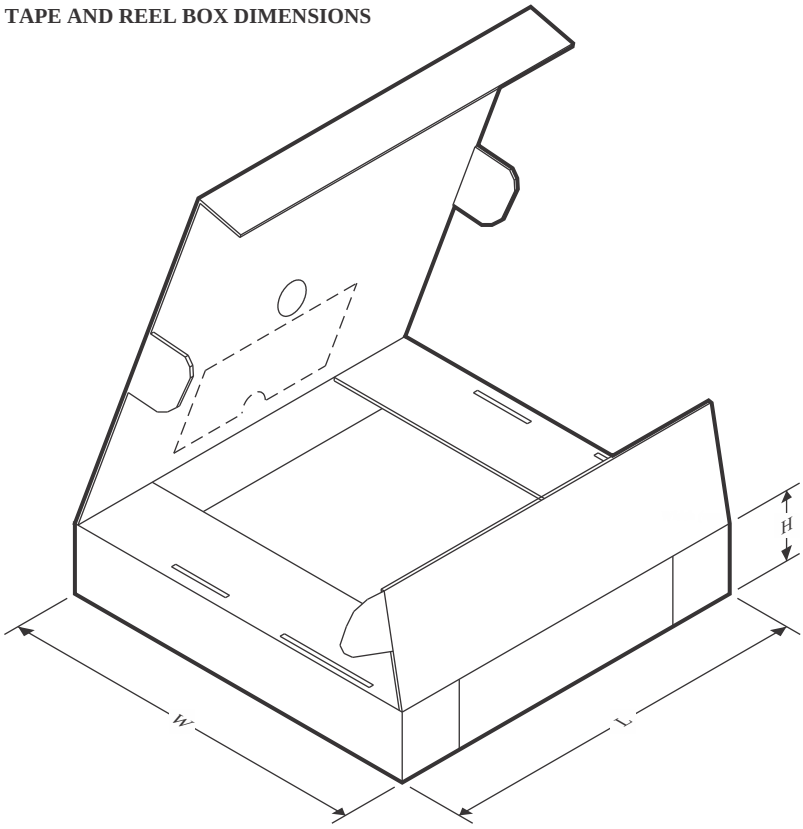
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3128D2DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPA3128D2DAPRG4	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPA3129D2DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1
TPA3129D2DAPRG4	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

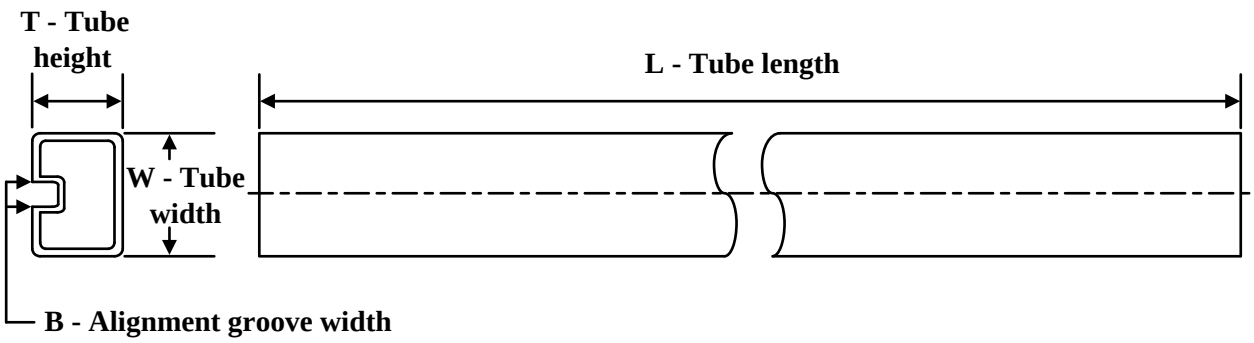
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3128D2DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0
TPA3128D2DAPRG4	HTSSOP	DAP	32	2000	350.0	350.0	43.0
TPA3129D2DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0
TPA3129D2DAPRG4	HTSSOP	DAP	32	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3128D2DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TPA3128D2DAP.A	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TPA3129D2DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TPA3129D2DAP.A	DAP	HTSSOP	32	46	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

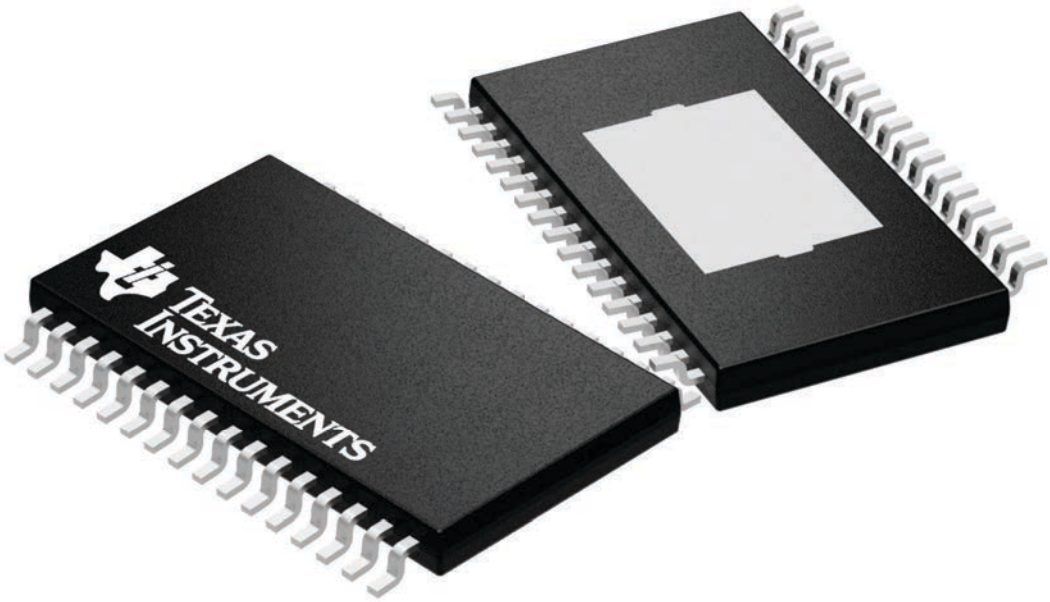
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 11, 0.65 mm pitch

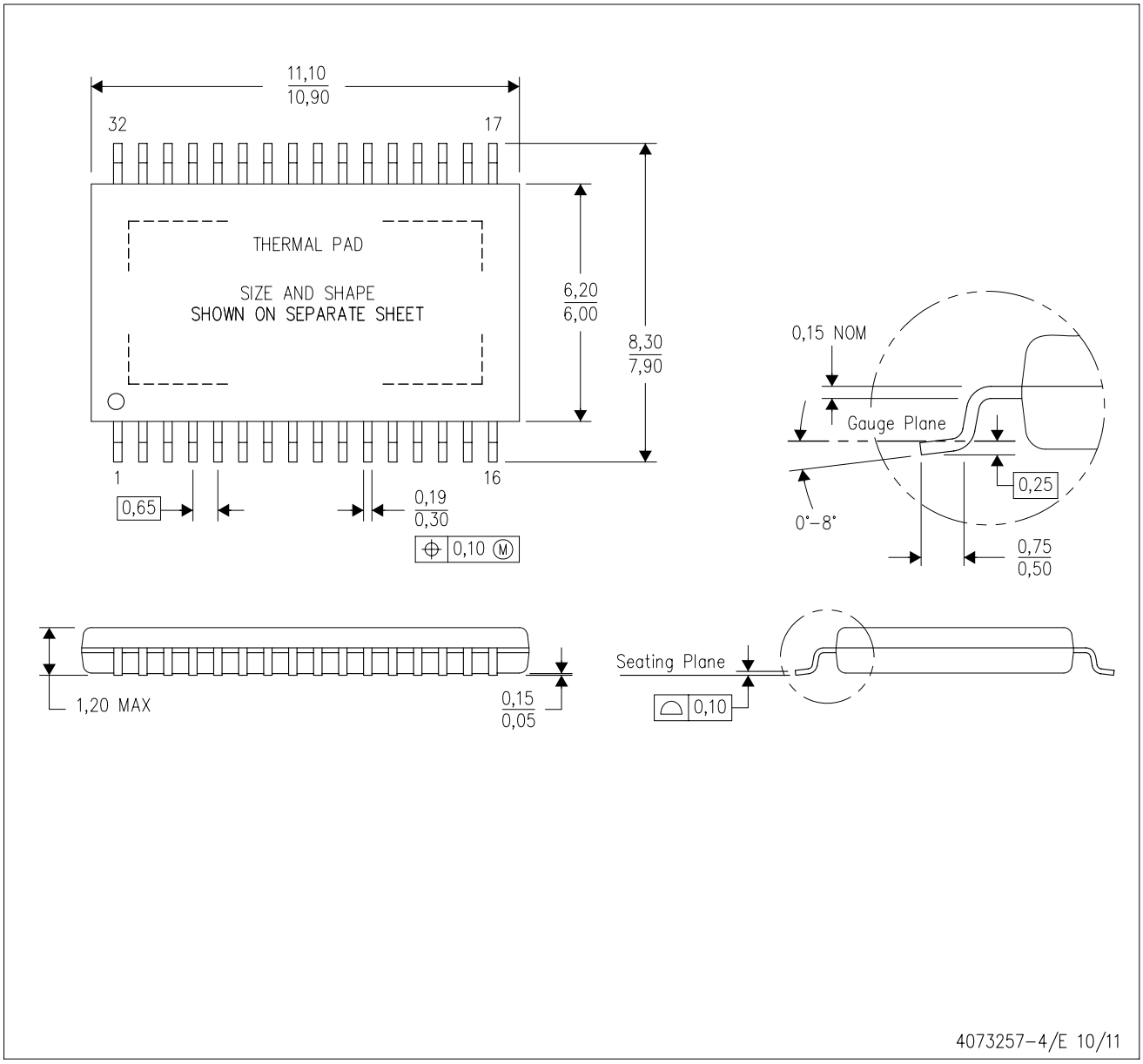
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- F. Falls within JEDEC MO-153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

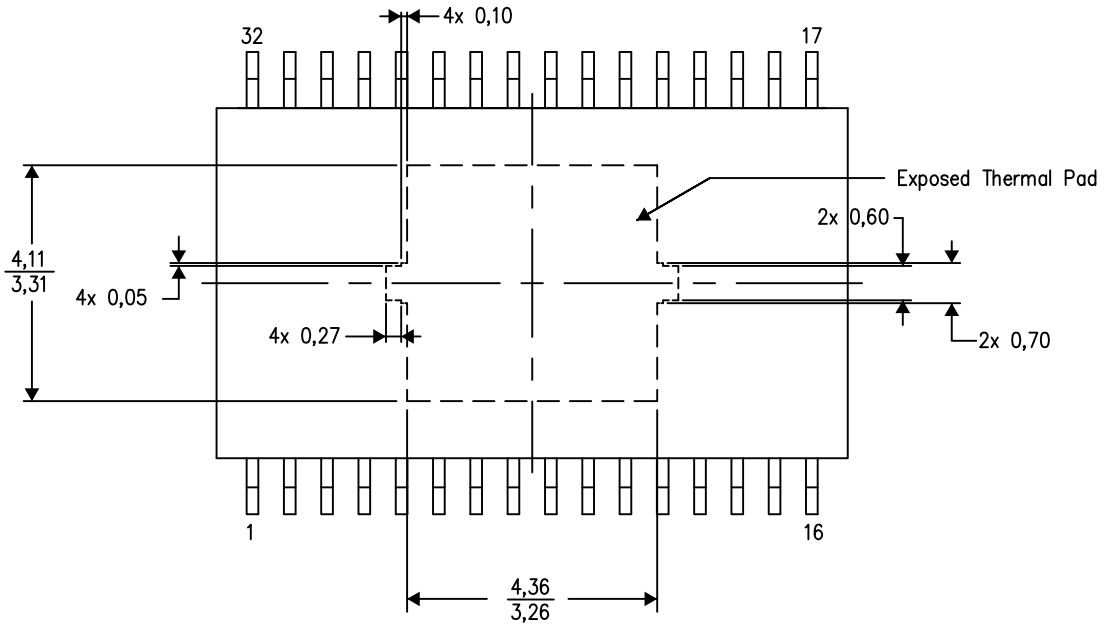
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

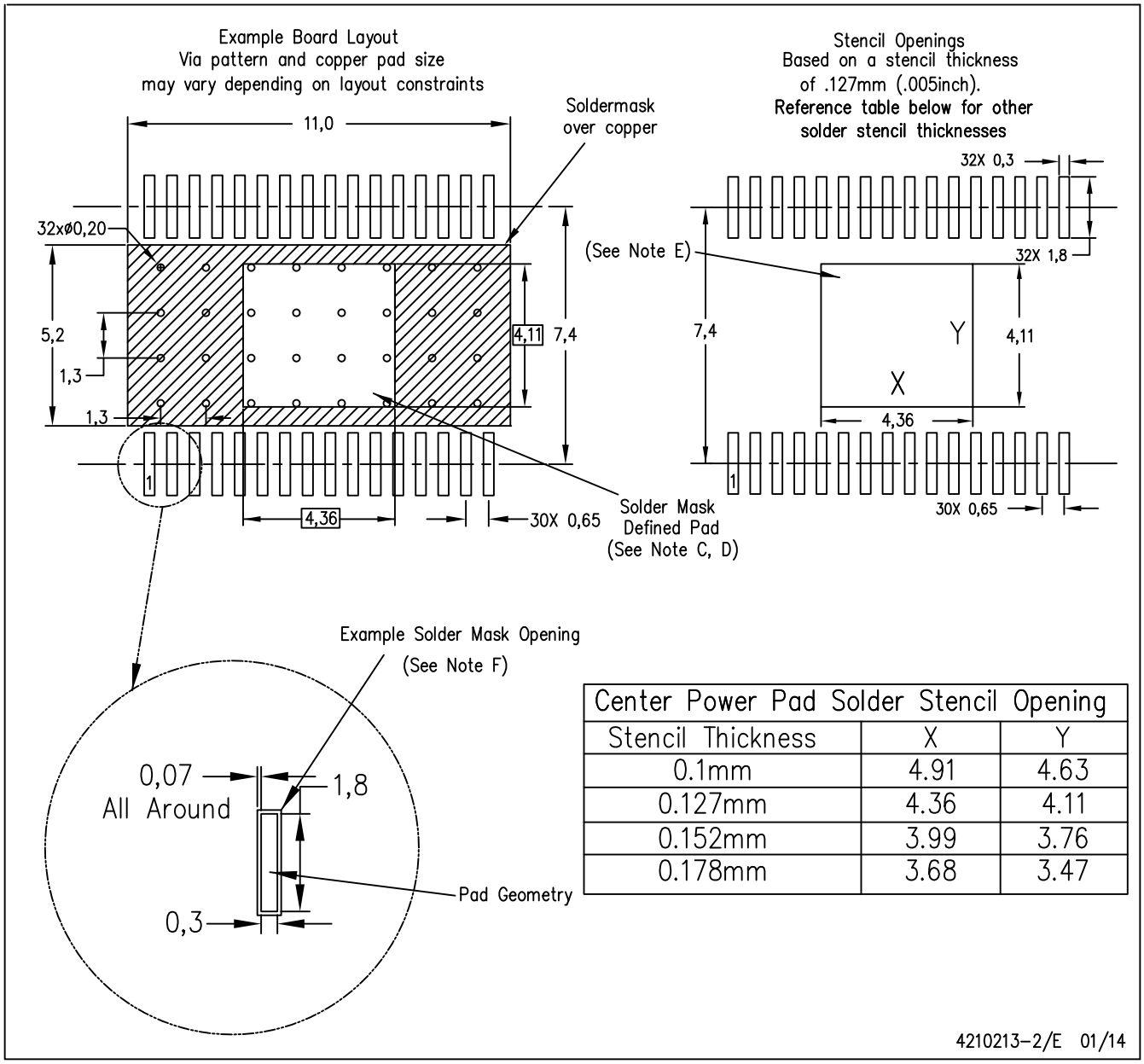
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- F. Contact the board fabrication site for recommended soldermask tolerances.

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