CLASS-G DIRECTPATH™ STEREO HEADPHONE AMPLIFIER WITH I²C VOLUME CONTROL

Check for Samples: TPA6140A2

FEATURES

- **TI Class-G Technology Significantly Prolongs Battery Life and Music Playback Time**
  - **0.6 mA / Ch Quiescent Current**
  - **50% to 80% Lower Quiescent Current than Ground-Referenced Class-AB Headphone Amplifiers**
- **DirectPath™ Technology Eliminates Large Output DC-Blocking Capacitors**
  - **Outputs Biased at 0 V**
  - **Improves Low Frequency Audio Fidelity**
- **I²C Volume Control**
  - **–59 dB to +4 dB Gain**
- **Active Click and Pop Suppression**
- **Fully Differential Inputs Reduce System Noise**
  - **Also Configurable as Single-Ended Inputs**
- **SGND Pin Eliminates Ground Loop Noise**
- **Wide Power Supply Range: 2.5 V to 5.5 V**
- **100 dB Power Supply Noise Rejection**
- **Short-Circuit Current Limiter**
- **Thermal-Overload Protection**
- **Software Compatible with TPA6130A2**
- **0,4 mm Pitch, 1,6 mm × 1,6 mm WCSP Package**

APPLICATIONS

- **Cellular Phones / Music Phones**
- **Portable Media / MP3 Players**
- **Portable CD / DVD Players**

DESCRIPTION

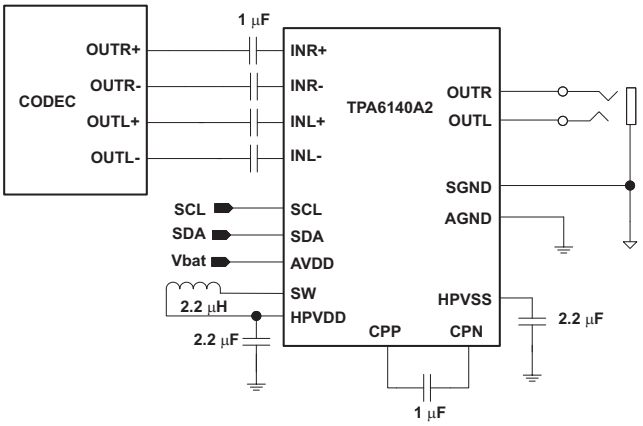
The TPA6140A2 (also known as TPA6140) is a Class-G DirectPath™ stereo headphone amplifier with built-in I²C volume control. Class-G technology maximizes battery life by adjusting the voltage supplies of the headphone amplifier based on the audio signal level. At low level audio signals, the internal supply voltage is reduced to minimize power dissipation. DirectPath™ technology eliminates external DC-blocking capacitors.

The device operates from a 2.5 V to 5.5 V supply voltage. Class-G operation keeps total supply current below 5.0 mA while delivering 500 µW per channel into 32 Ω. Shutdown mode reduces the supply current to less than 3 µA and is activated through the I²C interface.

The TPA6140A2 (TPA6140) I²C register map is compatible to the TPA6130A2, simplifying software development.

The amplifier outputs have short-circuit and thermal-overload protection along with ±8 kV HBM ESD protection, simplifying end equipment compliance to the IEC 61000-4-2 ESD standard.

The TPA6140A2 (TPA6140) is available in a 0,4 mm pitch, 16-bump 1,6 mm × 1,6 mm WCSP (YFF) package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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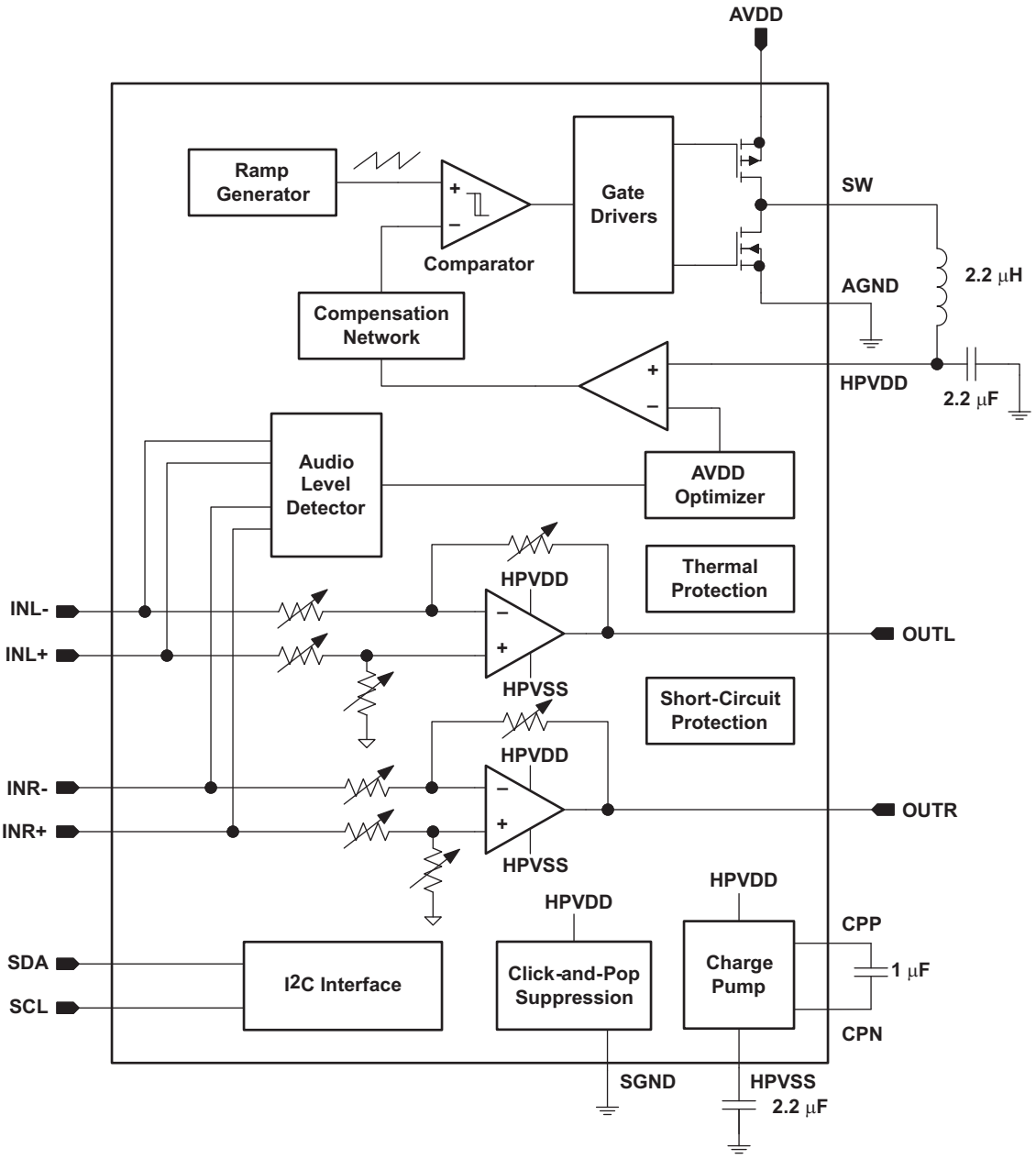
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

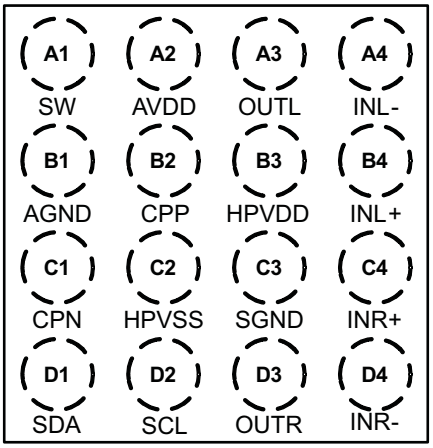
FUNCTIONAL BLOCK DIAGRAM



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DEVICE PINOUT

WCSP PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		INPUT / OUTPUT / POWER (I/O/P)	DESCRIPTION
NAME	BALL WCSP		
INL–	A4	I	Inverting left input for differential signals; connect to left input signal through 1 µF capacitor for single-ended input applications
INL+	B4	I	Non-inverting left input for differential signals; connect to ground through 1 µF capacitor for single-ended input applications
INR–	D4	I	Inverting right input for differential signals; connect to right input signal through 1 µF capacitor for single-ended input applications
INR+	C4	I	Non-inverting right input for differential signals; connect to ground through 1 µF capacitor for single-ended input applications
SGND	C3	I	Sense Ground; connect to shield terminal of headphone jack or to AGND
SDA	D1	I/O	I^2C Data; 1.8 V logic compliant
SCL	D2	I	I^2C Clock; 1.8 V logic compliant
OUTL	A3	O	Left headphone amplifier output; connect to left terminal of headphone jack
OUTR	D3	O	Right headphone amplifier output; connect to right terminal of headphone jack
CPP	B2	P	Charge pump positive flying cap; connect to positive side of capacitor between CPP and CPN
CPN	C1	P	Charge pump negative flying cap; connect to negative side of capacitor between CPP and CPN
SW	A1	P	Buck converter switching node
AVDD	A2	P	Primary power supply for device
HPVDD	B3	P	Power supply for headphone amplifier (DC/DC output node)
AGND	B1	P	Main Ground for headphone amplifiers, DC/DC converter, and charge pump
HPVSS	C2	P	Charge pump output; connect 2.2 µF capacitor to GND

ORDERING INFORMATION

T_A	PACKAGED DEVICES (1)	PART NUMBER (2)	SYMBOL
–40°C to 85°C	16-ball, 1,6 mm × 1,6 mm WCSP	TPA6140A2YFFR	AIFI
	16-ball, 1,6 mm × 1,6 mm WCSP	TPA6140A2YFFT	AIFI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) YFF packages are only available taped and reeled. The suffix “R” indicates a reel of 3000, the suffix “T” indicates a reel of 250.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

			VALUE / UNIT
	Supply voltage, AVDD		–0.3 V to 6.0 V
	Amplifier supply voltage, HPVDD		–0.3 V to 2.0 V
V_I	Input voltage		–0.3 V to HPV_{DD} +0.3 V
	I^2C voltage		–0.3 V to AVDD
	Output continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 85°C
	ESD Protection – HBM	OUTL, OUTR, SGND	8 kV
		All other pins	2 kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE(1) (2)

PACKAGE	T_A < 25°C POWER RATING	OPERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
YFF (WCSP)	1.25 W	10 mW/°C	800 mW	650 mW

(1) Derating factor measured with JEDEC High K board: 1S0P – One signal layer and zero plane layers.
(2) See JEDEC Standard 51-3 for Low-K board, JEDEC Standard 51-7 for High-K board, and JEDEC Standard 51-12 for using package thermal information. See JEDEC document page for downloadable copies: http://www.jedec.org/download/default.cfm.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
	Supply voltage, AV_{DD}		2.5	5.5	V
V_{IH}	High-level input voltage	SDA, SCL	1.3		V
V_{IL}	Low-level input voltage	SDA, SCL		0.35	V
	Voltage applied to Output; OUTR, OUTL (when SWS = 1, device disabled)		–0.3	3.6	V
	Voltage applied to Output; OUTR, OUTL (when SWS = 0, HiZ_L = HiZ_R = 1, device in HI-Z mode)		–1.8	1.8	V
T_A	Operating free-air temperature		–40	85	°C

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ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	AV_{DD} = 2.5 V to 5.5 V, inputs grounded, GAIN = 0 dB		90	105		dB
CMRR	Common-mode rejection ratio	HPV_{DD} = 1.3 V to 1.8 V, GAIN = 0 dB			68		dB
$\|I_{IH}\|$	High-level input current	AV_{DD} = 2.5 V to 5.5 V, V_I = AV_{DD}	SCL, SDA			1	µA
$\|I_{IL}\|$	Low-level input current	AV_{DD} = 2.5 V to 5.5 V, V_I = 0 V	SCL, SDA			1	µA
I_{SD}	Soft shutdown current	SW Shutdown mode, V_{DD} = 2.5 V to 5.5 V, SWS bit = 1			1	3	µA
I_{DD}	Total supply current	AV_{DD} = 3.6 V HPVDD = 1.3 V, Amplifiers active, no load, no input signal			1.2	2.0	mA
		AV_{DD} = 3.6 V, P_{OUT} = 100 µW into 32 Ω(1), f_{AUD} = 1 kHz			2.5		
		AV_{DD} = 3.6 V, P_{OUT} = 500 µW into 32 Ω(1), f_{AUD} = 1 kHz			4.0		
		AV_{DD} = 3.6 V, P_{OUT} = 1 mW into 32 Ω(1), f_{AUD} = 1 kHz			6.8		
		AV_{DD} = 3.6 V, HiZ_L = HiZ_R = HIGH (High output impedance mode)			1.0	2.0	

(1) Per channel output power assuming a 10 dB crest factor

TIMING CHARACTERISTICS

For I^2C interface signals over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Frequency, SCL	No wait states			400	kHz
$t_{W(H)}$	Pulse duration, SCL high		0.6			µs
$t_{W(L)}$	Pulse duration, SCL low		1.3			µs
t_{SU1}	Setup time, SDA to SCL		100			µs
t_{H1}	Hold time, SCL to SDA		10			ns
$t_{(BUF)}$	Bus free time between stop and start condition		1.3			µs
t_{SU2}	Setup time, SCL to start condition		0.6			µs
t_{H2}	Hold time, start condition to SCL		0.6			µs
t_{SU3}	Setup time, SCL to stop condition		0.6			µs

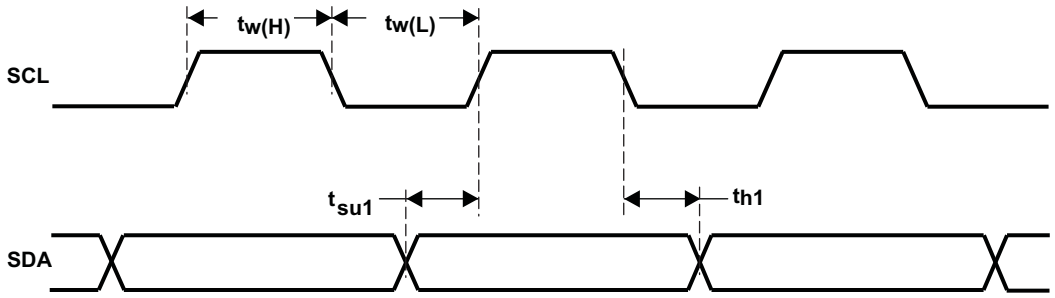


Figure 1. SCL and SDA Timing

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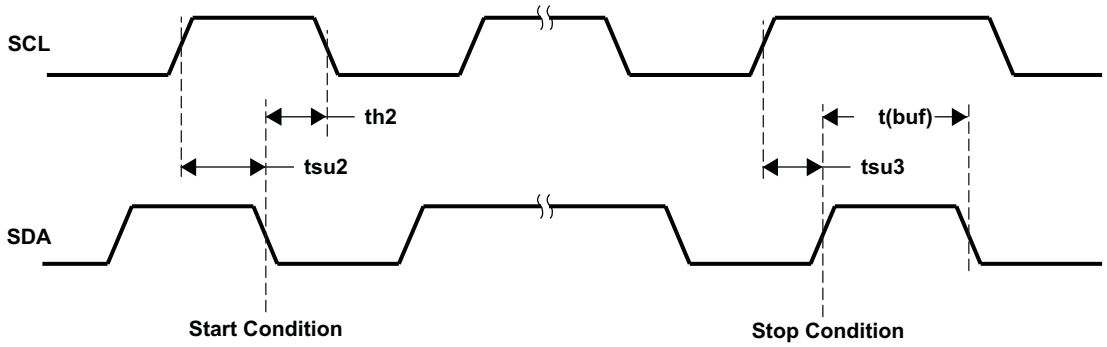


Figure 2. Start and Stop Conditions Timing

OPERATING CHARACTERISTICS

AV_{DD} = 3.6 V , T_A = 25°C, GAIN = 0 dB, R_L = 32 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power(1) (Outputs in Phase)	AV_{DD} = 2.7V, THD = 1%, f = 1 kHz		26		mW
		AV_{DD} = 2.7V, THD = 10%, f = 1 kHz		32		
		AV_{DD} = 2.7V, THD = 1%, f = 1 kHz, R_L = 16Ω		25		
THD+N	Total harmonic distortion plus noise(2)	P_O = 10 mW into 16 Ω, f = 1 kHz		0.02%		
		P_O = 20 mW into 32 Ω, f = 1 kHz		0.01%		
k_{SVR}	AC-Power supply rejection ratio	200 mVpp ripple, f = 217 Hz	80	100		dB
		200 mVpp ripple, f = 4 kHz		90		
ΔA_V	Gain matching	Between left and right channels		1%		
V_{OS}	Output offset voltage	AV_{DD} = 2.5 V to 5.5 V, inputs grounded	–0.5	0	0.5	mV
E_n	Noise output voltage	A-weighted		5.3		μV_{RMS}
f_{BUCK}	Buck converter switching frequency	P_O = 0.5 mW into 32 Ω, f = 1 kHz		600		kHz
f_{PUMP}	Charge pump switching frequency	P_O = 0.5 mW into 32 Ω, f = 1 kHz		315		kHz
		P_O = 15 mW into 32 Ω, f = 1 kHz		1260		
	Start-up time from shutdown			5		ms
$R_{IN,SE}$	Single Ended Input impedance	Gain = 4 dB, per input node		15.6		kΩ
$R_{IN,DF}$	Differential input impedance	Gain = 4 dB, per input node		31.2		kΩ
SNR	Signal-to-noise ratio	V_{OUT} = 1 V_{RMS}, GAIN = 4 dB, no load		105		dB
	Thermal shutdown	Threshold		165		°C
		Hysteresis		35		
$Z_{O,SD}$	Output impedance in shutdown	SWS = 1, DC value		8		kΩ
$Z_{O,HI-Z}$	Output impedance in Hi-Z mode	40 kHz, 1.8 V_{PEAK} signal max		8.5		kΩ
		6 MHz, 1.8 V_{PEAK} signal max		600		Ω
		13 MHz, 1.8 V_{PEAK} signal max		400		Ω
	Crosstalk	P_O = 15 mW, f = 1 kHz		–80		dB
V_{CM}	Input common-mode voltage range		0		1.4	V

(1) Per channel output power
(2) A-weighted

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TYPICAL CHARACTERISTICS

T_A = 25°C, AV_{DD} (V_{DD}) = 3.6 V, GAIN = 0 dB, C_{HPVDD} = C_{HPVSS} = 2.2 µF, C_{INPUT} = C_{FLYING} = 1 µF, Outputs out of phase

QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

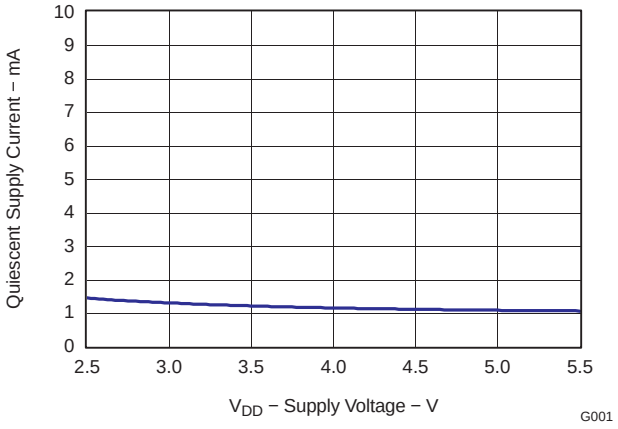


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

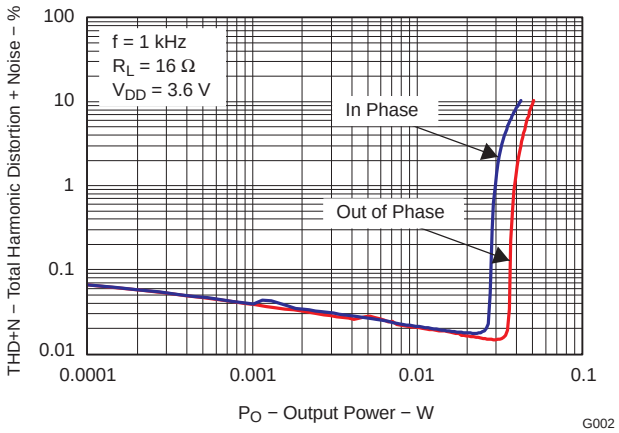


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

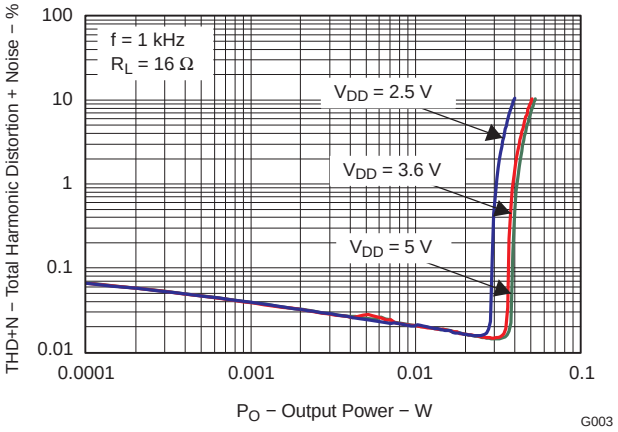


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

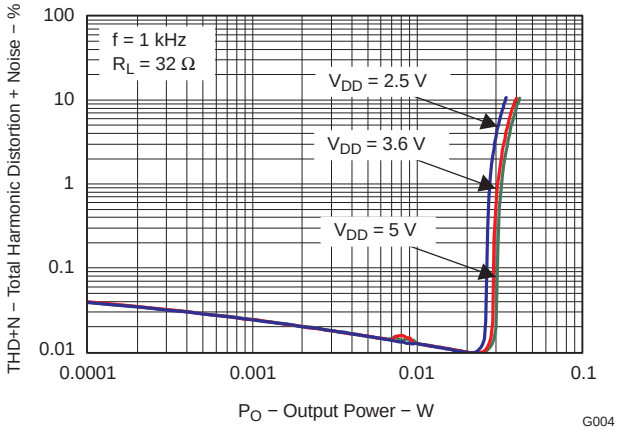


Figure 6.

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AV_{DD} (V_{DD}) = 3.6 V, GAIN = 0 dB, C_{HPVDD} = C_{HPVSS} = 2.2 µF, C_{INPUT} = C_{FLYING} = 1 µF, Outputs out of phase

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

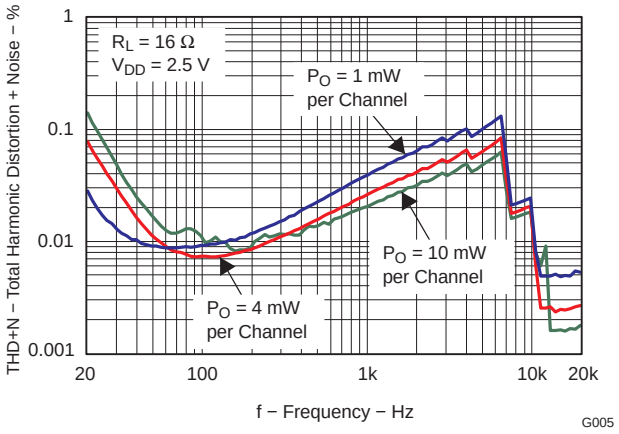


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

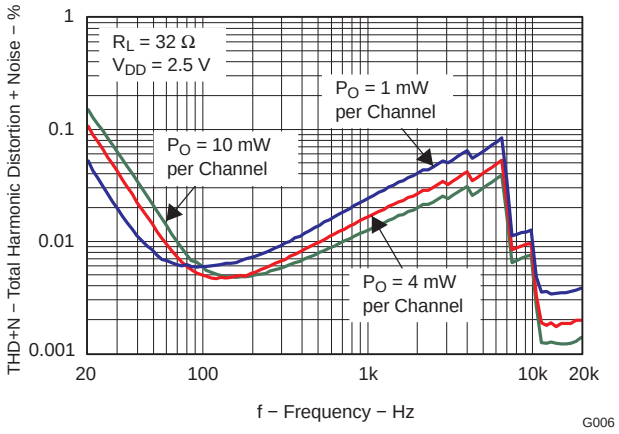


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

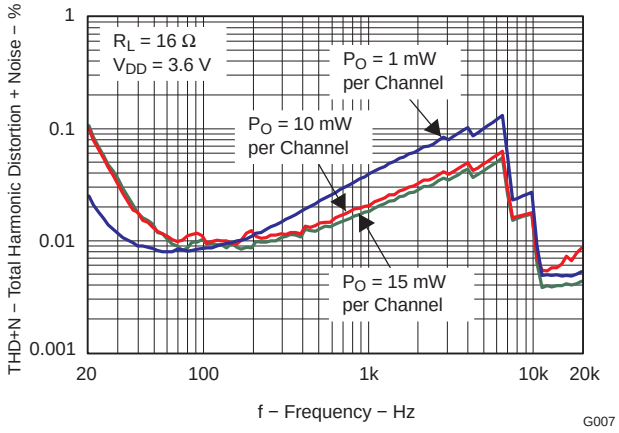


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

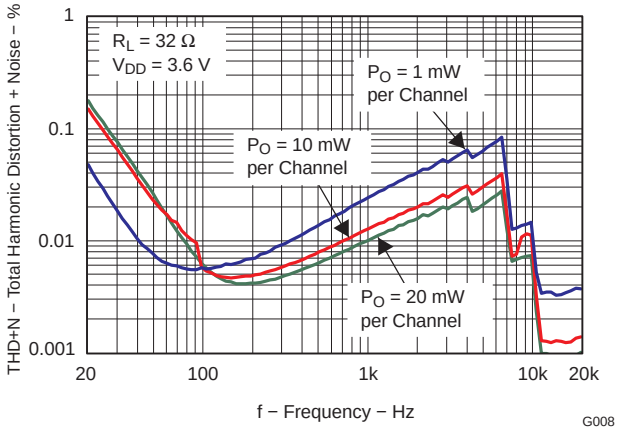


Figure 10.

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AV_{DD} (V_{DD}) = 3.6 V, GAIN = 0 dB, C_{HPVDD} = C_{HPVSS} = 2.2 µF, C_{INPUT} = C_{FLYING} = 1 µF, Outputs out of phase

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

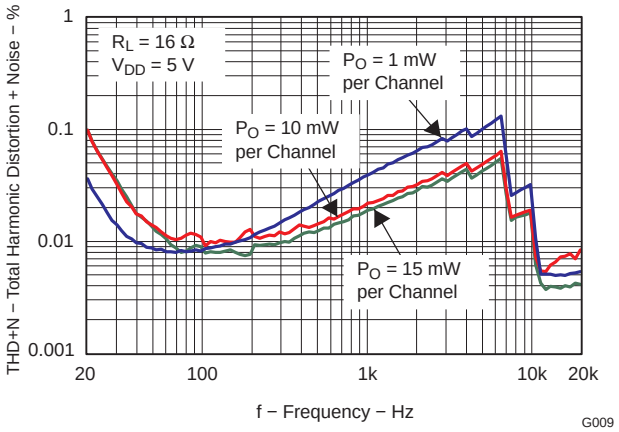


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

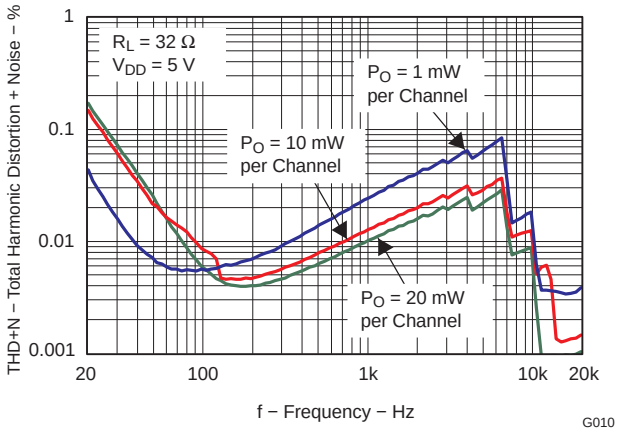


Figure 12.

OUTPUT POWER PER CHANNEL vs SUPPLY VOLTAGE

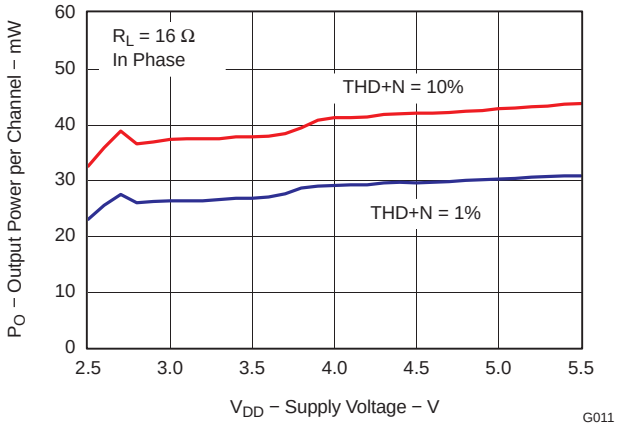


Figure 13.

OUTPUT POWER PER CHANNEL vs SUPPLY VOLTAGE

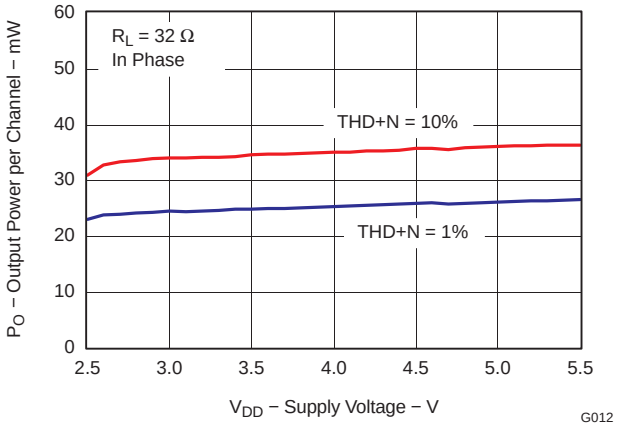


Figure 14.

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AV_{DD} (V_{DD}) = 3.6 V, GAIN = 0 dB, C_{HPVDD} = C_{HPVSS} = 2.2 µF, C_{INPUT} = C_{FLYING} = 1 µF, Outputs out of phase

OUTPUT POWER vs LOAD RESISTANCE

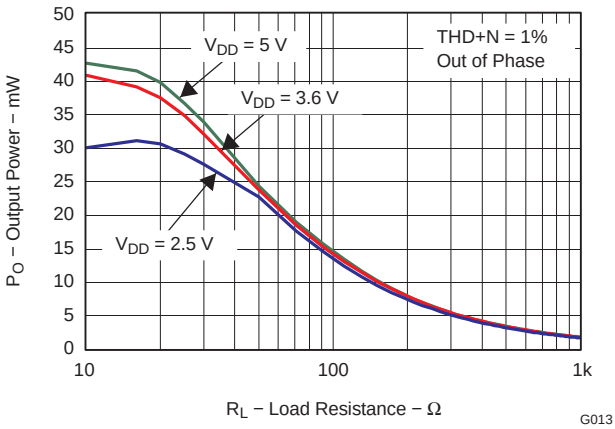


Figure 15.

OUTPUT POWER vs LOAD RESISTANCE

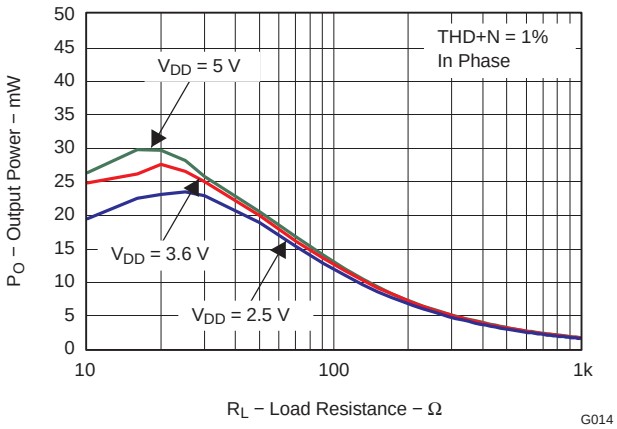


Figure 16.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

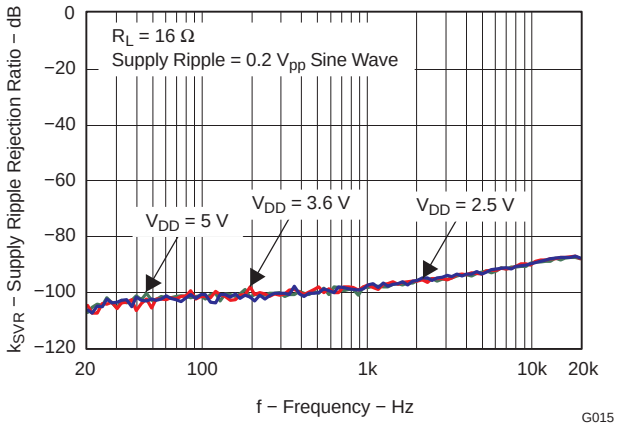


Figure 17.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

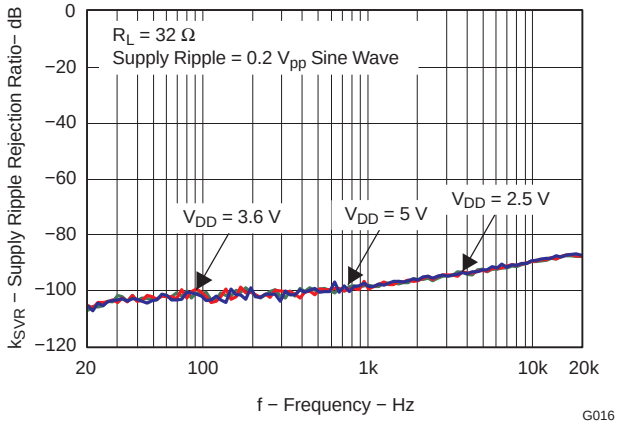


Figure 18.

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AV_{DD} (V_{DD}) = 3.6 V, GAIN = 0 dB, C_{HPVDD} = C_{HPVSS} = 2.2 µF, C_{INPUT} = C_{FLYING} = 1 µF, Outputs out of phase

SUPPLY CURRENT vs TOTAL OUTPUT POWER

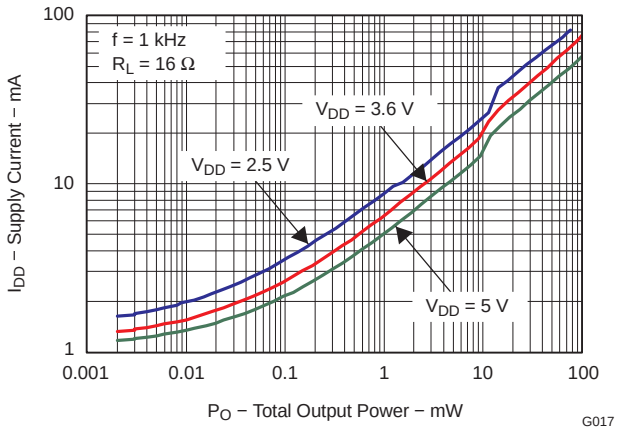


Figure 19.

SUPPLY CURRENT vs TOTAL OUTPUT POWER

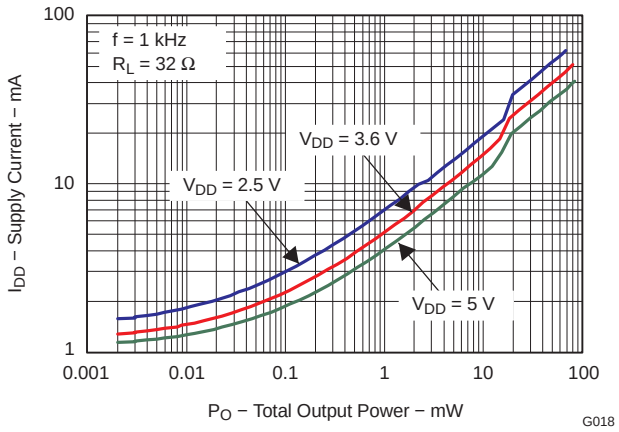


Figure 20.

TOTAL POWER DISSIPATION vs TOTAL OUTPUT POWER

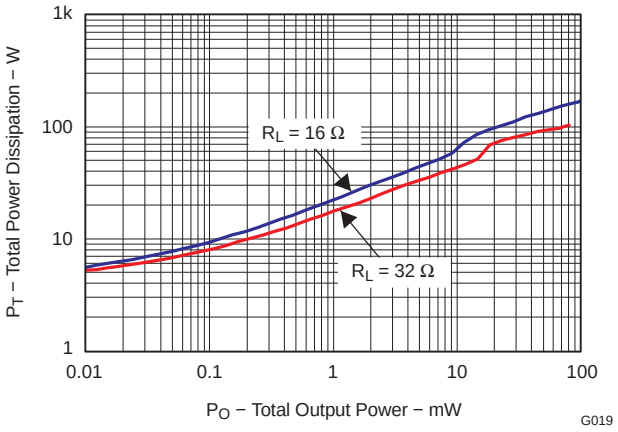


Figure 21.

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

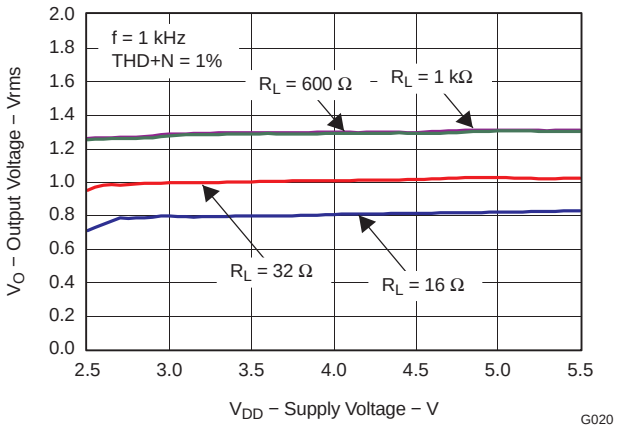


Figure 22.

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TYPICAL CHARACTERISTICS (continued)

T_A = 25°C, AV_{DD} (V_{DD}) = 3.6 V, GAIN = 0 dB, C_{HPVDD} = C_{HPVSS} = 2.2 µF, C_{INPUT} = C_{FLYING} = 1 µF, Outputs out of phase

CROSSTALK vs FREQUENCY

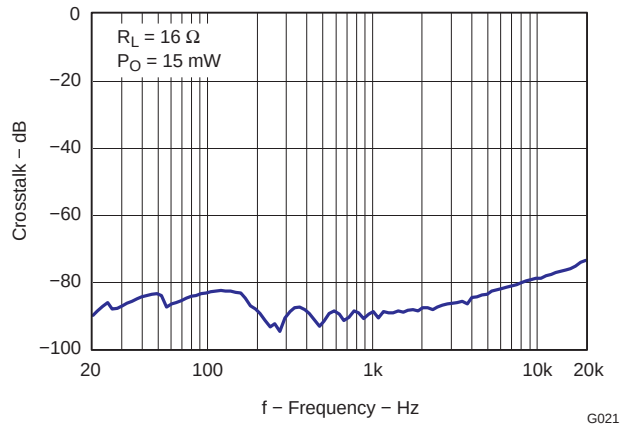


Figure 23.

OUTPUT AMPLITUDE vs FREQUENCY

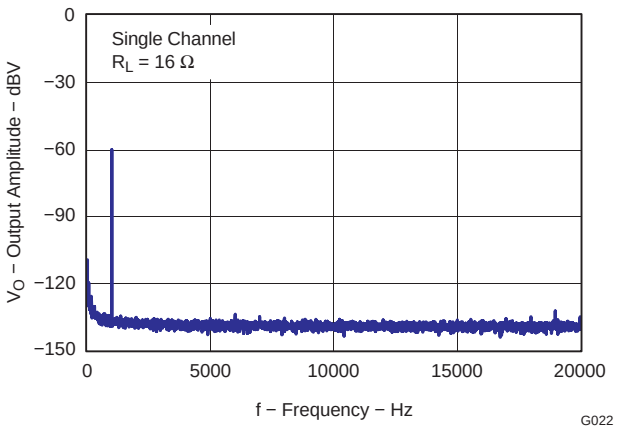


Figure 24.

STARTUP WAVEFORM vs TIME

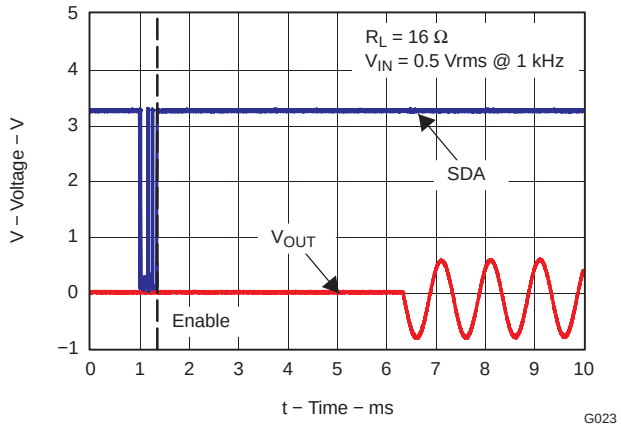


Figure 25.

SHUTDOWN WAVEFORM vs TIME

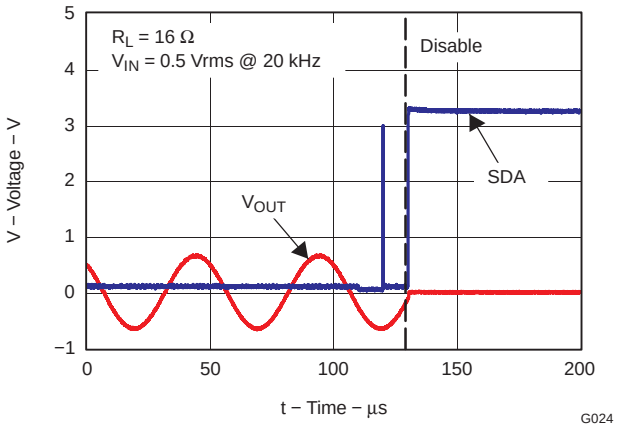


Figure 26.

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APPLICATION INFORMATION

APPLICATION CIRCUIT

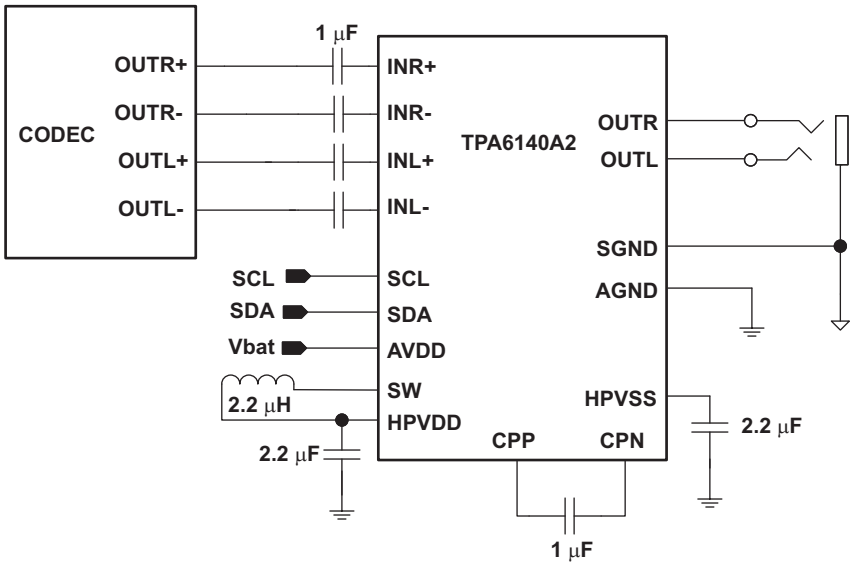


Figure 27. Typical Apps Configuration with Differential Input Signals

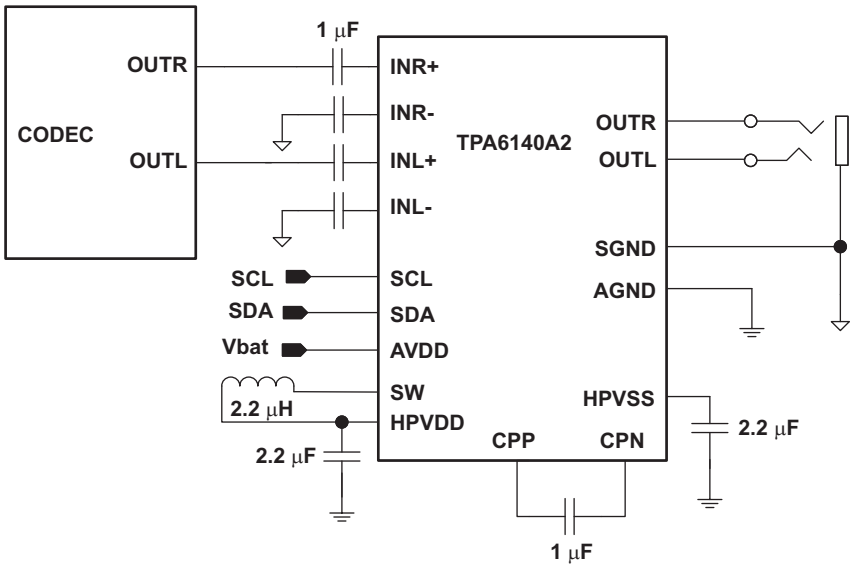


Figure 28. Typical Apps Configuration with Single-Ended Input Signals

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CLASS-G HEADPHONE AMPLIFIER

Class-G amplifiers use adaptive supply rails. The TPA6140A2 includes a built-in step-down converter to create the headphone amplifier positive supply voltage, HPVDD. A charge pump inverts HPVDD and creates the amplifier negative supply voltage, HPVSS. This allows the headphone amplifier output to be centered at 0 V and eliminates DC blocking capacitors.

When audio signal amplitude is low, the step-down converter generates a low HPVDD voltage. This minimizes TPA6140A2 power consumption while playing low amplitude, high fidelity audio. If audio amplitude increases, either due to louder music or a transient peak, then the step-down converter generates a higher HPVDD voltage. The HPVDD rise rate is faster than the audio peak rise time. This prevents audio distortion or clipping. Audio quality and noise floor are not affected by HPVDD.

This adaptive HPVDD minimizes TPA6140A2 supply current while avoiding clipping and distortion. Because normal listening levels are below 200 mV_{RMS}, HPVDD is most often at its lowest voltage. Thus, the TPA6140A2 has higher efficiency than traditional Class-AB headphone amplifiers.

The following equations compare a Class-AB amplifier to a Class-G amplifier. Both operate with identical battery voltage, load impedance, and output voltage swing. For this study case, we assume a normal listening level of 200 mV_{RMS} with no DirectPath™ in order to simplify the calculations.

- P_{SUP}: Supplied power
- V_{SUP}: Supply voltage
- I_{SUP}: Supply current
- V_{REG}: DC/DC converter output voltage
- P_{REG}: DC/DC converter output power
- V_{LOAD}: Voltage across the load
- R_{LOAD}: Load impedance
- P_{LOAD}: Power dissipated at the load
- I_{LOAD}: Current supplied to the load

Given an amplifier driving 200 mV_{RMS} into a 32 Ω load, the output current to the load is:

$$I_{LOAD} = \frac{V_{LOAD}}{R_{LOAD}} = \frac{200\ mV_{RMS}}{32\ \Omega} = 6.25\ mA \quad (1)$$

Assuming a quiescent current of 1 mA (I_{DDQ}) the total current supplied to the amplifier is:

$$I_{SUP} = I_{LOAD} + I_{DDQ} = 7.25\ mA \quad (2)$$

The total power supplied to a Class-AB amplifier is then calculated as:

$$P_{SUP} = V_{SUP} \times I_{SUP} = 4.2\ V \times 7.25\ mA = 30.45\ mW \quad (3)$$

For a Class-G amplifier where the voltage rails are generated by a switching DC/DC converter, the supplied power will depend on the DC/DC converter output voltage and efficiency. Assuming the DC/DC converter output voltage is 1.3 V:

$$P_{REG} = V_{REG} \times I_{SUP} = 1.3\ V \times 7.25\ mA = 9.425\ mW \quad (4)$$

The total supplied power will be the DC/DC converter output power divided by the efficiency of the DC/DC converter. Assuming 90% step-down efficiency, total power supplied to the Class-G amplifier is:

$$P_{SUP} = \frac{P_{REG}}{90\%} = 11.09\ mW \quad (5)$$

Class-G headphone amplifiers achieve much higher efficiency than equivalent Class-AB amplifiers.

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INDUCTOR SELECTION

The TPA6140A2 requires one inductor for its DC/DC converter. The following table lists recommended inductors. Inductors not shown on this table can be be used if they have similar performance characteristics.

When selecting an inductor observe the following rules:

- Lower DCR increases DC/DC converter efficiency.
- The minimum working inductance should never be below 1 µH.
- Include temperature and aging derating factors into the inductor value calculations.

MANUFACTURER	PART NUMBER
TOKO	MDT2012-CH2R2A
Murata	LQM21PN2R2MC0D
	LQH2MCN2R2M02L
Taiyo Yuden	BRL2012T2R2M
	BRC1608T2R2M

GROUND SENSE FUNCTION

The ground sense pin, SGND, reduces ground-loop noise when the audio output jack is connected to a different ground reference than codec and amplifier ground. Always connect the SGND pin to the headphone jack. This reduces output offset voltage and eliminates turn-on pop. Figure 29 shows how to connect SGND when an FM radio antenna function is implemented on the headphone wire. The nH coil and capacitor separate the RF signal from the audio GND signal. In this case, SGND is used to eliminate the offset voltage that is generated from the audio signal current and the RF coil low-frequency impedance.

The voltage difference between SGND and AGND cannot be greater than ±300 mV. The amplifier performance degrades if the voltage difference between SGND and AGND is greater than ±300 mV.

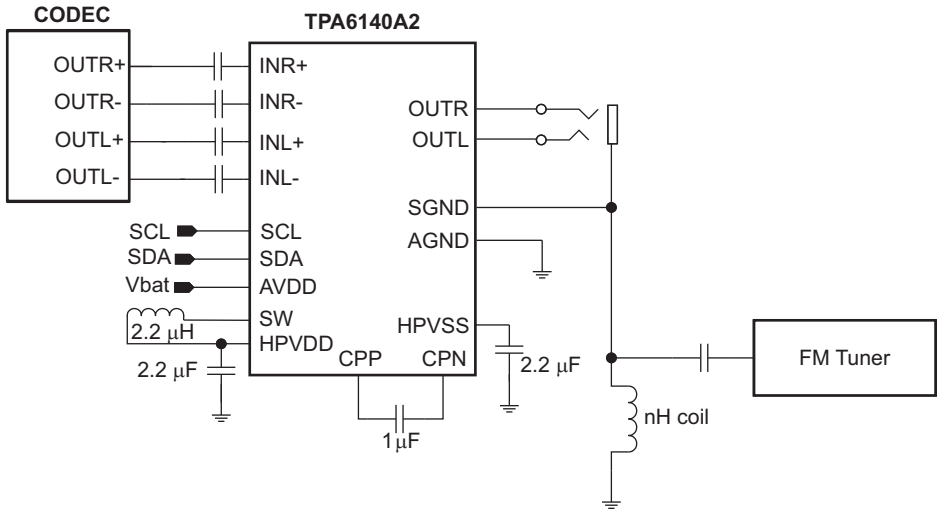


Figure 29. Sense Ground

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HIGH OUTPUT IMPEDANCE

The TPA6140A2 has a HI-Z bit option that increases output impedance while muting the amplifier. Set the HiZ_L and HiZ_R bits (register 3, bits 1 and 0) to HIGH to activate the HI-Z mode. This feature allows the headphone output jack to be shared for other functions besides audio. For example, sharing of a headphone jack between audio and video as shown in Figure 30. In HI-Z mode, the TPA6140A2 output impedance is high enough to prevent video signal attenuation.

SWS BIT	HI-Z BIT	OUTPUT IMPEDANCE	SUPPLY CURRENT	MAXIMUM EXTERNAL VOLTAGE ALLOWED ON OUTPUT PINS	COMMENTS
1	0	8 kΩ	< 3 µA	–0.3 V to 3.3 V(1)	Shutdown mode
1	1	8.5 kΩ			
0	0	≤ 1 Ω	1.2 mA	–	Active mode
0	1	8.5 kΩ @ 40kHz	1 mA	–1.8 V to 1.8 V	HI-Z mode
		600 Ω @ 6 MHz			
		400 Ω @ 13 MHz			

(1) If AV_{DD} is < 3.3 V, then maximum allowed external voltage applied is AV_{DD} in this mode

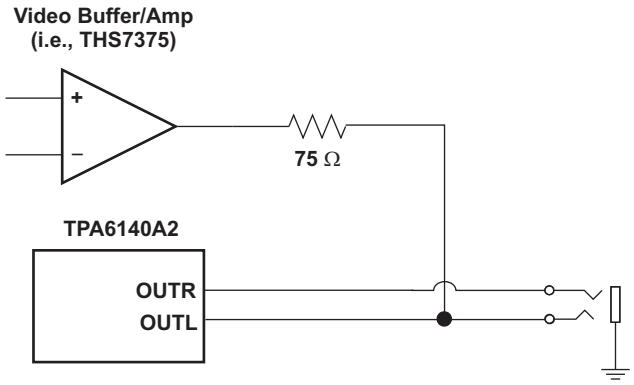


Figure 30. Sharing One Connector Between Audio and Video Signals Example

HEADPHONE AMPLIFIERS

Single-supply headphone amplifiers typically require dc-blocking capacitors to remove dc bias from their output voltage. The top drawing in Figure 31 illustrates this connection. If dc bias is not removed, large dc current will flow through the headphones which wastes power, clips the output signal, and potentially damages the headphones.

These dc-blocking capacitors are often large in value and size. Headphone speakers have a typical resistance between 16 Ω and 32 Ω. This combination creates a high-pass filter with a cutoff frequency as shown in Equation 6, where R_L is the load impedance, C_O is the dc-blocking capacitor, and f_C is the cutoff frequency.

$$f_C = \frac{1}{2\pi R_L C_O} \tag{6}$$

For a given high-pass cutoff frequency and load impedance, the required dc-blocking capacitor is found as:

$$C_O = \frac{1}{2\pi f_C R_L} \tag{7}$$

Reducing f_C improves low frequency fidelity and requires a larger dc-blocking capacitor. To achieve a 20 Hz cutoff with 16 Ω headphones, C_O must be at least 500 µF. Large capacitor values require large packages, consuming PCB area, increasing height, and increasing cost of assembly. During start-up or shutdown the dc-blocking capacitor has to be charged or discharged. This causes an audible pop on start-up and power-down. Large dc-blocking capacitors also reduce audio output signal fidelity.

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Two different headphone amplifier architectures are available to eliminate the need for dc-blocking capacitors. The Capless amplifier architecture provides a reference voltage to the headphone connector shield pin as shown in the middle drawing of Figure 31. The audio output signals are centered around this reference voltage, which is typically half of the supply voltage to allow symmetrical output voltage swing.

When using a Capless amplifier do not connect the headphone jack shield to any ground reference or large currents will result. This makes Capless amplifiers ineffective for plugging non-headphone accessories into the headphone connector. Capless amplifiers are useful only with floating GND headphones.

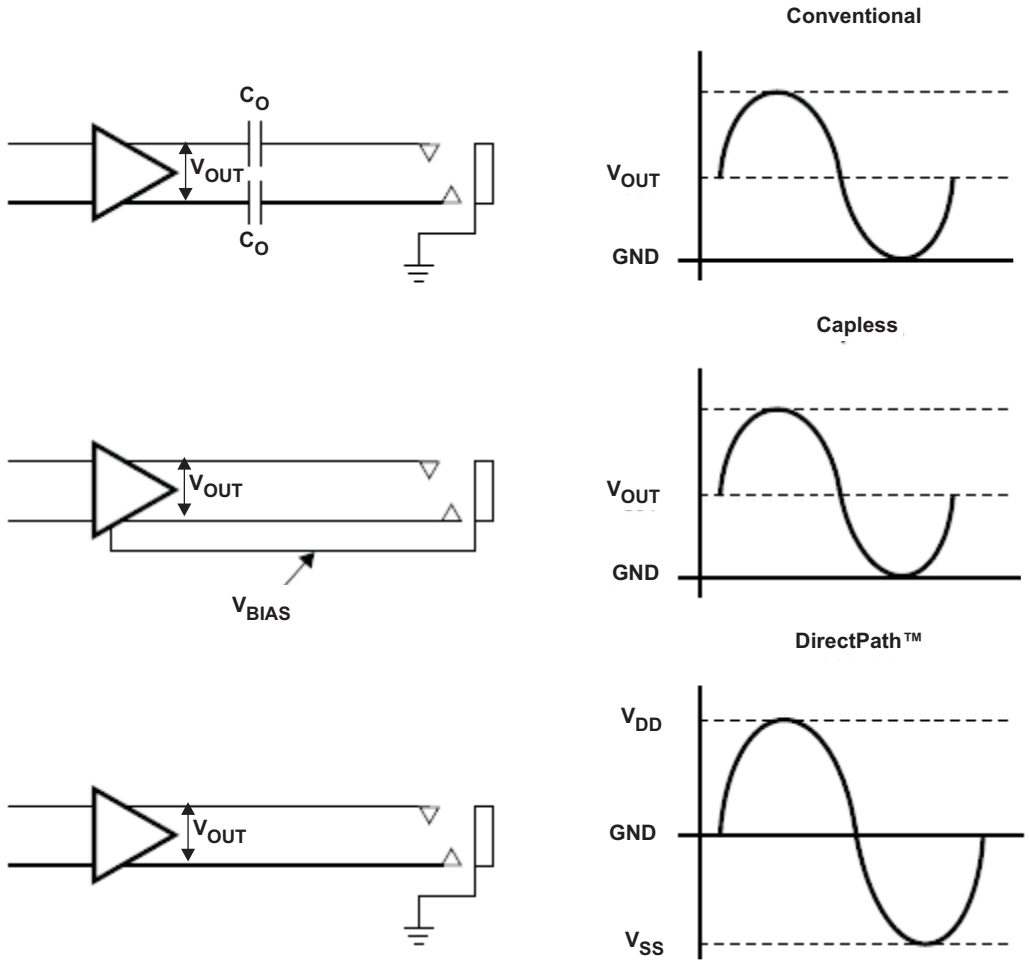


Figure 31. Amplifier Applications

The DirectPath™ amplifier architecture operates from a single supply voltage and uses an internal charge pump to generate a negative supply rail for the headphone amplifier. The output voltages are centered around 0 V and are capable of positive and negative voltage swings as shown in the bottom drawing of Figure 31. DirectPath amplifiers require no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The TPA6140A2 is a DirectPath amplifier.

ELIMINATING TURN-ON POP AND POWER SUPPLY SEQUENCING

The TPA6140A2 has excellent noise and turn-on / turn-off pop performance. It uses an integrated click-and-pop suppression circuit to allow fast start-up and shutdown without generating any voltage transients at the output pins. Typical start-up time from shutdown is 5 ms.

DirectPath technology keeps the output dc voltage at 0 V even when the amplifier is powered up. The DirectPath technology together with the active pop-and-click suppression circuit eliminates audible transients during start up and shutdown.

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Use input coupling capacitors to ensure inaudible turn-on pop. Activate the TPA6140A2 after all audio sources have been activated and their output voltages have settled. During power-down, deactivate the TPA6140A2 before deactivating the audio input source.

RF AND POWER SUPPLY NOISE IMMUNITY

The TPA6140A2 employs a new differential amplifier architecture to achieve high power supply noise rejection and RF noise rejection. RF and power supply noise are common in modern electronics. Although RF frequencies are much higher than the 20 kHz audio band, signal modulation often falls in-band. This, in turn, modulates the supply voltage, allowing a coupling path into the audio amplifier. A common example is the 217 Hz GSM frame-rate buzz often heard from an active speaker when a cell phone is placed nearby during a phone call.

The TPA6140A2 has excellent rejection of power supply and RF noise, preventing audio signal degradation.

INPUT COUPLING CAPACITORS

Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize TPA6140A2 turn-on pop to an inaudible level.

The input capacitors are in series with TPA6140A2 internal input resistors, creating a high-pass filter. Equation 8 calculates the high-pass filter corner frequency. The input impedance, R_{IN}, is dependent on device gain. Larger input capacitors decrease the corner frequency. See the Operating Characteristics table for input impedance values.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \tag{8}$$

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}} \tag{9}$$

Example: Design for a 20 Hz corner frequency with a TPA6140A2 gain of +6 dB. The Operating Characteristics table gives R_{IN} as 13.2 kΩ. Equation 9 shows the input coupling capacitors must be at least 0.6 µF to achieve a 20 Hz high-pass corner frequency. Choose a 0.68 µF standard value capacitor for each TPA6140A2 input (X5R material or better is required for best performance).

Input capacitors can be removed provided the TPA6140A2 inputs are driven differentially with less than ±1 V_{RMS} and the common-mode voltage is within the input common-mode range of the amplifier. Without input capacitors turn-on pop performance may be degraded and should be evaluated in the system.

CHARGE PUMP FLYING CAPACITOR AND HPVSS CAPACITOR

The TPA6140A2 uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CPP and CPN. It transfers charge to generate the negative supply voltage. The HPVSS capacitor must be at least equal in value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1 µF to 2.2 µF for the HPVSS and flying capacitors. Although values down to 0.47 µF can be used, total harmonic distortion (THD) will increase.

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POWER SUPPLY AND HPVDD DECOUPLING CAPACITORS AND CONNECTIONS

The TPA6140A2 DirectPath headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2 µF capacitor within 5 mm of the AVDD pin. Reducing the distance between the decoupling capacitor and AVDD minimizes parasitic inductance and resistance, improving TPA6140A2 supply rejection performance. Use 0402 or smaller size capacitors if possible. Ensure that the ground connection of each of the capacitors has a minimum length return path to the device. Failure to properly decouple the TPA6140A2 may degrade audio or EMC performance.

For additional supply rejection, connect an additional 10 µF or higher value capacitor between AVDD and ground. This will help filter lower frequency power supply noise. The high power supply rejection ratio (PSRR) of the TPA6140A2 makes the 10 µF capacitor unnecessary in most applications.

Connect a 2.2 µF capacitor between HPVDD and ground. This ensures the amplifier internal bias supply remains stable and maximizes headphone amplifier performance.

DO NOT connect HPVDD directly to AVDD or an external supply voltage. The voltage at HPVDD is generated internally. Connecting HPVDD to an external voltage can damage the device.

LAYOUT RECOMMENDATIONS

GND CONNECTIONS

The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than ±0.3 V to SGND.

AGND is a power ground. Connect supply decoupling capacitors for AVDD, HPVDD, and HPVSS to AGND.

GENERAL I^2C OPERATION

The I^2C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially one bit at a time. The address and data 8-bit bytes are transferred most significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions bust occur within the low time of the clock period. Figure 32 shows a typical sequence. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TPA6140A2 holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

The TPA6140A2 operates as an I^2C slave. The I^2C voltage can not exceed the TPA6140A2 supply voltage, AVDD.

An external pull-up resistor must be used for the SDA and SCL signals to set the logic high level for the bus. When the bus level is 3.3 V, use pull-up resistors between 660 Ω and 1.2 kΩ.

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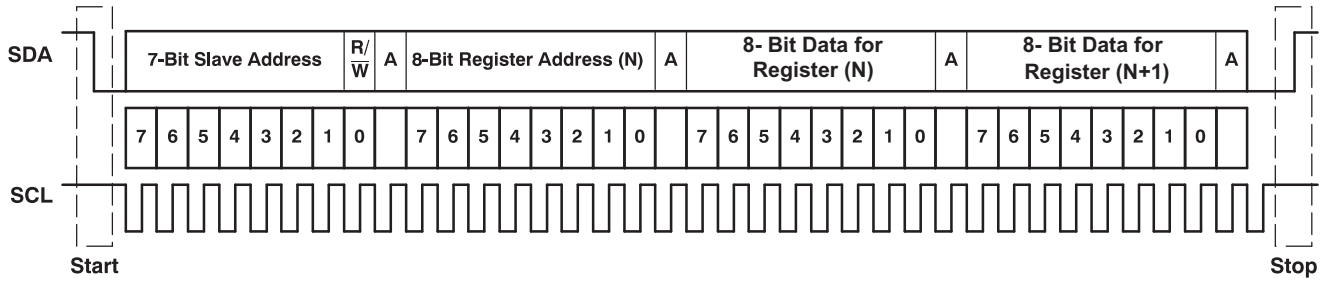


Figure 32. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 32.

SINGLE-AND MULTIPLE-BYTE TRANSFERS

The serial control interface supports both single-byte and multi-byte read/write operations for all registers.

During multiple-byte read operations, the TPA6140A2 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TPA6140A2 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

SINGLE-BYTE WRITE

As shown in Figure 33, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TPA6140A2 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TPA6140A2 internal memory address being accessed. After receiving the register byte, the TPA6140A2 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

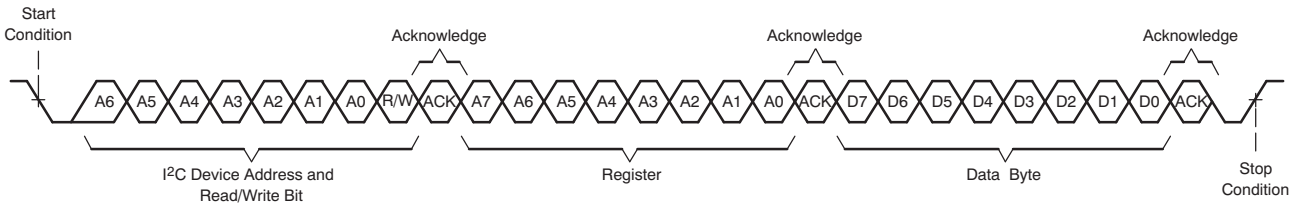


Figure 33. Single-Byte Write Transfer

MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TPA6140A2 as shown in Figure 34. After receiving each data byte, the TPA6140A2 responds with an acknowledge bit.

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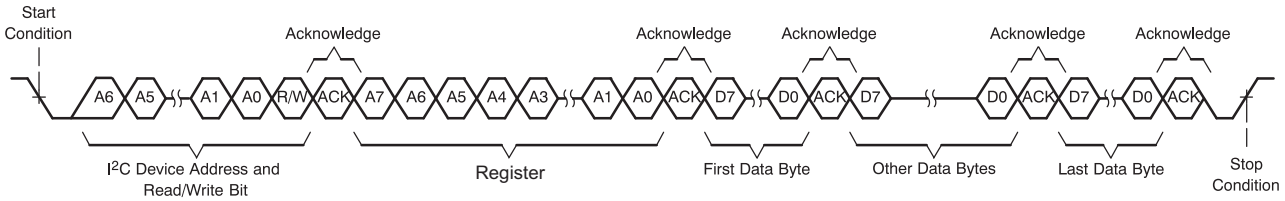


Figure 34. Multiple-Byte Write Transfer

SINGLE-BYTE READ

As shown in Figure 35, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TPA6140A2 address and the read/write bit, the TPA6140A2 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TPA6140A2 issues an acknowledge bit. The master device transmits another start condition followed by the TPA6140A2 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TPA6140A2 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

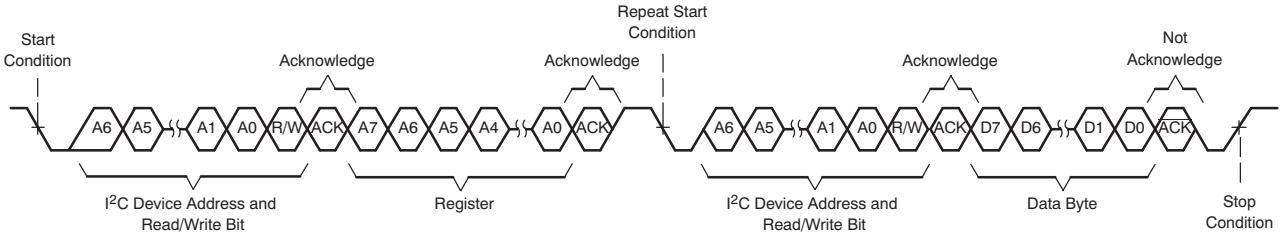


Figure 35. Single-Byte Read Transfer

MULTIPLE-BYTE READ

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TPA6140A2 to the master device as shown in Figure 36. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

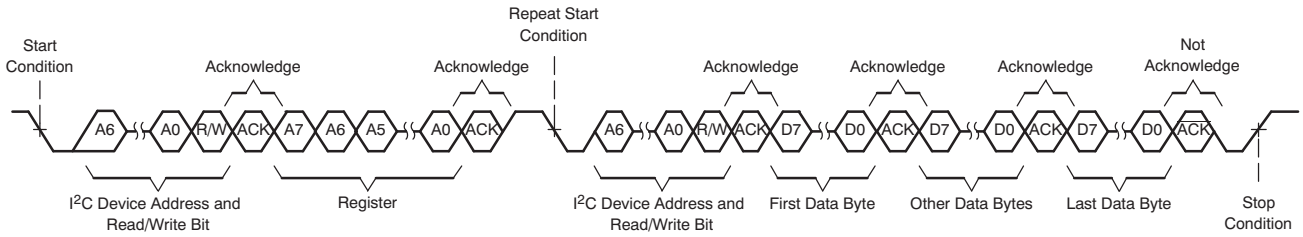


Figure 36. Multiple-Byte Read Transfer

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REGISTER MAP

Table 1. Register Map

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	HP_EN_L	HP_EN_R	0	0	0	0	Thermal	SWS
2	Mute_L	Mute_R	Volume[4]	Volume[3]	Volume[2]	Volume[1]	Volume[0]	0
3	0	0	0	0	0	0	HiZ_L	HiZ_R
4	0	0	0	0	Version[3]	Version[2]	Version[1]	Version[0]
5	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT
6	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT
7	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT
8	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT

Bits labeled "Reserved" are reserved for future enhancements. They may not be written to. When read, they will show a "0" value.

Bits labeled "RFT" are reserved for TI testing. Under no circumstances must any data be written to these registers. If read, these bits may assume any value.

The TPA6140A2 I^2C address is 0xC0 (binary 11000000) for writing an 0xC1 (binary 11000001) for reading. If a different I^2C address is required, please contact your local TI representative.

Fault Register (Address: 1)

BIT	7	6	5	4	3	2	1	0
Function	HP_EN_L	HP_EN_R	0	0	0	0	Thermal	SWS
Reset Value	0	0	0	0	0	0	0	1

HP_EN_L Enable bit for the left-channel amplifier. Amplifier is active when bit is high.

HP_EN_R Enable bit for the right-channel amplifier. Amplifier is active when bit is high.

Thermal Bit sets to 1 to indicate thermal shutdown. Once temperature decreases below a safe level, the TPA6140A2 re-activates regardless of previous bit status. This bit is clear-on-read.

SWS Software shutdown control. Set bit to 1 to initiate software shutdown. Set bit to 0 to activate charge-pump. SWS must remain at 0 for normal operation.Use SWS instead of HP_EN_L and HP_EN_R to ensure lowest current consumption and highest input to output signal attenuation when disabling the amplifier.

Volume and Mute Register (Address: 2)

BIT	7	6	5	4	3	2	1	0
Function	Mute_L	Mute_R	Volume[4]	Volume[3]	Volume[2]	Volume[1]	Volume[0]	0
Reset Value	1	1	0	0	0	0	0	0

Mute_L Left channel mute. Set bit to 1 to mute left channel.

Mute_R Right channel mute. Set bit to 1 to mute right channel.

Volume[5:0] Volume control byte. Set to 111110 for highest gain, 4 dB; set to 000000 for lowest gain, –59 dB

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Output Impedance Register (Address: 3)

BIT	7	6	5	4	3	2	1	0
Function	0	0	0	0	0	0	HiZ_L	HiZ_R
Reset Value	0	0	0	0	0	0	0	0

Reserved These bits are reserved for future enhancements. Do not write to these bits as writing to these bits may change device function. If read these bits may assume any value.

HiZ_L Set to 1 to put left channel amplifier output in three-state high impedance mode.

HiZ_R Set to 1 to put right channel amplifier output in three-state high impedance mode.

I^2C Address and Version Register (Address: 4)

BIT	7	6	5	4	3	2	1	0
Function	0	0	0	0	Version[3]	Version[2]	Version[1]	Version[0]
Reset Value	0	0	0	0	0	0	0	0

Version[3:0] The version bits track the revision of the silicon. Valid values are 0000 for the first silicon TPA6140A2.

Reserved for Test (Addresses: 5-8)

BIT	7	6	5	4	3	2	1	0
Function	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT
Reset Value	x	x	x	x	x	x	x	x

RFT Reserved for Test. Do NOT write to these registers.

VOLUME CONTROL

Set the TPA6140A2 volume control through the I^2C interface. Write to the Volume[5:0] byte at Register 2, Bits 5-0. Although the gain byte is a 6-bit word, only 32 steps are available. The least significant bit of the Volume[5:0] byte is treated as a don't care bit.

GAIN CONTROL BYTE: MUTE [7:6], VOLUME[5:0]	NOMINAL GAIN		GAIN CONTROL BYTE: MUTE [7:6], VOLUME[5:0]	NOMINAL GAIN
11XXXXXX	–80 dB		0010000x	–11 dB
0000000x	–59 dB		0010001x	–10 dB
0000001x	–55 dB		0010010x	–9.0 dB
0000010x	–51 dB		0010011x	–8.0 dB
0000011x	–47 dB		0010100x	–7.0 dB
0000100x	–43 dB		0010101x	–6.0 dB
0000101x	–39 dB		0010110x	–5.0dB
0000110x	–35 dB		0010111x	–4.0 dB
0000111x	–31 dB		0011000x	–3.0 dB
0001000x	–27 dB		0011001x	–2.0 dB
0001001x	–25 dB		0011010x	–1.0 dB
0001010x	–23 dB		0011011x	+0.0 dB
0001011x	–21 dB		0011100x	+1.0 dB
0001100x	–19 dB		0011101x	+2.0 dB
0001101x	–17 dB		0011110x	+3.0 dB
0001110x	–15 dB		0011111x	+4.0 dB
0001111x	–13 dB			

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OPERATING MODES

HARDWARE SHUTDOWN

Hardware shutdown is not available in the TPA6140A2. The SWS register (Software Shutdown) must be used to shutdown the amplifier.

SOFTWARE SHUTDOWN

Set software shutdown by writing a logic 1 in register 1, bit 0 (SWS bit). Software shutdown places the device in the lowest power state (see the Electrical Characteristics Table for values). Engaging software shutdown turns off the buck regulator and charge pump and disables the amplifier outputs. Write a logic 0 to the SWS bit to reactivate the device.

Note that when the device is in SWS mode all registers will maintain their values. The HP_EN_L and HP_EN_R bits can be reset because a full word must be used when writing just one bit to the register.

To ensure lowest current consumption and highest input to output signal attenuation, SWS must be used instead of HP_EN_L and HP_EN_R (set HP_EN_L and HP_EN_R to logic 1) when disabling both channels of the amplifier simultaneously. Set HP_EN_L and HP_EN_R to logic 1 before changing SWS from logic 0 to logic 1.

MUTE MODE

Set the Mute_L bit to 1 to mute the left channel output. Set the Mute_R bit to 1 to mute the right channel output. They are respectively located at Register 2, Bits 7 and 6. Mute attenuation is -80 dB, typical. Mute attenuation can only be guaranteed when the amplifier is operational (SWS = 0) and enabled (HP_EN_L or HP_EN_R = 1)

HI-Z MODE

HI-Z mode mutes the device and puts the amplifier outputs into a high impedance state. Use this configuration when the outputs of the TPA6140A2 share traces with other devices whose outputs may be active. Write a logic 1 in register 3, bits 0 and 1 to enable Hi-Z mode for the left and right outputs. Place a logic 0 in register 3, bits 0 and 1 to disable the Hi-Z state. The left and right outputs can be placed into a Hi-Z state individually.

Note that to use the Hi-Z mode, the SWS bit must be equal to logic 0 (amplifier operational) and the output headphone amplifiers must NOT be enabled (HP_EN_L and HP_EN_R = 0).

DEFAULT MODE AT START-UP

On power-up, the TPA6140A2 initializes in the following conditions:

- SWS = 1 (Shutdown mode)
- HP_EN_L = HP_EN_R = 0 (Outputs disabled)
- Hi-Z_L = Hi-Z_R = 0 (Hi-Z off)
- Mute_L = Mute_R = 1 (Amplifiers muted)
- VOLUME = –59 dB

PACKAGE INFORMATION

Package Dimensions

The package dimensions for this YFF package are shown in the table below. See the package drawing at the end of this data sheet for more details.

Table 2. YFF Package Dimensions

Packaged Devices	D	E
TPA6140A2YFF	Min = 1530µm Max = 1590µm	Min = 1530µm Max = 1590µm

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REVISION HISTORY

Changes from Original (March 2009) to Revision A **Page**

- Changed C4 to D4 in terminal functions 3
- Changed D4 to C4 in terminal functions 3
- Deleted lead temperature from absolute maximum ratings 4

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6140A2YFFR	Active	Production	DSBGA (YFF) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIFI
TPA6140A2YFFR.A	Active	Production	DSBGA (YFF) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIFI
TPA6140A2YFFR.B	Active	Production	DSBGA (YFF) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIFI
TPA6140A2YFFT	Active	Production	DSBGA (YFF) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIFI
TPA6140A2YFFT.A	Active	Production	DSBGA (YFF) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIFI
TPA6140A2YFFT.B	Active	Production	DSBGA (YFF) | 16	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AIFI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

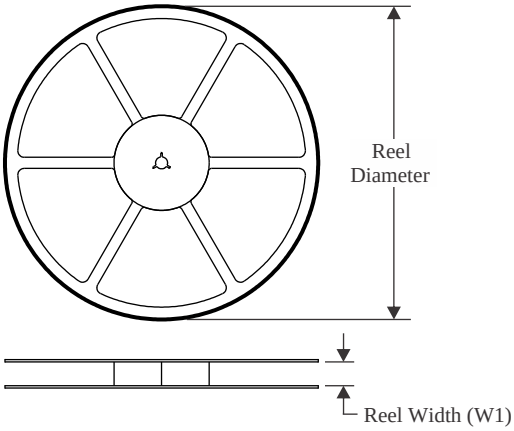
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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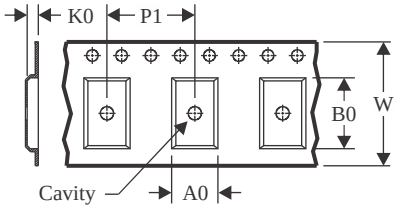
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

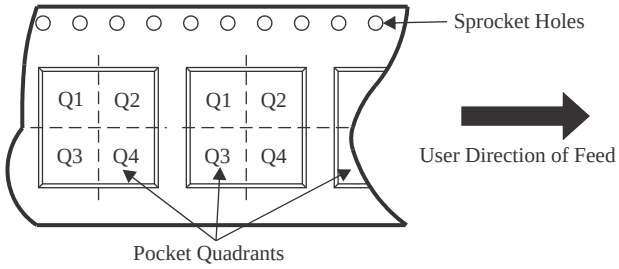


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

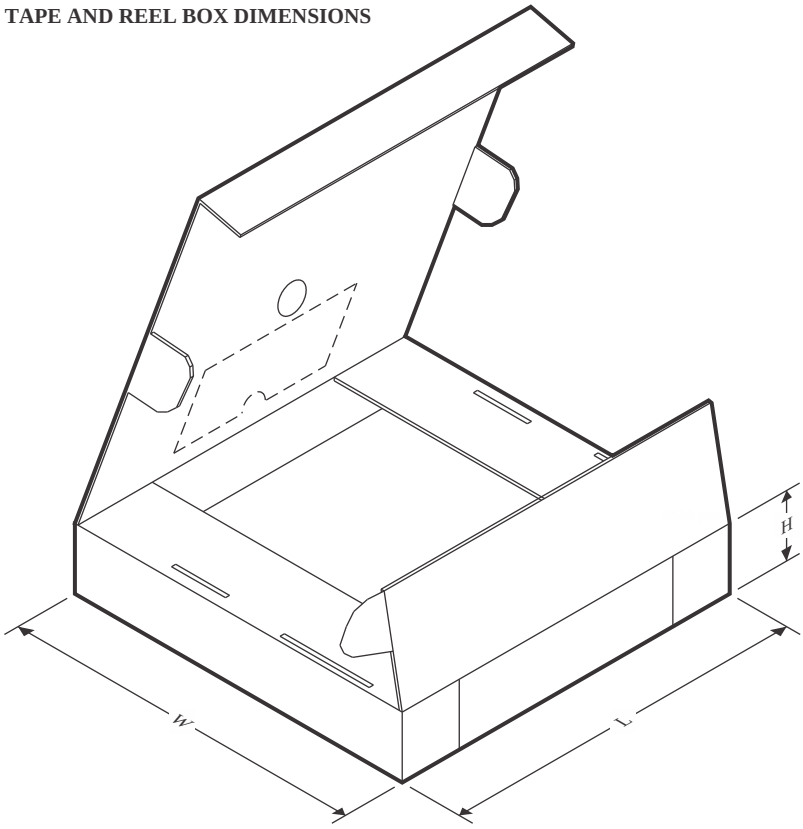
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

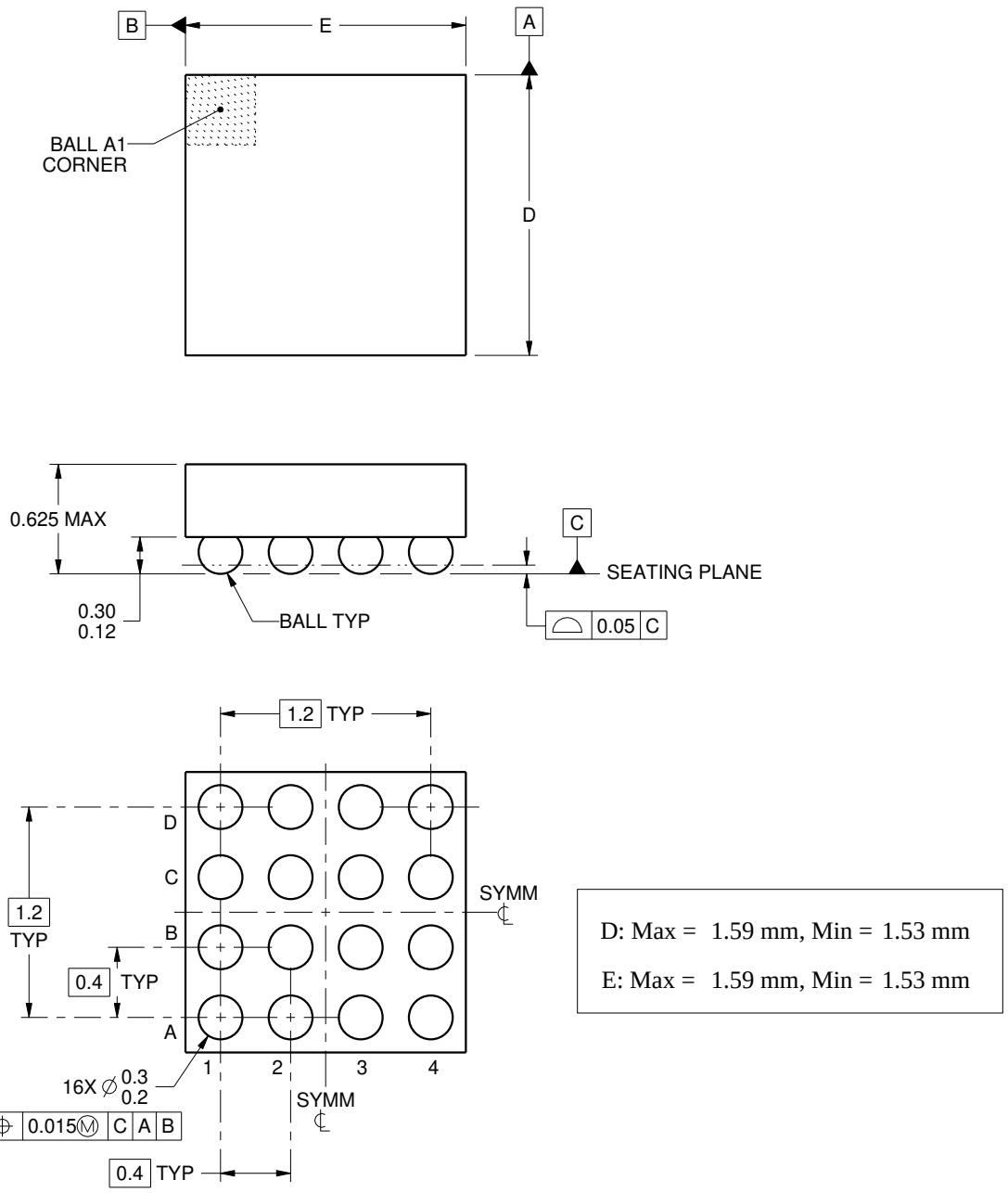
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6140A2YFFR	DSBGA	YFF	16	3000	180.0	8.4	1.71	1.71	0.81	4.0	8.0	Q1
TPA6140A2YFFT	DSBGA	YFF	16	250	180.0	8.4	1.71	1.71	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

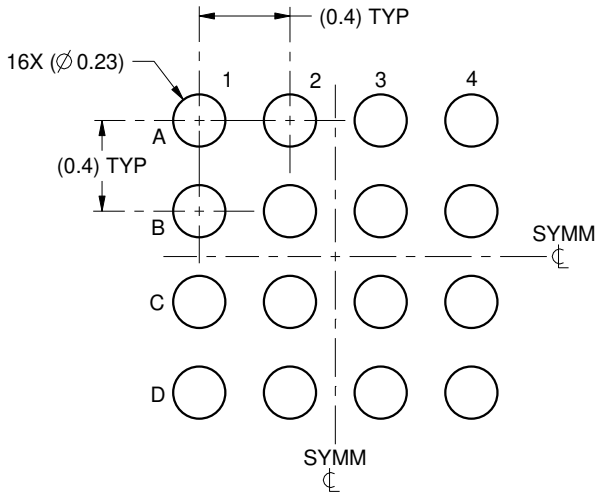
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6140A2YFFR	DSBGA	YFF	16	3000	182.0	182.0	20.0
TPA6140A2YFFT	DSBGA	YFF	16	250	182.0	182.0	20.0



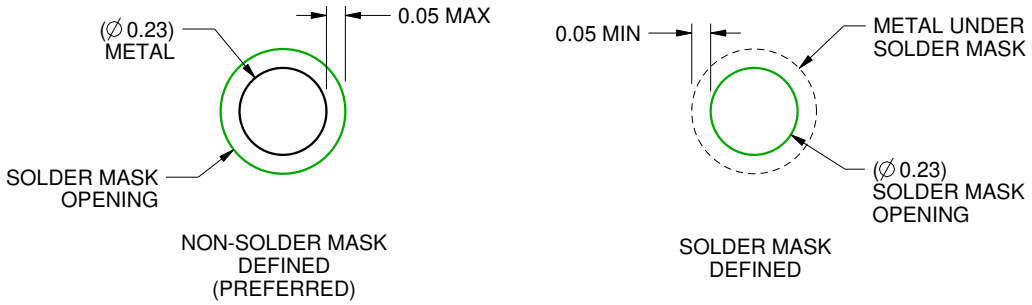
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

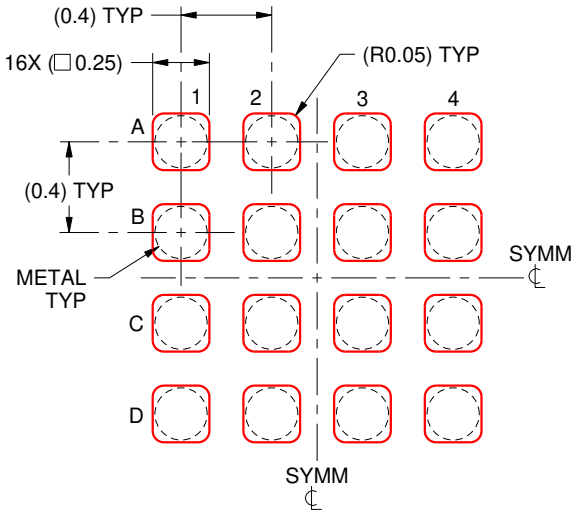
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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