TPA6205A1 1.25-W Mono Fully Differential Audio Power Amplifier With 1.8-V Input logic Thresholds

1 Features

- 1.25 W Into 8-Ω From a 5-V Supply at THD = 1% (Typical)
- Shutdown Pin has 1.8-V Compatible Thresholds
- Low Supply Current: 1.7 mA Typical
- Shutdown Current < 10 µA
- Only Five External Components
  - Improved PSRR (90 dB) and Wide Supply Voltage (2.5 V to 5.5 V) for Direct Battery Operation
  - Fully Differential Design Reduces RF Rectification
  - Improved CMRR Eliminates Two Input Coupling Capacitors
  - $C_{(BYPASS)}$ Is Optional Due to Fully Differential Design and High PSRR
- Available in 3-mm × 3-mm QFN Package (DRB)
- Available in an 8-Pin PowerPAD™ MSOP (DGN)
- Available in a 2-mm × 2-mm MicroStar Junior™ BGA Package (ZQV)

2 Applications

- Designed for Wireless Handsets, PDAs, and Other Mobile Devices
- Compatible With Low Power (1.8-V Logic) I/O Threshold Control Signals

3 Description

The TPA6205A1 device is a 1.25-W mono fully differential amplifier designed to drive a speaker with at least 8-Ω impedance while consuming less than 37 mm2 (ZQV package option) total printed-circuit-board (PCB) area in most applications. This device operates from 2.5 V to 5.5 V, drawing only 1.7 mA of quiescent supply current. The TPA6205A1 is available in the space-saving 2-mm × 2-mm MicroStar Junior BGA package, and the space saving 3-mm × 3-mm QFN (DRB) package.

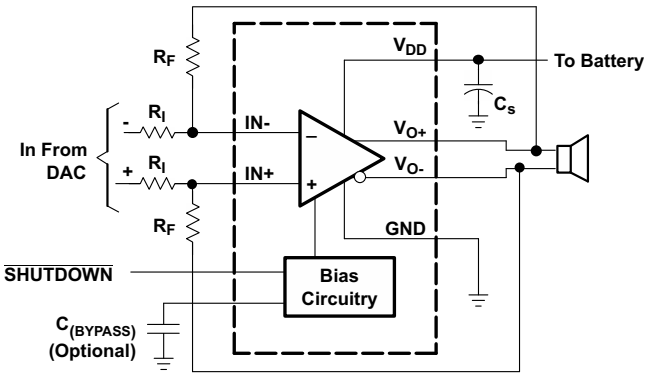
Features like 85-dB PSRR from 90 Hz to 5 kHz, improved RF-rectification immunity, and small PCB area makes the TPA6205A1 ideal for wireless handsets. A fast start-up time of 4s with minimal pop makes the TPA6205A1 ideal for PDA applications.

Device Information(1)

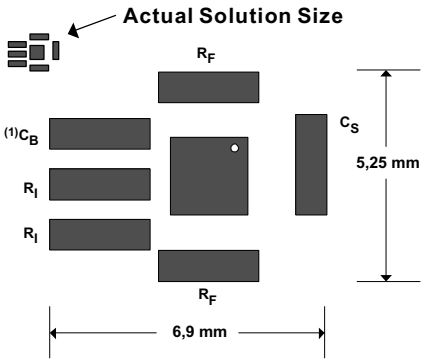
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6205A1	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm
	SON (8)	3.00 mm × 3.00 mm
	BGA MICROSTAR JUNIOR (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Circuit



Example Solution Size



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2008) to Revision C	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Removed *Ordering Information* table	1

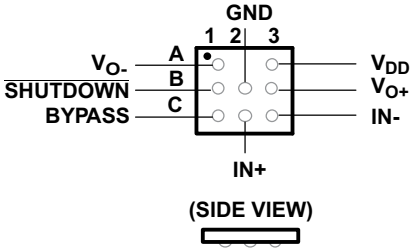
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5 Device Comparison Table

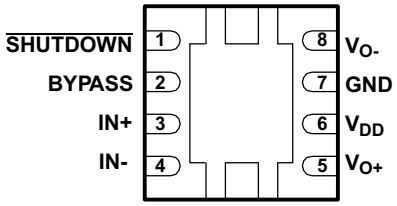
DEVICE NUMBER	SPEAKER CHANNELS	SPEAKER AMP TYPE	OUTPUT POWER (W)	PSRR (dB)
TPA6203A1	Mono	Class AB	1.25	90
TPA6204A1	Mono	Class AB	1.7	85
TPA6205A1 (1.8-V comp SD)	Mono	Class AB	1.25	90
TPA6211A1	Mono	Class AB	3.1	85

6 Pin Configuration and Functions

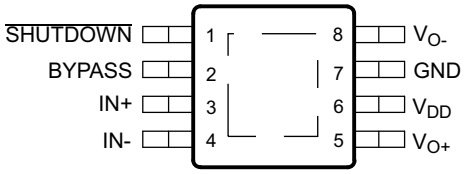
ZQV Package
8-Pin BGA MICROSTAR JUNIOR
Top View



DRB Package
8-Pin SON
Top View



DGN Package
8-Pin MSOP-PowerPAD
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	BGA MICROSTAR JUNIOR	SON, MSOP-PowerPAD		
BYPASS	C1	2	I	Mid-supply voltage. Adding a bypass capacitor improves PSRR.
GND	B2	7	I	High-current ground
IN–	C3	4	I	Negative differential input
IN+	C2	3	I	Positive differential input
$\overline{\text{SHUTDOWN}}$	B1	1	I	Shutdown terminal (active low logic)
V_{DD}	A3	6	I	Supply voltage terminal
V_{O+}	B3	5	O	Positive BTL output
$V_{O–}$	A1	8	O	Negative BTL output
Thermal Pad	N/A	—	—	Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.3	6	V
V_I	Input voltage	INx and $\overline{\text{SHUTDOWN}}$ pins	–0.3	0.3	V
	Continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature		–40	85	ºC
T_J	Junction temperature		–40	125	ºC
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	ZQV, DRB, DGN		260	ºC
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.5		5.5	V
V_{IH}	High-level input voltage	$\overline{\text{SHUTDOWN}}$	1.15			V
V_{IL}	Low-level input voltage	$\overline{\text{SHUTDOWN}}$			0.5	V
V_{IC}	Common-mode input voltage	VDD = 2.5 V, 5.5 V, CMRR ≤ –60 dB	0.5		VDD–0.8	V
T_A	Operating free-air temperature		–40		85	°C
Z_L	Load impedance		6.4	8		Ω

7.4 Thermal Information

THERMAL METRIC(1)		TPA6205A1			UNIT
		BGA MICROSTAR JUNIOR	SON	MSOP PowerPAD	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.4	57.3	109.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.8	84.0	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.1	32.2	47.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.3	3.7	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.0	32.2	47.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.8	15.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
[V_{OO}]	Output offset voltage (measured differentially)	V_I = 0 V, VDD = 2.5 V to 5.5 V				9	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V			–90	–70	dB
CMRR	Common-mode rejection ratio	V_{DD} = 3.6 V to 5.5 V, V_{IC} = 0.5 V to V_{DD} – 0.8			–70	–65	dB
		V_{DD} = 2.5 V, V_{IC} = 0.5 V to 1.7 V			–62	–55	
V_{OL}	Low-level output voltage	R_L = 8 Ω, V_{IN+} = V_{DD}, $V_{IN–}$ = 0 V or V_{IN+} = 0 V, $V_{IN–}$ = V_{DD}	VDD = 5.5 V		0.3	0.46	V
			VDD = 3.6 V		0.22		
			VDD = 2.5 V		0.19	0.26	
V_{OH}	High-level output voltage	R_L = 8 Ω, VIN+ = V_{DD}, $V_{IN–}$ = 0 V or V_{IN+} = 0 V, $V_{IN–}$ = V_{DD}	VDD = 5.5 V	4.8	5.12		V
			VDD = 3.6 V		3.28		
			VDD = 2.5 V	2.1	2.24		
[I_{IH}]	High-level input current	V_{DD} = 5.5 V, V_I = 5.8 V				1.2	µA
[I_{IL}]	Low-level input current	V_{DD} = 5.5 V, V_I = –0.3 V				1.2	µA
I_{DD}	Supply current	V_{DD} = 2.5 V to 5.5 V, No load, $\overline{SHUTDOWN}$ = V_{IH}			1.7	2	mA
$I_{DD(SD)}$	Supply current in shutdown mode	$\overline{SHUTDOWN}$ = VIL , VDD = 2.5 V to 5.5 V, No load			0.01	0.9	µA

7.6 Operating Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N = 1%, f = 1 kHz	V_{DD} = 5 V		1.25		W
			V_{DD} = 3.6 V		0.63		
			V_{DD} = 2.5 V		0.3		
THD+N	Total harmonic distortion plus noise	V_{DD} = 5 V, P_O = 1 W, f = 1 kHz			0.06%		
		V_{DD} = 3.6 V, P_O = 0.5 W, f = 1 kHz			0.07%		
		V_{DD} = 2.5 V, P_O = 200 mW, f = 1 kHz			0.08%		
k_{SVR}	Supply ripple rejection ratio	$C_{(BYPASS)}$ = 0.47°F, V_{DD} = 3.6 V to 5.5 V, Inputs AC-grounded with C_I = 2 F	f = 217 Hz to 2 kHz, V_{RIPPLE} = 200 mV_{PP}		–87		dB
		$C_{(BYPASS)}$ = 0.47 F, V_{DD} = 2.5 V to 3.6 V, Inputs AC-grounded with C_I = 2 F	f = 217 Hz to 2 kHz, V_{RIPPLE} = 200 mV_{PP}		–82		
		$C_{(BYPASS)}$ = 0.47 F, V_{DD} = 2.5 V to 5.5 V, Inputs AC-grounded with C_I = 2 F	f = 40 Hz to 20 kHz, V_{RIPPLE} = 200 mV_{PP}		≤ –74		
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O= 1 W			104		dB
V_n	Output voltage noise	f = 20 Hz to 20 kHz	No weighting		17		VRMS
			A weighting		13		
CMRR	Common-mode rejection ratio	V_{DD}= 2.5 V to 5.5 V, Resistor tolerance = 0.1%, Gain = 4V/V, VICM = 200 mV_{PP}	f = 20 Hz to 1 kHz		≤ –85		dB
			f = 20 Hz to 20 kHz		≤ –74		
Z_I	Input impedance				2		MΩ
Z_O	Output impedance	Shutdown mode		>10			kΩ
	Shutdown attenuation	f = 20 Hz to 20 kHz, R_F = R_I = 20 kΩ			–80		dB

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7.7 Dissipation Ratings

PACKAGE	TA ≤ 25°C POWER RATING	DERATING FACTOR	TA ≤ 70°C POWER RATING	TA ≤ 85°C POWER RATING
ZQV	885 mW	8.8 mW/°C	486 mW	354 mW
DGN	2.13 W	17.1 mW/°C	1.36 W	1.11 W
DRB	2.7 W	21.8 mW/°C	1.7 W	1.4 W

7.8 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
P_O	Output power	vs Supply voltage	Figure 1
		vs Load resistance	Figure 2, Figure 3
P_D	Power dissipation	vs Output power	Figure 4, Figure 5
	Maximum ambient temperature	vs Power dissipation	Figure 6
	Total harmonic distortion + noise	vs Output power	Figure 7, Figure 8
		vs Frequency	Figure 9, Figure 10, Figure 11, Figure 12
		vs Common-mode input voltage	Figure 13
	Supply voltage rejection ratio	vs Frequency	Figure 14, Figure 15, Figure 16, Figure 17
	Supply voltage rejection ratio	vs Common-mode input voltage	Figure 18
	GSM Power supply rejection	vs Time	Figure 19
	GSM Power supply rejection	vs Frequency	Figure 20
CMRR	Common-mode rejection ratio	vs Frequency	Figure 21
		vs Common-mode input voltage	Figure 22
	Closed loop gain/phase	vs Frequency	Figure 23
	Open loop gain/phase	vs Frequency	Figure 24
I_{DD}	Supply current	vs Supply voltage	Figure 25
	Start-up time	vs Bypass capacitor	Figure 26

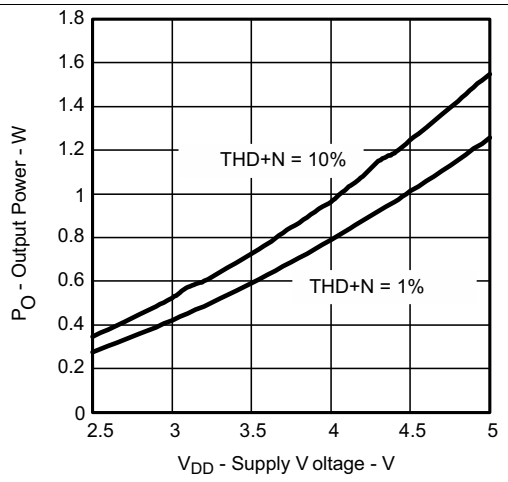


Figure 1. Output Power vs Supply Voltage

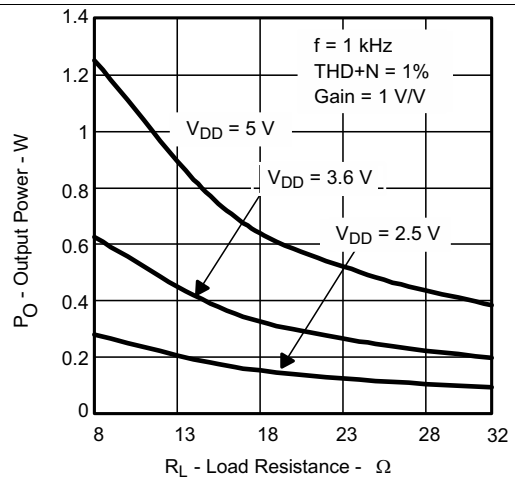


Figure 2. Output Power vs Load Resistance

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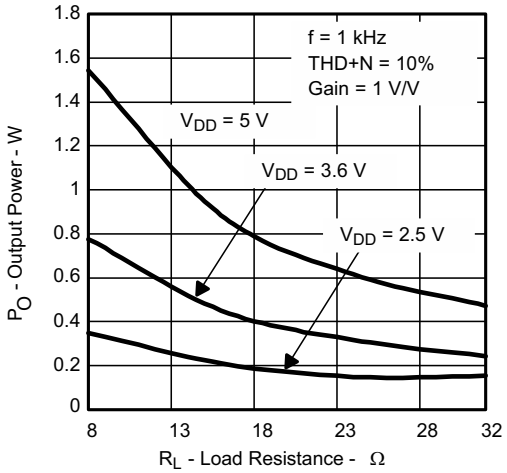


Figure 3. Output Power vs Load Resistance

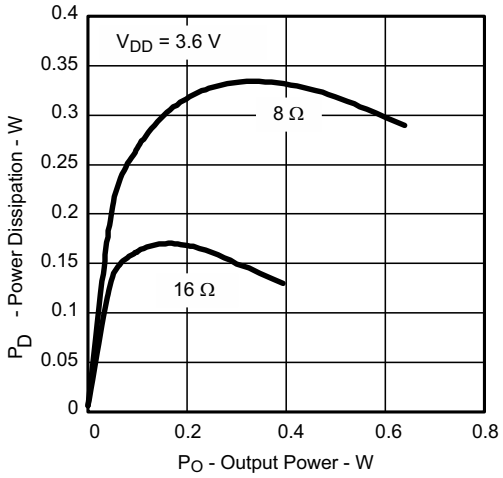


Figure 4. Power Dissipation vs Output Power

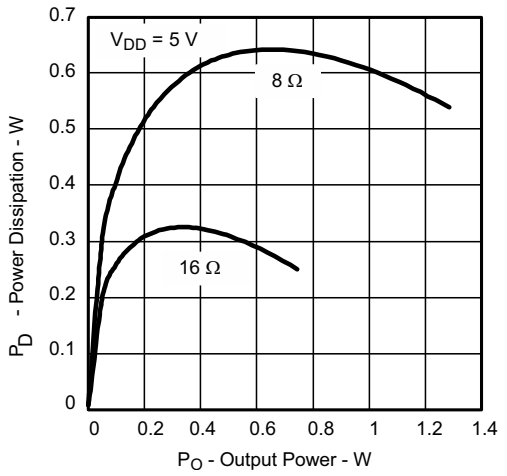


Figure 5. Power Dissipation vs Output Power

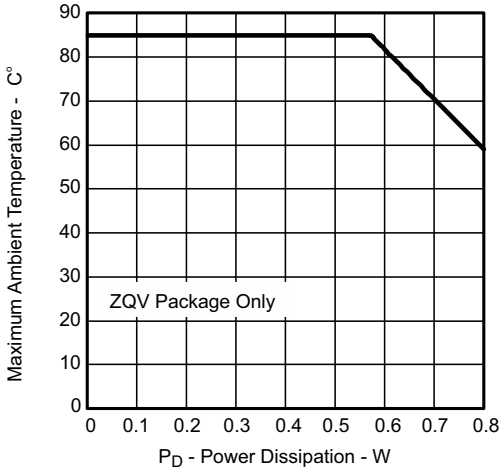


Figure 6. Maximum Ambient Temperature vs Power Dissipation

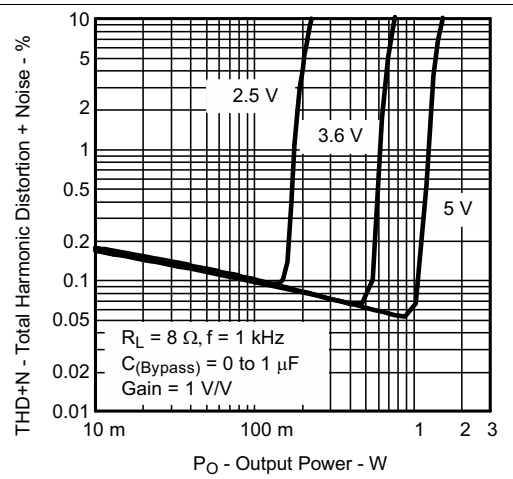


Figure 7. Total Harmonic Distortion + Noise vs Output Power

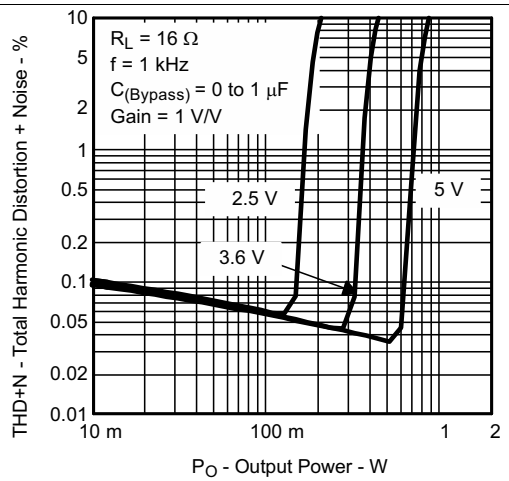


Figure 8. Total Harmonic Distortion + Noise vs Output Power

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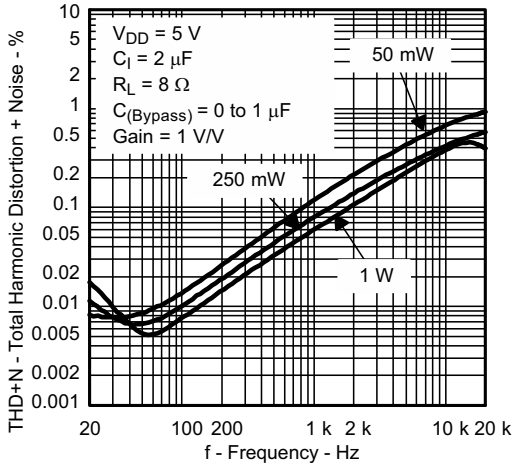


Figure 9. Total Harmonic Distortion + Noise vs Frequency

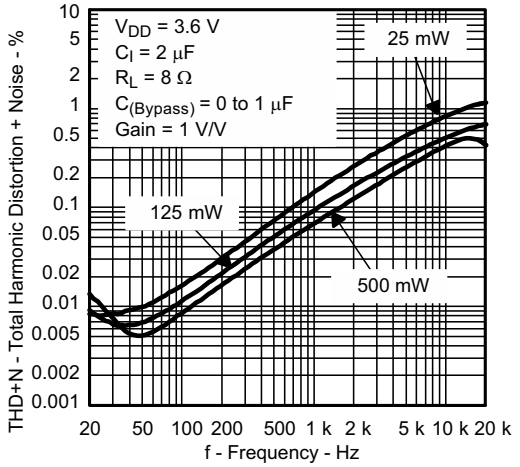


Figure 10. Total Harmonic Distortion + Noise vs Frequency

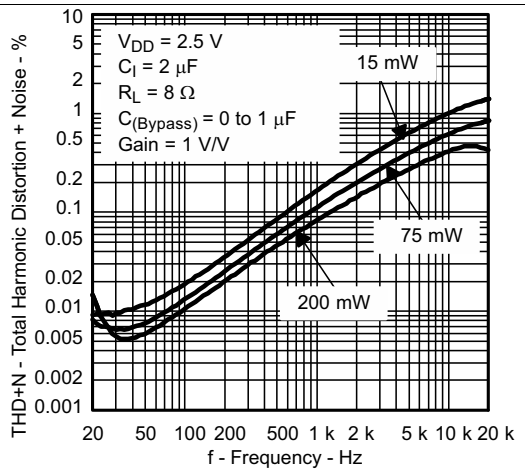


Figure 11. Total Harmonic Distortion + Noise vs Frequency

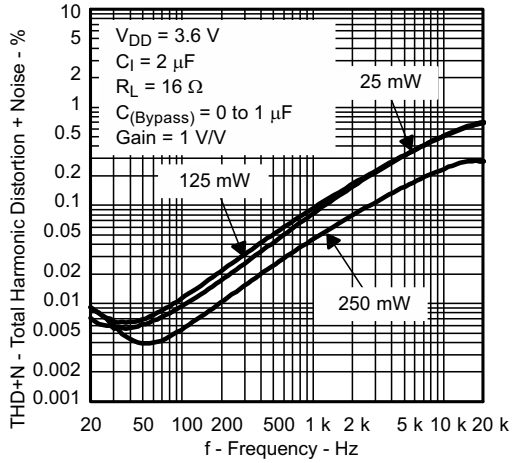


Figure 12. Total Harmonic Distortion + Noise vs Frequency

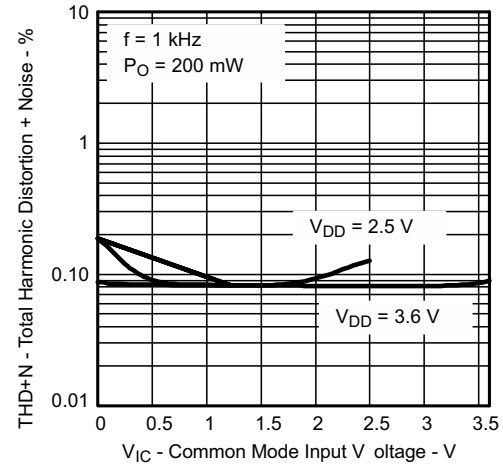


Figure 13. Total Harmonic Distortion + Noise vs Common-Mode Input Voltage

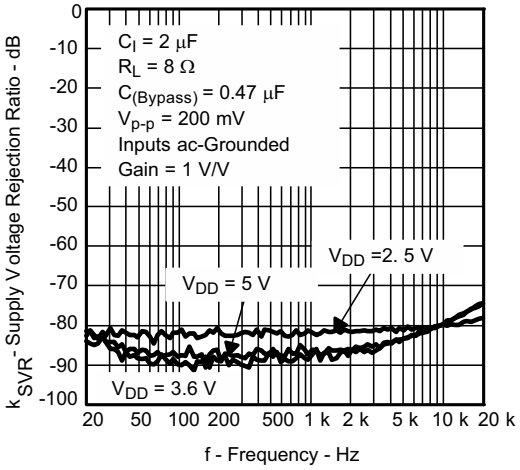


Figure 14. Supply Voltage Rejection Ratio vs Frequency

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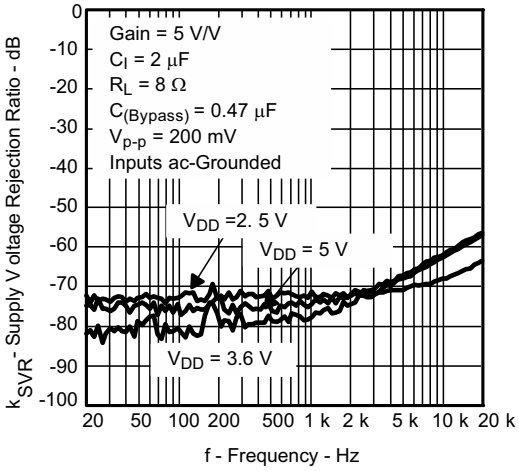


Figure 15. Supply Voltage Rejection Ratio vs Frequency

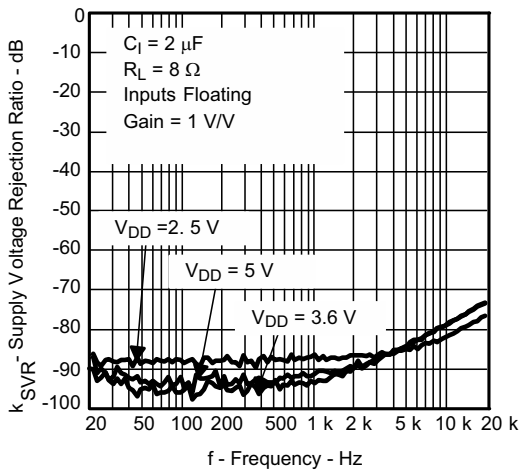


Figure 16. Supply Voltage Rejection Ratio vs Frequency

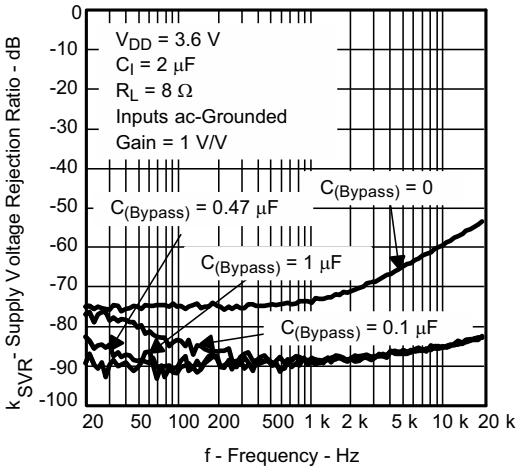


Figure 17. Supply Voltage Rejection Ratio vs Frequency

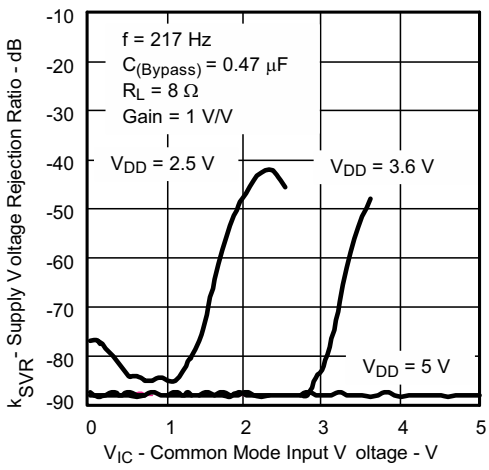


Figure 18. Supply Voltage Rejection Ratio vs Common-Mode Input Voltage

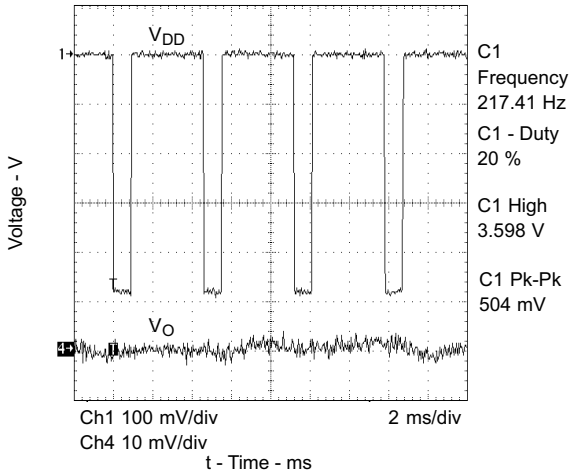


Figure 19. GSM Power Supply Rejection vs Time

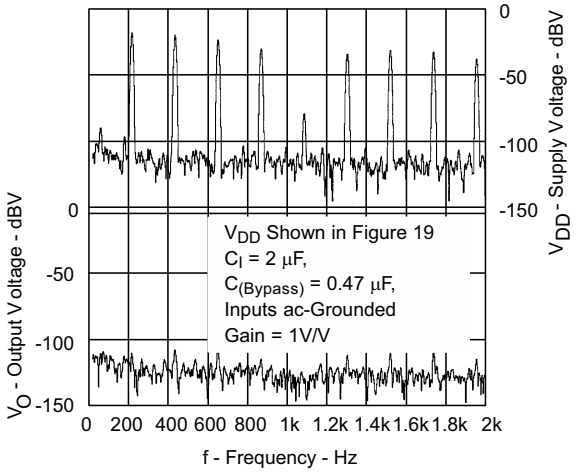


Figure 20. GSM Power Supply Rejection vs Frequency

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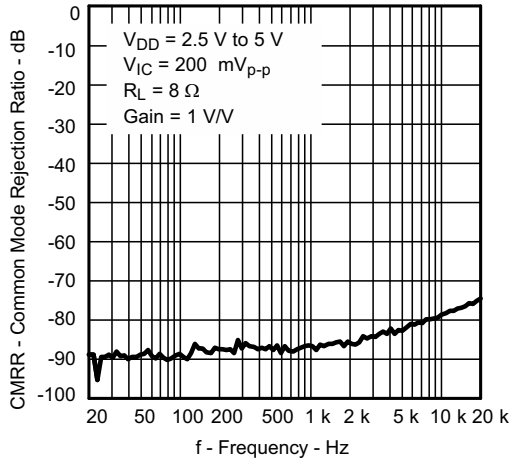


Figure 21. Common-Mode Rejection Ratio vs Frequency

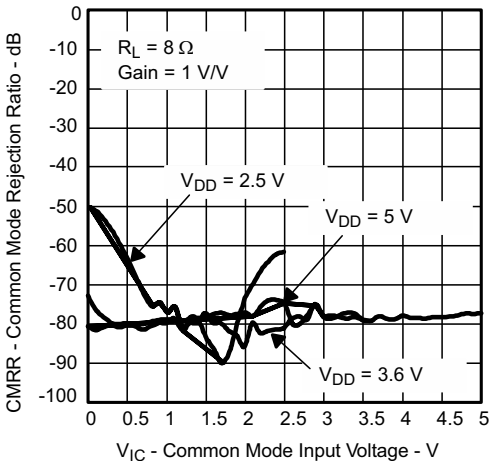


Figure 22. Common-Mode Rejection Ratio vs Common-Mode Input Voltage

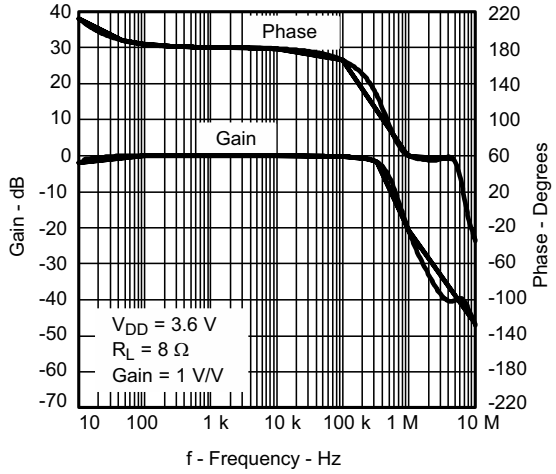


Figure 23. Closed-Loop Gain / Phase vs Frequency

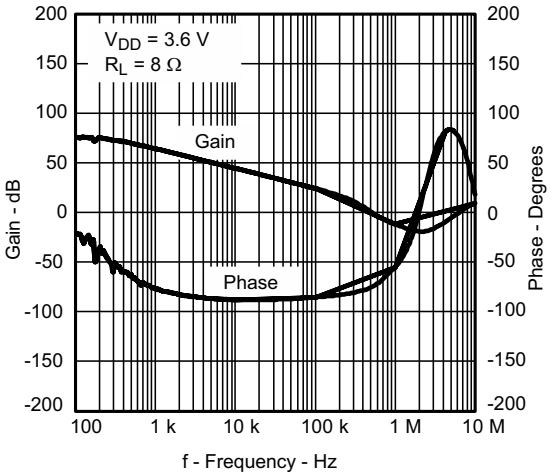


Figure 24. Open-Loop Gain / Phase vs Frequency

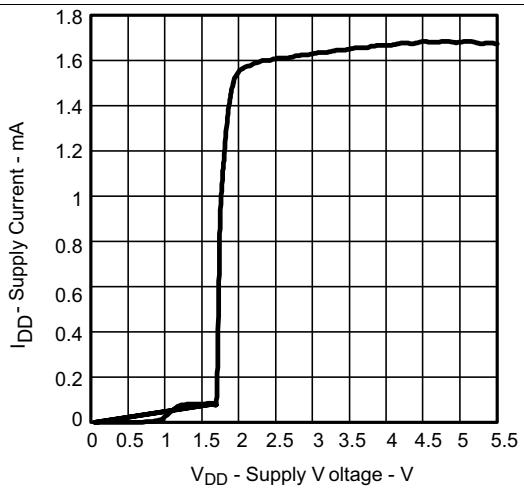
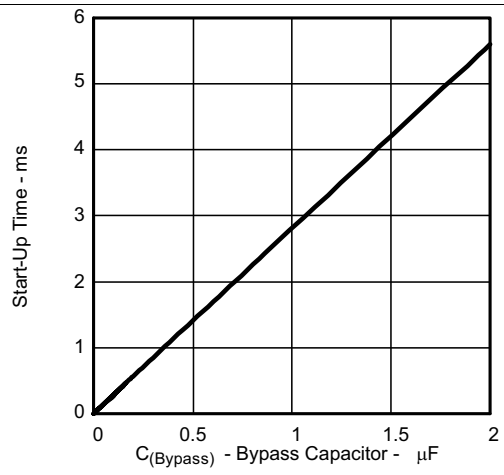


Figure 25. Supply Current vs Supply Voltage



Start-Up time is the time it takes (from a low-to-high transition on SHUTDOWN) for the gain of the amplifier to reach –3 dB of the final gain

Figure 26. Start-Up Time vs Bypass Capacitor

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8 Parameter Measurement Information

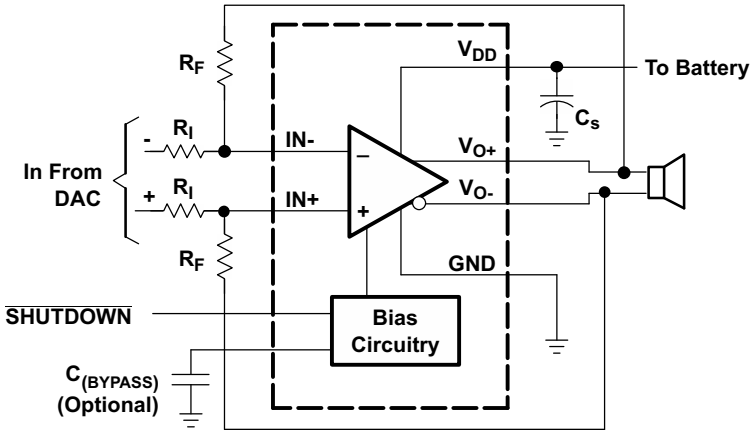
All parameters are measured according to the conditions described in the *Specifications* section.

9 Detailed Description

9.1 Overview

The TPA6205A1 is a 1.25-W mono fully differential amplifier. The devices operates in the range of 2.5 V to 5.5 V and with at least 8-Ω impedance load. It's fully differential input allows it to avoid using input coupling capacitors and improves its RF-immunity.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fully Differential Amplifiers

The TPA6205A1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input.

9.3.1.1 Advantages of Fully Differential Amplifiers

- Input coupling capacitors not required: A fully differential amplifier with good CMRR, like the TPA6205A1, allows the inputs to be biased at voltage other than mid-supply. For example, if a DAC has mid-supply lower than the mid-supply of the TPA6205A1, the common-mode feedback circuit adjusts for that, and the TPA6205A1 outputs are still biased at mid-supply of the TPA6205A1. The inputs of the TPA6205A1 can be biased from 0.5 V to V_{DD} – 0.8 V. If the inputs are biased outside of that range, input coupling capacitors are required.
- Mid-supply bypass capacitor, $C_{(BYPASS)}$, not required: The fully differential amplifier does not require a bypass capacitor. This is because any shift in the mid-supply affects both positive and negative channels equally and cancels at the differential output. However, removing the bypass capacitor slightly worsens power supply rejection ratio (k_{SVR}), but a slight decrease of k_{SVR} may be acceptable when an additional component can be eliminated (see Figure 17).
- Better RF-immunity: GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

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Feature Description (continued)

9.3.2 Fully Differential Amplifier Efficiency and Thermal Information

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or DC voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the average value of the supply current, $I_{DD(avg)}$, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts Although the voltages and currents for SE and BTL out as being equal to the ratio of power from the are sinusoidal in the load, currents from the supply power supply to the power delivered to the load. To are very different between SE and BTL accurately calculate the RMS and average values of configurations. In an SE application the current power in the load and in the amplifier, the current and waveform is a half-wave rectified shape, whereas in voltage waveform shapes must first be understood BTL it is a full-wave rectified waveform. This means (see Figure 27). RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. Equation 1 through Equation 7 are the basis for calculating amplifier efficiency.

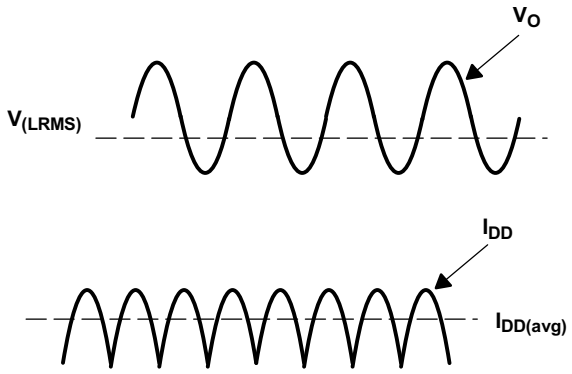


Figure 27. Voltage and Current Waveforms for BTL Amplifiers

$$\text{Efficiency a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

where

- $P_L = \frac{V_L\text{rms2}}{R_L}$
- $V_{LRMS} = \frac{V_P}{\sqrt{2}}$
- P_L = Power delivered to load
- P_{SUP} = Power drawn from power supply
- V_{LRMS} = RMS voltage on BTL load
- R_L = Load resistance
- V_P = Peak voltage on BTL load (1)

Therefore, P_L is calculated by Equation 2:

$$P_L = \frac{V_L^2}{2R_L} \quad (2)$$

And P_{SUP} is calculated by Equation 3:

$$P_{SUP} = V_{DD}I_{DD}\text{avg}$$

where

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Feature Description (continued)

- P_{SUP} = Power drawn from power supply
- I_{DDavg} = Average current drawn from the power supply
- V_{DD} = Power supply voltage (3)

I_{DDavg} can be found in Equation 4:

$$I_{DD}avg = \frac{1}{\pi}\int_0^{\pi}\frac{V_P}{R_L}\sin(t)\,dt = -\frac{1}{\pi}\times\frac{V_P}{R_L}\left[\cos(t)\right]_0^{\pi} = \frac{2V_P}{\pi R_L} \quad (4)$$

Therefore P_{SUP} is calculated by Equation 5:

$$P_{SUP} = \frac{2V_{DD}V_P}{\pi R_L} \quad (5)$$

substituting PL and PSUP into Equation 6,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{{V_P}^2}{2R_L}}{\frac{2V_{DD}V_P}{\pi R_L}} = \frac{\pi V_P}{4V_{DD}}$$

where

- $V_P = \sqrt{2P_L R_L}$ (6)

Therefore:

$$\eta_{BTL} = \frac{\pi\sqrt{2P_L R_L}}{4V_{DD}}$$

where

- η_{BTL} = Efficiency of a BTL amplifier (7)

Table 2. Efficiency and Maximum Ambient Temperature vs Output Power in 5-V 8- Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	INTERNAL DISSIPATION (W)	POWER FROM SUPPLY (W)	MAX AMBIENT TEMPERATURE (°C)
0.25	31.4	0.55	0.75	62
0.5	44.4	0.62	1.12	54
1	62.8	0.59	1.59	58
1.25	70.2	0.53	1.78	65

Table 2 employs Equation 7 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a 1.25-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 1.8 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in Equation 7, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

Equation 8 is a simple formula for calculating the maximum power dissipated, P_{Dmax}, may be used for a differential output application:

$$P_{Dmax} = \frac{2\,{V^2}_{DD}}{\pi^2 R_L} \quad (8)$$

P_{Dmax} for a 5-V, 8-Ω system is 634 mW.

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The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the 2 mm × 2 mm Microstar Junior package is shown in the dissipation rating table. Converting this to θJA is shown in Equation 9:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0088} = 113°C / W \tag{9}$$

Given θJA, the maximum allowable junction temperature, and the maximum internal dissipation, the maximum ambient temperature can be calculated with Equation 10. The maximum recommended junction temperature for the TPA6205A1 is 125°C.

$$T_A Max = T_J Max - \Theta_{JA} P_{D max}$$
$$= 125 - 113(0.634) = 53.3°C \tag{10}$$

Equation 10 shows that the maximum ambient temperature is 53.3°C at maximum power dissipation with a 5-V supply. Table 2 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA6205A1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using more resistive than 8-Ω packages, it is good practice minimize the speakers dramatically increases the thermal performance by reducing the output current.

9.3.3 Differential Output Versus Single-Ended Output

Figure 28 shows a Class-AB audio power amplifier (APA) in a fully differential configuration. The TPA6205A1 amplifier has differential outputs driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging 2 × $V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 11).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$
$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \tag{11}$$

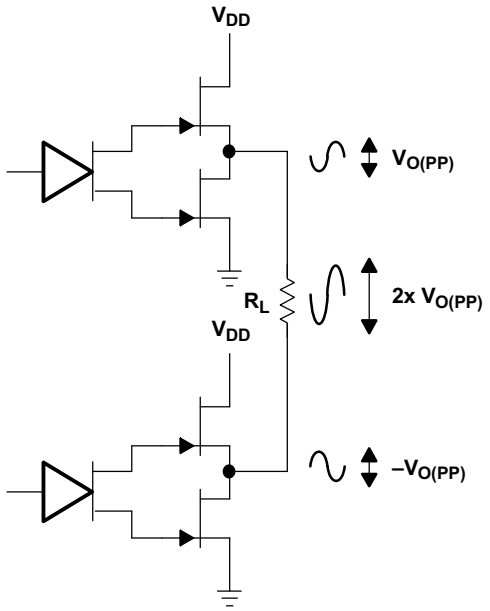


Figure 28. Differential Output Configuration

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In a typical wireless handset operating at 3.6 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 200 mW to 800 mW. In sound power that is a 6-dB improvement—which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 29. A coupling capacitor is required to block the DC offset voltage from reaching the load. This capacitor can be quite large (approximately 33 µF to 1000 µF) so it tends to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency-limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 12.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{12}$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the DC offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

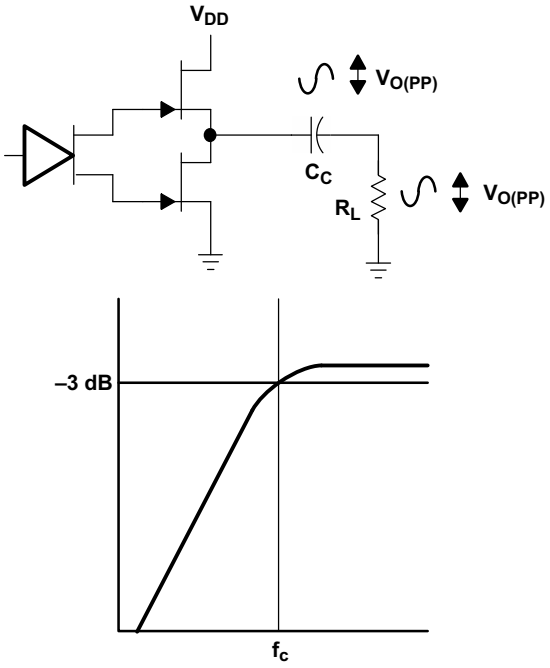


Figure 29. Single-Ended Output and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration.

9.4 Device Functional Modes

9.4.1 Summing Input Signals With The TPA6205A1

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The TPA6205A1 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

9.4.1.1 Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 10 components). The gain for each input source can be set independently (see Equation 13 and Equation 14, and Figure 30).

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Device Functional Modes (continued)

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = -\frac{R_F}{R_{I1}}\left(\frac{V}{V}\right) \quad (13)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = -\frac{R_F}{R_{I2}}\left(\frac{V}{V}\right) \quad (14)$$

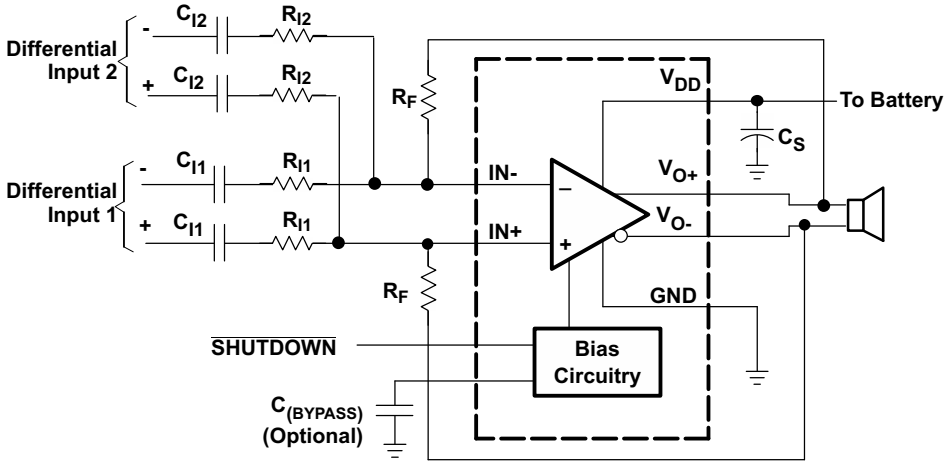


Figure 30. Application Schematic With TPA6205A1 Summing Two Differential Inputs

9.4.1.2 Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 31 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use. Both input nodes must see the same impedance for optimum performance, thus the use of RP and CP.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = -\frac{R_F}{R_{I1}}\left(\frac{V}{V}\right) \quad (15)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = -\frac{R_F}{R_{I2}}\left(\frac{V}{V}\right) \quad (16)$$

9.4.1.3 Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (fc1 and fc2) for each input source can be set independently. Resistor, RP, and capacitor, CP, are needed on the IN+ terminal to match the impedance on the IN- terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an AC signal.

$$\textit{Gain 1} = \frac{V_o}{V_{I1}} = \frac{2 \times 150\ k\Omega}{R_{I2}} \quad (17)$$

$$\textit{Gain 2} = \frac{V_o}{V_{I2}} = \frac{2 \times 150\ k\Omega}{R_{I2}} \quad (18)$$

$$C_{I1} = \frac{1}{2\pi R_{I1} F_{C1}} \quad (19)$$

$$C_{I2} = \frac{1}{2\pi R_{I2} F_{C2}} \quad (20)$$

$$C_P = C_{I1} + C_{I2} \quad (21)$$

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Device Functional Modes (continued)

$$R_P = \frac{R_{I1} \times R_{I2}}{R_{I1} + R_{I2}} \quad (22)$$

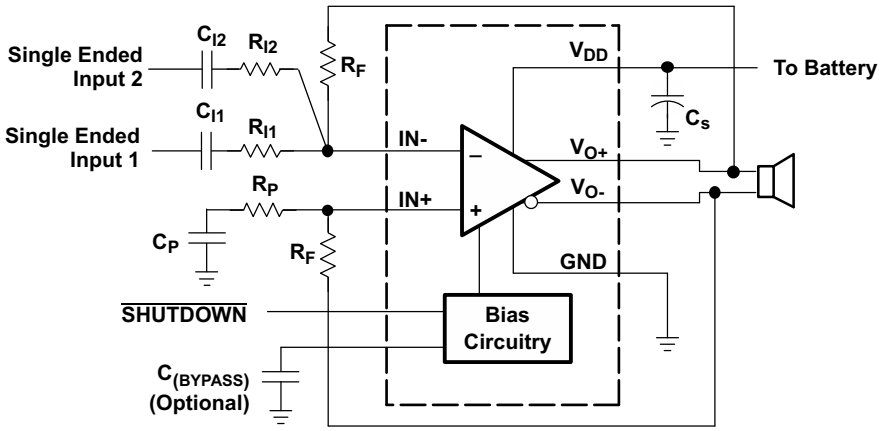


Figure 31. Application Schematic With TPA6205A1 Summing Two Single-Ended Inputs

9.4.2 Shutdown Mode

The TPA6205A1 can be put in shutdown mode when asserting SHUTDOWN pin to a logic LOW. While in shutdown mode, the device output stage is turned off, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to SHUTDOWN pin. SHUTDOWN pin is 1.8-V compatible.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular cases. Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.2 Typical Applications

Figure 32 through Figure 31 show application schematics for differential and single-ended inputs.

10.2.1 TPA6205A1 With Differential Input

The TPA6205A1 can be used with differential input without input capacitors. This section describes the design considerations for this application.

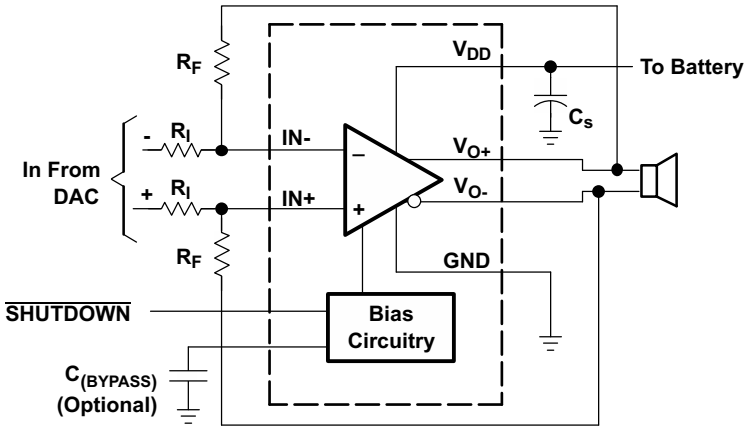


Figure 32. Typical Differential Input Application Schematic

10.2.1.1 Design Requirements

Table 3 lists the design parameters of the device.

Table 3. Design Parameters

PARAMETER	EXAMPLE VALUE
Power Supply	5 V
Shutdown Input	High > 2 V
	Low < 0.8 V
Speaker	8 Ω

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10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Selecting Components

Typical values are shown in Table 4.

Table 4. Typical Component Values

COMPONENT	VALUE
R_I	10 kΩ
R_F	10 kΩ
$C_{(BYPASS)}$ (1)	0.22 µF
C_S	1 µF
C_I	0.22 µF

(1) $C_{(BYPASS)}$ is optional

10.2.1.2.1.1 Resistors (RF and RI)

The input (R_I) and feedback resistors (R_F) set the gain of the amplifier according to Equation 23.

$$\text{Gain} - R_F / R_I \tag{23}$$

R_F and R_I should range from 1 kΩ to 100 kΩ. Most graphs were taken with $R_F = R_I = 20$ kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

10.2.1.2.1.2 Bypass Capacitor (C_{BYPASS}) and Start-Up Time

The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{DD}/2$. Adding a capacitor to this pin filters any noise into this pin and increases the k_{SVR}. $C_{(BYPASS)}$also determines the rise time of V_{O+} and V_{O-} when the device is taken out of shutdown. The larger the capacitor, the slower the rise time. Although the output rise time depends on the bypass capacitor value, the device passes audio 4 µs after taken out of shutdown and the gain is slowly ramped up based on $C_{(BYPASS)}$.

To minimize pops and clicks, design the circuit so the impedance (resistance and capacitance) detected by both inputs, IN+ and IN–, is equal.

10.2.1.2.1.3 Input Capacitor (C_I)

The TPA6205A1 does not require input coupling capacitors if using a differential input source that is biased from 0.5 V to V_{DD} – 0.8 V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper DC level. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in Equation 24.

$$f_c = \frac{1}{2\pi R_I C_I} \tag{24}$$

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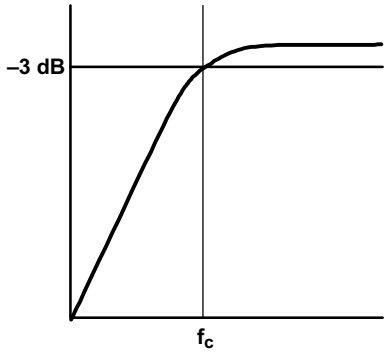


Figure 33. C_I and R_I High-Pass Filter Cutoff Frequency

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 100 Hz. Equation 24 is reconfigured as Equation 25.

$$C_I = \frac{1}{2\pi R_I f_c} \tag{25}$$

In this example, C_I is 0.16 µF, so one would likely choose a value in the range of 0.22 µF to 0.47 µF. A further consideration for this capacitor is the leakage path from the input source through the input network

(R_I , C_I) and the feedback resistor (R_F) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

10.2.1.2.1.4 Decoupling Capacitor (C_S)

The TPA6205A1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF to 1 µF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

10.2.1.2.2 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

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10.2.1.3 Application Curves

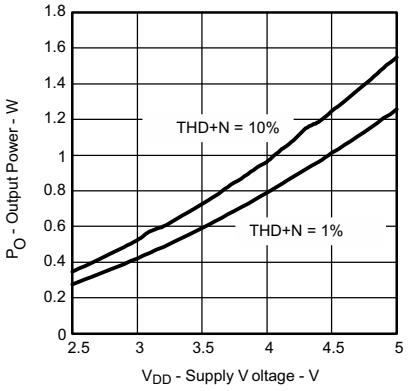


Figure 34. Output Power vs Supply Voltage

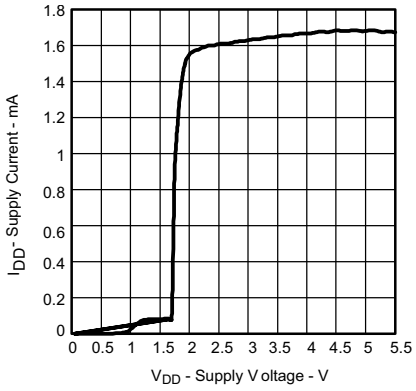


Figure 35. Supply Current vs Supply Voltage

10.2.2 TPA6205A1 With Differential Input and Input Capacitors

The TPA6205A1 supports differential input operation with input capacitors. This section describes the design considerations for this application.

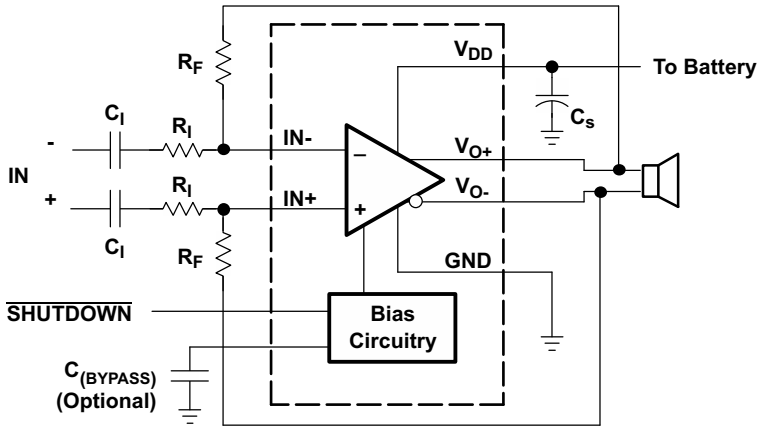


Figure 36. Differential Input Application Schematic Optimized With Input Capacitors

10.2.2.1 Design Requirements

Refer to the *Design Requirements*.

10.2.2.2 Detailed Design Procedure

Refer to the *Detailed Design Procedure*.

10.2.2.3 Application Curves

Refer to the *Application Curves*.

10.2.3 TPA6205A1 With Single-Ended Input

The TPA6205A1 can be used with single-ended inputs, using Input capacitors. This section describes the design considerations for this application.

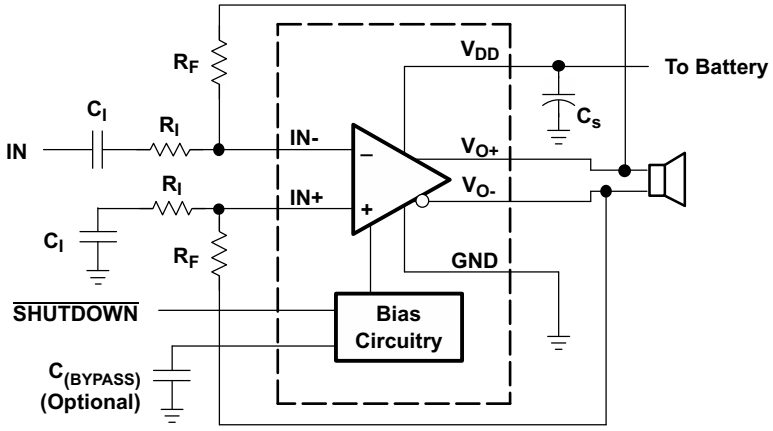


Figure 37. Single-Ended Input Application Schematic

10.2.3.1 Design Requirements

Refer to the *Design Requirements*.

10.2.3.2 Detailed Design Procedure

Refer to the *Detailed Design Procedure*.

10.2.3.3 Application Curves

Refer to the *Application Curves*.

11 Power Supply Recommendations

The TPA6205A1 is designed to operate from an input voltage supply range between 2.5-V and 5.5-V. Therefore, the output voltage range of power supply should be within this range and well regulated. The current capability of upper power should not exceed the maximum current limit of the power switch.

11.1 Power Supply Decoupling Capacitors

The TPA6205A1 requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD). Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, within 2 mm of the VDD pin. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. In addition to the 0.1 µF ceramic capacitor, is recommended to place a 2.2 µF to 10 µF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any drop in the supply voltage.

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12 Layout

12.1 Layout Guidelines

Placing the decoupling capacitors as close as possible to the device is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

For the DRB (QFN/SON) and DGN (MSOP) to presence of voids within the exposed thermal pad interconnection. Total elimination is difficult, but the design of the exposed pad stencil is key. The stencil design proposed in the Texas Instruments application note *QFN/SON PCB Attachment* (SLUA271) enables out-gassing of the solder paste during reflow as well as regulating the finished solder thickness. Typically the solder paste coverage is approximately 50% of the pad area.

In making the pad size for the BGA balls, it is recommended that the layout use soldermask-defined (SMD) land. With this method, the copper pad is made larger than the desired land area, and the opening size is defined by the opening in the solder mask material. The advantages normally associated with this technique include more closely controlled size and better copper adhesion to the laminate. Increased copper also increases the thermal performance of the IC. Better size control is the result of photo imaging the stencils for masks. Small plated vias should be placed near the center ball connecting ball B2 to the ground plane. Added plated vias and ground plane act as a heatsink and increase the thermal performance of the device. Figure 38 shows the appropriate diameters for a 2 mm × 2 mm MicroStar Junior™ BGA layout.

It is very important to keep the TPA6205A1 external components very close to the TPA6205A1 to limit noise pickup. The TPA6205A1 layout is shown in the next section as a layout example.

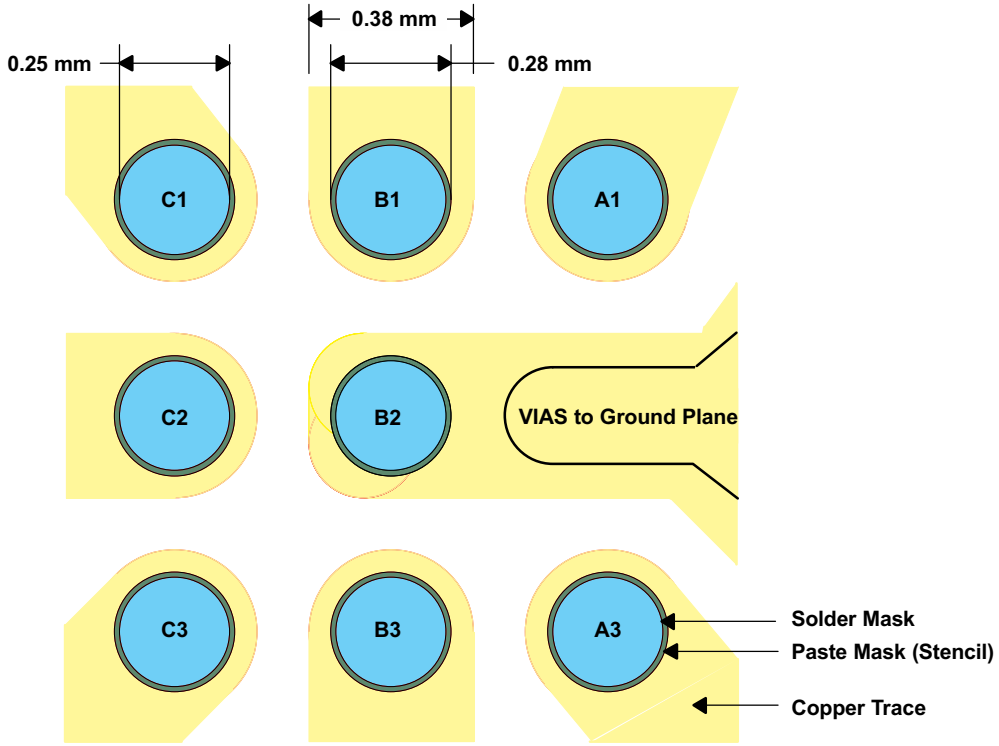


Figure 38. MicroStar Junior™ BGA Recommended Layout

12.2 Layout Example

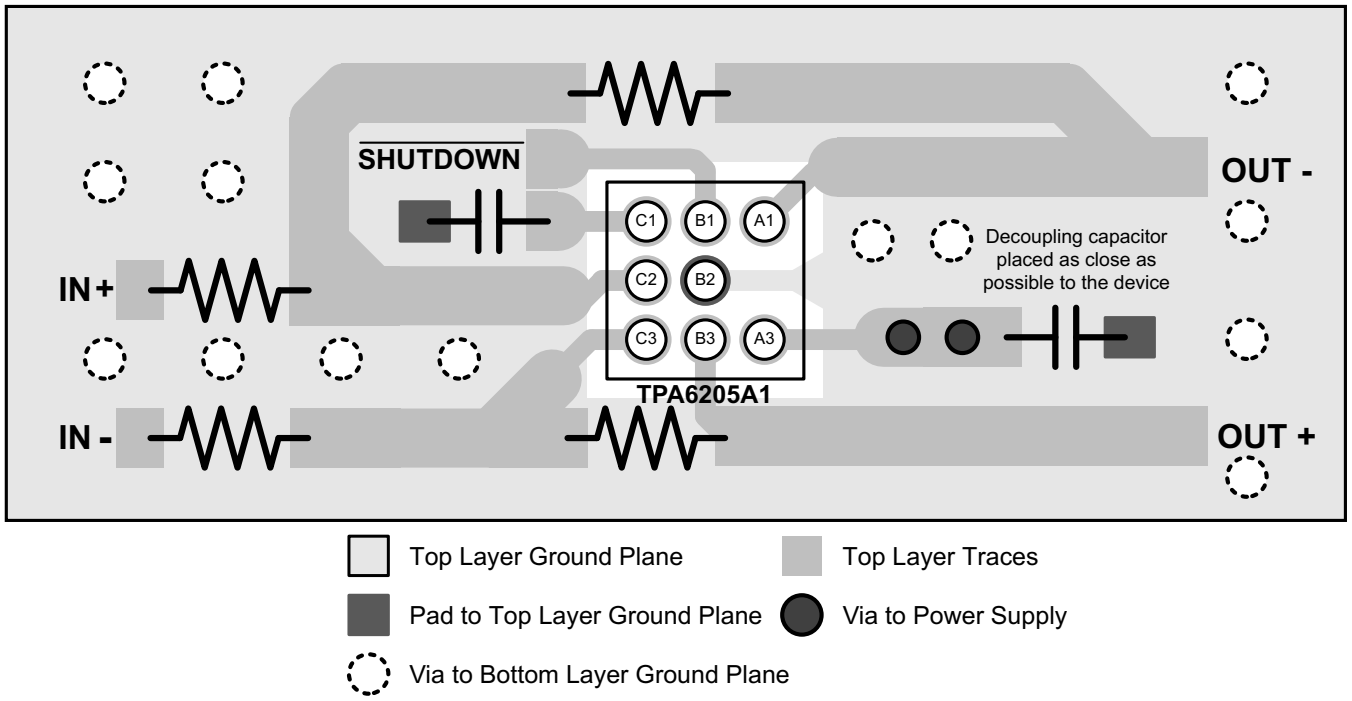


Figure 39. TPA6205A1 BGA Layout

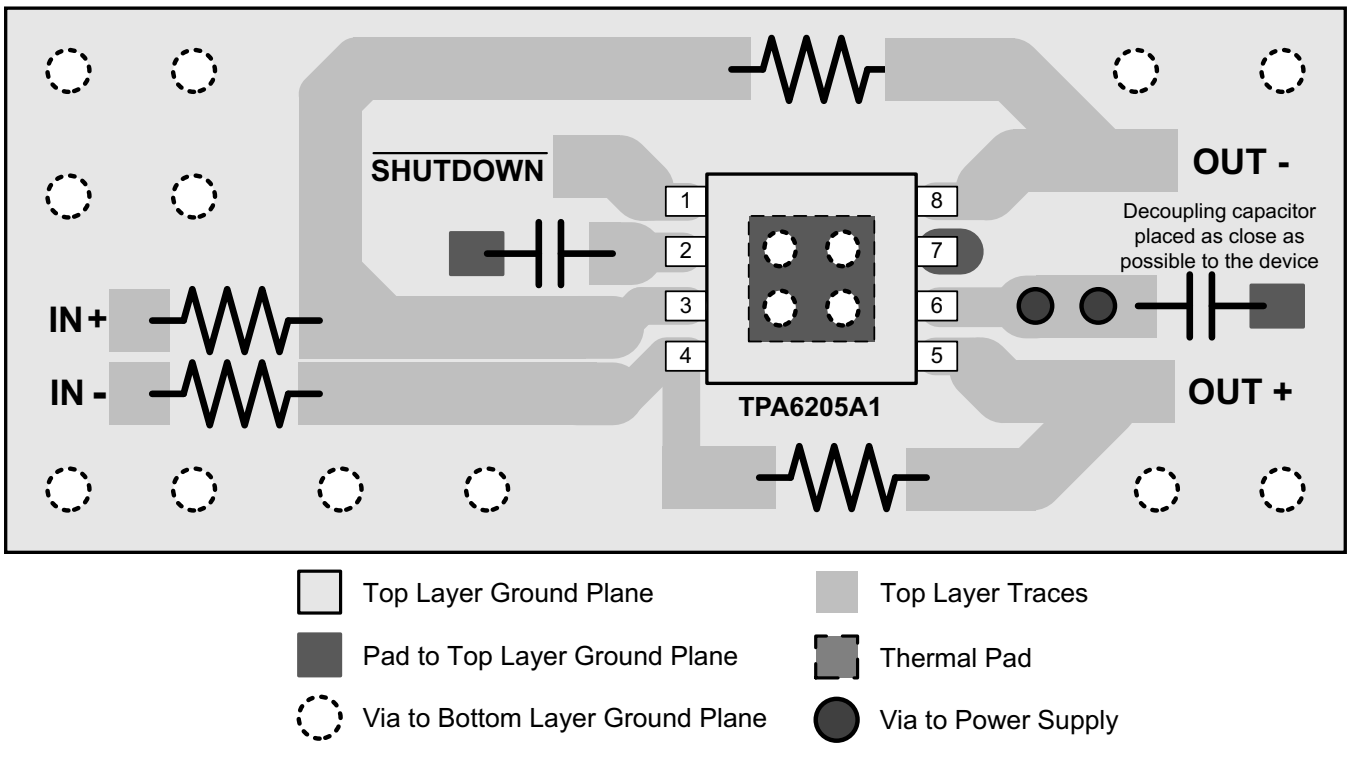


Figure 40. TPA6205A1 HVSSOP Layout

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Layout Example (continued)

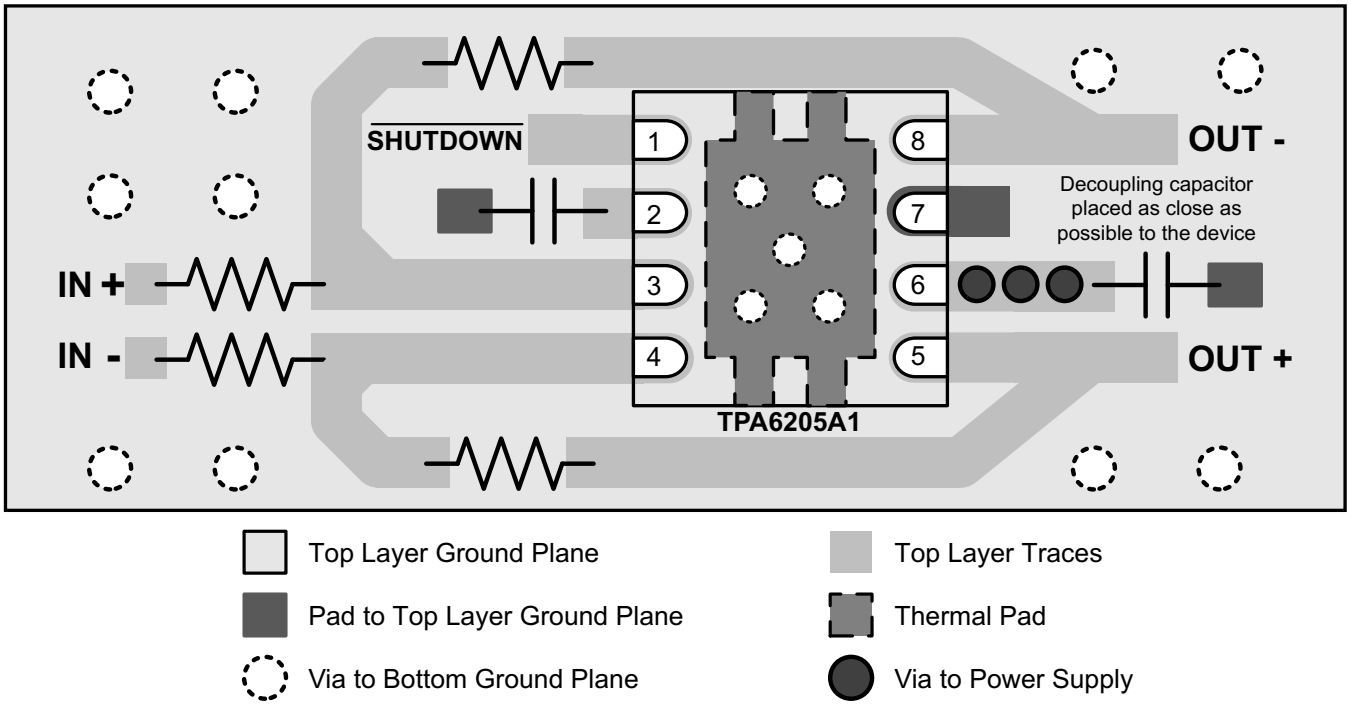


Figure 41. TPA6205A1 VSON Layout

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

MicroStar Junior, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6205A1DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AAPI
TPA6205A1DGN.B	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAPI
TPA6205A1DGNG4	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAPI
TPA6205A1DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AAPI
TPA6205A1DGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAPI
TPA6205A1DGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AAPI
TPA6205A1DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AAOI
TPA6205A1DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AAOI
TPA6205A1DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AAOI
TPA6205A1DRBRG4.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AAOI
TPA6205A1DRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AAOI
TPA6205A1DRBT.B	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AAOI
TPA6205A1NMBR	Active	Production	NFBGA (NMB) | 8	2500 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	AANI
TPA6205A1NMBR.B	Active	Production	NFBGA (NMB) | 8	2500 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	AANI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

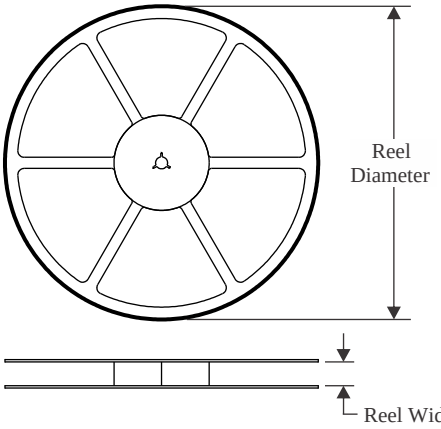
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

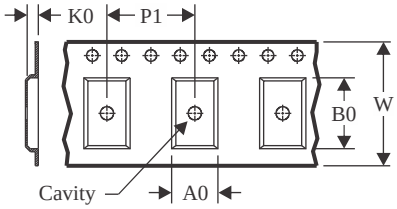
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

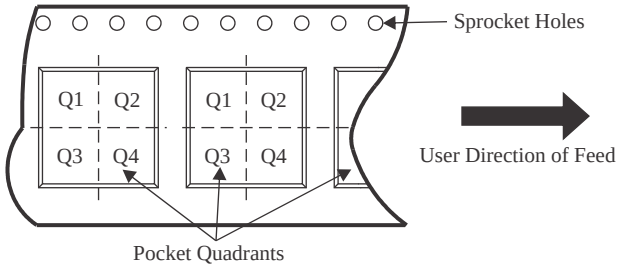


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

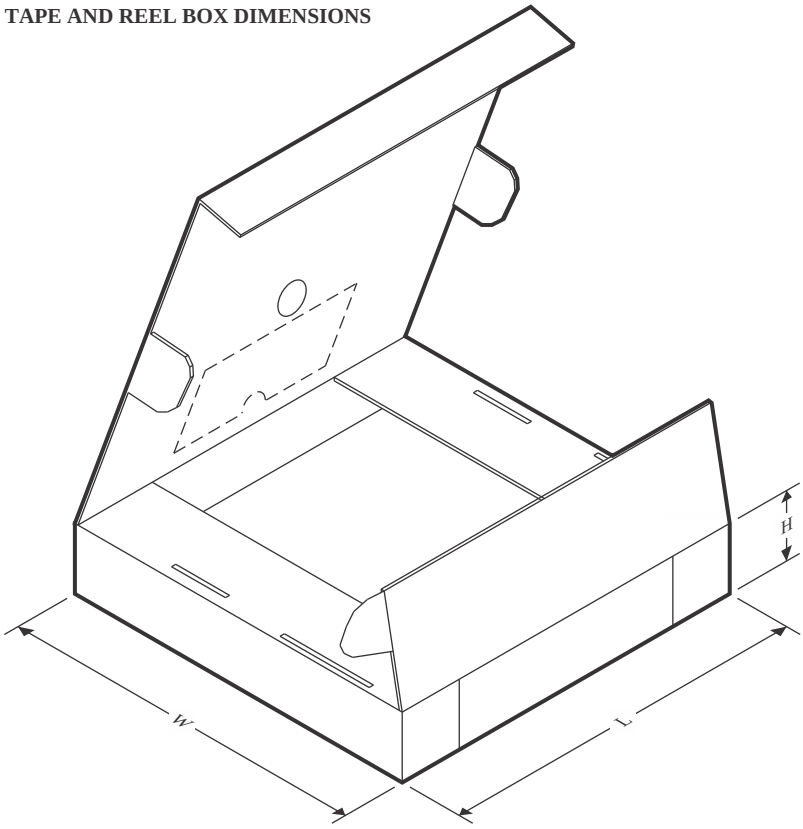
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6205A1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6205A1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6205A1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6205A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6205A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6205A1DRBRG4	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6205A1DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6205A1NMBR	NFBGA	NMB	8	2500	330.0	8.4	2.3	2.3	1.4	4.0	8.0	Q1

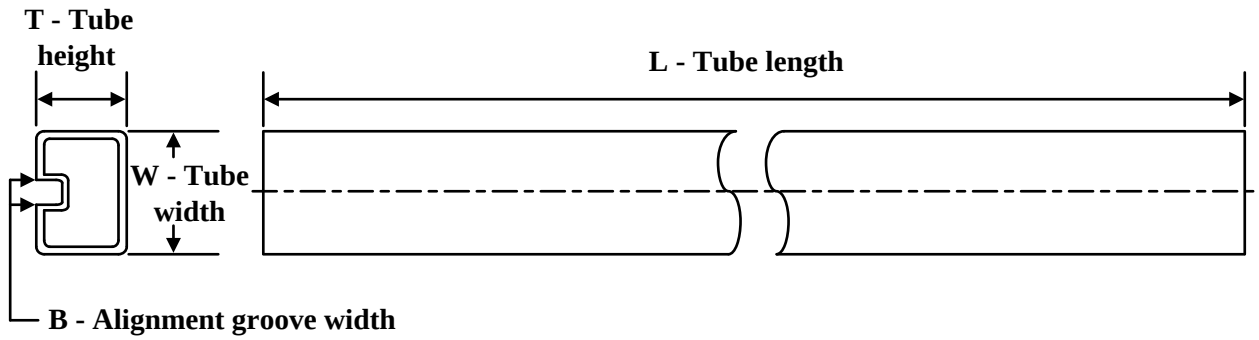
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6205A1DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPA6205A1DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPA6205A1DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPA6205A1DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPA6205A1DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPA6205A1DRBRG4	SON	DRB	8	3000	367.0	367.0	35.0
TPA6205A1DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPA6205A1NMBR	NFBGA	NMB	8	2500	338.1	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA6205A1DGN	DGN	HVSSOP	8	80	330.2	6.6	3005	1.88
TPA6205A1DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPA6205A1DGN.B	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPA6205A1DGN.B	DGN	HVSSOP	8	80	330.2	6.6	3005	1.88
TPA6205A1DGNG4	DGN	HVSSOP	8	80	330.2	6.6	3005	1.88
TPA6205A1DGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

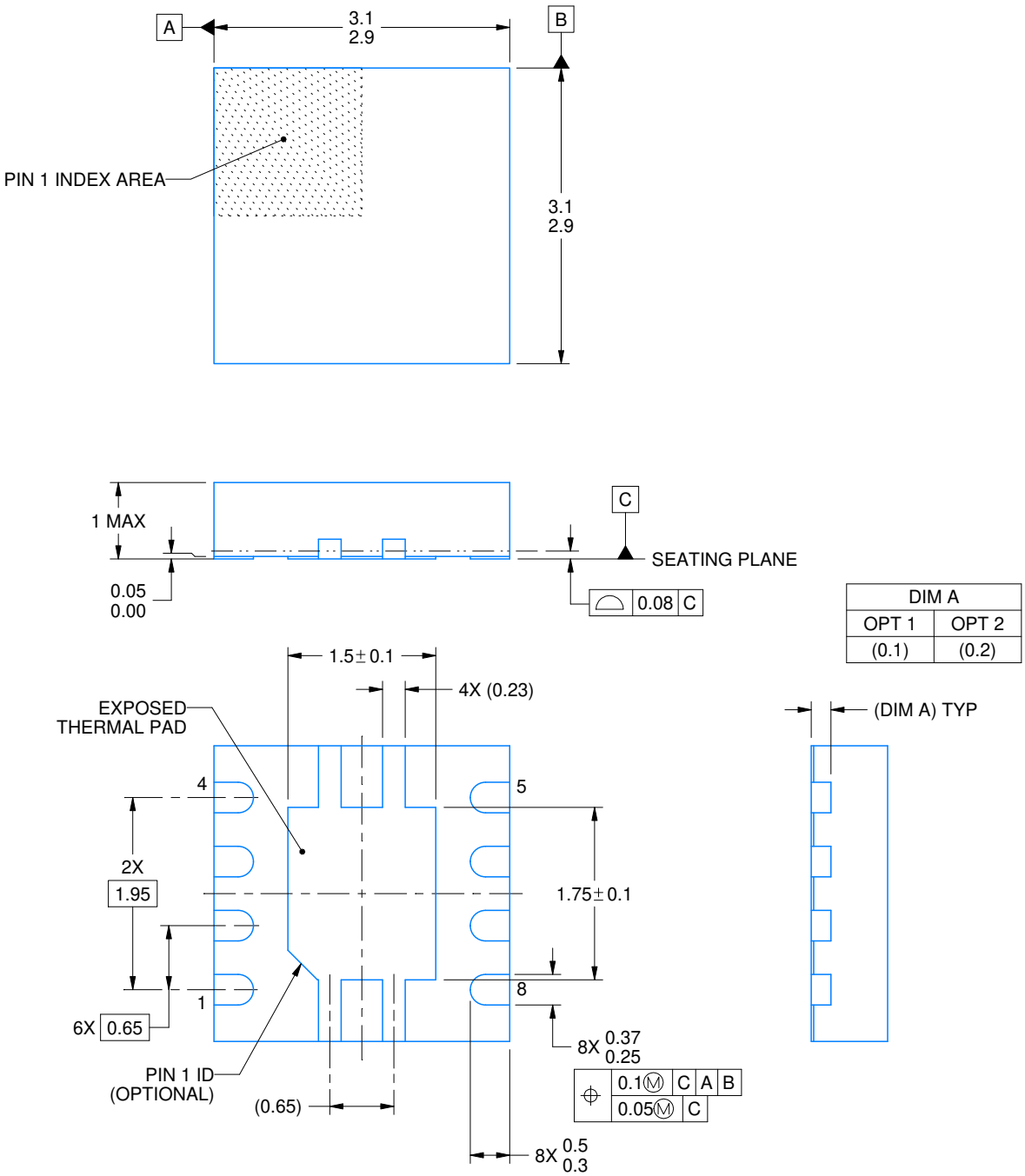
4203482/L

PACKAGE OUTLINE

DRB0008A

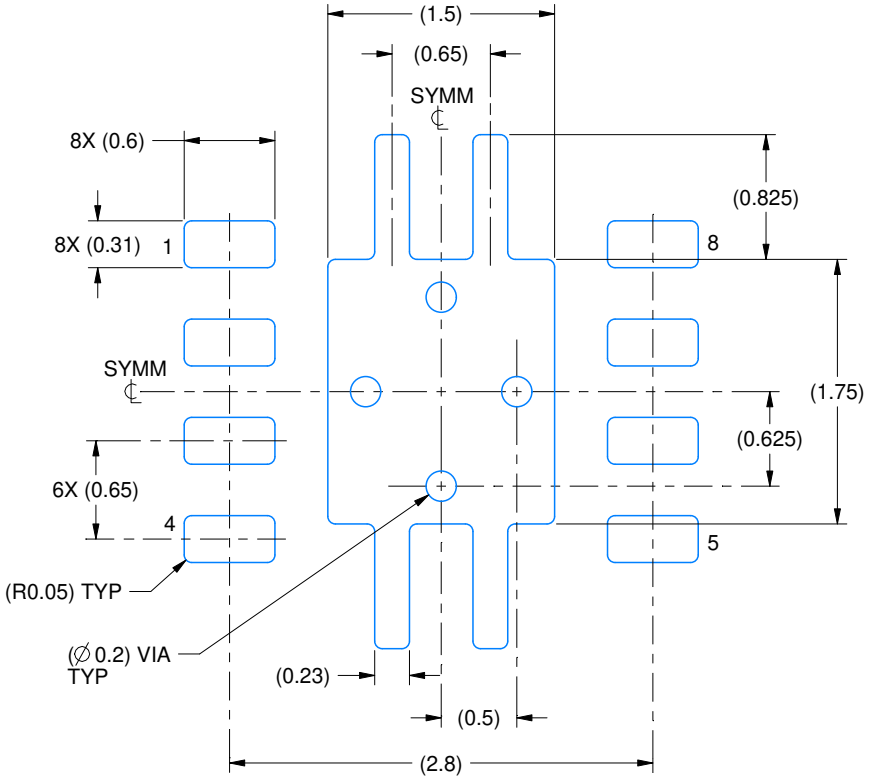
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

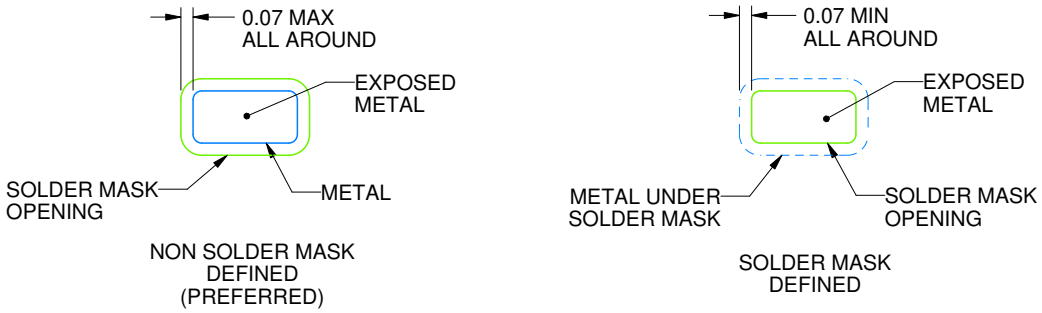


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

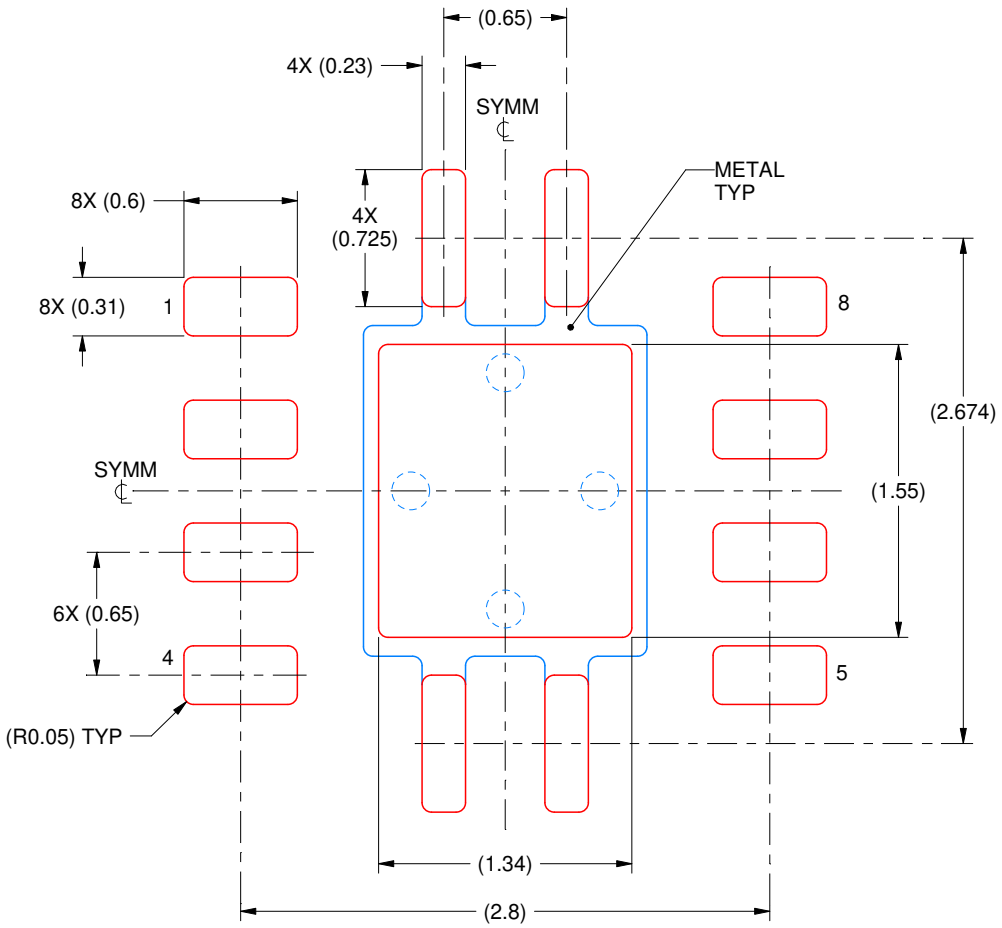


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

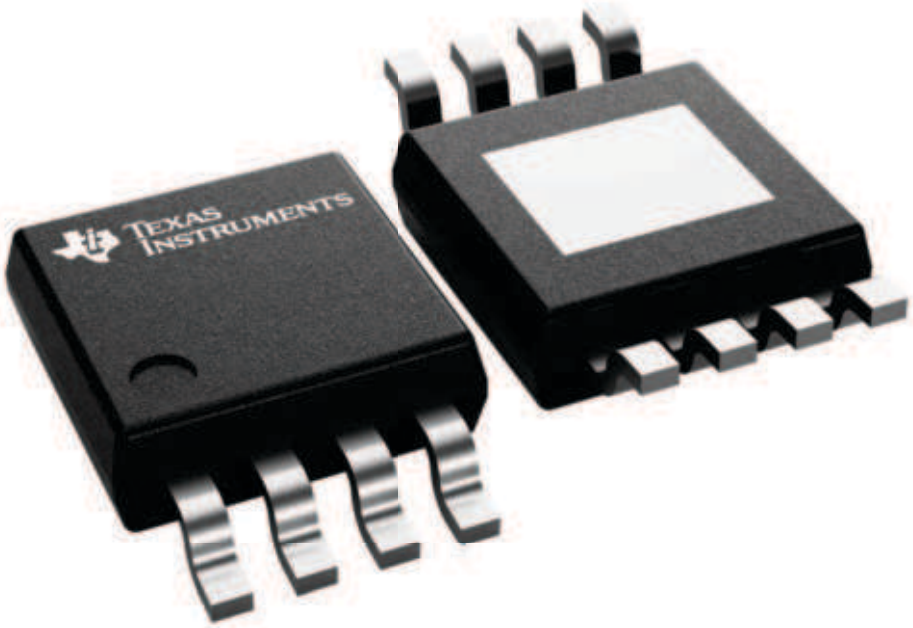
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

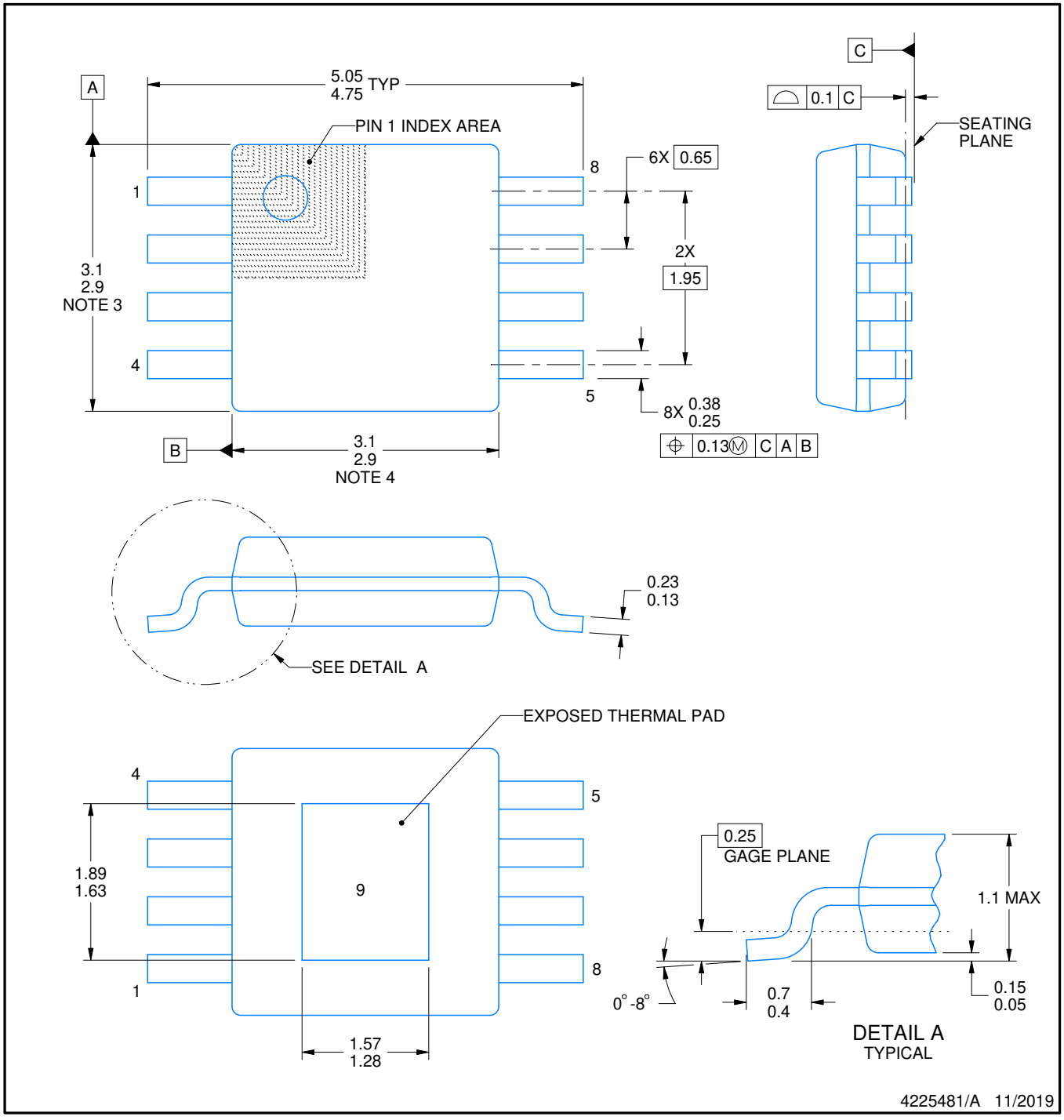
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

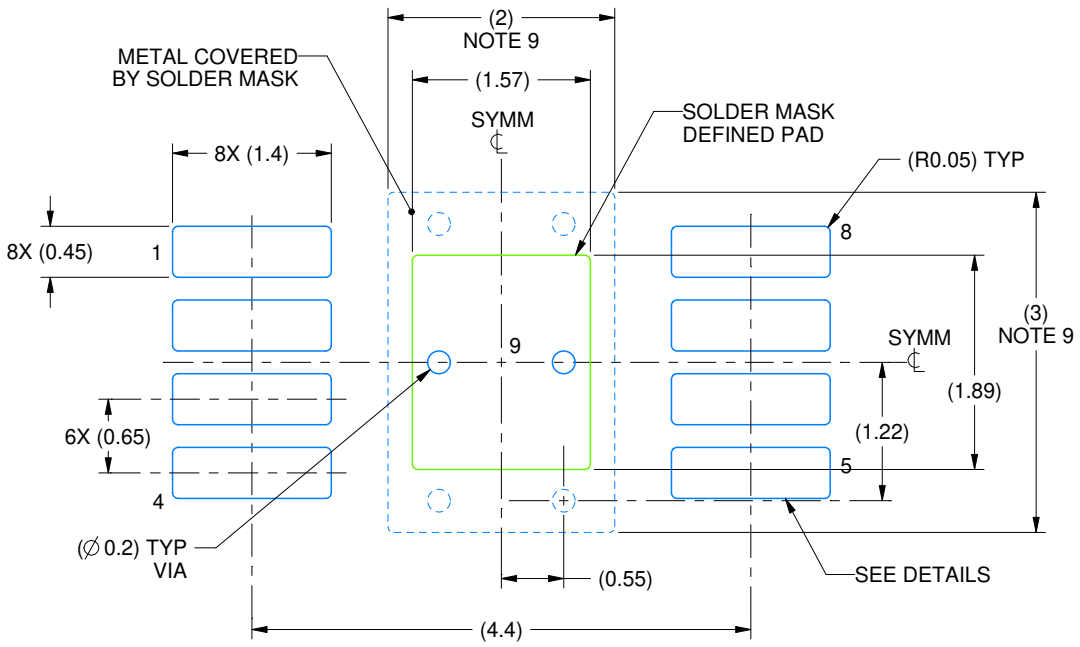
SMALL OUTLINE PACKAGE



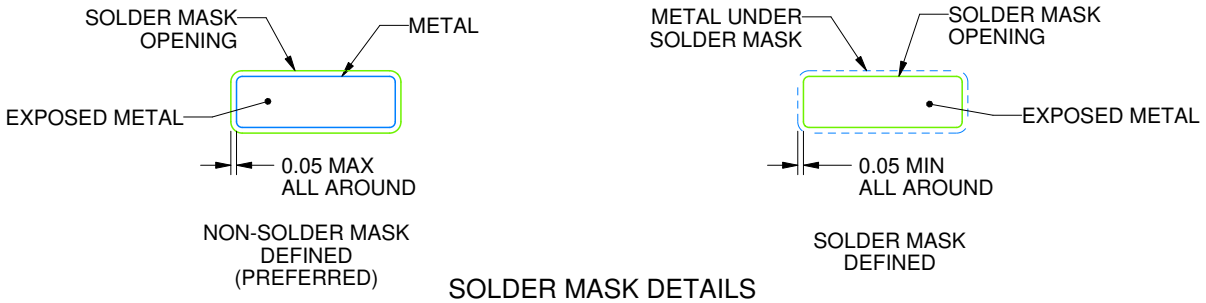
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

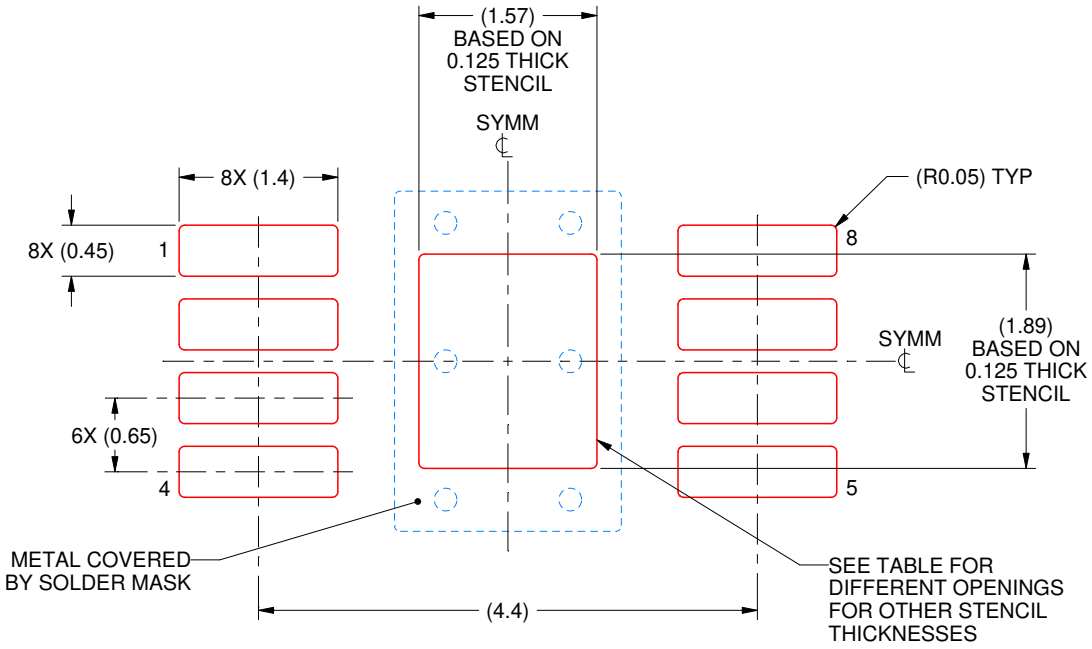


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

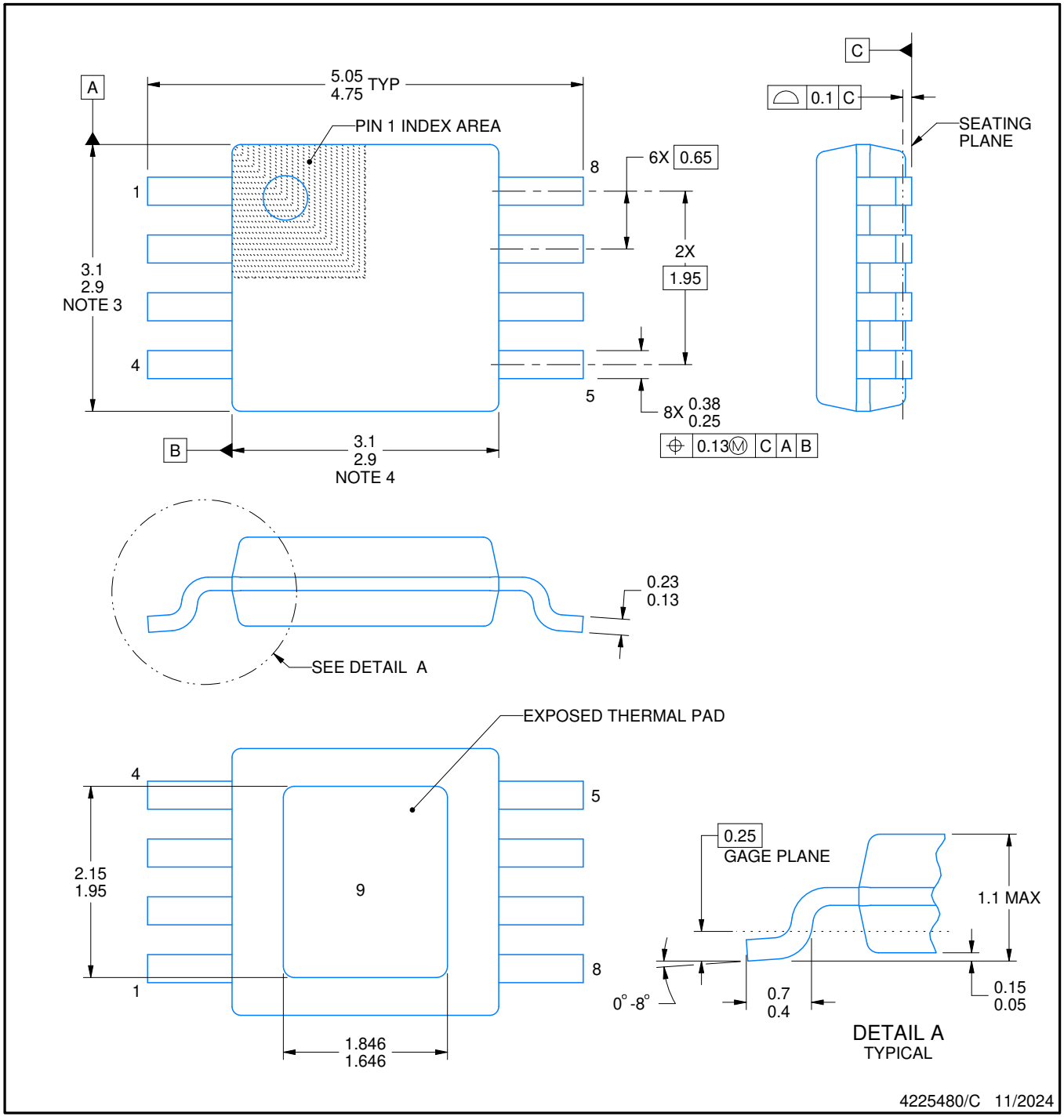
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

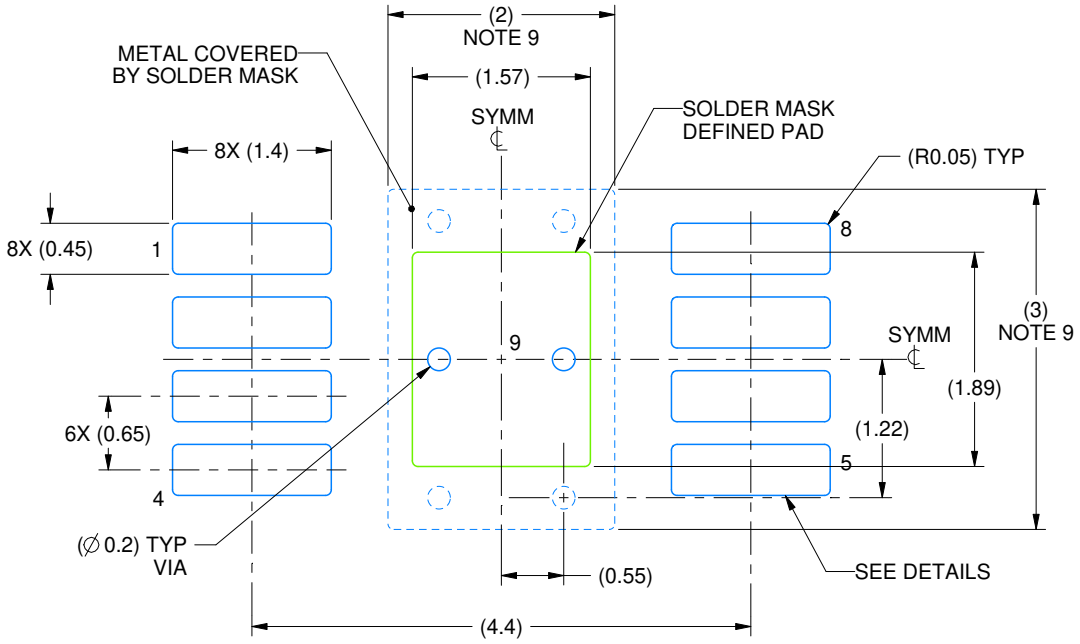
SMALL OUTLINE PACKAGE



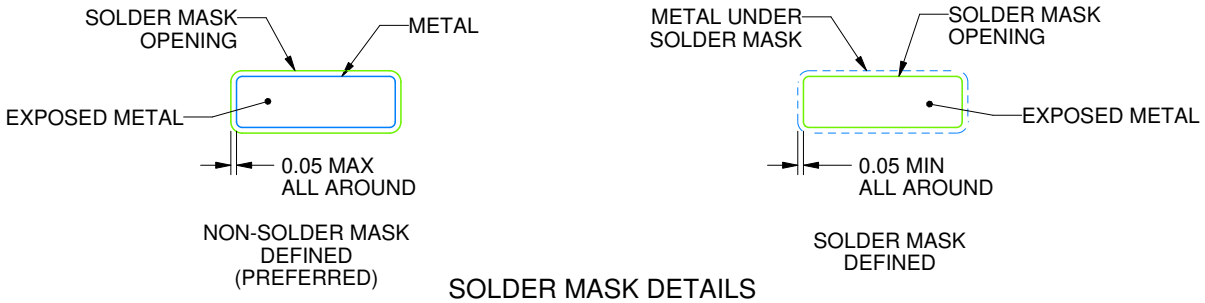
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

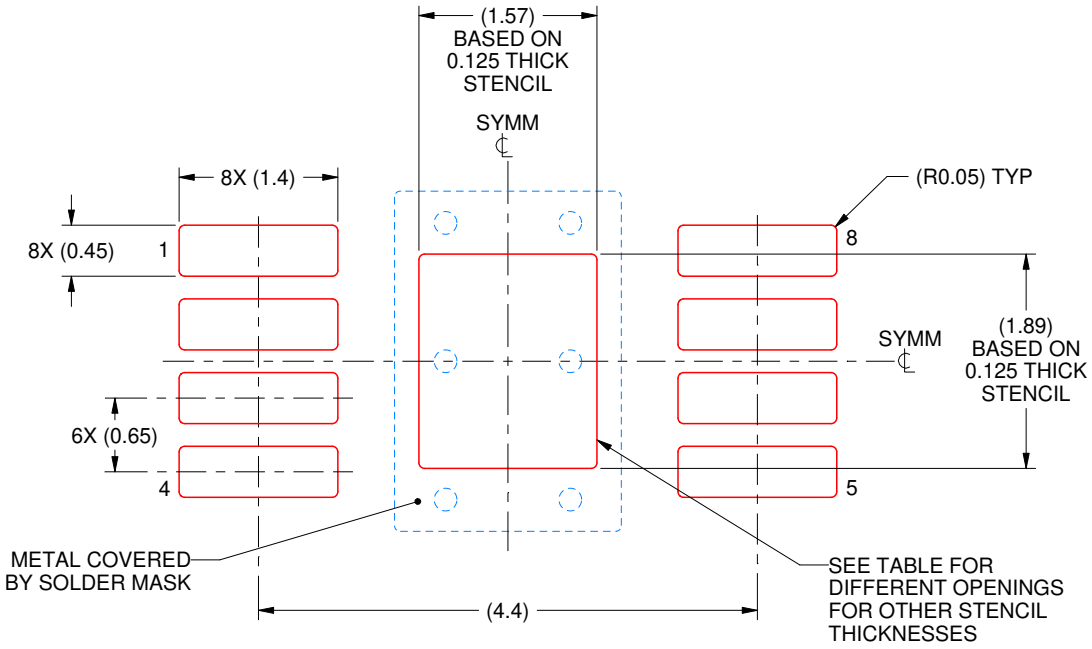


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

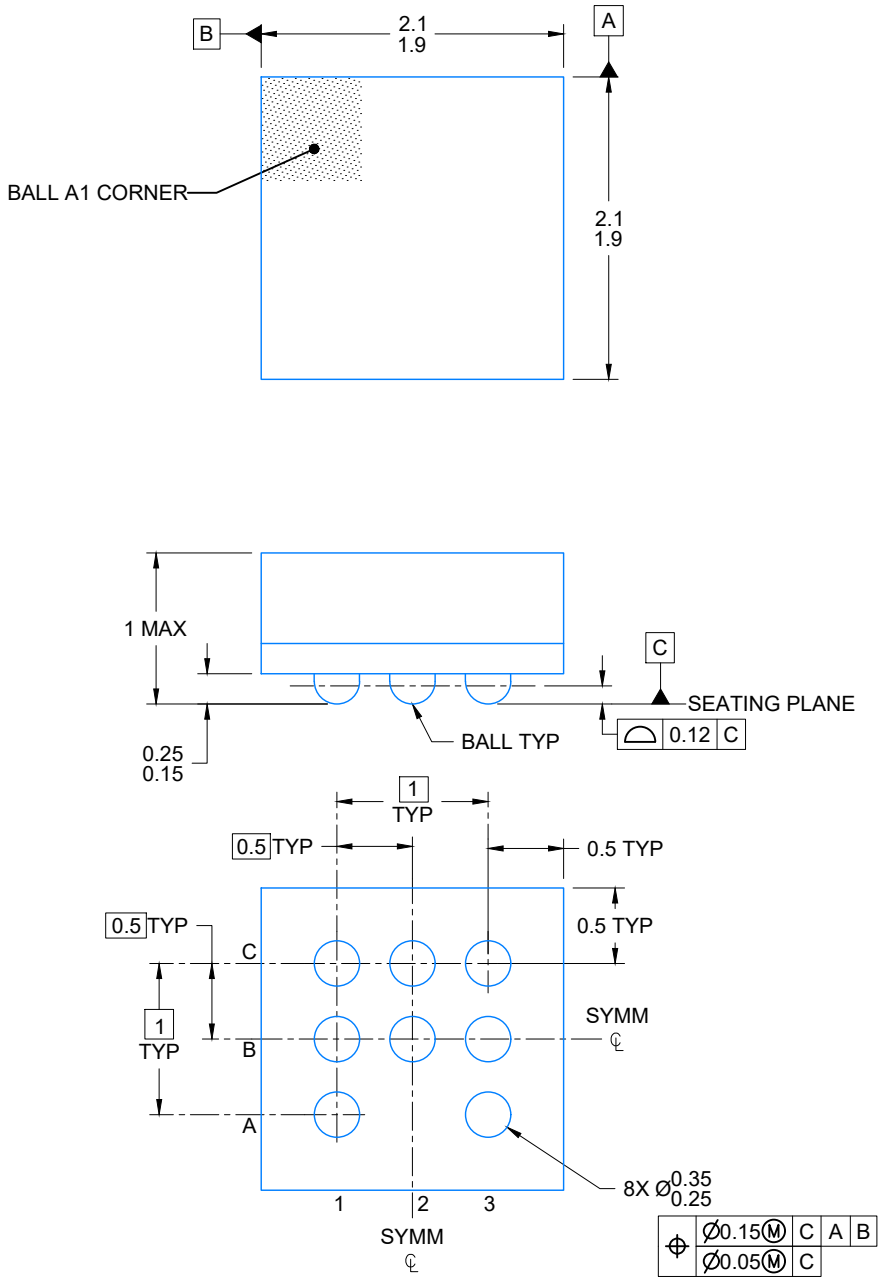
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

NMB0008A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY

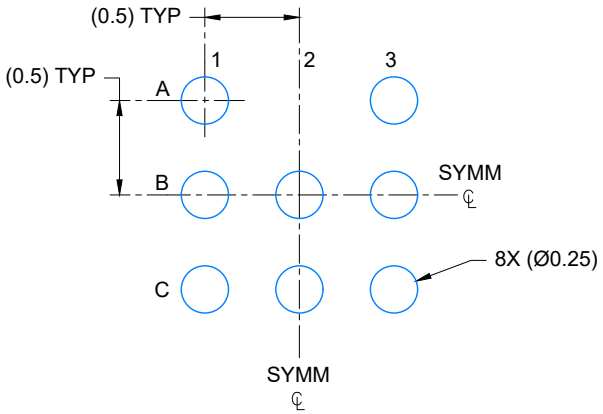


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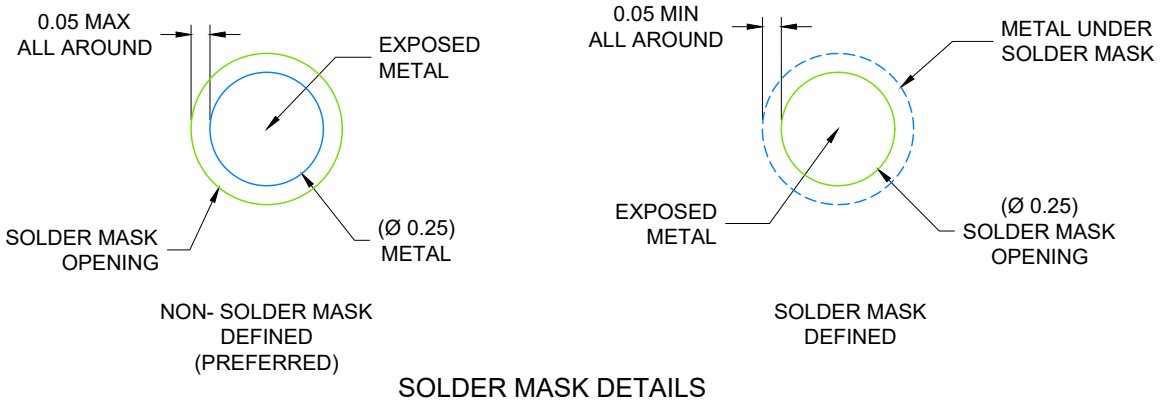
NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 25X

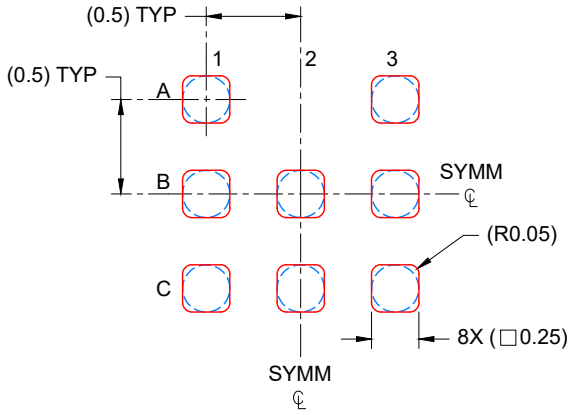


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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