TPD12S520 Single-Chip HDMI Receiver Port Protection and Interface Device

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±8-kV Contact Discharge on External Lines
- Single-Chip ESD Solution for HDMI Driver
- 12 Channel ESD Protection Diodes
- Supports All HDMI 1.3 and HDMI 1.4*b* Data Rates (–3 dB Frequency > 3 GHz)
- 0.8-pF Capacitance for the High Speed TMDS Lines
- 0.05-pF Matching Capacitance Between the Differential Signal Pair
- 38-Pin TSSOP Provides Seamless Layout Option with HDMI Connector
- 24-Pin WQFN Package for Space Constrained Applications
- Backdrive Protection
- Lead-Free Package

2 Applications

- Video Interface
- Consumer Electronics
- Displays and Digital Televisions
- Handheld Displays

3 Description

The TPD12S520 is a single-chip electro-static discharge (ESD) circuit protection device for the high-definition multimedia interface (HDMI) receiver port. While providing ESD protection with transient voltage suppression (TVS) diodes, the TVS protection adds little or no additional glitch in the high-speed differential signals. The high-speed transition minimized differential signaling (TMDS) ESD protection lines add only 0.8-pF capacitance.

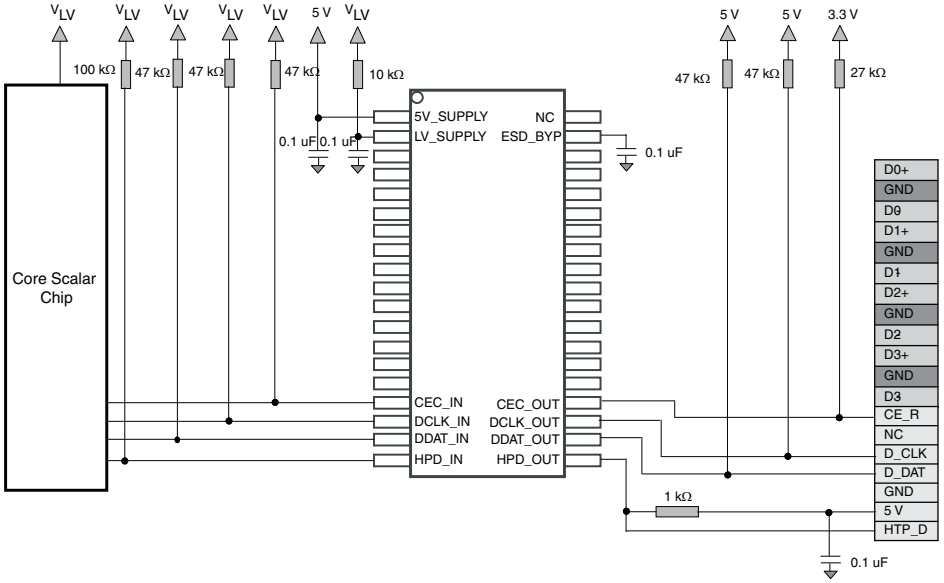
The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage level-shifter IC. The control line TVS diodes add 3.5-pF capacitance to the control lines. The 38-pin DBT package offers a seamless layout routing option to eliminate the routing glitch for the differential signal pairs. The DBT package pitch (0.5 mm) matches with the HDMI connector pitch. In addition, the pin mapping follows the same order as the HDMI connector pin mapping. This HDMI receiver port protection and interface device is designed specifically for HDMI receiver-interface protection. The 24-pin RMN package offers flow through routing using only two layers for highly integrated, space-efficient full HDMI protection.

Device Information[1]

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
TPD12S520	TSSOP (38)	6.40 mm × 9.70 mm
	WQFN (24)	4.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Circuit Protection Scheme



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision E (September 2014) to Revision F — **Page**

- Added clarification to HDMI data rates. ... 1
- Added clarification to HDMI data rates. ... 8

Changes from Revision D (December 2013) to Revision E — **Page**

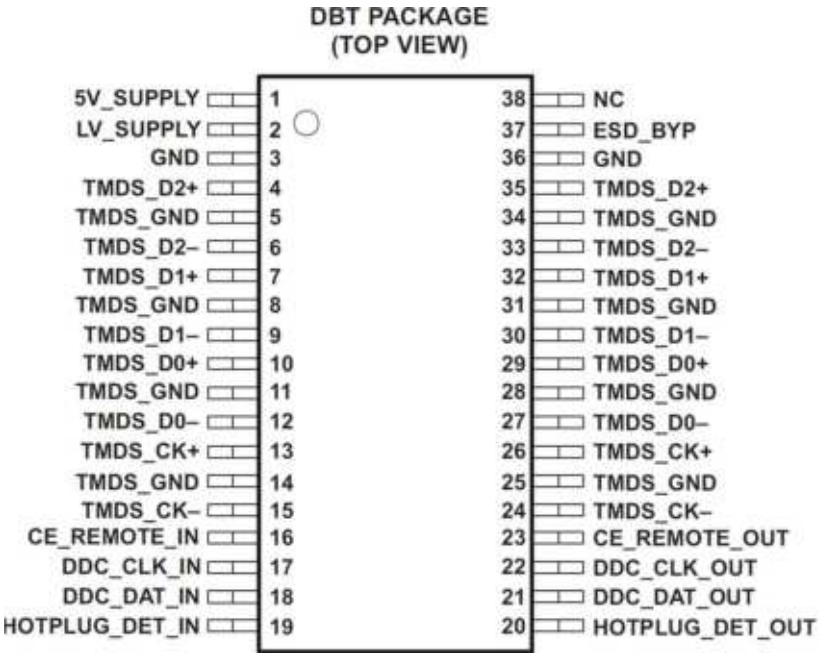
- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

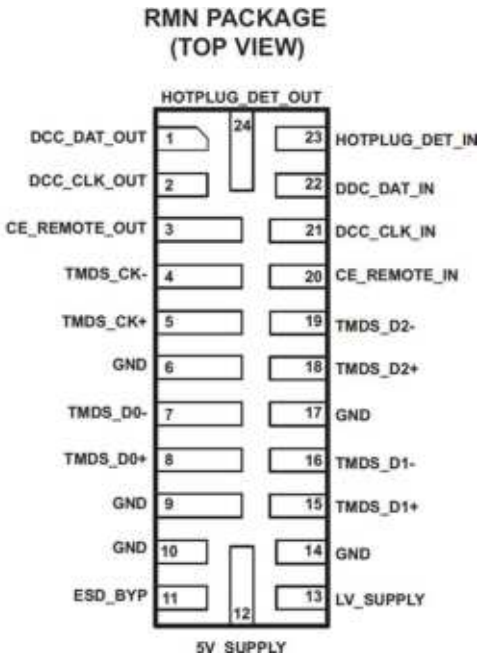
Changes from Revision C (April 2009) to Revision D — **Page**

- Added new application to Applications section. ... 1
- Added RMN Package to Datasheet. ... 1
- Updated RMN Package. ... 1
- Updated Pin Description Table. ... 4
- Added additonal graphs to Typical Performance section. ... 6

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5 Pin Configuration and Functions





Pin Functions

NAME	PIN NO.		TYPE	ESD LEVEL	DESCRIPTION
	DBT	RMN			
5V_SUPPLY	1	12	PWR	2 kV(1)	Bias for TMDS protection
LV_SUPPLY	2	13	PWR	2 kV(1)	Bias for CE/DDC/HOTPLUG level shifters
GND, TMDS_GND	3, 5, 8, 11,14, 25, 28, 31, 34, 36	6, 9, 10, 14, 17	GND	NA	TMDS ESD and parasitic GND return(2)
TMDS_D2+	4, 35	18	IO	8 kV (3)	TMDS 0.8-pF ESD protection(4)
TMDS_D2–	6, 33	19	IO	8 kV(3)	TMDS 0.8-pF ESD protection(4)
TMDS_D1+	7, 32	15	IO	8 kV(3)	TMDS 0.8-pF ESD protection(4)
TMDS_D1–	9, 30	16	IO	8 kV(3)	TMDS 0.8-pF ESD protection(4)
TMDS_D0+	10, 29	8	IO	8 kV(3)	TMDS 0.8-pF ESD protection(4)
TMDS_D0–	12, 27	7	IO	8 kV(3)	TMDS 0.8-pF ESD protection(4)
TMDS_CK+	13, 26	5	IO	8 kV(3)	TMDS 0.8-pF ESD protection(4)
TMDS_CK–	15, 24	4	IO	8 kV(3)	TMDS 0.8-pF ESD protection(4)
CE_REMOTE_IN	16	20	IO	2 kV(1)	LV_SUPPLY referenced logic level into ASIC
DDC_CLK_IN	17	21	IO	2 kV(1)	LV_SUPPLY referenced logic level into ASIC
DDC_DAT_IN	18	22	IO	2 kV(1)	LV_SUPPLY referenced logic level into ASIC
HOTPLUG_DET_IN	19	23	IO	2 kV(1)	LV_SUPPLY referenced logic level into ASIC
HOTPLUG_DET_OUT	20	24	IO	8 kV(3)	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD(5) to connector

(1) Human body model (HBM) per MIL-STD-883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-µF ceramic capacitor connected to GND.
(2) These pins should be routed directly to the associated GND pins on the HDMI connector, with single-point ground vias at the connector.
(3) Standard IEC 61000-4-2, $C_{DISCHARGE}$ = 150 pF, $R_{DISCHARGE}$ = 330 Ω, 5V_SUPPLY and LV_SUPPLY within recommended operating conditions, GND = 0 V, and ESD_BYP (pin 37) and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1-µF ceramic capacitor connected to GND.
(4) These two pins must be connected together inline on the PCB.
(5) This output can be connected to an external 0.1-µF ceramic capacitor, resulting in an increased ESD withstand voltage rating.

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Pin Functions (continued)

NAME	PIN NO.		TYPE	ESD LEVEL	DESCRIPTION
	DBT	RMN			
DDC_DAT_OUT	21	1	IO	8 kV(3)	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector
DDC_CLK_OUT	22	2	IO	8 kV(3)	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector
CE_REMOTE_OUT	23	3	IO	8 kV(3)	5 V_SUPPLY referenced logic level out, plus 3.5-pF ESD to connector
ESD_BYP	37	11	IO	2 kV(1)	ESD bypass. This pin must be connected to a 0.1-µF ceramic capacitor.
NC	38			NA	No connection

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{5V_SUPPLY} V_{LV_SUPPLY}	Supply voltage	–0.3	6	V
$V_{I/O}$	DC voltage at any channel input	–0.5	6	V
T_A	Operating Free Air Temperature	–40	85	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per MIL-STD-883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ(1)	See *Pin Configuration and Functions*	±2000	V
		IEC 61000-4-2 Contact Discharge(2)	See *Pin Configuration and Functions*	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
T_A	Operating free-air temperature	–40		85	°C
5V_SUPPLY	Operating supply voltage	GND	5	5.5	V
LV_SUPPLY	Bias supply voltage	1	3.3	5.5	V

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6.4 Thermal Information

THERMAL METRIC[1]		TPD12S520		UNIT
		DBT	RMN	
		38 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.6	80.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.8	36.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.7	27.1	
ψ_{JT}	Junction-to-top characterization parameter	2.9	1.4	
ψ_{JB}	Junction-to-board characterization parameter	44.1	27.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{5V}	Operating supply current	5V_SUPPLY = 5 V				1	5	µA
I_{LV}	Bias supply current	LV_SUPPLY = 3.3 V				1	2	mA
I_{OFF}	OFF-state leakage current, level-shifting NFET	LV_SUPPLY = 0 V				0.1	1	µA
$I_{BACK\ DRIVE}$	Current conducted from output pins to V_SUPPLY rails when powered down	5V_SUPPLY < V_{CH_OUT}	TMDS_D[2:0]+/–, TMDS_CK+/–, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT			0.1	5	µA
V_{ON}	Voltage drop across level-shifting NFET when ON	LV_SUPPLY = 2.5 V, V_S = GND, I_{DS} = 3 mA			75	95	140	mV
V_F	Diode forward voltage	I_F = 8 mA, T_A = 25°C[1]	Top diode			1		V
			Bottom diode			1		
V_{CL}	Channel clamp voltage at ±8 kV HBM ESD	TA = 25°C[1][2]	Positive transients			9		V
			Negative transients			-9		
R_{DYN}	Dynamic resistance	I = 1 A, T_A = 25°C[3]	Positive transients			0.6		Ω
			Negative transients			0.5		
I_{LEAK}	TMDS channel leakage current	T_A = 25°C[1]				0.01	1	µA
C_{IN}, TMDS	TMDS channel input capacitance	5V_SUPPLY= 5 V, Measured at 1 MHz, V_{BIAS} = 2.5 V[1]				0.8	1.0	pF
ΔC_{IN}, TMDS	TMDS channel input capacitance matching	5V_SUPPLY= 5 V, Measured at 1 MHz, V_{BIAS} = 2.5 V[1][4]				0.05		pF
C_{MUTUAL}	Mutual capacitance between signal pin and adjacent signal pin	5V_SUPPLY= 0 V, Measured at 1 MHz, V_{BIAS} = 2.5 V[1]				0.07		pF
C_{IN}	Level-shifting input capacitance, capacitance to GND	5V_SUPPLY= 0 V, Measured at 100 KHz, V_{BIAS} = 2.5 V[1]		DDC		3.5	4	pF
				CEC		3.5	4	
				HP		3.5	4	

(1) This parameter is specified by design and verified by device characterization
(2) Human-Body Model (HBM) per MIL-STD-883, Method 3015, $C_{DISCHARGE}$ = 100 pF, $R_{DISCHARGE}$ = 1.5 kΩ
(3) These measurements performed with no external capacitor on ESD_BYP.
(4) Intrapair matching, each TMDS pair (i.e., D+, D–)

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6.6 Typical Characteristics

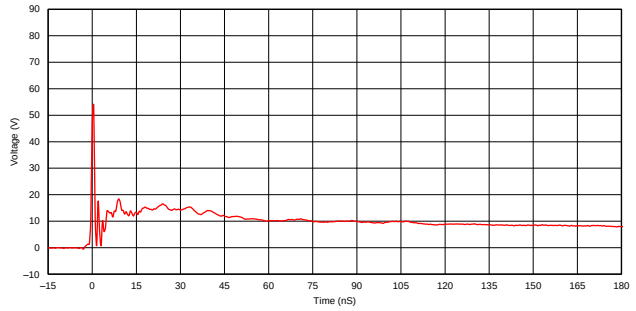


Figure 1. TPD12S520RMN IEC Clamping Waveforms +8kV Contact

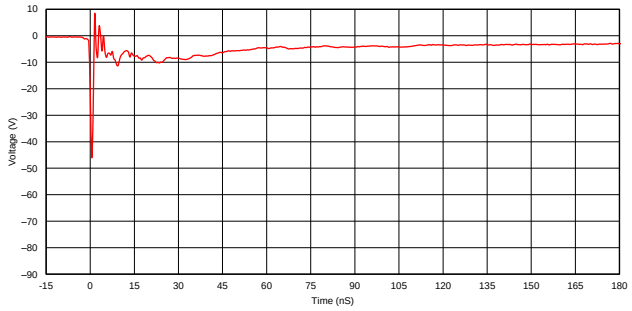


Figure 2. TPD12S520RMN IEC Clamping Waveforms -8kV Contact

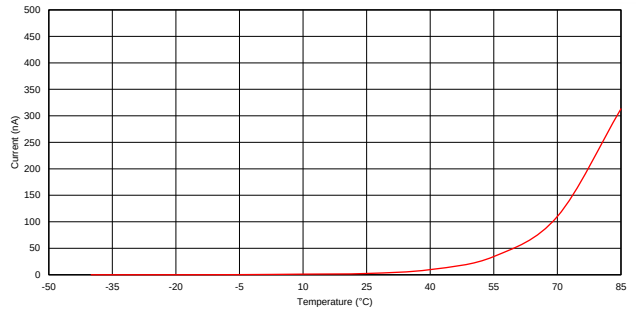


Figure 3. I_{LEAK} vs. Temperature VIN = 5.0V

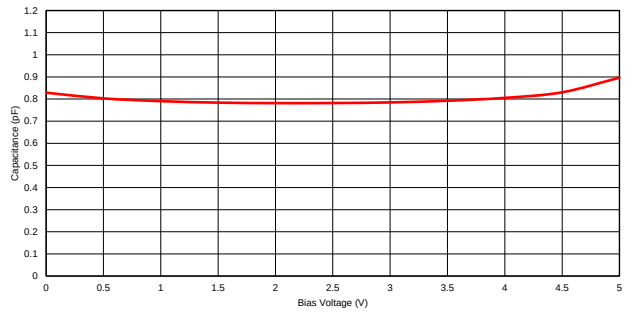


Figure 4. Capacitance vs. V_{BIAS}

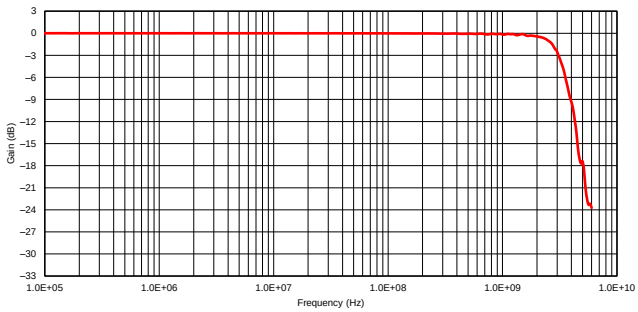


Figure 5. Insertion Loss Performance Across Frequency

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7 Detailed Description

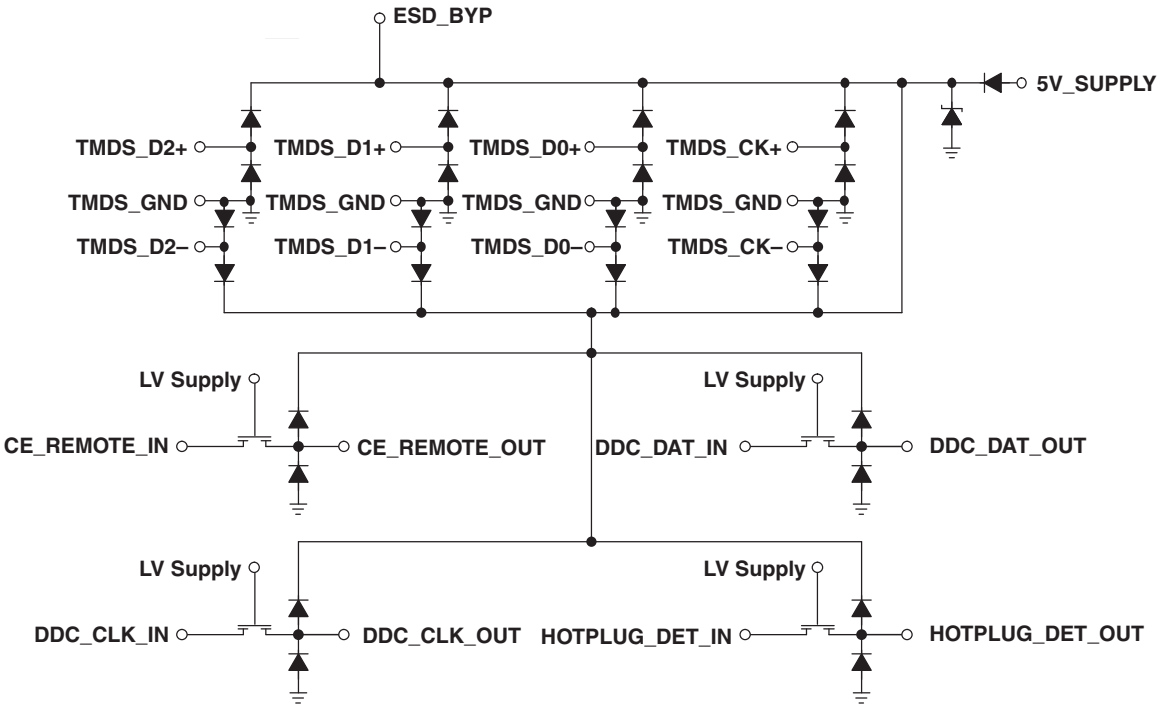
7.1 Overview

The TPD12S520 is a single-chip ESD solution for the HDMI receiver port. In many cases the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S520 provides the desired system-level ESD protection, such as the IEC61000-4-2 (Level 4) ESD, by absorbing the energy associated with the ESD strike.

While providing the ESD protection, the TPD12S520 adds little or no additional glitch in the high-speed differential signals (see Figure 7 and Figure 8). The high-speed TMDS lines add only 0.8-pF capacitance to the lines. In addition, the monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line. This is a direct advantage over discrete ESD clamp solutions where variations between two different ESD clamps may significantly degrade the differential signal quality.

The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage level-shifter IC. The control line ESD clamps add 3.5-pF capacitance to the control lines. The 38-pin DBT package offers a seamless layout routing option to eliminate the routing glitch for the differential signal pairs. DBT package pitch (0.5 mm) matches with HDMI connector pitch. In addition, pin mapping follows the same order as the HDMI connector pin mapping. The 24-pin RMN package offers flow through routing using only two layers for highly integrated, space-efficient full HDMI protection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ±8-kV Contact ESD Protection on External Lines

In many cases, the core ICs, such as the scalar chipset, may not have robust ESD cells to sustain system-level ESD strikes. In these cases, the TPD12S520 provides the desired system-level ESD protection, such as the IEC61000-4-2 (Level 4) ESD, by absorbing the energy associated with the ESD strike.

7.3.2 Single-Chip ESD Solution for HDMI Driver

TPD12S520 provides a complete ESD protection scheme for an HDMI 1.4 compliant port. The monolithic integrated circuit technology ensures that there is excellent matching between the two-signal pair of the differential line. This is a direct advantage over discrete ESD clamp solutions where variations between two different ESD clamps may significantly degrade the differential signal quality. The 38-pin DBT package offers a seamless layout routing option to eliminate the routing glitch for the differential signal pair.

7.3.3 Supports All HDMI 1.3 and HDMI 1.4*b* Data Rates

The high-speed TMDS pins of the TPD12S520 add only 0.8 pF of capacitance to the TMDS lines. Excellent intra-pair capacitance matching of 0.05 pF provides ultra low intra-pair skew. Insertion loss -3 dB point > 3 GHz provides enough bandwidth to pass all HDMI 1.4*b* TMDS data rates.

7.3.4 38-Pin TSSOP Provides Seamless Layout Option With HDMI Connector

The 38-pin DBT package offers seamless layout routing option to eliminate the routing glitch for the differential signal pair. DBT package pitch (0.5 mm) matches with HDMI connector pitch. In addition, pin mapping follows the same order as the HDMI connector pin mapping. This HDMI receiver port protection and interface device is specifically designed for next-generation HDMI receiver protection.

7.3.5 24-Pin WQFNPackage for Space Constrained Applications

The 24-pin RMN package offers flow through routing using only two layers for highly integrated, space-efficient full HDMI protection.

7.3.6 Integrated Level Shifting for the Control Lines

The low-speed control lines offer voltage-level shifting to eliminate the need for an external voltage level-shifter IC. The control line ESD clamps add 3.5-pF capacitance to the control lines.

7.3.7 Backdrive Protection

Backdrive protection is offered on the connector side pins.

7.3.8 Lead-Free Package

Lead-Free Package for RoHS Compliance.

7.4 Device Functional Modes

TPD12S520 is active with the conditions in the *Recommended Operating Conditions* met. The bi-directional voltage-level translators provide non-inverting level shifting from either 5V (for SDA , SCL, HPD), or 3.3 V (for CEC) on the connector side to V_{LV} on the system side. Each connector side pin has an ESD clamp that triggers when voltages are above V_{BR} or below the lower diode's V_f. During ESD events, voltages as high as ±8-kV (contact ESD) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below these trigger levels (usually within 10's of nano-seconds), these pins revert to a non-conductive state.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD12S520 provides IEC61000-4-2 Level 4 Contact ESD rating to the HDMI 1.4 receiver port. Integrated voltage-level shifting reduces the board space needed to implement the control lines.

8.2 Typical Application

TPD12S520 is designed to protect a typical HDMI 1.4 receiver port. Refer to Figure 6 for a typical schematic. The eight TMDS data lines (D2+/-, D1+/-, D0+/-, CLK+/-) each have two pins on TPD12S520 to connect to. The TMDS data lines flow through their respective pin pairs, attaching to the passive ESD protection circuitry.

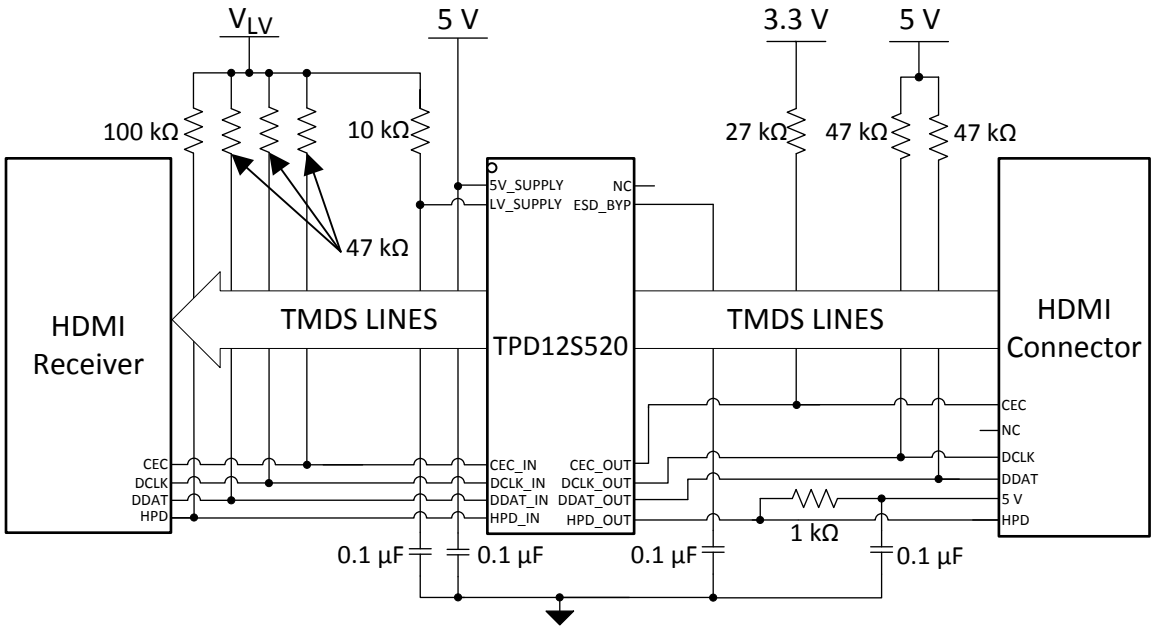


Figure 6. TPD12S520 Configured with an HDMI 1.4 Receiver Port

8.2.1 Design Requirements

For this example, use the following table as input parameters:

DESIGN PARAMETERS	EXAMPLE VALUE
Voltage on 5V_SUPPLY	4.5 V - 5.5 V
Voltage on LV_SUPPLY	1.7 V - 1.9 V

8.2.2 Detailed Design Procedure

To begin the design process the designer needs to know the 5V_SUPPLY voltage range and the logic level, LV_SUPPLY, voltage range.

8.2.3 Application Curves

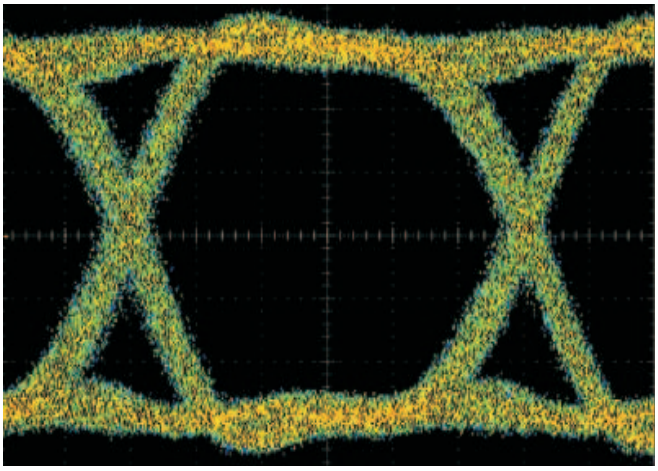


Figure 7. HDMI 1.65Gbps Eye Diagram With TPD12S520 on a Test Board

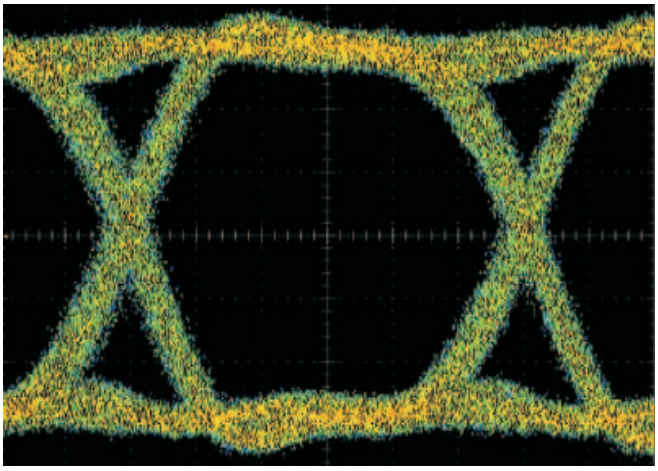


Figure 8. HDMI 1.65Gbps Eye Diagram Without TPD12S520 on a Test Board

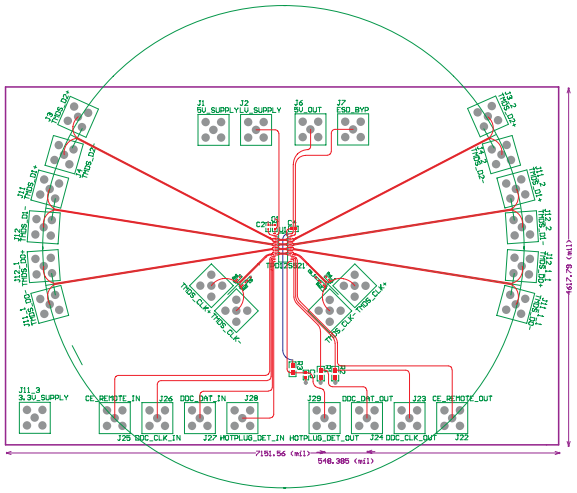


Figure 9. Test Board to Measure Eye Diagram for the TPD12S520 (Refer to Eye Diagram Plot)

9 Power Supply Recommendations

This device is designed to operate from an input voltage range of between 1.0 V and 5.5 V. This input supply should be well regulated. If the input supply is more than a few inches from TPD12S520 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. Otherwise, the device is a passive ESD protection device and there is no need to power it. Care should be taken to not violate the maximum voltage specifications to ensure that the device functions properly. The 5V_SUPPLY TVS diode can tolerate up to 6 V.

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10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

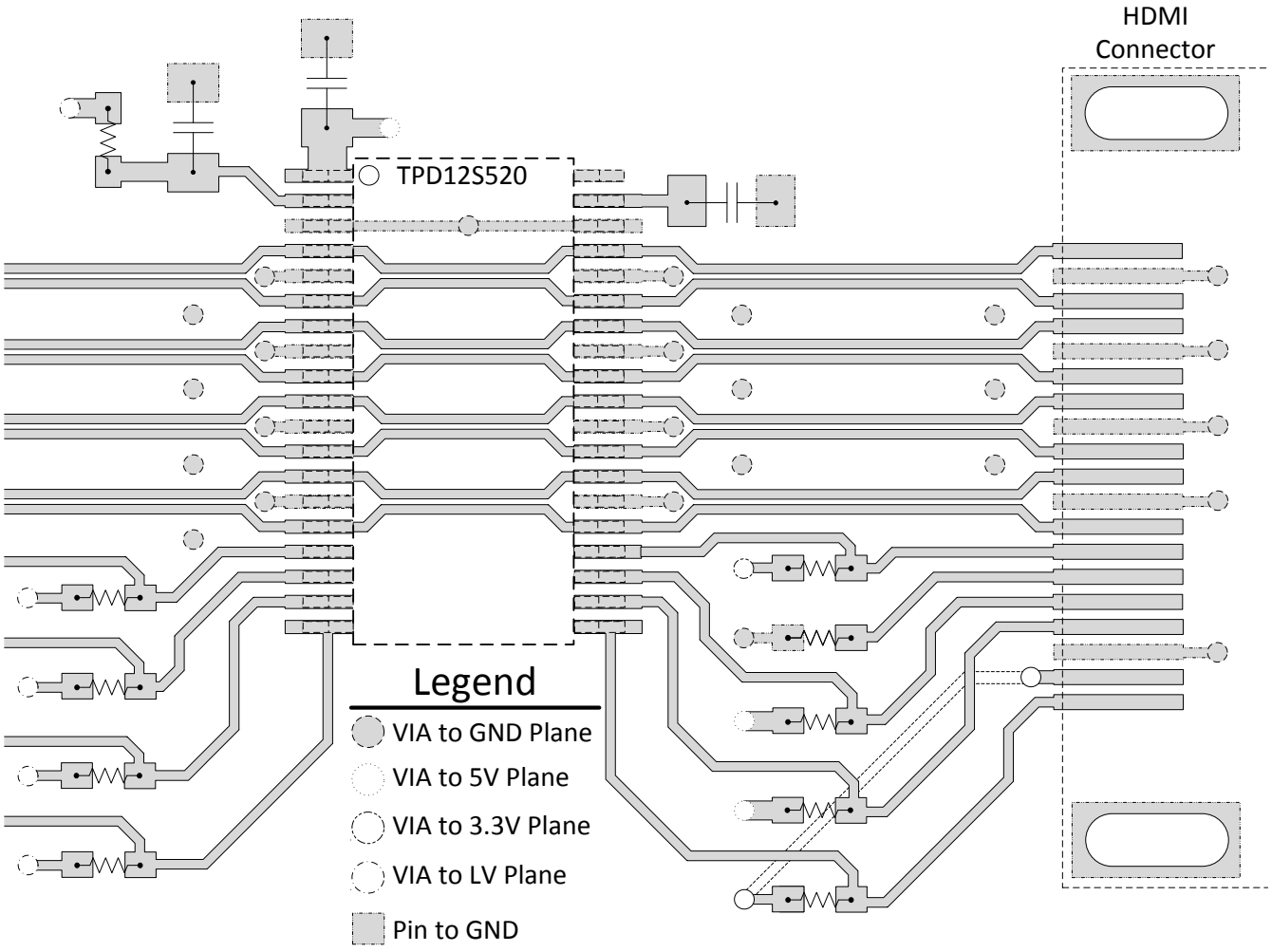


Figure 10. TPD12S520DBT Layout Example

Use external and internal ground planes and stitch them together with VIAs as close to the GND pins of TPD12S520 as possible. This allows for a low impedance path to ground so that the device can properly dissipate an ESD event.

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11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD12S520DBTR	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PN520
TPD12S520DBTR.B	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PN520
TPD12S520DBTRG4	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PN520
TPD12S520DBTRG4.B	Active	Production	TSSOP (DBT) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PN520
TPD12S520RMNR	Active	Production	WQFN (RMN) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	P520S
TPD12S520RMNR.B	Active	Production	WQFN (RMN) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	P520S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

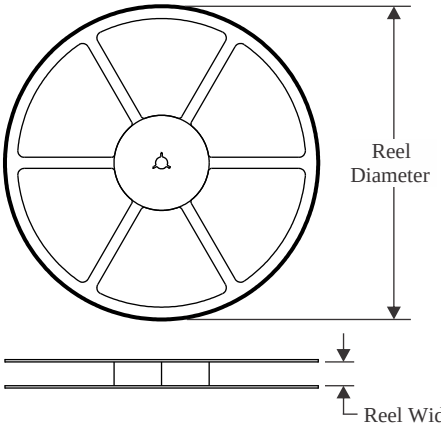
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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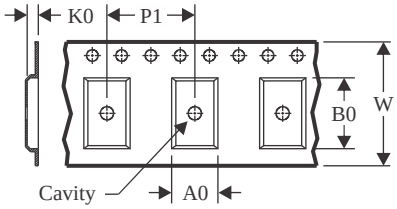
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

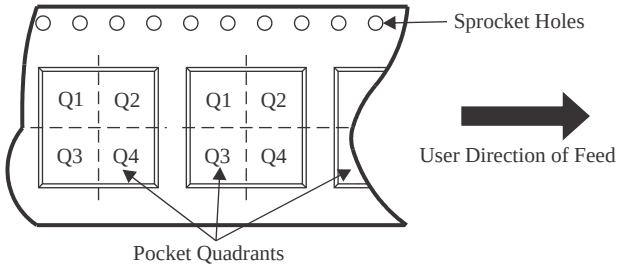


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

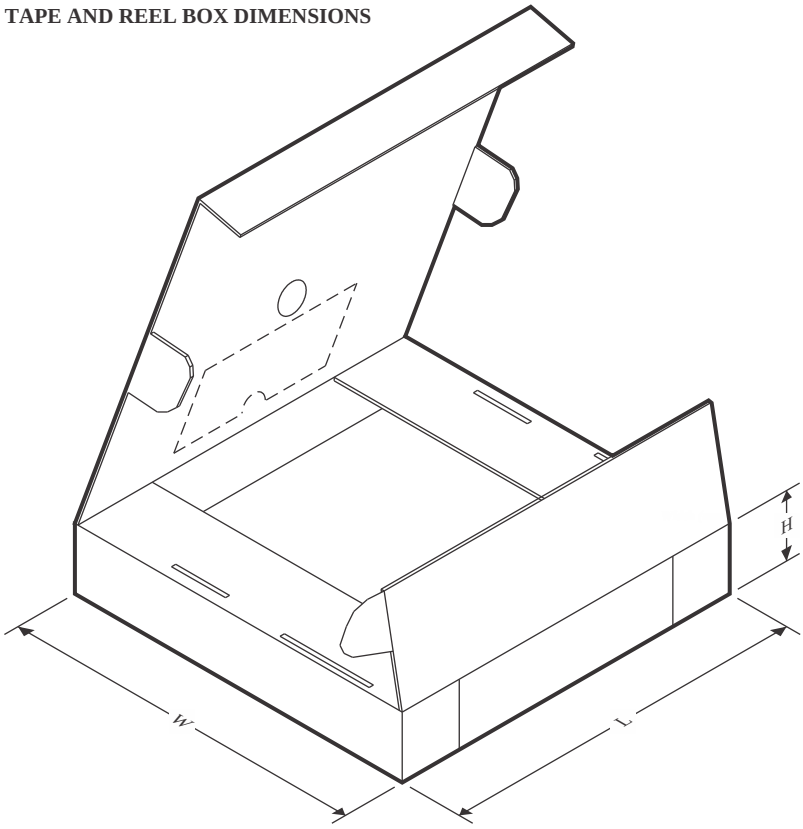
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD12S520DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TPD12S520DBTRG4	TSSOP	DBT	38	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TPD12S520RMNR	WQFN	RMN	24	3000	330.0	12.4	1.8	4.8	0.95	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

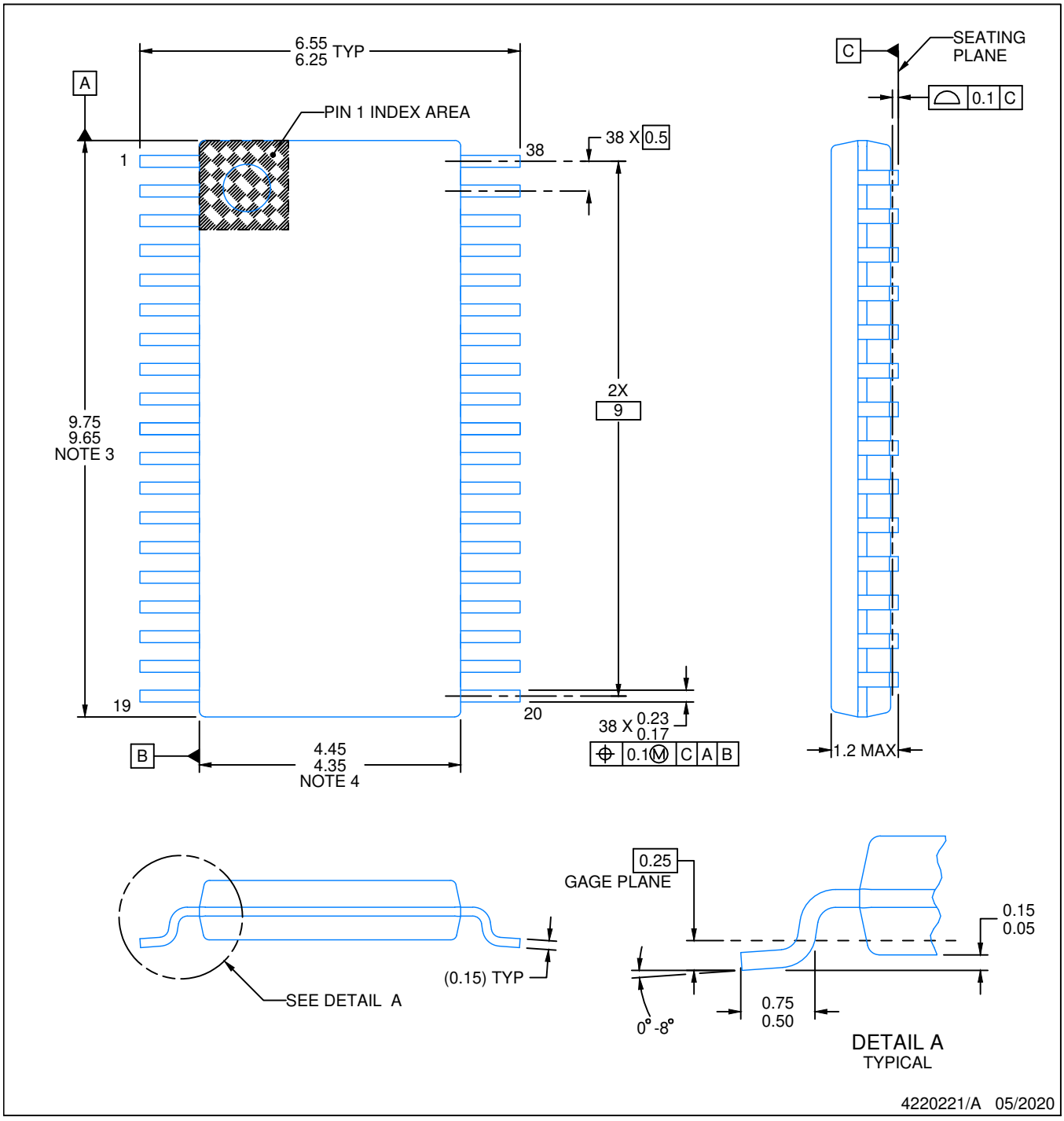
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD12S520DBTR	TSSOP	DBT	38	2000	353.0	353.0	32.0
TPD12S520DBTRG4	TSSOP	DBT	38	2000	353.0	353.0	32.0
TPD12S520RMNR	WQFN	RMN	24	3000	338.0	355.0	35.0

PACKAGE OUTLINE

DBT0038A

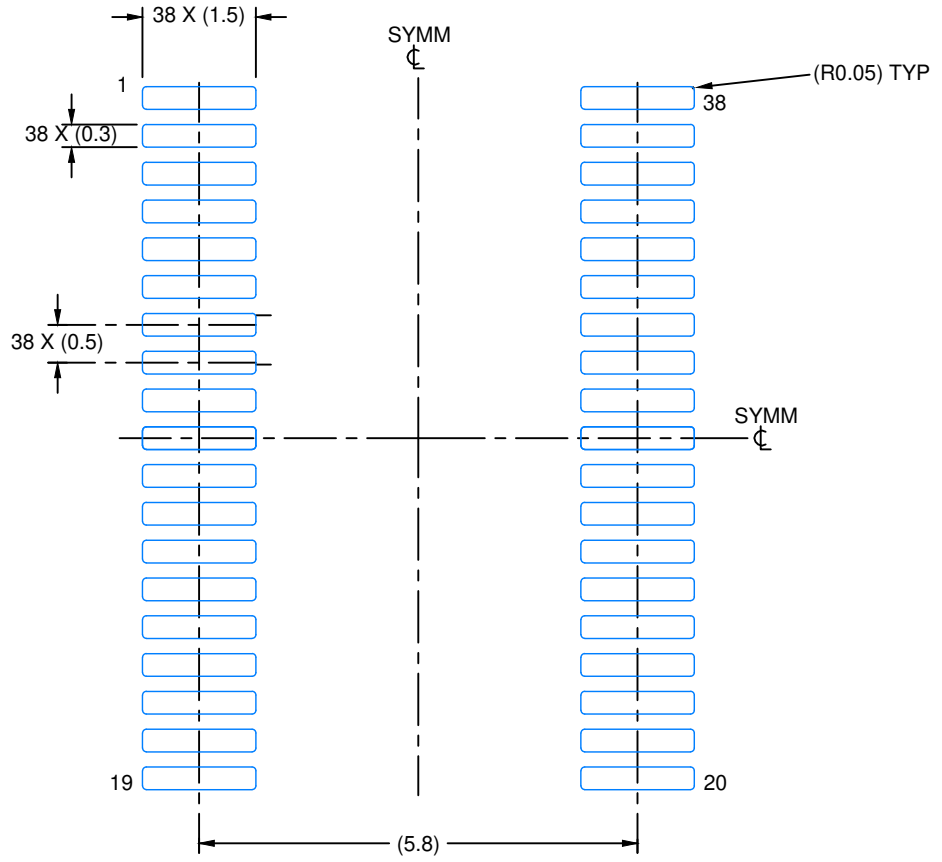
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

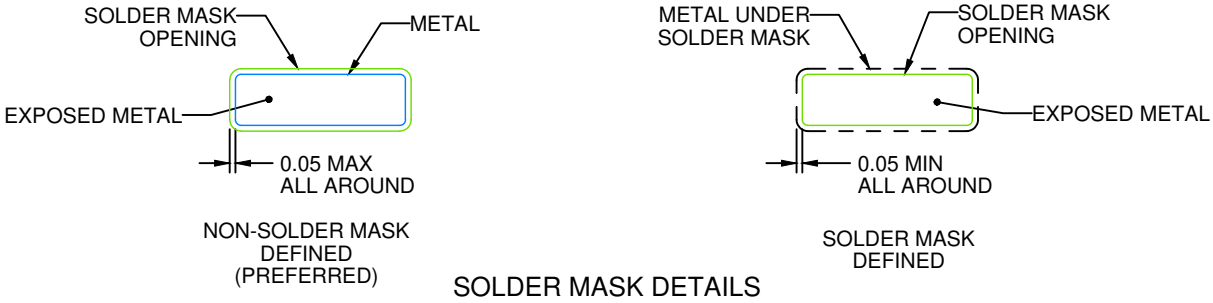


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

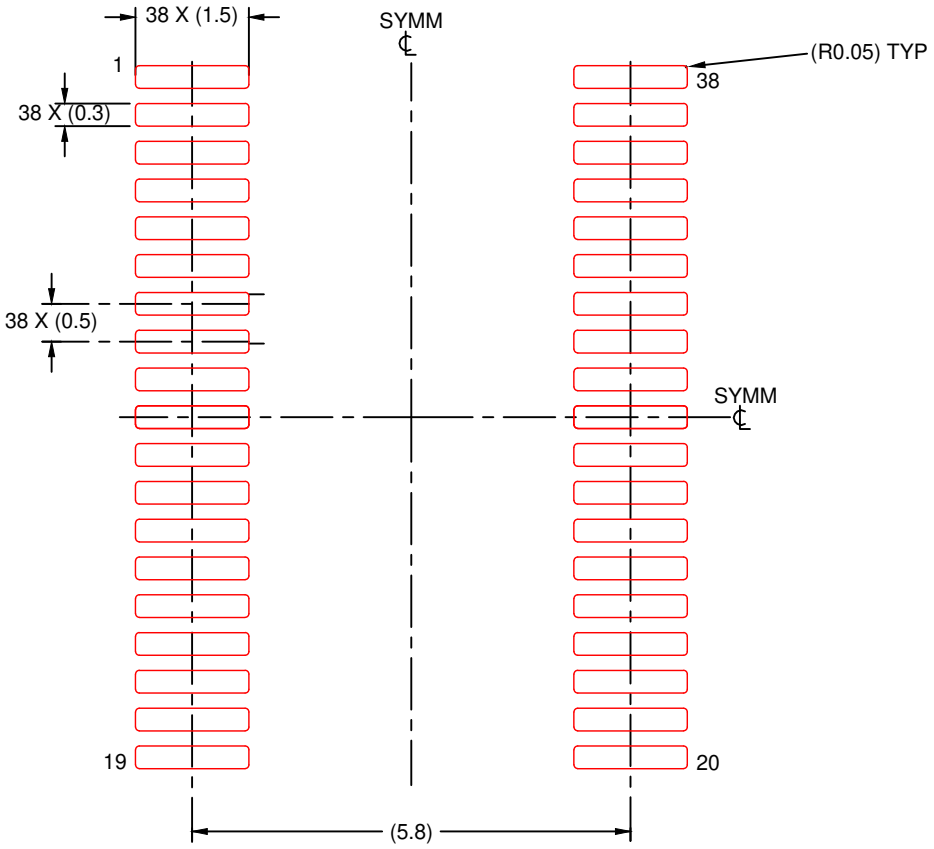


SOLDER MASK DETAILS

4220221/A 05/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220221/A 05/2020

NOTES: (continued)

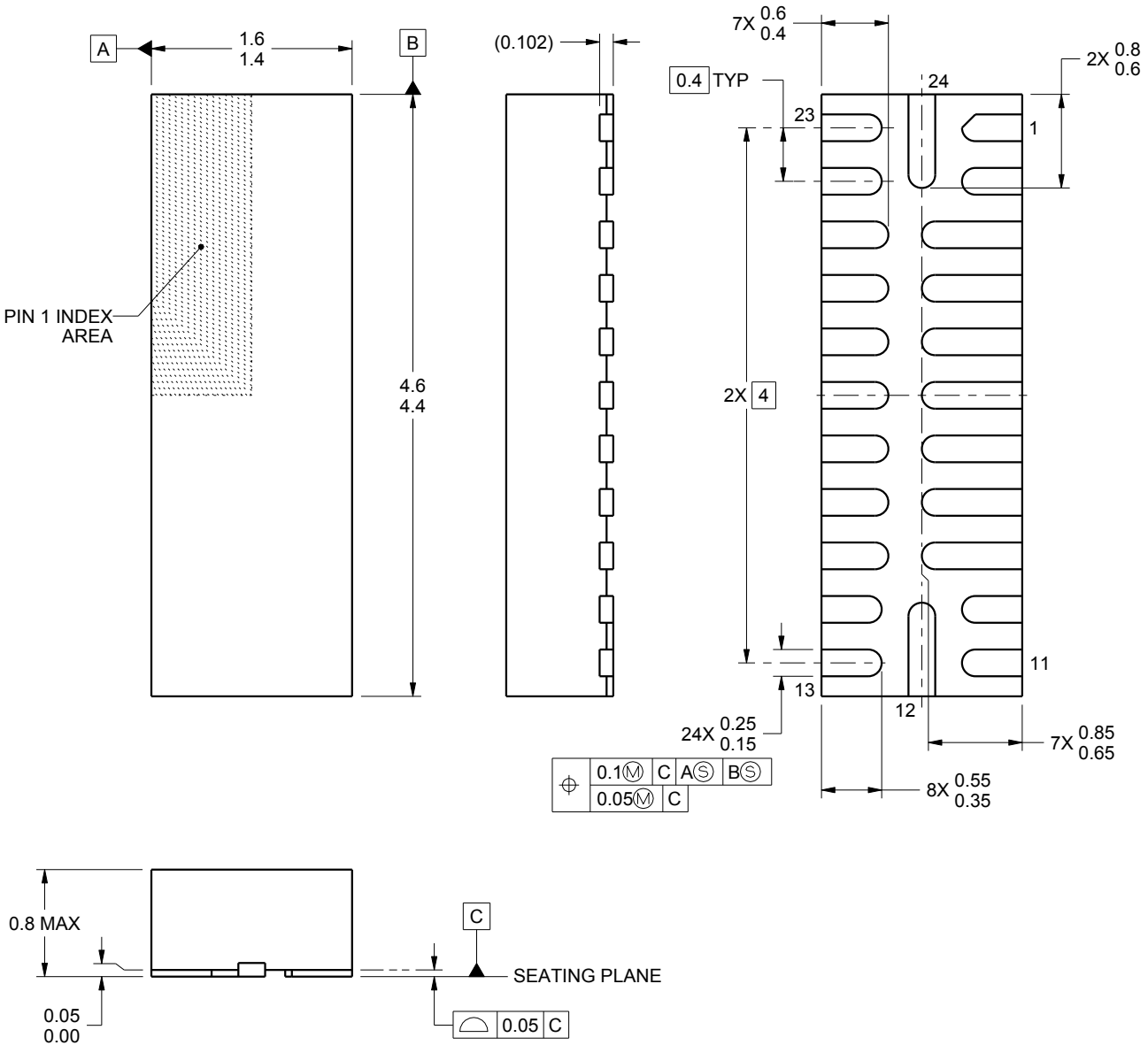
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RMN0024A

WQFN - 0.8 mm max height

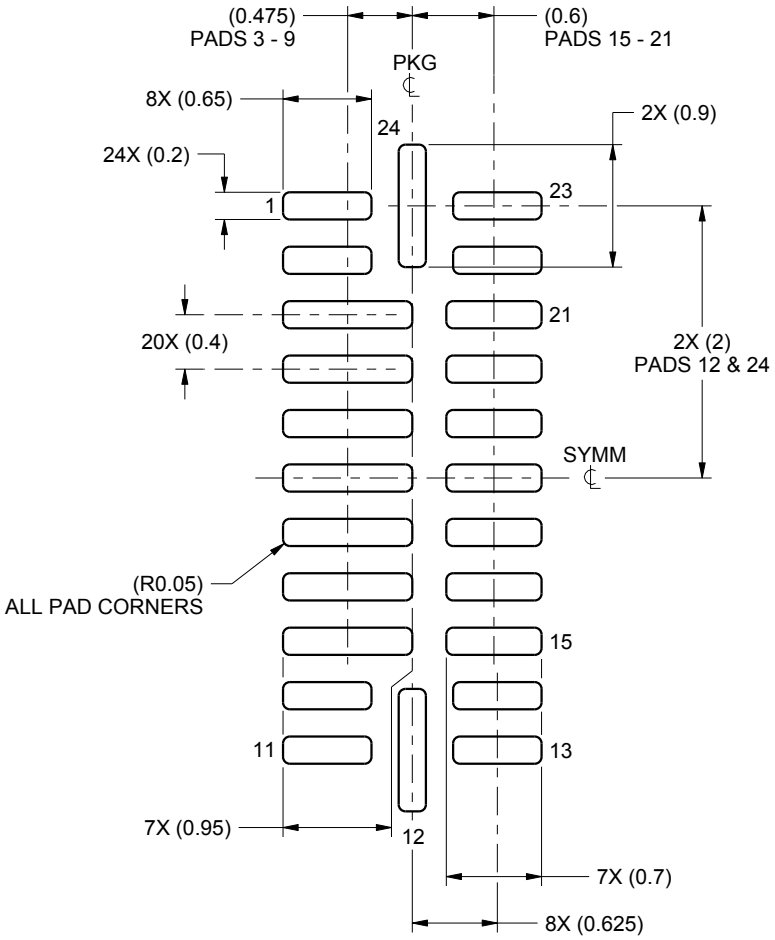
PLASTIC QUAD FLATPACK - NO LEAD



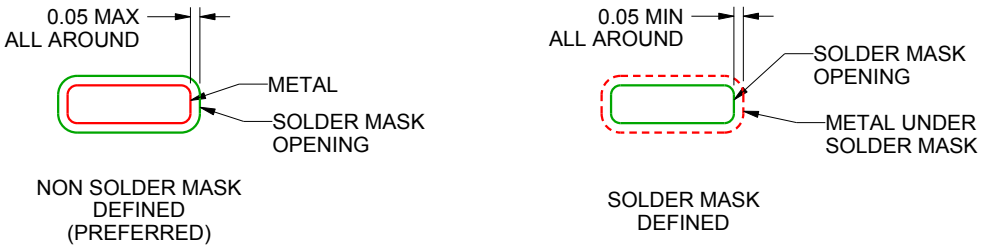
4221011/C 12/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:18X

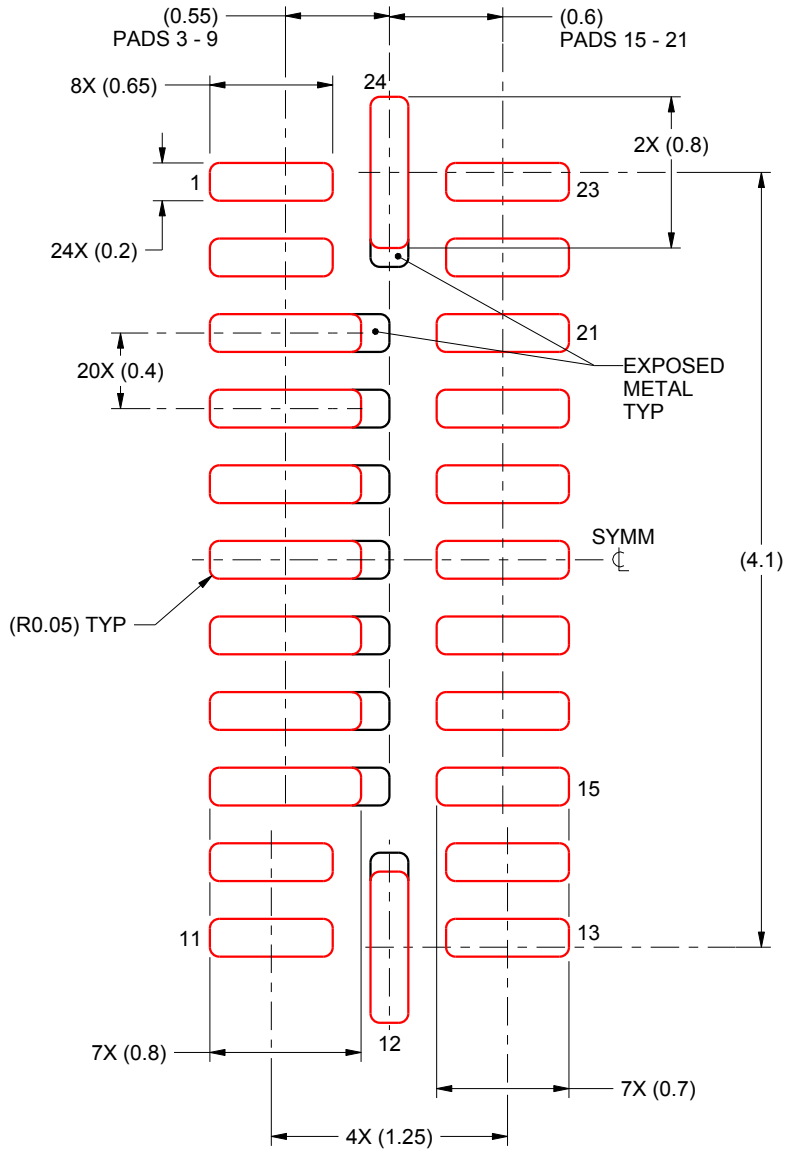


SOLDER MASK DETAILS

4221011/C 12/2015

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4221011/C 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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