TPS53311 3-A Step-Down Regulator With Integrated Switcher

1 Features

- 95.5% Maximum Efficiency
- Continuous 3-A Output Current
- Supports All MLCC Output Capacitor
- SmoothPWM™ Auto-Skip Eco-mode™ for Light-Load Efficiency
- Voltage Mode Control
- Supports Master-Slave Interleaved Operation
- Synchronization up to ±20% of Nominal Frequency
- Conversion Voltage Range From 2.9 V to 6 V
- Soft-Stop Output Discharge During Disable
- Adjustable Output Voltage Ranging From 0.6 V to 0.84 V × V_{IN}
- Overcurrent, Overvoltage, and Overtemperature Protection
- Small, 3 mm × 3 mm, 16-Pin VQFN Package
- Open-Drain Power Good Indication
- Internal Boot Strap Switch
- Low $R_{DS(on)}$, 24 mΩ With 3.3-V Input and 19-mΩ With 5-V Input
- Supports Prebias Start-Up Functionality

2 Applications

- 5-V Step-Down Rail
- 3.3-V Step-Down Rail

3 Description

The TPS53311 provides a fully integrated 3-V to 5-V V_{IN} integrated synchronous FET converter solution with 16 total components, in 200 mm^2 of PCB area. Due to the low $R_{DS(on)}$ and TI Proprietary SmoothPWM™ skip mode of operation, it enables 95.5% peak efficiency, and over 90% efficiency at loads as light as 100 mA. It requires only two 22-µF ceramic output capacitors for a power-dense, 3-A solution.

The TPS53311 features a 1.1-MHz switching frequency, SKIP mode operation support, prebias start-up, internal soft start, output soft discharge, internal VBST switch, power good, EN/input UVLO, overcurrent, overvoltage, undervoltage, and overtemperature protections and all ceramic output capacitor support. It supports supply voltage from 2.9 V to 3.5 V and conversion voltage from 2.9 V to 6 V, and output voltage is adjustable from 0.6 V to 0.84 V × V_{IN}.

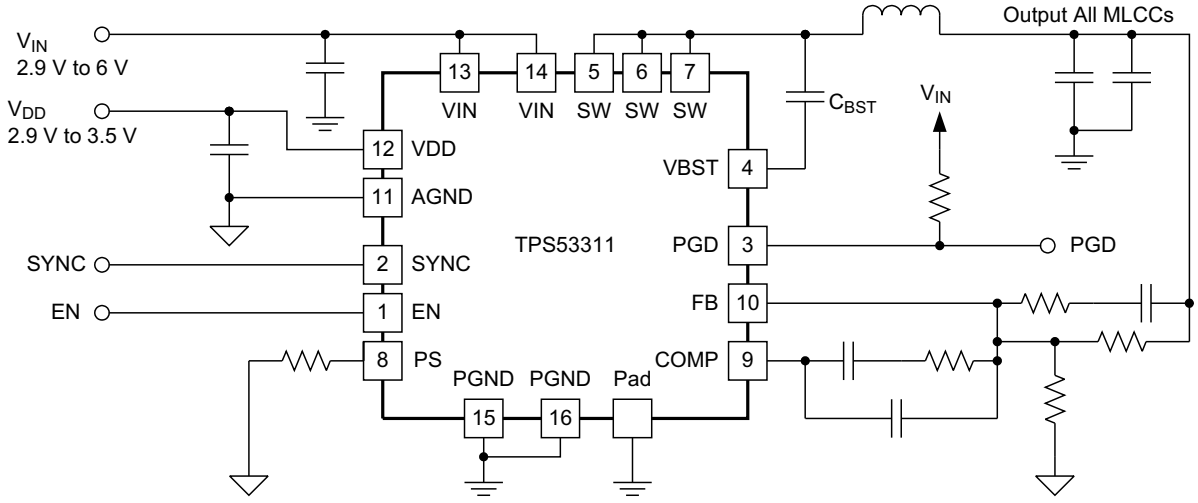
The TPS53311 is available in the 3 mm × 3 mm 16-pin VQFN package (Green RoHs compliant and Pb free) and operates between –40°C and 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53311	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2011) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see POA at the end of the data sheet ... 1
- Added *Thermal Information* table ... 5
- Deleted *Package Dissipation Ratings* table ... 5
- Changed value of component R2 in *Typical Application Circuit Diagram* From: 4.02 kΩ To: 2.67 kΩ ... 13
- Changed value of component V_{OUT} on TPS53311 Master in *Master and Slave Configuration Schematic* From: 1.2 V To: 1.5 V ... 17
- Changed value of component R2 on TPS53311 Master in *Master and Slave Configuration Schematic* From: 4.02 kΩ To: 2.67 kΩ ... 17
- Changed value of component V_{OUT} on TPS53311 Slave in *Master and Slave Configuration Schematic* From: 1.5 V To: 1.2 V ... 17
- Changed value of component R12 on TPS53311 Slave in *Master and Slave Configuration Schematic* From: 2.67 kΩ To: 4.02 kΩ ... 17

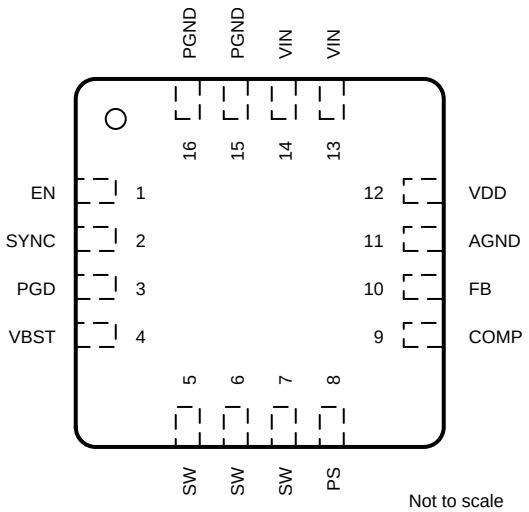
Changes from Original (June 2010) to Revision A **Page**

- Added bullets to *Features* ... 1
- Changed *Description* for clarity ... 1
- Changed *Absolute Maximum Ratings* output voltage (SW pin DC) minimum from 0.3 V to –1 V (typographical error) ... 4
- Added information regarding DE mode in *Master/Slave Operation and Synchronization* section ... 11
- Changed value of component C2 in *Typical Application Circuit Diagram* to 2.2 nF (typographical error) ... 13
- Changed component labels and values in Master/Slave Configuration Schematic (typographical error) ... 17

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5 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Not to scale

Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	EN	I	Enable. Internally pulled up to VDD with a 1.35-MΩ resistor.
2	SYNC	B	Synchronization signal for input interleaving. Master SYNC pin sends out 180° out-of-phase signal to slave SYNC. SYNC frequency must be within ±20% of slave nominal frequency.
3	PGD	O	Power good output flag. Open drain output. Pull up to an external rail through a resistor.
4	VBST	P	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
5	SW	B	Output inductor connection to integrated power devices.
6	SW	B	Output inductor connection to integrated power devices.
7	SW	B	Output inductor connection to integrated power devices.
8	PS	I	Mode configuration pin (with 10 µA current): Connecting to ground: Forced CCM slave. Pulled high or floating (internal pulled high): Forced CCM master. Connect with 24.3 kΩ to GND: DE slave. Connect with 57.6 kΩ to GND: HEF mode. Connect with 105 kΩ to GND: reserved mode. Connect with 174 kΩ to GND: DE master.
9	COMP	O	Error amplifier compensation terminal. Type III compensation method is recommended for stability.
10	FB	I	Voltage feedback. Also used for OVP, UVP, and PGD determination.
11	AGND	G	Device analog ground terminal.
12	VDD	P	Input bias supply for analog functions.
13	VIN	P	Gate driver supply and power conversion voltage.
14	VIN	P	Gate driver supply and power conversion voltage.
15	PGND	P	IC power GND terminal.
16	PGND	P	IC power GND terminal.

(1) B = Bidirectional, G = Ground, I = Input, O = Output, P = Supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage	VIN, EN		–0.3	7	V
	VBST		–0.3	17	
	VBST(with respect to SW)		–0.3	7	
	FB, PS, VDD		–0.3	3.7	
Output voltage	SW	DC	–1	7	V
		Pulse < 20 ns, E = 5 µJ	–3	10	
	PGD		–0.3	7	
	COMP, SYNC		–0.3	3.7	
	PGND		–0.3	0.3	
Operating temperature, T_A			–40	85	°C
Junction temperature, T_J			–40	150	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN	2.9		6	V
	VDD	2.9	3.3	3.5	
	VBST	–0.1		13.5	
	VBST(with respect to SW)	–0.1		6	
	EN	–0.1		6	
	FB, PS	–0.1		3.5	
Output voltage	SW	–1		6.5	V
	PGD	–0.1		6	
	COMP, SYNC	–0.1		3.5	
	PGND	–0.1		0.1	
Junction temperature, T_J		–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		TPS53311 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended free-air temperature range, V_{IN} = 3.3 V, V_{VDD} = 3.3 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: VOLTAGE, CURRENTS, AND UVLO						
V_{IN}	VIN supply voltage	Nominal input voltage	2.9		6	V
I_{VINSDN}	VIN shutdown current	EN = LO			3	µA
V_{UVLO}	VIN UVLO threshold	Ramp up, EN = HI		2.8		V
$V_{UVLOHYS}$	VIN UVLO hysteresis	VIN UVLO Hysteresis		130		mV
V_{DD}	Internal circuitry supply voltage	Nominal 3.3-V input voltage	2.9	3.3	3.5	V
I_{DDSDN}	VDD shut down current	EN = LO			5	µA
I_{DD}	Standby current	EN = HI, no switching		2.2	3.5	mA
V_{DDUVLO}	3.3-V UVLO threshold	Ramp up, EN = HI		2.8		V
$V_{DDUVLOHYS}$	3.3-V UVLO hysteresis			75		mV
VOLTAGE FEEDBACK LOOP: VREF AND ERROR AMPLIFIER						
V_{VREF}	VREF	Internal precision reference voltage		0.6		V
$TOLV_{REF}$	VREF Tolerance	0°C ≤ T_A ≤ 85°C	–1%		1%	
		–40°C ≤ T_A ≤ 85°C	–1.25%		1.25%	
UGBW[1]	Unity gain bandwidth		14			MHz
A_{OL}[1]	Open loop gain		80			dB
I_{FBINT}	FB input leakage current	Sourced from FB pin			30	nA
I_{EAMAX}[1]	Output sinking and sourcing current	C_{COMP} = 20 pF		5		mA
SR[1]	Slew rate			5		V/µs
OCP: OVER CURRENT AND ZERO CROSSING						
I_{OCPL}	Overcurrent limit on upper FET	When I_{OUT} exceeds this threshold for 4 consecutive cycles. V_{IN} = 3.3 V, V_{OUT} = 1.5 V with 1-µH inductor, T_A = 25°C	4.2	4.5	4.8	A
I_{OCPH}	One time overcurrent latch off on the lower FET	Immediately shut down when sensed current reach this value. V_{IN} = 3.3 V, V_{OUT} = 1.5 V with 1-µH inductor, T_A = 25°C	4.8	5.1	5.5	A
V_{ZXOFF}[1]	Zero crossing comparator internal offset	PGND – SW, SKIP mode	–4.5	–3	–1.5	mV
PROTECTION: OVP, UVP, PGD, AND INTERNAL THERMAL SHUTDOWN						
V_{OVP}	Overvoltage protection threshold voltage	Measured at FB wrt. VREF	114%	117%	120%	
V_{UVP}	Undervoltage protection threshold voltage	Measured at FB wrt. VREF	80%	83%	86%	
V_{PGDL}	PGD low threshold	Measured at FB wrt. VREF	80%	83%	86%	

(1) Ensured by design. Not production tested.

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Electrical Characteristics (continued)

over recommended free-air temperature range, V_{IN} = 3.3 V, V_{VDD} = 3.3 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PGDU}	PGD upper threshold	Measured at FB wrt. VREF	114%	117%	120%	
$V_{INMINPG}$	Minimum V_{IN} voltage for valid PGD at start up.	Measured at V_{IN} with 1-mA (or 2-mA) sink current on PGD pin at start up		1		V
THSD(1)	Thermal shutdown	Latch off controller, attempt soft-stop	130	140	150	°C
$THSD_{HYS}$(1)	Thermal Shutdown hysteresis	Controller restarts after temperature has dropped		40		°C
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{PGPD}	PGD pulldown voltage	Pulldown voltage with 4-mA sink current		0.2	0.4	V
I_{PGLK}	PGD leakage current	Hi-Z leakage current, apply 3.3-V in off state	–2	0	2	µA
R_{ENPU}	Enable pullup resistor			1.35		MΩ
V_{ENH}	EN logic high threshold		1.1	1.18	1.3	V
V_{ENHYS}	EN hysteresis			0.18	0.24	V
PS_{THS}	PS mode threshold voltage	Level 1 to level 2(2)		0.12		V
		Level 2 to level 3		0.4		
		Level 3 to level 4		0.8		
		Level 4 to level 5		1.4		
		Level 5 to level 6		2.2		
I_{PS}	PS source	10-µA pullup current when enabled	8	10	12	µA
f_{SYNCSL}	Slave SYNC frequency range	Versus nominal switching frequency	–20%		20%	
PW_{SYNC}	SYNC low pulse width			110		ns
I_{SYNC}	SYNC pin sink current			10		µA
$V_{SYNCTHS}$(1)	SYNC threshold	Falling edge		1		V
$V_{SYNCHYS}$(1)	SYNC hysteresis			0.5		V
BOOT STRAP: VOLTAGE AND LEAKAGE CURRENT						
I_{VBSTLK}	VBST leakage current	V_{IN} = 3.3 V, V_{VBST} = 6.6 V, T_A = 25°C			1	µA
TIMERS: SS, FREQUENCY, RAMP, ON TIME AND I/O TIMING						
t_{SS_1}	Delay after EN asserting	EN = HI, master or HEF mode		0.2		ms
t_{SS_2}	Delay after EN asserting	EN = HI, slave waiting time		0.5		ms
t_{SS_3}	Soft-start ramp-up time	Rising from V_{SS} = 0 V to V_{SS} = 0.6 V		0.4		ms
$t_{PGDENDLY}$	PGD startup delay time	Rising from V_{SS} = 0 V to V_{SS} = 0.6 V, from V_{SS} reaching 0.6 V to V_{PGD} going high		0.4		ms
t_{OVPDLY}	Overvoltage protection delay time	Time from FB out of 20% of VREF to OVP fault	1.0	1.7	2.5	µs
t_{UVPDLY}	Undervoltage protection delay time	Time from FB out of –20% of VREF to UVP fault		11		µs
f_{SW}	Switching frequency control	Forced CCM mode	0.99	1.1	1.21	MHz
	Ramp amplitude(1)	2.9 V < V_{IN} < 6 V		V_{IN}/4		V
$t_{MIN(off)}$	Minimum OFF time	FCCM mode or DE mode		100	140	ns
		HEF mode		175	250	
D_{MAX}	Maximum duty cycle	FCCM mode and DE mode, f_{SW} = 1.1 MHz, 0°C ≤ T_A ≤ 85°C	84%	89%		
		HEF mode, f_{SW} = 1.1 MHz, 0°C ≤ T_A ≤ 85°C	75%	81%		
R_{SFTSTP}	Soft-discharge transistor resistance	V_{EN} = Low, V_{IN} = 3.3 V, V_{OUT} = 0.5 V		60		Ω

(2) See PS pin description for levels.

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6.6 Typical Characteristics

Inductor IN06142 (1 µH, 5.4 mΩ) is used.

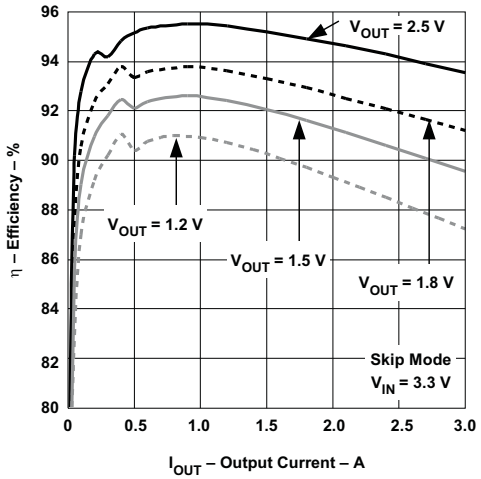


Figure 1. Efficiency vs Output Current, Skip Mode, V_{IN} = 3.3 V

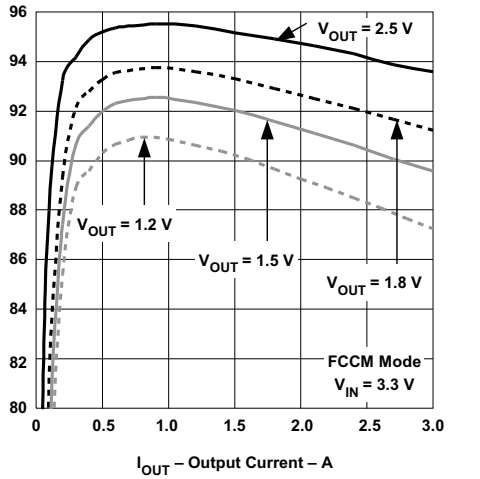


Figure 2. Efficiency vs Output Current, FCCM, V_{IN} = 3.3 V

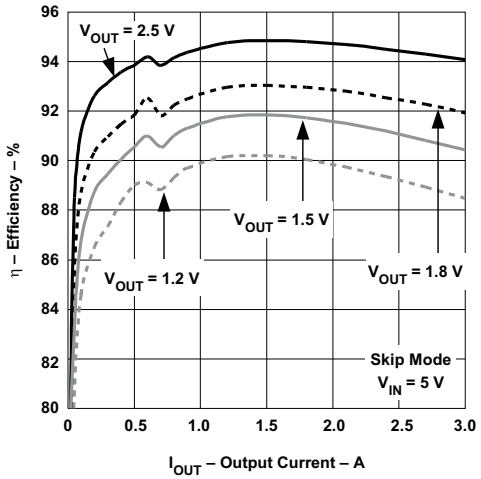


Figure 3. Efficiency vs Output Current, Skip Mode, V_{IN} = 5 V

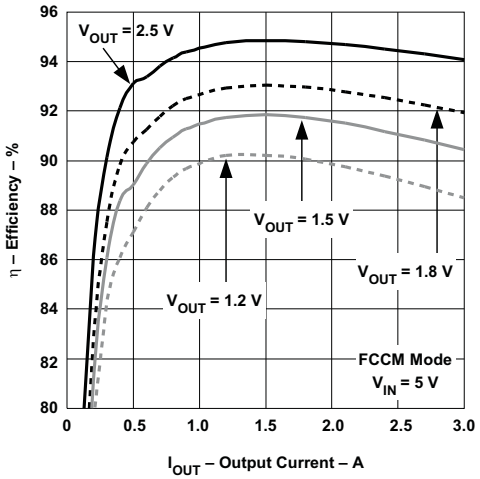


Figure 4. Efficiency vs Output Current, FCCM, V_{IN} = 5 V

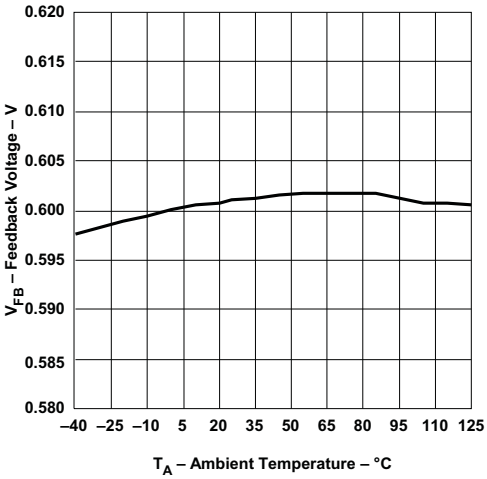


Figure 5. Feedback Voltage vs Ambient Temperature

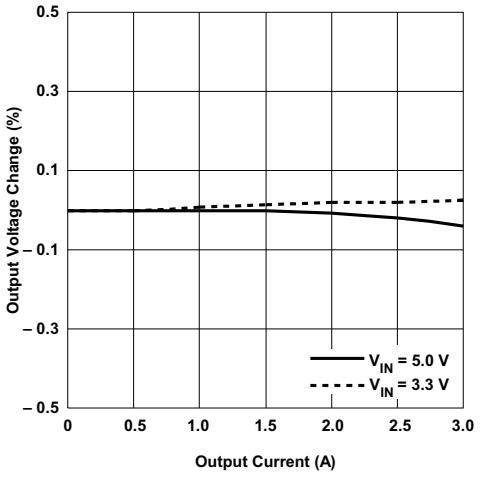


Figure 6. Output Voltage Change vs Output Current

Typical Characteristics (continued)

Inductor IN06142 (1 µH, 5.4 mΩ) is used.

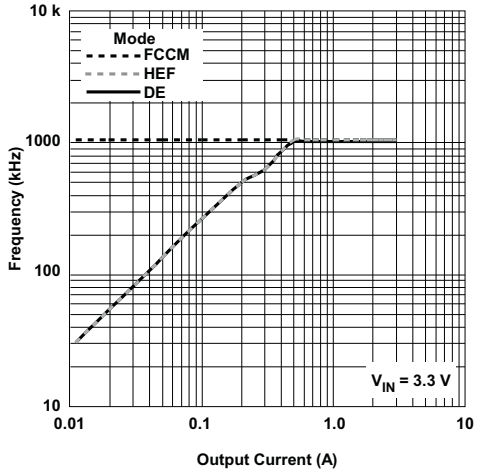


Figure 7. Frequency vs Output Current at V_{IN} = 3.3 V

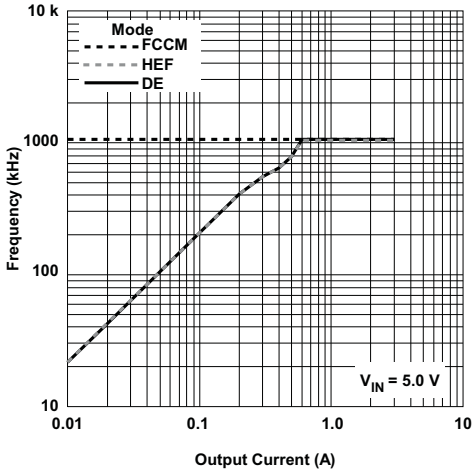


Figure 8. Frequency vs Output Current at V_{IN} = 5 V

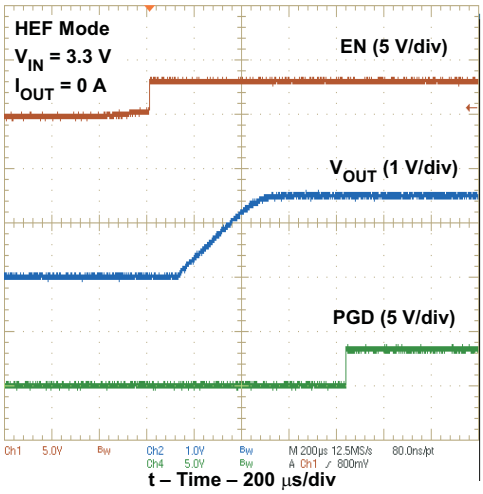


Figure 9. Normal Start-Up Waveform

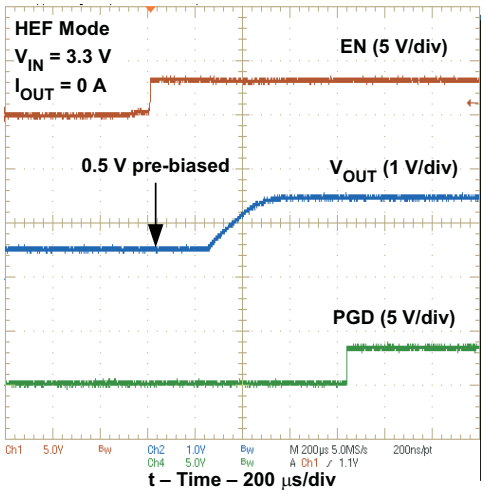


Figure 10. Prebias Start-Up Waveform

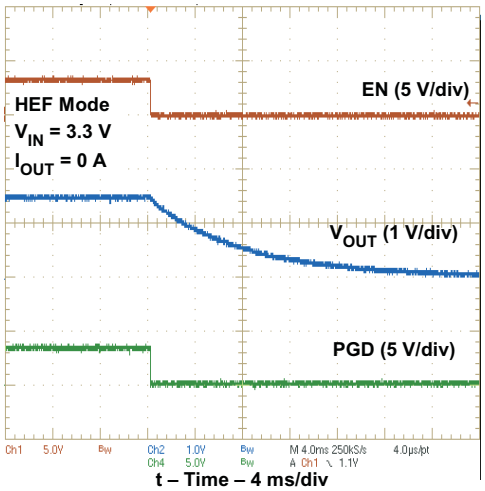


Figure 11. Soft-Stop Waveform

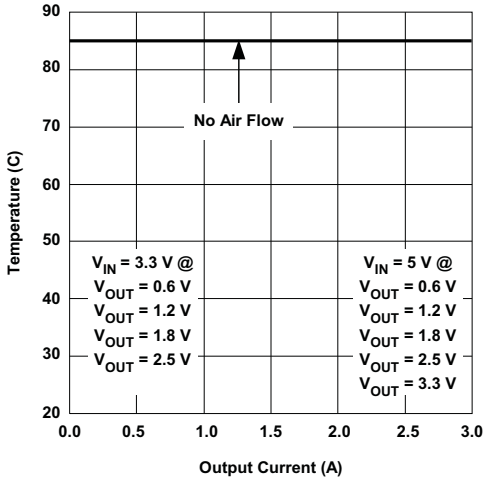


Figure 12. Safe Operating Area

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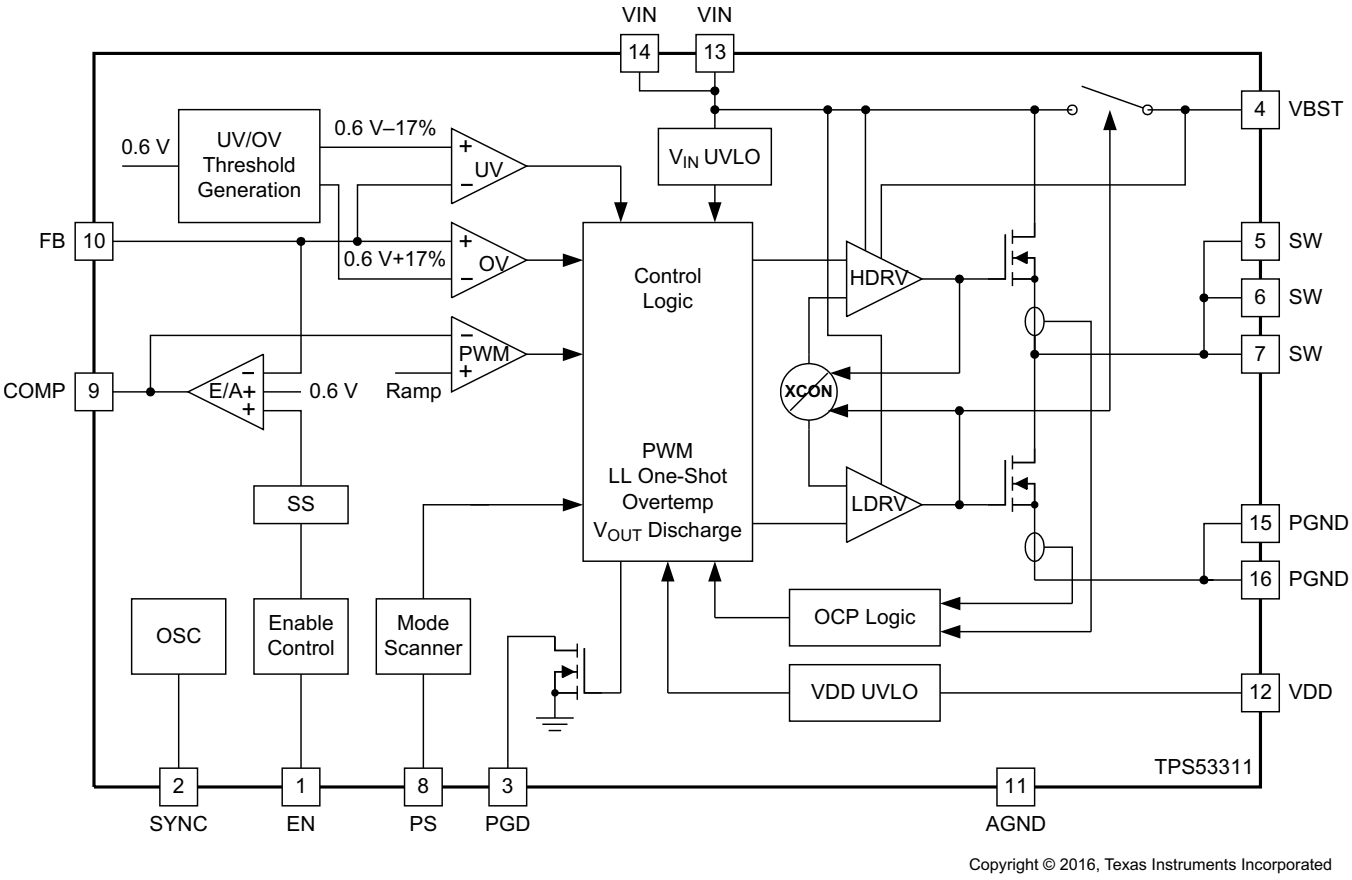
7 Detailed Description

7.1 Overview

The TPS53311 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 3 A of load current. The TPS53311 provides output voltage between 0.6 V and 0.84 × V_{IN} from 2.9-V to 6-V wide input voltage range.

This device employs five operation modes to fit various application requirements. The *master and slave* mode enables a two-phase interleaved operation to reduce input ripple. The *skip* mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Soft Start

The soft-start function reduces the inrush current during the start-up sequence. A slow-rising reference voltage is generated by the soft-start circuitry and sent to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, the error amplifier switches to a fixed 600-mV reference. The typical soft-start time is 400 µs.

Feature Description (continued)

7.3.2 Power Good

The TPS53311 monitors the voltage on the FB pin. If the FB voltage is between 83% and 117% of the reference voltage, the power good signal remains high. If the FB voltage falls outside of these limits, the internal open-drain output pulls the power good pin (PGD) low.

During start-up, the input voltage must be higher than 1 V to have valid power good logic, and the power good signal is delayed for 400 µs after the FB voltage falls to within the power good limits. There is also 10-µs delay during the shutdown sequence.

7.3.3 Undervoltage Lockout (UVLO) Function

The TPS53311 provides undervoltage lockout (UVLO) protection for both power input (V_{IN}) and bias input (VDD) voltage. If either of them is lower than the UVLO threshold voltage minus the hysteresis, the device shuts off. When the voltage rises above the threshold voltage, the device restarts. The typical UVLO rising threshold is 2.8 V for both V_{IN} and V_{VDD}. A hysteresis voltage of 130 mV for V_{IN} and 75 mV for V_{VDD} is also provided to prevent glitch.

7.3.4 Overcurrent Protection

The TPS53311 continuously monitors the current flowing through the high-side and the low-side MOSFETs. If the current through the high-side FET exceeds 4.5 A, the high-side FET turns off and the low-side FET turns on until the next PWM cycle. An overcurrent (OC) counter starts to increment each occurrence of an overcurrent event. The converter shuts down immediately when the OC counter reaches four. The OC counter resets if the detected current is less 4.5 A after an OC event.

Another set of overcurrent circuitry monitors the current flowing through low-side FET. If the current through the low-side FET exceeds 5.1 A, the overcurrent protection is enabled and immediately turns off both the high-side and the low-side FETs and shuts down the converter. The device is fully protected against overcurrent during both on-time and off-time. This protection is latched. See TPS53310 data sheet, *3-A Step-Down Regulator with Integrated Switcher* (SLUSA68), for information on hiccup overcurrent protection.

7.3.5 Overvoltage Protection

The TPS53311 monitors the voltage divided feedback voltage to detect overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, the high-side MOSFET turns off and the low-side MOSFET turns on. The output voltage then drops until it reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device enters a high-impedance state.

7.3.6 Undervoltage Protection

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection timer starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10 µs, the device turns off both the high-side and the low-side MOSFETs and goes into a high-impedance state. This protection is latched.

7.3.7 Overtemperature Protection

The TPS53311 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140°C typical), the device shuts off. When the device temperature falls to 40°C below the overtemperature threshold, it restarts and returns to normal operation.

7.3.8 Output Discharge

When the enable pin is low, the TPS53311 discharges the output capacitors through an internal MOSFET switch between SW and PGND while high-side and low-side MOSFETs remain off. The typical discharge switch-on resistance is 60 Ω. This function is disabled when V_{IN} is less than 1 V.

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Feature Description (continued)

7.3.9 Master and Slave Operation and Synchronization

Two TPS53311 can operate interleaved when configured as master and slave. The SYNC pins of the two devices are connected together for synchronization. In CCM, the master device sends the 180° out-of-phase pulse to the slave device through the SYNC pin, which determines the leading edge of the PWM pulse. If the slave device does not receive the SYNC pulse from the master device or if the SYNC connection is broken during operation, the slave device continues to operate using its own internal clock.

In DE mode, the master and slave switching node does not synchronize to each other if either one of them is operating in DCM. When both master and slave enters CCM, the switching nodes of master and slave synchronize to each other.

The SYNC pin of the slave device can also connect to external clock source within ±20% of the 1.1-MHz switching frequency. The falling edge of the SYNC triggers the rising edge of the PWM signal.

7.4 Device Functional Modes

7.4.1 Operation Mode

The TPS53311 offers five operation modes determined by the PS pin connections listed in Table 1.

Table 1. Operation Mode Selection

PS PIN CONNECTION	OPERATION MODE	AUTO-SKIP AT LIGHT LOAD	MASTER AND SLAVE SUPPORT
GND	FCCM Slave	—	Slave
24.3 kΩ to GND	DE Slave	Yes	Slave
57.6 kΩ to GND	HEF Mode	Yes	—
174 kΩ to GND	DE Master	Yes	Master
Floating or pulled to VDD	FCCM Master	—	Master

In *forced continuous conduction mode* (FCCM), the high-side FET is ON during the on-time and the low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In *diode emulation* mode (DE), the high-side FET is ON during the on-time and low-side FET is ON during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET.

When the load is increased, the inductor current is always positive and the zero-crossing comparator does not send a zero-crossing signal. The converter enters into *continuous conduction mode* (CCM) when no zero-crossing is detected for two consecutive PWM pulses. The switching synchronizes to the internal clock and the switching frequency is fixed.

In *high-efficiency* mode (HEF), the operation is the same as diode emulation mode at light load. However, the converter does not synchronize to the internal clock during CCM. Instead, the PWM modulator determines the switching frequency.

7.4.2 Light Load Operation

In skip modes (DE and HEF) when the load current is less than one-half of the inductor peak current, the inductor current becomes negative by the end of off-time. During light load operation, the low-side MOSFET is turned off when the inductor current reaches zero. The energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation and the switching frequency is reduced. The switching loss is reduced, thereby improving efficiency.

In both DE and HEF mode, the switching frequency is reduced in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. The difference between V_{VBST} and V_{SW} must be maintained at a value higher than 2.4 V.

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7.4.3 Forced Continuous Conduction Mode

When the PS pin is grounded or greater than 2.2 V, the TPS53311 is operating in *forced continuous conduction mode* in both light-load and heavy-load conditions. In this mode, the switching frequency remains constant over the entire load range, making it suitable for applications that need tight control of switching frequency at a cost of lower efficiency at light load.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53311 device is a high-efficiency synchronous-buck converter. The device suits low-output voltage point-of-load applications with 3-A or lower output current in computing and similar digital consumer applications.

8.2 Typical Application

This design example describes a voltage-mode, 3-A synchronous buck converter with integrated MOSFETs. The TPS53311 device provides a fixed 1.5-V output at up to 3 A from a 3.3-V input bus.

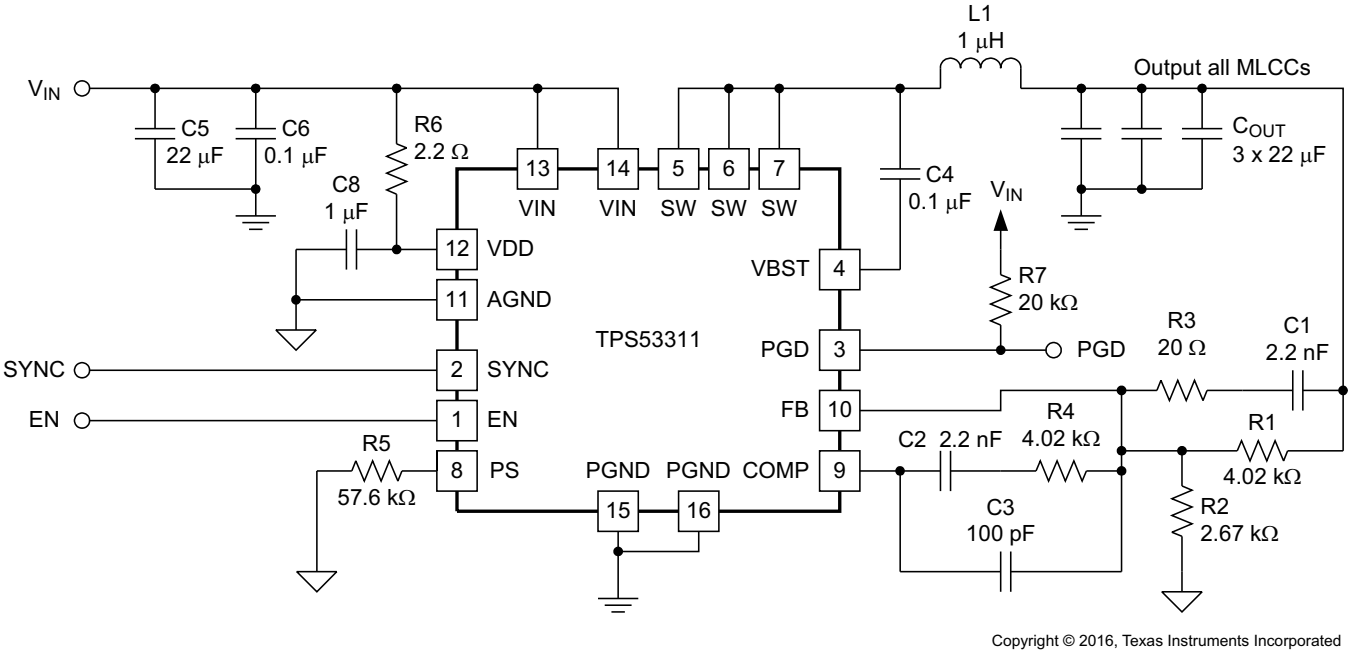


Figure 13. Typical 3.3-V Input Application Circuit Diagram

8.2.1 Design Requirements

Table 2 lists the parameters for this design example.

Table 2. TPS53311 Design Example Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage, V_{IN}	V_{IN}	2.9	3.3	6	V
Maximum input current	V_{IN} = 3.3 V, 1.5 V or 3 A			2.82	A
No load input current	V_{IN} = 3.3 V, 1.5 V or 0 A			40	mA
OUTPUT CHARACTERISTICS					
Output voltage, V_O		1.485	1.5	1.515	V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		1%		

Typical Application (continued)

Table 2. TPS53311 Design Example Specifications (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage ripple	V_{IN} = 3.3 V, 1.5 V or 0 A to 3 A			20	mVpp
Output load current		0		3	A
Output over current			4.5		A
SYSTEMS CHARACTERISTICS					
Switching frequency	Fixed		1.1		MHz
1.5-V full load efficiency	V_{IN} = 3.3 V, 1.5 V or 3 A		88.82%		
	V_{IN} = 5 V, 1.5 V or 3 A		89.5%		
Operating temperature			25		°C

8.2.2 Detailed Design Procedure

Select the external components using the following steps.

8.2.2.1 Determine the Value of R1 and R2

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 13. R1 is connected between the FB pin and the output, and R2 is connected between the FB pin and GND. The recommended value for R1 is from 1 kΩ to 5 kΩ. Determine R2 using equation in Equation 1.

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \tag{1}$$

8.2.2.2 Choose the Inductor

The inductance value must be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by Equation 2.

$$I_{L(ripple)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{2}$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

8.2.2.3 Choose the Output Capacitor(s)

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components calculated with Equation 3 through Equation 6.

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \tag{3}$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \tag{4}$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \tag{5}$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \tag{6}$$

When ceramic output capacitors are used, the ESL component is usually negligible. In the case when multiple output capacitors are used, ESR and ESL must be the equivalent of ESR and ESL of all the output capacitor in parallel.

When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in Equation 7.

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$$V_{RIPPLE(DCM)} = \frac{\left(\alpha \times I_{L(ripple)} - I_{OUT}\right)^2}{2 \times C_{OUT} \times f_{SW} \times I_{L(ripple)}}$$

where

- α is the DCM on-time coefficient and can be expressed in Equation 8 (typical value 1.25) (7)

$$\alpha = \frac{t_{ON(DCM)}}{t_{ON(CCM)}} \quad (8)$$

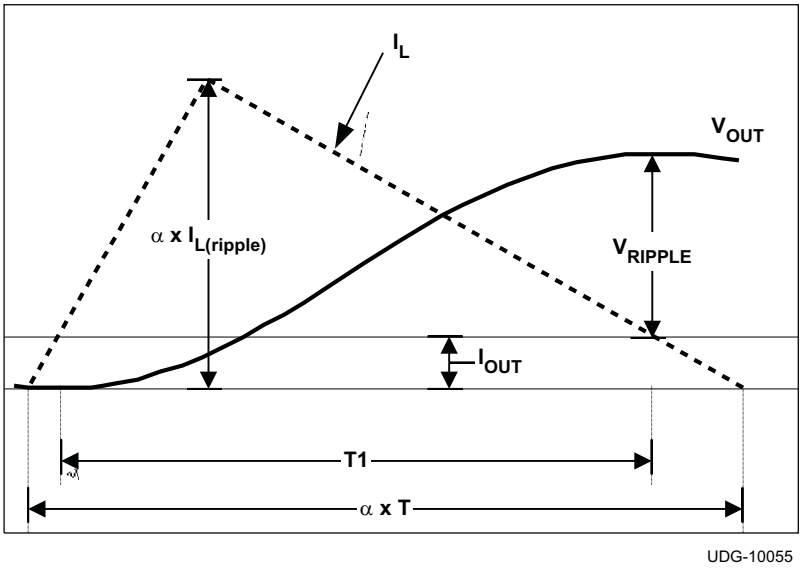


Figure 14. DCM V_{OUT} Ripple Calculation

8.2.2.4 Choose the Input Capacitor

The selection of input capacitor must be determined by the ripple current requirement. The ripple current generated by the converter needs to be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed in Equation 9.

$$I_{IN(ripple)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where

- D is the duty cycle and can be expressed as shown in Equation 10 (9)

$$D = \frac{V_{OUT}}{V_{IN}} \quad (10)$$

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors must be placed close to the device. TI recommends the ceramic capacitor because it provides low ESR and low ESL. The input voltage ripple can be calculated as shown in Equation 11 when the total input capacitance is determined.

$$V_{IN(ripple)} = \frac{I_{OUT} \times D}{f_{SW} \times C_{IN}} \quad (11)$$

8.2.2.5 Compensation Design

The TPS53311 uses voltage mode control. To effectively compensate the power stage and ensure fast transient response, Type III compensation is typically used.

The control to output transfer function can be described in Equation 12.

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$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \quad (12)$$

The output L-C filter introduces a double pole which can be calculated as shown in Equation 13.

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \quad (13)$$

The ESR zero can be calculated as shown in Equation 14.

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (14)$$

Figure 15 and Figure 16 show the configuration of Type III compensation and typical pole and zero locations. Equation 16 through Equation 20 describe the compensator transfer function and poles and zeros of the Type III network.

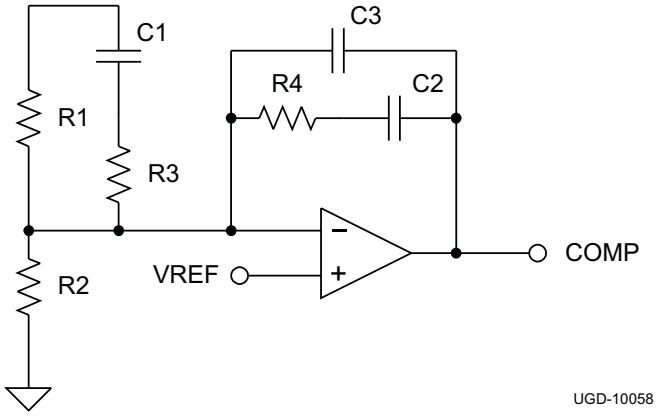


Figure 15. Type III Compensation Network Configuration Schematic

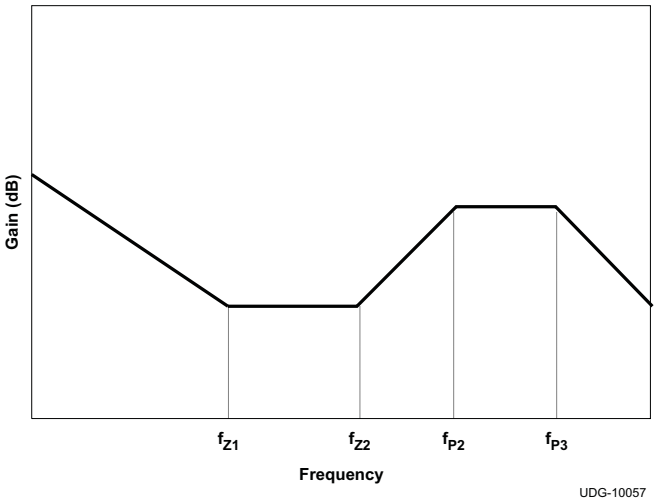


Figure 16. Type III Compensation Gain Plot and Zero/Pole Placement

$$G_{EA} = \frac{(1 + s \times C_1 \times (R_1 + R_3))(1 + s \times R_4 \times C_2)}{(s \times R_1 \times (C_2 + C_3)) \times (1 + s \times C_1 \times R_3) \times \left(1 + s \times R_4 \frac{C_2 \times C_3}{C_2 + C_3}\right)} \quad (15)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_2} \quad (16)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R_1 + R_3) \times C_1} \cong \frac{1}{2 \times \pi \times R_1 \times C_1} \quad (17)$$

$$f_{P1} = 0 \quad (18)$$

$$f_{P2} = \frac{1}{2 \times \pi \times R_3 \times C_1} \quad (19)$$

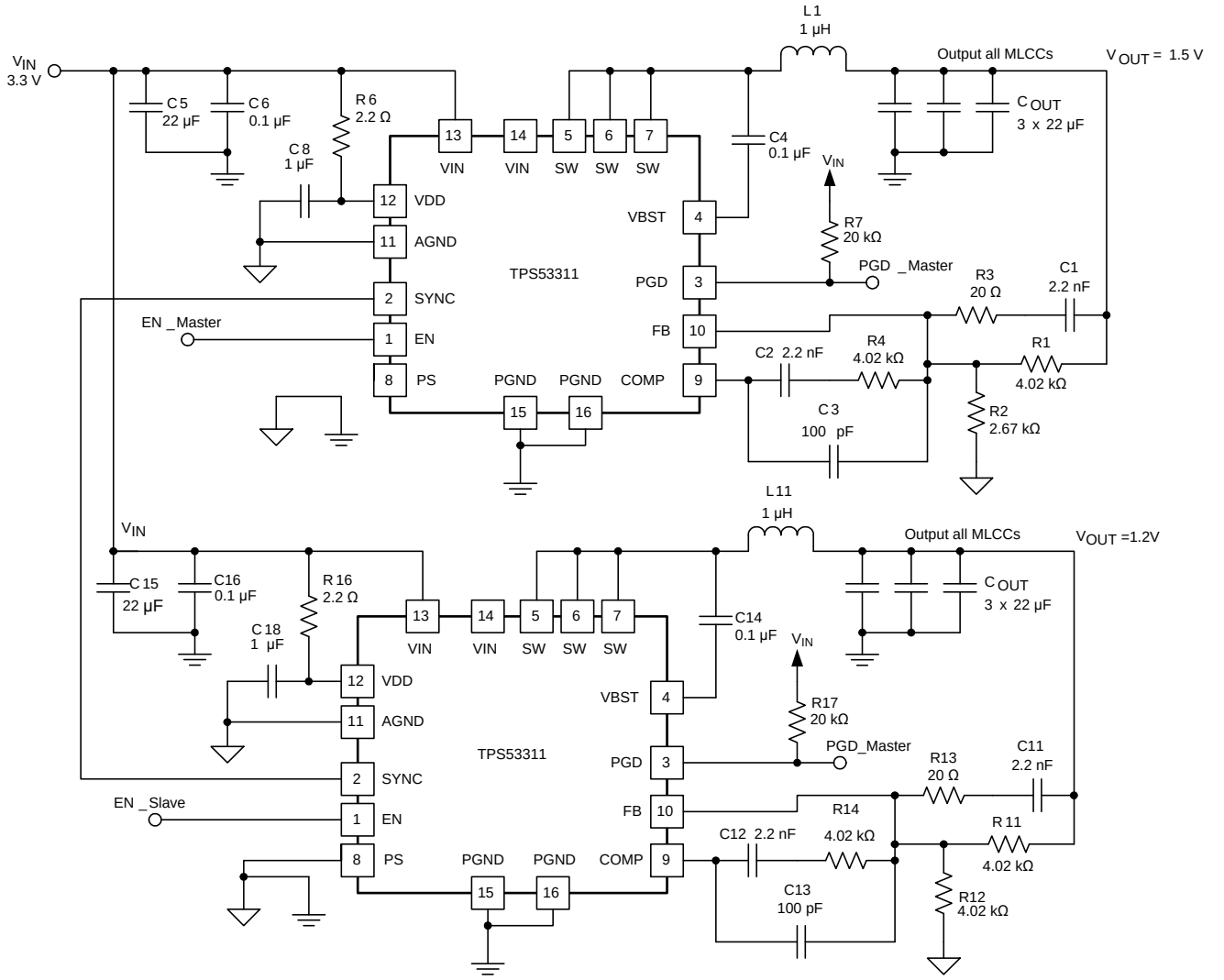
$$f_{P3} = \frac{1}{2 \times \pi \times R_4 \times \left(\frac{C_2 \times C_3}{C_2 + C_3}\right)} \cong \frac{1}{2 \times \pi \times R_4 \times C_3} \quad (20)$$

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The two zeros can be placed near the double pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45 degrees is required for stable operation.

For DCM operation, a C3 between 56 pF and 150 pF is recommended for output capacitance between 20 µF to 200 µF.

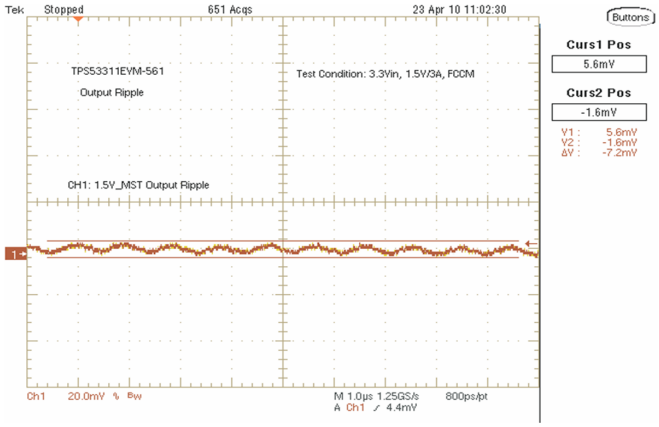
Figure 17 shows the master and slave configuration schematic for a design with a 3.3-V input.



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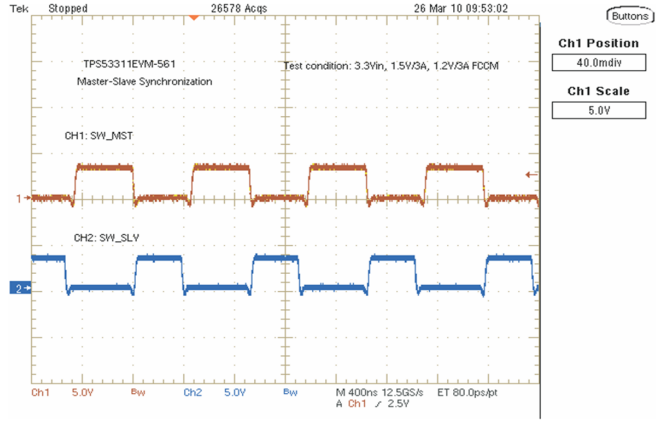
Figure 17. Master and Slave Configuration Schematic

8.2.3 Application Curves



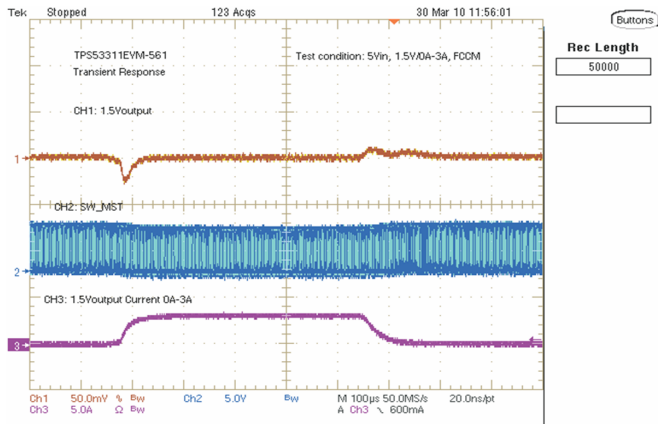
3.3 V_{IN}, 1.5 V/3 A

Figure 18. 1.5-V Output Ripple



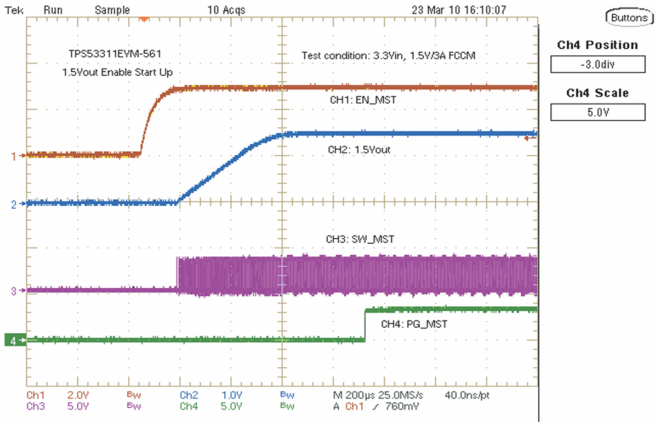
3.3 V_{IN}, 1.5 V/3 A and 1.2 V/3 A

Figure 19. Master-Slave 180° Synchronization



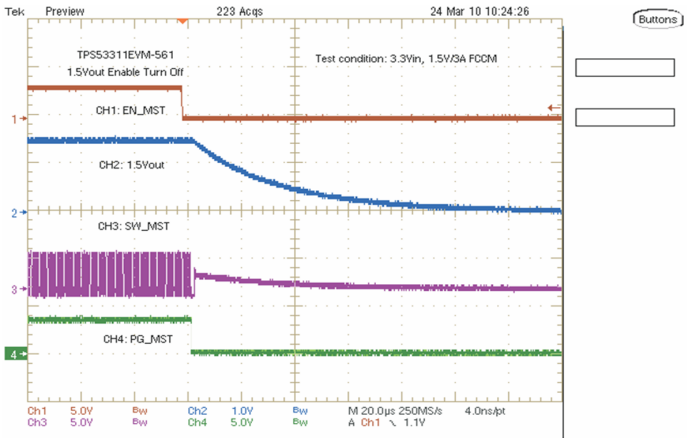
5 V_{IN}, 1.5 V/0 A-3 A

Figure 20. 1.5-V Output Transient



3.3 V_{IN}, 1.5 V/3 A

Figure 21. 1.5-V Turnon Waveform



3.3 V_{IN}, 1.5 V/3 A

Figure 22. 1.5-V Turnoff Waveform

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9 Power Supply Recommendations

The TPS53311 device is designed to operate from an input voltage supply range from 2.9 V to 6 V (2.9 V to 3.5 V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in *Layout*.

10 Layout

10.1 Layout Guidelines

Good layout is essential for stable power supply operation. Follow these guidelines for a clean PCB layout:

- Separate the power ground and analog ground planes. Connect them together at one location.
- Use four vias to connect the thermal pad to power ground.
- Place V_{IN} and V_{DD} decoupling capacitors as close to the device as possible.
- Use wide traces for V_{IN}, V_{OUT}, PGND and SW. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, SYNC, VBST).
- See *Using the TPS53311EVM-561, a 3-A Eco-mode™ Integrated Switcher With Master Slave* (SLUU428) for a layout example.

10.2 Layout Example

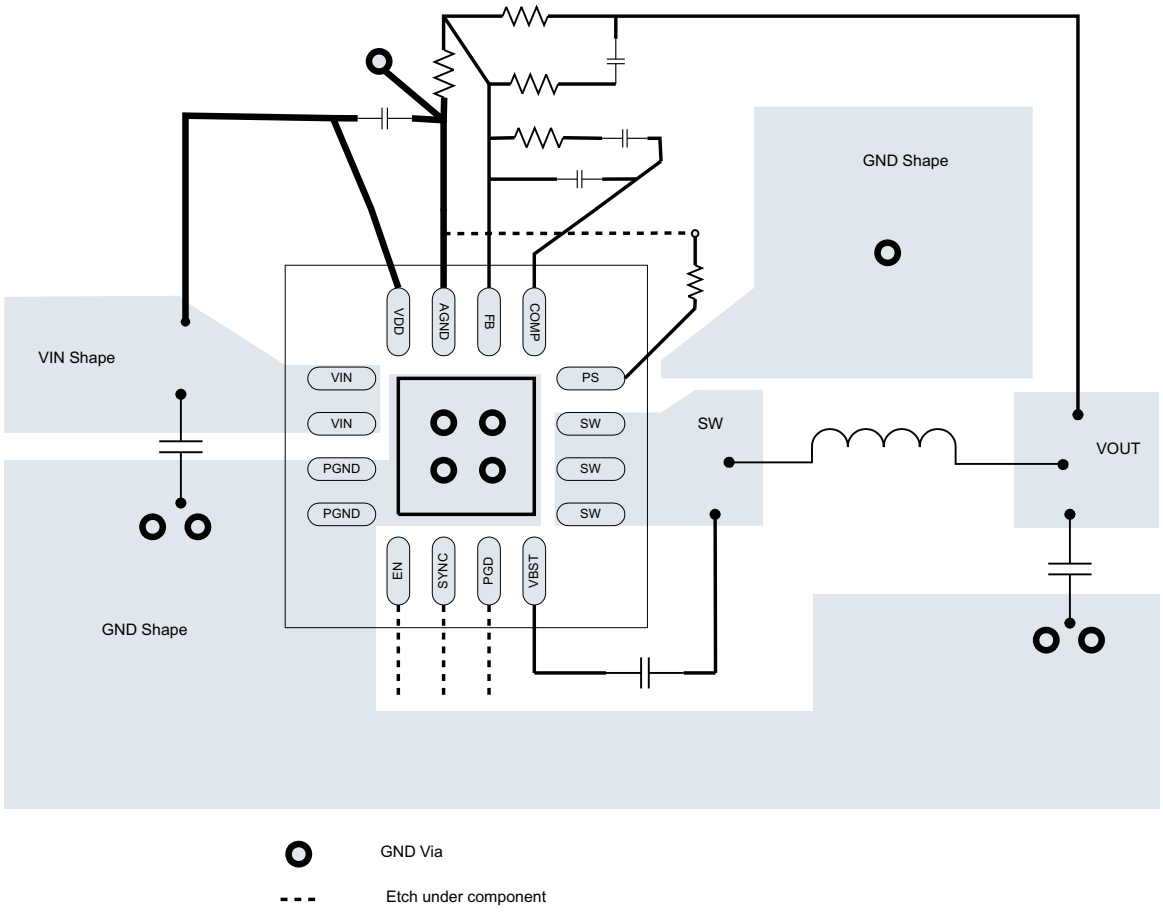


Figure 23. TPS533x Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *3-A Step-Down Regulator with Integrated Switcher* (SLUSA68)
- *Using the TPS53311EVM-561, a 3-A Eco-mode™ Integrated Switcher With Master Slave* (SLUU428)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

SmoothPWM, Eco-mode, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53311RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3311
TPS53311RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3311
TPS53311RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3311
TPS53311RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3311
TPS53311RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3311
TPS53311RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	3311

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

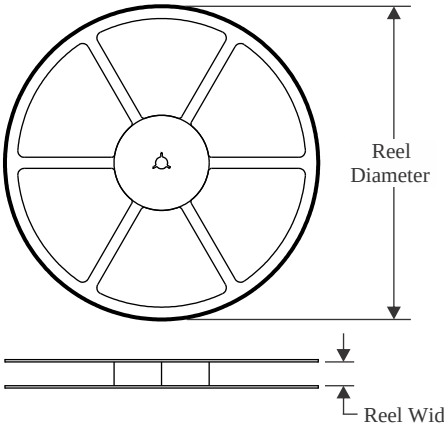
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

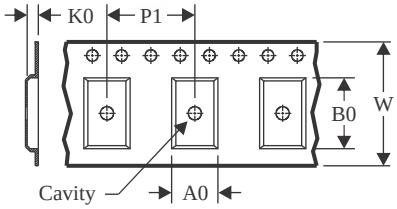
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

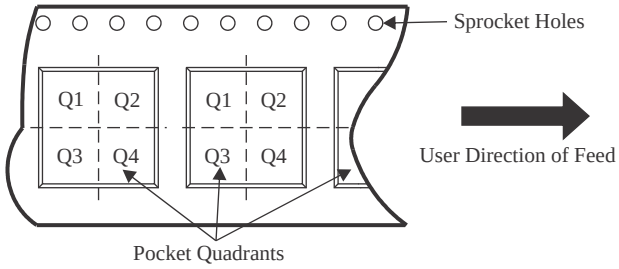


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

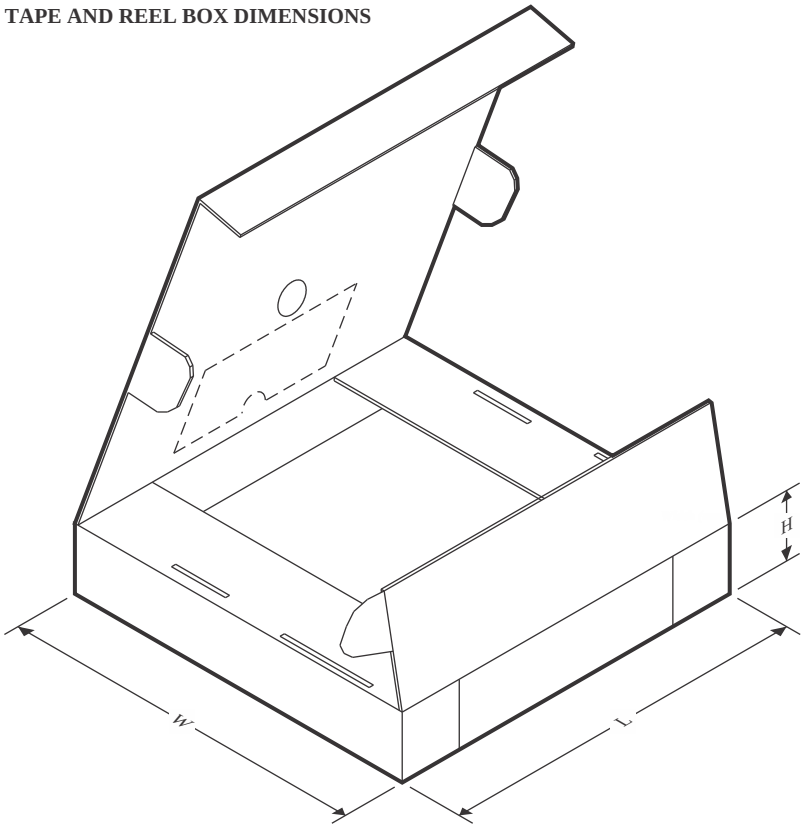
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53311RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53311RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53311RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

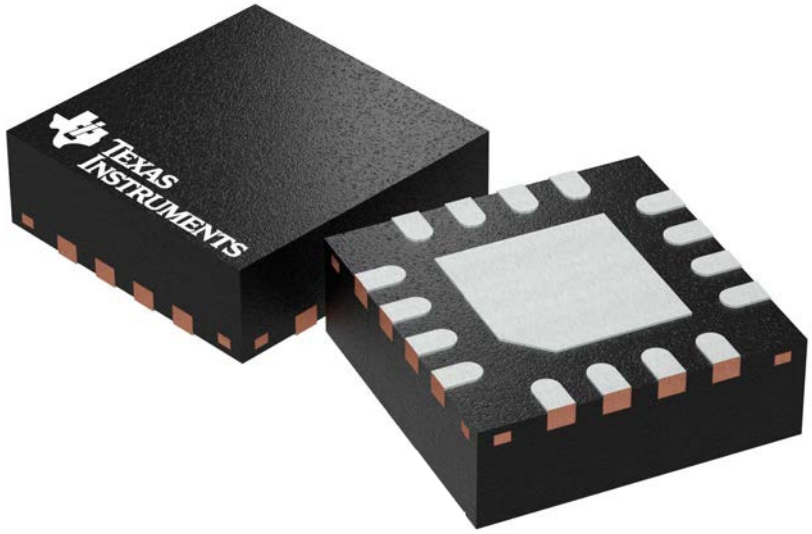


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53311RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS53311RGTR	VQFN	RGT	16	3000	338.0	355.0	35.0
TPS53311RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



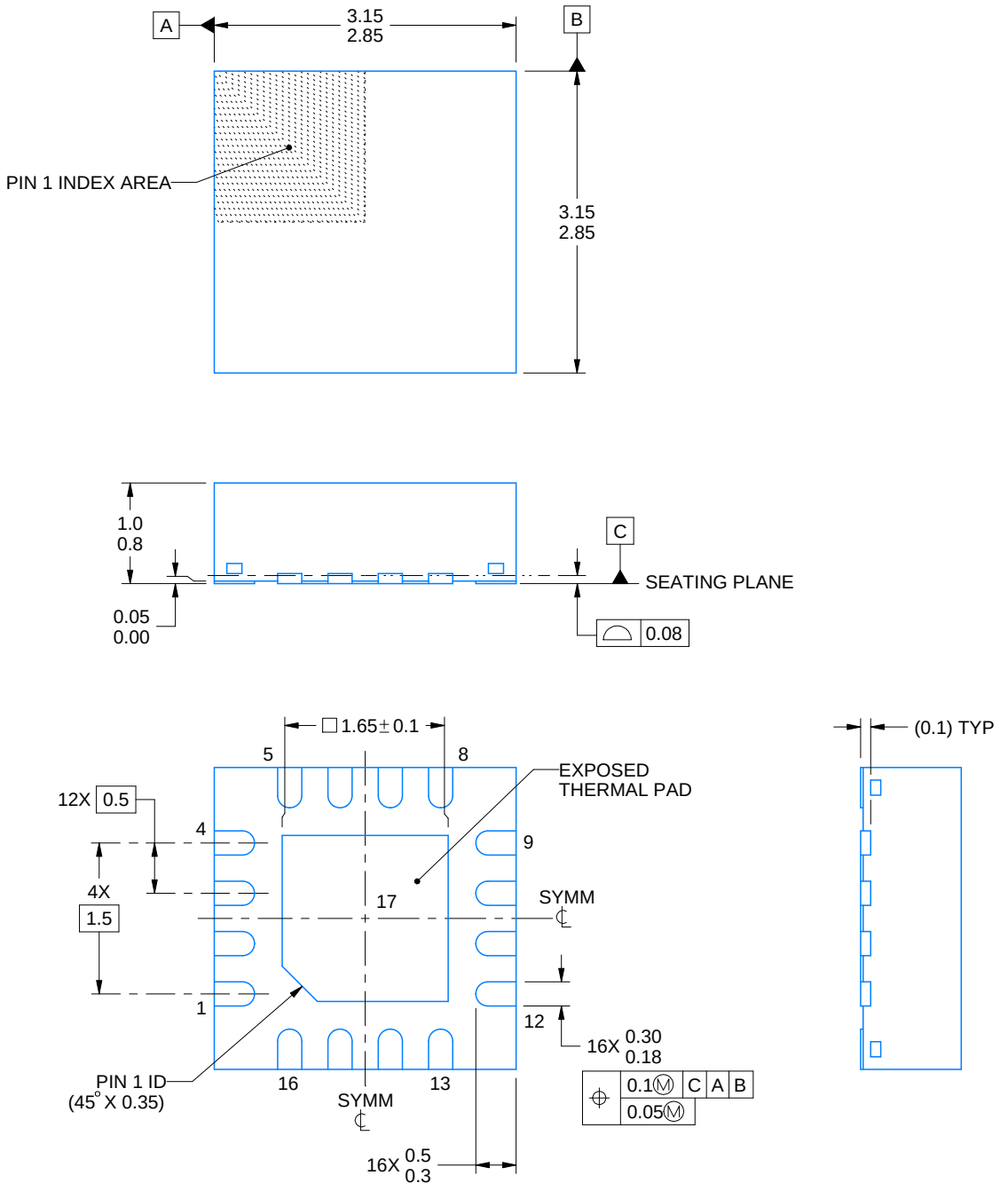
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016F

PACKAGE OUTLINE

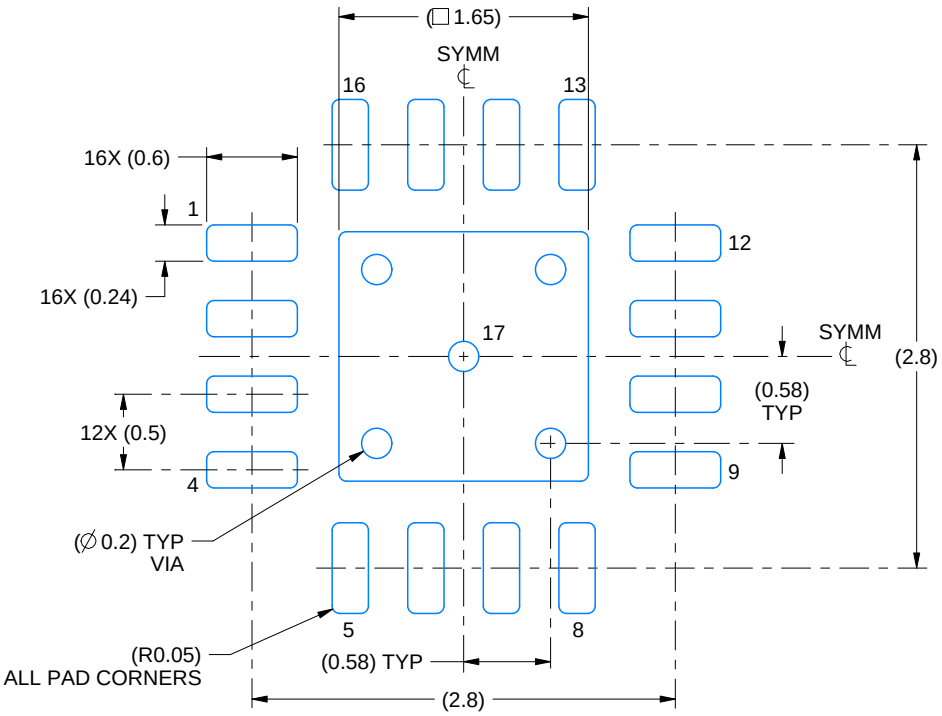
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

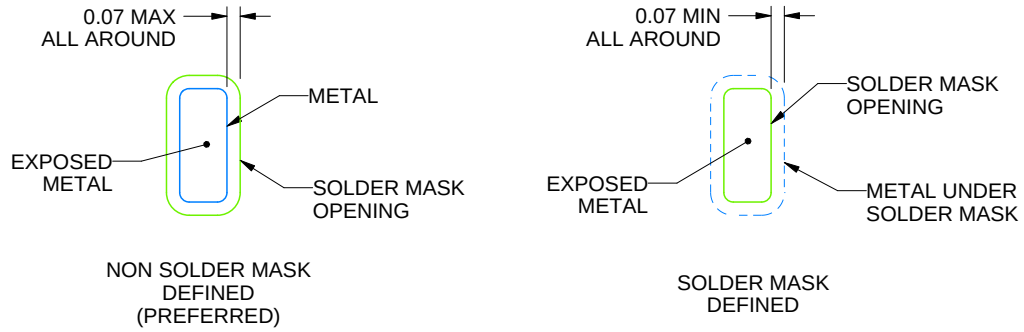


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

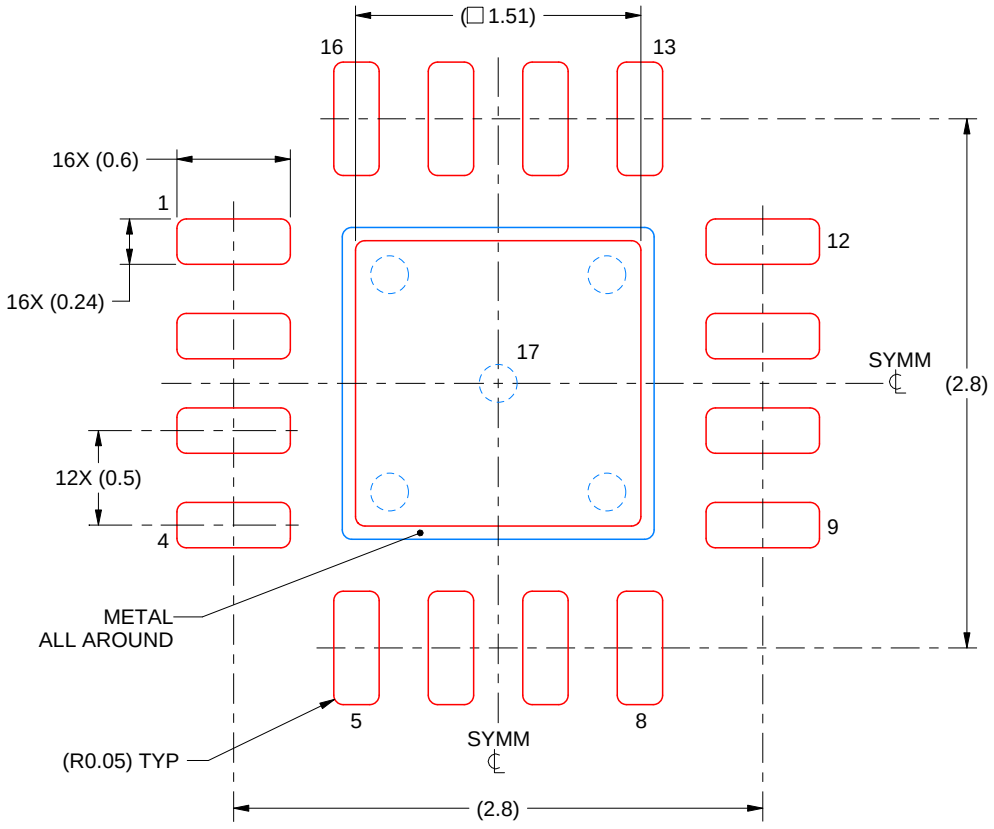


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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