4.5-V TO 20-V INPUT, 3-A OUTPUT SYNCHRONOUS PWM SWITCHES WITH INTEGRATED FET (SWIFT™)

FEATURES

- 100-mΩ, 4.5-A Peak MOSFET Switch for High Efficiency at 3-A Continuous Output Current
- Use External Low-Side MOSFET or Diode
- Fixed-Output Versions – 1.2 V/1.5 V/1.8 V/ 2.5 V/3.3 V/5 V
- Internally Compensated for Low Parts Count
- Synchronize to External Clock
- 180° Out-of-Phase Synchronization
- Wide Pulse Width Modulation (PWM) Frequency – Fixed 250 kHz, 500 kHz, or Adjustable 250 kHz to 700 kHz
- Internal Slow Start
- Load Protected by Peak Current Limit and Thermal Shutdown
- Adjustable Undervoltage Lockout
- 16-Pin PowerPAD™ Thin Shrink Small-Outline Package (TSSOP) (PWP)

APPLICATIONS

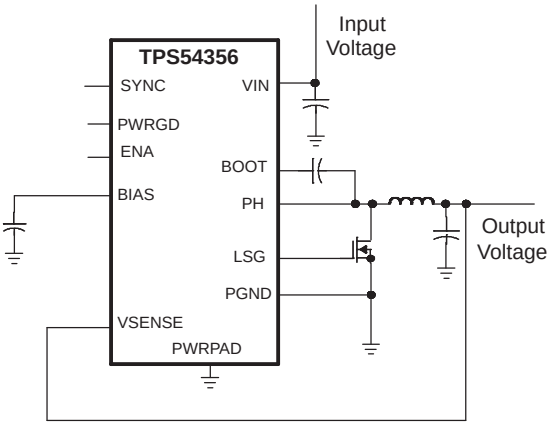
- Industrial and Commercial Low-Power Systems
- LCD Monitors and TVs
- Computer Peripherals
- Point-of-Load Regulation for High Performance DSPs, FPGAs, ASICs, and Microprocessors

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

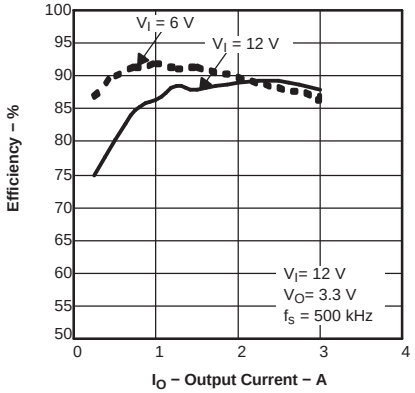
- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military (–55°C/125°C) Temperature Range(1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(1) Additional temperature ranges are available - contact factory

SIMPLIFIED SCHEMATIC



EFFICIENCY vs OUTPUT CURRENT



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DESCRIPTION/ORDERING INFORMATION

The TPS5435x is a medium-output-current synchronous buck PWM converter with an integrated high-side MOSFET and a gate driver for an optional low-side external MOSFET. Features include a high-performance voltage error amplifier that enables maximum performance under transient conditions. The TPS5435x has an undervoltage lockout (UVLO) circuit to prevent start-up until the input voltage reaches a preset value, an internal slow-start circuit to limit in-rush currents, and a power-good (PWRGD) output to indicate valid output conditions. The synchronization feature is configurable as either an input or an output for easy 180° out-of-phase synchronization.

The TPS5435x devices are available in a thermally enhanced 16-pin PowerPAD™ Thin Shrink Small-Outline Package (TSSOP). TI provides evaluation modules and the SWIFT™ Designer software tool to aid in quickly achieving high-performance power-supply designs to meet aggressive equipment development cycles.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	PACKAGE(1)	OUTPUT VOLTAGE	PART NUMBER	PACKAGE MARKING
–55°C to 125°C	Plastic HTSSOP – PWP	1.2 V	TPS54352MPWPREP(2)	TBD
	Plastic HTSSOP – PWP	1.5 V	TPS54353MPWPREP(2)	TBD
	Plastic HTSSOP – PWP	1.8 V	TPS54354MPWPREP	PMDM
	Plastic HTSSOP – PWP	2.5 V	TPS54355MPWPREP(2)	TBD
	Plastic HTSSOP – PWP	3.3 V	TPS54356MPWPREP	PMEM
	Plastic HTSSOP – PWP	5 V	TPS54357MPWPREP(2)	TBD

(1) The PWP package also is available taped and reeled. Add an R suffix to the device type (i.e., TPS5435xPWPR).
(2) Product preview

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
Input voltage range, V_I	VIN	–0.3 V to 21.5 V
	VSENSE	–0.3 V to 8 V
	UVLO	–0.3 V to 8 V
	SYNC	–0.3 V to 4 V
	ENA	–0.3 V to 4 V
	BOOT	VI(PH) + 8 V
Output voltage range, V_O	VBIAS	–0.3 V to 8.5 V
	LSG	–0.3 V to 8.5 V
	SYNC	–0.3 V to 4 V
	RT	–0.3 V to 4 V
	PWRGD	–0.3 V to 6 V
	COMP	–0.3 V to 4 V
	PH	–1.5 V to 22 V
Source current, I_O	PH	Internally Limited (A)
	LSG (steady-state current)	10 mA
	COMP, VBIAS	3 mA
Sink current, I_S	SYNC	5 mA
	LSG (steady-state current)	100 mA
	PH (steady-state current)	500 mA
	COMP	3 mA
	ENA, PWRGD	10 mA
Voltage differential	AGND to PGND	±0.3 V
Operating virtual junction temperature range, T_J		–55°C to 150°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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Electrostatic Discharge (ESD) Protection

	MIN	MAX	UNIT
Human-Body Model (HBM)		600	V
Charged-Device Model (CDM)		1.5	kV

Recommended Operating Conditions

		MIN	MAX	UNIT
Input voltage range, V_I	TPS54352-6	4.5	20	V
	TPS54357	6.65	20	
Operating junction temperature, T_J		–55	125	°C

Electrical Characteristics

T_J = –55°C to 125°C, VIN = 4.5 V to 20 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current							
I_Q	Quiescent current		Operating current, PH pin open, No external low side MOSFET, RT = Hi-Z		5		mA
			Shutdown, ENA = 0 V		1		
VIN	Start threshold voltage	TPS54352-6			4.32	4.48	V
		TPS54357			6.4	6.65	
	Stop threshold voltage	TPS54352-6		3.69	3.97		V
		TPS54357		5.45	5.8		
	Hysteresis	TPS54352-6			350		mV
		TPS54357			600		
Output Voltage							
V_O	Output voltage	TPS54352	T_J = 25°C, I_O = 100 mA to 3 A	1.88	1.2	1.212	V
			I_O = 100 mA to 3 A	1.176	1.2	1.224	
		TPS54353	T_J = 25°C, I_O = 100 mA to 3 A	1.485	1.5	1.515	
			I_O = 100 mA to 3 A	1.47	1.5	1.53	
		TPS54354	T_J = 25°C, I_O = 100 mA to 3 A	1.782	1.8	1.818	
			I_O = 100 mA to 3 A	1.764	1.8	1.836	
		TPS54355	T_J = 25°C, I_O = 100 mA to 3 A	2.475	2.5	2.525	
			I_O = 100 mA to 3 A	2.45	2.5	2.55	
		TPS54356	T_J = 25°C, VIN = 5.5 V to 20 V, I_O = 100 mA to 3 A	3.267	3.3	3.333	
			VIN = 5.5 V to 20 V, I_O = 100 mA to 3 A	3.234	3.3	3.366	
		TPS54357	T_J = 25°C, VIN = 7.5 V to 20 V, I_O = 100 mA to 3 A	4.95	5	5.05	
			VIN = 7.5 V to 20 V, I_O = 100 mA to 3 A	4.9	5	5.1	
Under Voltage Lockout (UVLO)							
UVLO	Start threshold voltage				1.2	1.25	V
	Stop threshold voltage			1.02	1.1		V
	Hysteresis				100		mV
Bias Voltage (VBIAS)							
VBIAS	Output voltage		I_{VBIAS} = 5 mA, VIN ≥ 12 V	7.5	7.8	8	V
			I_{VBIAS} = 5 mA, VIN = 4.5 V	4.4	4.47	4.5	
Oscillator (RT)							
	Internally set PWM switching frequency		RT grounded	200	250	300	kHz
			RT open	400	500	600	
	Externally set PWM switching frequency		RT = 100 kΩ (1% resistor to AGND)	425	500	575	kHz

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Electrical Characteristics (continued)

T_J = –55°C to 125°C, VIN = 4.5 V to 20 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Falling-Edge-Triggered Bidirectional Sync System (SYNC)							
	SYNC out low-to-high rise time (10%/90%)(1)		25 pF to ground		200	500	ns
	SYNC out high-to-low fall time (90%/10%)(1)		25 pF to ground		5	10	ns
	Falling-edge delay time(1)		Delay from rising edge to rising edge of PH pins, See Figure 19		180		°
	Minimum input pulse width(1)		RT = 100 kΩ		100		ns
	Delay (falling-edge SYNC to rising-edge PH)(1)		RT = 100 kΩ		360		ns
	SYNC out high-level voltage		50-kΩ resistor to ground, No pullup resistor	2.5			V
	SYNC out low-level voltage					0.6	V
	SYNC in low-level threshold			0.8			V
	SYNC in high-level threshold					2.3	V
	SYNC in frequency range(1)		Percentage of programmed frequency	–10%		10%	
				225		770	kHz
Feed-Forward Modulator (Internal Signal)							
	Modulator gain		VIN = 12 V, T_J = 25°C		8		
	Modulator gain variation				±25%		
	Minimum controllable ON time(1)				180		ns
	Maximum duty factor(1)		VIN = 4.5 V	80%	86%		
VSENSE							
	Input bias current, VSENSE				1		µA
Enable (ENA)							
	Disable low-level input voltage					0.5	V
	Internal slow-start time (10% to 90%)	TPS54352	f_s = 250 kHz, RT = ground(1)		3.2		ms
			f_s = 500 kHz, RT = Hi-Z(1)		1.6		
		TPS54353	f_s = 250 kHz, RT = ground(1)		4		
			f_s = 500 kHz, RT = Hi-Z(1)		2		
		TPS54354	f_s = 250 kHz, RT = ground(1)		4.6		
			f_s = 500 kHz, RT = Hi-Z(1)		2.3		
		TPS54355	f_s = 250 kHz, RT = ground(1)		4.4		
			f_s = 500 kHz, RT = Hi-Z(1)		2.2		
		TPS54356	f_s = 250 kHz, RT = ground(1)		5.9		
			f_s = 500 kHz, RT = Hi-Z(1)		2.9		
		TPS54357	f_s = 250 kHz, RT = ground(1)		5.4		
			f_s = 500 kHz, RT = Hi-Z(1)		2.7		
	Pullup current source			1.8	5	10	µA
	Pulldown MOSFET		$I_{I(ENA)}$ = 1 mA		0.1		V
Power Good (PWRGD)							
	Power-good threshold		Rising voltage		97%		
	Rising-edge delay(1)		f_s = 250 kHz		4		ms
			f_s = 500 kHz		2		
PWRGD	Output saturation voltage		I_{sink} = 1 mA, VIN > 4.5 V		0.05		V
	Output saturation voltage		I_{sink} = 100 µA, VIN = 0 V		0.76		V
	Open-drain leakage current		Voltage on PWRGD = 6 V			3	µA

(1) Specified by design, not production tested

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Electrical Characteristics (continued)

T_J = –55°C to 125°C, VIN = 4.5 V to 20 V (unless otherwise noted)

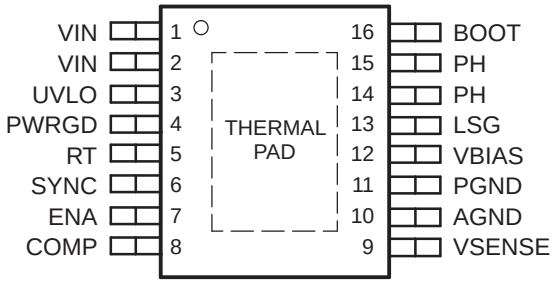
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit						
	Current limit	VIN = 12 V	3.3	4.5	6.5	A
	Current-limit hiccup time(2)	f_s = 500 kHz		4.5		ms
Thermal Shutdown						
	Thermal-shutdown trip point(2)			165		°C
	Thermal-shutdown hysteresis(2)			7		°C
Low-Side MOSFET Driver (LSG)						
	Turn-on rise time, (10/90%)(2)	VIN = 4.5 V, Capacitive load = 1000 pF		15		ns
	Deadtime	VIN = 12 V		60		ns
	Driver ON resistance	VIN = 4.5 V sink/source		7.5		Ω
		VIN = 12 V sink/source		5		
Output Power MOSFETS (PH)						
	Phase-node voltage when disabled	DC coinditions and no load, ENA = 0 V		0.5		V
	Voltage drop, low-side FET and diode	VIN = 4.5 V, Idc = 100 mA		1.13	1.42	V
		VIN = 12 V, Idc = 100 mA		1.08	1.38	
$r_{DS(ON)}$	High-side power MOSFET switch(3)	VIN = 4.5 V, BOOT-PH = 4.5 V, I_O = 0.5 A		150	300	mΩ
		VIN = 12 V, BOOT-PH = 8V, I_O = 0.5 A		100	200	

(2) Specified by design, not production tested
(3) Resistance from VIN to PH pins

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PIN ASSIGNMENTS

PWP PACKAGE
(TOP VIEW)



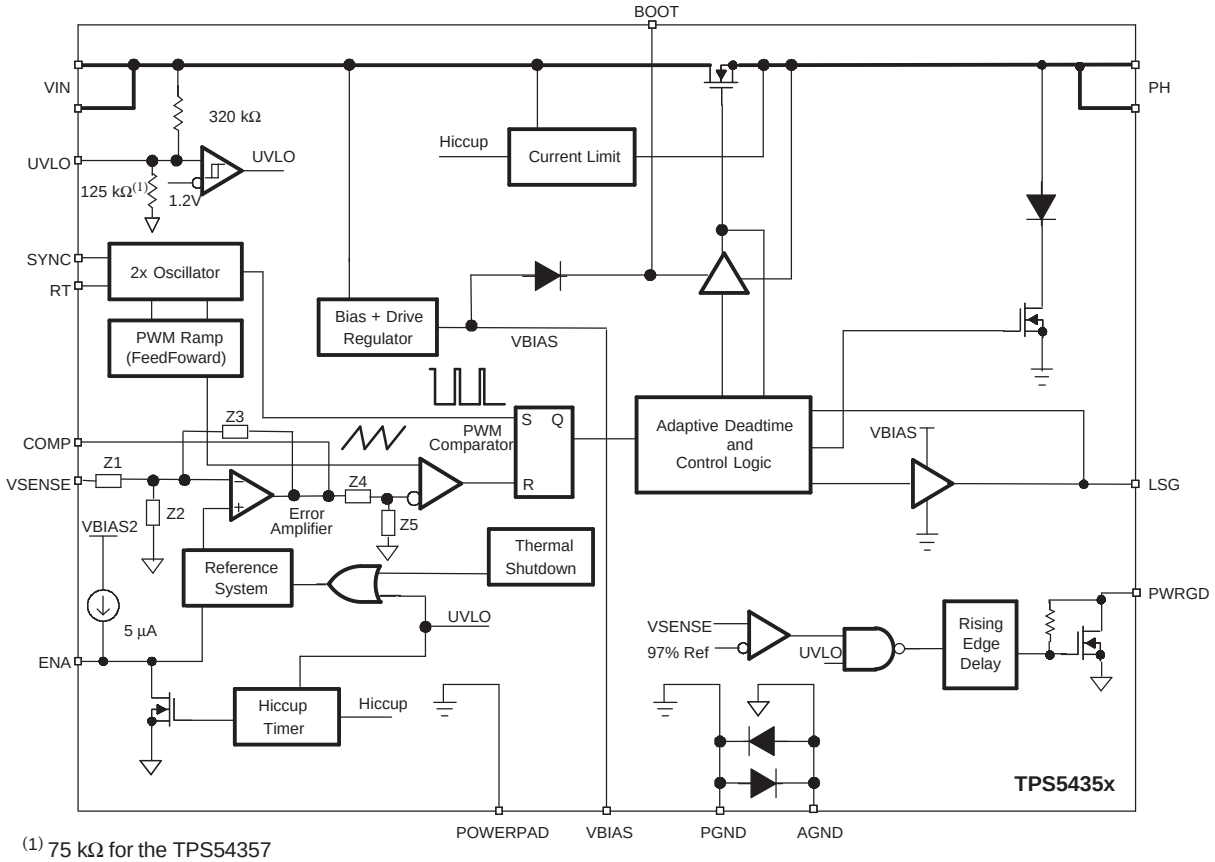
NOTE: If there is not a pin 1 indicator, turn device to enable reading the symbol from left to right. Pin 1 is at the lower left corner of the device.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1, 2	VIN	Input supply voltage, 4.5 V to 20 V. Must bypass with a low ESR 10-µF ceramic capacitor. Place cap as close to device as possible; see Figure 23 for an example.
3	UVLO	Undervoltage lockout. Connecting an external resistive voltage divider from VIN to the pin overrides the internal default VIN start and stop thresholds.
4	PWRGD	Power good output. Open-drain output. A low on the pin indicates that the output is less than the desired output voltage. There is an internal rising-edge filter on the output of the PWRGD comparator.
5	RT	Frequency setting. Connect a resistor from RT to AGND to set the switching frequency. Connecting the RT pin to ground or floating will set the frequency to an internally preselected frequency.
6	SYNC	Bidirectional synchronization I/O. SYNC is an output when the RT pin is floating or connected low. The output is a falling-edge signal out of phase with the rising edge of PH. SYNC may be used as an input to synchronize to a system clock by connecting to a falling edge signal when an RT resistor is used. See 180° Out of Phase Synchronization operation in the Application Information section. In all cases, a 10-kΩ resistor must be tied to the SYNC pin in parallel with ground. For information on how to extend slow start, see the Enable (ENA) and Internal Slow Start section.
7	ENA	Enable. Below 0.5 V, the device stops switching. Float pin to enable.
8	COMP	Error amplifier output. Do not connect anything to this pin.
9	VSENSE	Feedback
10	AGND	Analog ground. Internally connected to the sensitive analog ground circuitry. Connect to PGND and PowerPAD package.
11	PGND	Power ground. Noisy internal ground. Return currents from the LSG driver output return through the PGND pin. Connect to AGND and PowerPAD package.
12	VBIAS	Internal 8-V bias voltage. A 1-µF ceramic bypass capacitance is required on the VBIAS pin.
13	LSG	Gate drive for optional low-side MOSFET. Connect gate of n-channel MOSFET for a higher efficiency synchronous buck converter configuration. Otherwise, leave open and connect Schottky diode from ground to PH pins.
14, 15	PH	Phase node. Connect to external L-C filter.
16	BOOT	Bootstrap capacitor for high-side gate driver. Connect a 0.1-µF ceramic capacitor from BOOT to PH pins.
	PowerPAD	PGND and AGND pins must be connected to the exposed pad for proper operation. See Figure 23 for an example PCB layout.

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FUNCTIONAL BLOCK DIAGRAM



(1) 75 kΩ for the TPS54357

DETAILED DESCRIPTION

Undervoltage Lockout (UVLO)

The UVLO system has an internal voltage divider from VIN to AGND. The defaults for the start/stop values are labeled VIN and are given in Table 1. The internal UVLO threshold can be overridden by placing an external resistor divider from VIN to ground. The internal divider values are approximately 320 kΩ for the high-side resistor and 125 kΩ for the low-side resistor. The divider ratio (and, therefore, the default start/stop values) is quite accurate, but the absolute values of the internal resistors may vary as much as 15%. If high accuracy is required for an externally adjusted UVLO threshold, select lower-value external resistors to set the UVLO threshold. Using a 1-kΩ resistor for the low-side resistor (R2 see Figure 1) is recommended. Under no circumstances should the UVLO pin be connected directly to VIN.

Table 1. Start/Stop Voltage Threshold

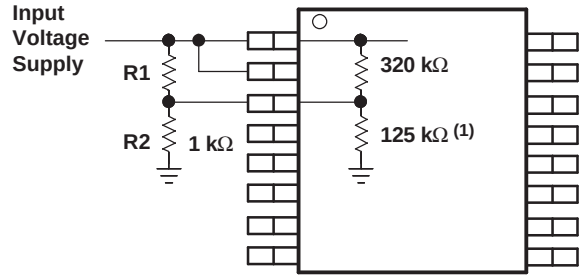
		START VOLTAGE THRESHOLD	STOP VOLTAGE THRESHOLD
VIN (default)	TPS54352-6	4.49	3.69
	TPS54357	6.65	5.45
UVLO		1.24	1.02

The equations for selecting the UVLO resistors are:

$$R1 = \frac{VIN(start) \times 1\ k\Omega}{1.24\ V} - 1\ k\Omega \quad (1)$$

$$VIN(stop) = \frac{(R1 + 1\ k\Omega) \times 1.02\ V}{1\ k\Omega} \quad (2)$$

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(1) 75 kΩ for the TPS54357

Figure 1. Circuit Using External UVLO Function

For applications that require an UVLO threshold greater than 4.49 V (6.6 V for TPS54357), external resistors may be implemented (see Figure 1) to adjust the start-voltage threshold. For example, an application needing a UVLO start voltage of approximately 7.8 V using equation 1, R1 is calculated to the nearest standard resistor value of 5.36 kΩ. Using equation 2, the input voltage stop threshold is calculated as 6.48 V.

Enable (ENA) and Internal Slow Start

The TPS5435x has an internal digital slow start that ramps the reference voltage to its final value in 1150 switching cycles. The internal slow-start time (10% to 90%) is approximated by the following expression:

$$T_{SS_INTERNAL}(ms) = \frac{1.15k}{f_S\,(kHz) \times n} \quad (3)$$

Use n in Table 2.

Table 2. Slow-Start Characteristics

DEVICE	n
TPS54352	1.485
TPS54353	1.2
TPS54354	1
TPS54355	1.084
TPS54356	0.818
TPS54357	0.900

Once the TPS5435x device is in normal regulation, the ENA pin is high. If ENA is pulled below the stop threshold of 0.5 V, switching stops and the internal slow start resets. If an application requires the TPS5435x to be disabled, use open-drain or open-collector output logic to interface to ENA (see Figure 2). ENA has an internal pullup current source. Do not use external pullup resistors.

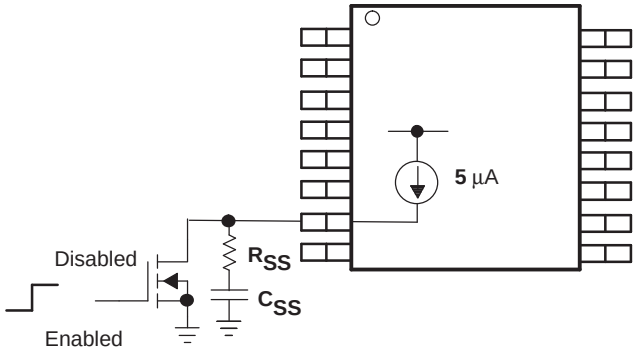


Figure 2. Interfacing to the ENA Pin

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Extending Slow-Start Time

In applications that use large values of output capacitance, there may be a need to extend the slow-start time to prevent the startup current from tripping the current limit. The current-limit circuit is designed to disable the high-side MOSFET and reset the internal voltage reference for a short amount of time when the high-side MOSFET current exceeds the current-limit threshold. If the output capacitance and load current cause the startup current to exceed the current-limit threshold, the power-supply output will not reach the desired output voltage. To extend the slow-start time and to reduce the startup current, an external resistor and capacitor can be added to the ENA pin. The slow-start capacitance is calculated using the following equation:

$$C_{SS}\,(\mu F) = 5.55 \times 10^{-3} \times n \times T_{ss}\,(ms)$$

Use n in Table 2. (4)

The R_{SS} resistor must be 2 kΩ and the slow-start capacitor must be less than 0.47 μF.

Switching Frequency (RT)

The TPS5435x has an internal oscillator that operates at twice the PWM switching frequency. The internal oscillator frequency is controlled by the RT pin. Grounding RT sets the PWM switching frequency to a default frequency of 250 kHz. Floating RT sets the PWM switching frequency to 500 kHz.

Connecting a resistor from RT to AGND sets the frequency according to the following equation (also see Figure 30).

$$RT\,(k\Omega) = \frac{46000}{f_S\,(kHz) - 35.9} \quad (5)$$

RT controls the SYNC pin functions. If RT is floating or grounded, SYNC is an output. If the switching frequency has been programmed using a resistor from RT to AGND, SYNC functions as an input.

The internal voltage-ramp charging current increases linearly with the set frequency and keeps the feed-forward modulator constant (Km = 8), regardless of the frequency set point.

Table 3.

SWITCHING FREQUENCY	SYNC PIN	RT PIN
250 kHz, internally set	Generates SYNC output signal	AGND
500 kHz, internally set	Generates SYNC output signal	Float
Externally set from 250 kHz to 700 kHz	Terminate to quiet ground with 10-kΩ resistor	R = 215 kΩ to 69 kΩ
Externally synchronized frequency	Synchronization signal	Set RT resistor equal to 90% to 110% of external synchronization frequency. When using a dual setup (see Figure 27 for example), if the master 35x device RT pin is left floating, use a 110-kΩ resistor to tie the slave RT pin to ground. Conversely, if the master 35x device RT pin is grounded, use a 237-kΩ resistor to tie the slave RT pin to ground.

180° Out-of-Phase Synchronization (SYNC)

The SYNC pin is configurable as an input or as an output, as noted in the previous section. When operating as an input, SYNC is a falling-edge-triggered signal (see Figure 3, Figure 4, and Figure 19). When operating as an output, the signal's falling edge is approximately 180° out of phase with the rising edge of the PH pins. Thus, two TPS5435x devices operating in a system can share an input capacitor and draw ripple current at twice the frequency of a single unit.

When operating the two TPS5435x devices 180° out of phase, the total RMS input current is reduced, thus, reducing the amount of input capacitance needed and increasing efficiency.

When synchronizing a TPS5435x to an external signal, the timing resistor on the RT pin must be set so that the oscillator is programmed to run at 90% to 110% of the synchronization frequency.

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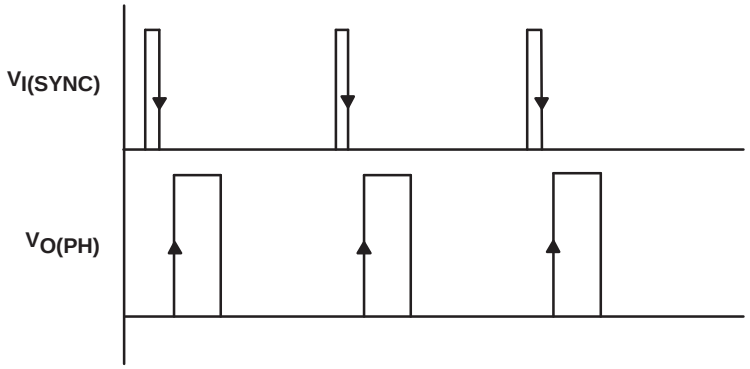


Figure 3. SYNC Input Waveform

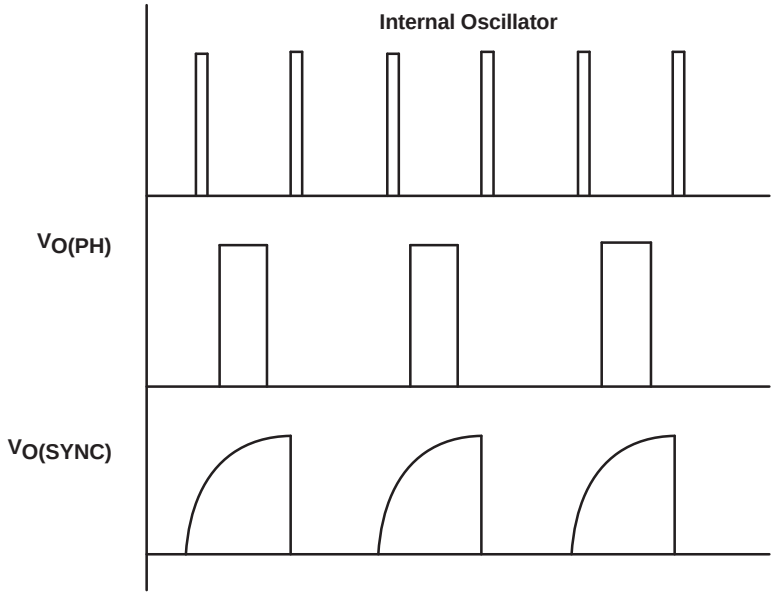


Figure 4. SYNC Output Waveform

Power Good (PWRGD)

The VSENSE pin is compared to an internal reference signal if the VSENSE is greater than 97% and no other faults are present. The PWRGD pin presents a high impedance. A low on PWRGD indicates a fault. PWRGD has been designed to provide a weak pulldown and indicates a fault even when the device is unpowered. If the TPS5435x has power and has any fault flag set, the TPS5435x indicates the power is not good by driving the PWRGD pin low. The following events, singly or in combination, indicate power is not good:

- VSENSE pin out of bounds
- Overcurrent
- Thermal shutdown
- UVLO undervoltage
- Input voltage not present (weak pulldown)
- Slow starting
- VBIAS voltage is low.

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Once the PWRGD pin presents a high impedance (i.e., power is good), a VSENSE pin out-of-bounds condition forces PWRGD low (i.e., power is bad) after a time delay. This time delay is a function of the switching frequency and is calculated using equation 6:

$$T_{delay} = \frac{1000}{f_S\,(kHz)}\ ms \quad (6)$$

Bias Voltage (VBIAS)

The VBIAS regulator provides a stable supply for the internal analog circuits and the low-side gate driver. Up to 1 mA of current can be drawn for use in an external application circuit. The VBIAS pin must have a bypass capacitor value of 1 μF. X7R- or X5R-grade dielectric ceramic capacitors are recommended because of their stable characteristics over temperature.

Bootstrap Voltage (BOOT)

The BOOT capacitor obtains its charge cycle by cycle from the VBIAS capacitor. A capacitor from the BOOT pin to the PH pins is required for operation. The bootstrap connection for the high-side driver must have a bypass capacitor of 0.1 μF.

Error Amplifier

The VSENSE pin is the error amplifier inverting input. The error amplifier is a true voltage amplifier, with 1.5 mA of drive capability with a minimum of 60 dB of open-loop voltage gain and a unity-gain bandwidth of 2 MHz.

Voltage Reference

The voltage-reference system produces a precision reference signal by scaling the output of a temperature-stable bandgap circuit. During production testing, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure improves the regulation, since it cancels offset errors in the scaling and error-amplifier circuits.

PWM Control and Feed Forward

Signals from the error-amplifier output, oscillator, and current-limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, PWM latch, and the adaptive dead-time control logic. During steady-state operation below the current-limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch.

Once the PWM latch is reset, the low-side driver and integrated pulldown MOSFET remain on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to the valley voltage. When the ramp begins to charge back up, the low-side driver turns off and the high-side FET turns on. The peak PWM ramp voltage varies inversely with input voltage to maintain a constant modulator and power-stage gain of 8 V.

As the PWM ramp voltage exceeds the error-amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side driver remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error-amplifier output can be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the internal low-side FET and driver on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set point, setting VSENSE to approximately the same voltage as the internal voltage reference. If the error-amplifier output is low, the PWM latch is reset continually and the high-side FET does not turn on. The internal low-side FET and low-side driver remain on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS5435x is capable of sinking current through the external low-side FET until the output voltage reaches the regulation set point.

The minimum on time is designed to be 180 ns. During the internal slow-start interval, the internal reference ramps from 0 V to 0.891 V. During the initial slow-start interval, the internal reference voltage is very small, resulting in skipped pulses because the minimum on time causes the actual output voltage to be slightly greater than the preset output voltage, until the internal reference ramps up.

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Deadtime Control

Adaptive dead-time control prevents shoot-through current from flowing in the integrated high-side MOSFET and the external low-side MOSFET during the switching transitions by actively controlling the turn-on times of the drivers. The high-side driver does not turn on until the voltage at the gate of the low-side MOSFET is below 1 V. The low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 1 V.

Low-Side Gate Driver (LSG)

LSG is the output of the low-side gate driver. The 100-mA MOSFET driver is capable of providing gate drive for most popular MOSFETs suitable for this application. Use the SWIFT Designer Software Tool to find the most appropriate MOSFET for the application. Connect the LSG pin directly to the gate of the low-side MOSFET. Do not use a gate resistor, as the resulting turn-on time may be too slow.

Integrated Pulldown MOSFET

The TPS5435x has a diode-MOSFET pair from PH to PGND. The integrated MOSFET is designed for light-load continuous-conduction-mode operation when only an external Schottky diode is used. The combination of devices keeps the inductor current continuous under conditions where the load current drops below the inductor's critical current. Care should be taken in the selection of inductor in applications using only a low-side Schottky diode. Since the inductor ripple current flows through the integrated low-side MOSFET at light loads, the inductance value should be selected to limit the peak current to less than 0.3 A during the high-side FET turn-off time. The minimum value of inductance is calculated using the following equation:

$$L(H) = \frac{VO \times \left(1 - \frac{VO}{VI}\right)}{f_S \times 0.6} \quad (7)$$

Thermal Shutdown

The device uses the thermal shutdown to turn off the MOSFET drivers and controller if the junction temperature exceeds 165°C. The device is restarted automatically when the junction temperature decreases to 7°C below the thermal shutdown trip point and starts up under control of the slow-start circuit.

Overcurrent Protection

Overcurrent protection is implemented by sensing the drain-to-source voltage across the high-side MOSFET and compared to a voltage level that represents the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit for more than 100 ns, the ENA pin is pulled low, the high-side MOSFET is disabled, and the internal digital slow-start is reset to 0 V. ENA is held low for approximately the time that is calculated by the following equation:

$$T_{HICCUP}\,(ms) = \frac{2250}{f_S\,(kHz)} \quad (8)$$

Once the hiccup time is complete, ENA is released and the converter initiates the internal slow start.

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TYPICAL CHARACTERISTICS

Conditions are V_I = 12 V, V_O = 3.3 V, f_s = 500 kHz, I_O = 3 A, T_A = 25°C (unless otherwise noted).

MEASURED LOOP RESPONSE

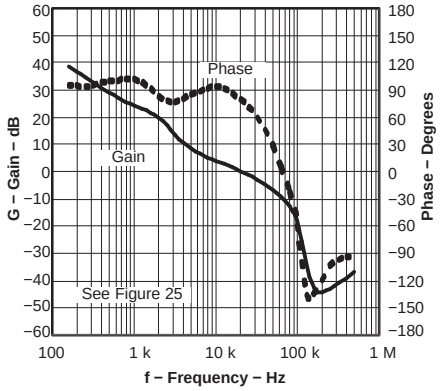


Figure 1

LOAD REGULATION

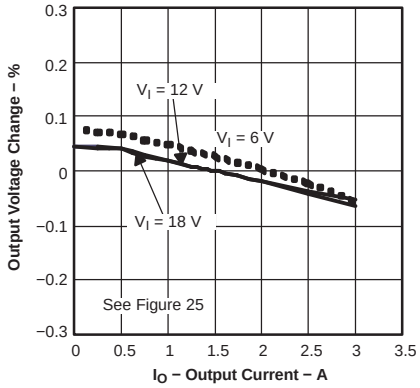


Figure 6.

LINE REGULATION

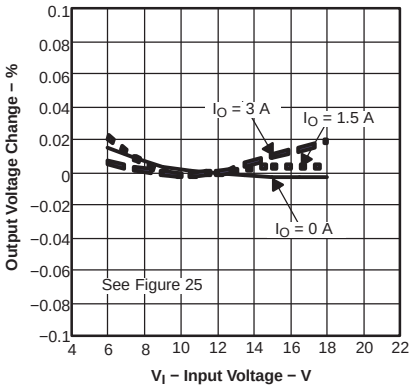


Figure 7.

EFFICIENCY vs OUTPUT CURRENT

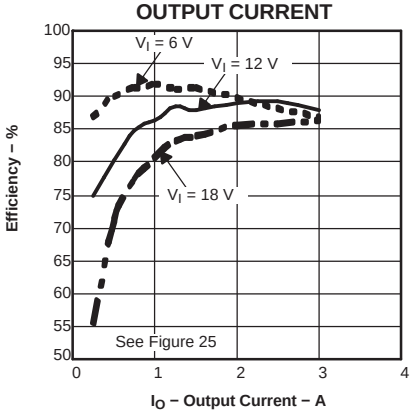


Figure 8.

INPUT RIPPLE VOLTAGE

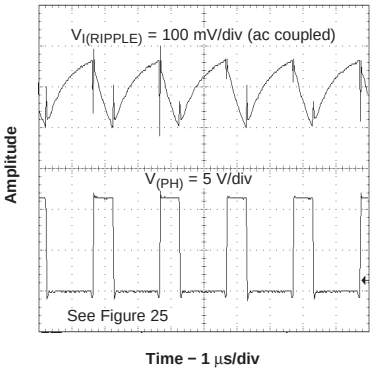


Figure 9.

OUTPUT RIPPLE VOLTAGE

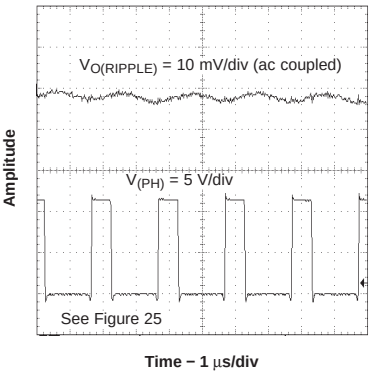


Figure 10.

GATE DRIVE VOLTAGE

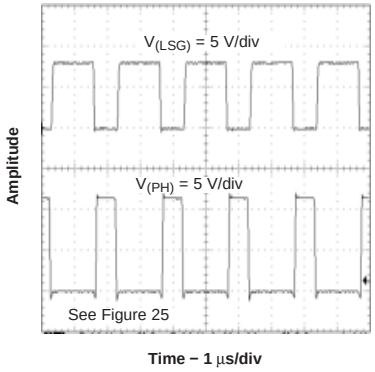


Figure 11.

LOAD TRANSIENT RESPONSE

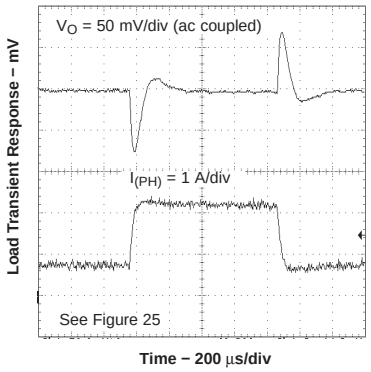


Figure 12.

POWER UP

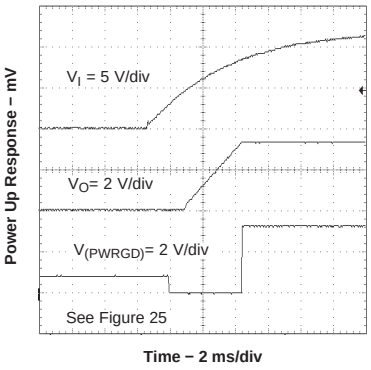


Figure 13.

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TYPICAL CHARACTERISTICS (continued)

Conditions are V_I = 12 V, V_O = 3.3 V, f_s = 500 kHz, I_O = 3 A, T_A = 25°C (unless otherwise noted).

POWER DOWN

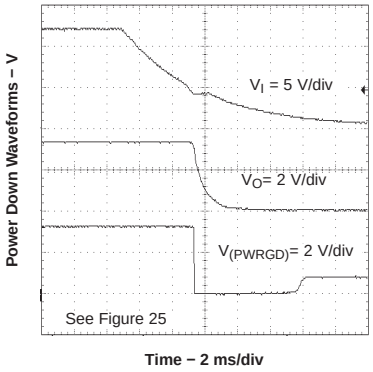


Figure 14.

EFFICIENCY VS OUTPUT CURRENT

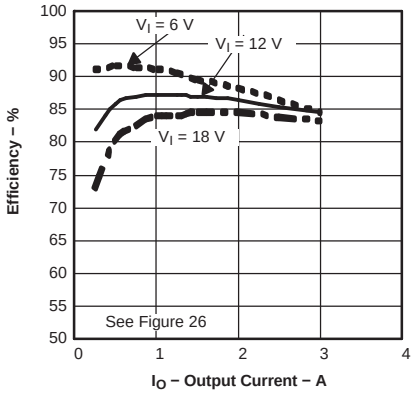


Figure 15.

CONTINUOUS CONDUCTION MODE

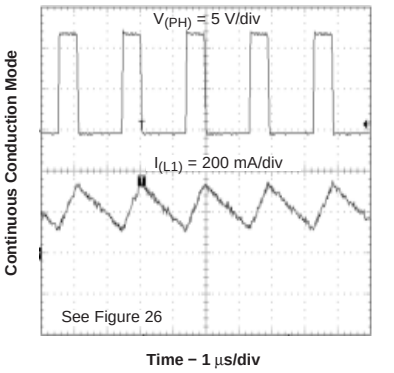


Figure 16.

LIGHT LOAD CONDUCTION

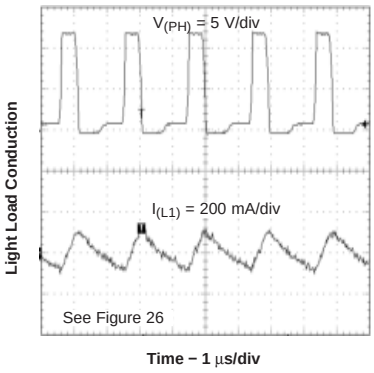


Figure 17.

SEQUENCING WAVEFORMS

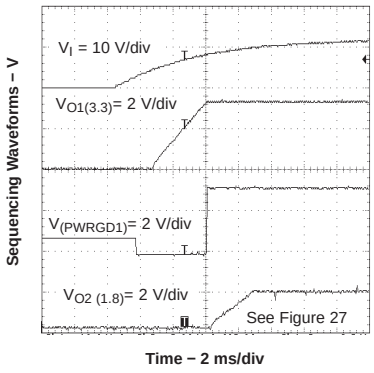


Figure 18.

INPUT RIPPLE CANCELLATION

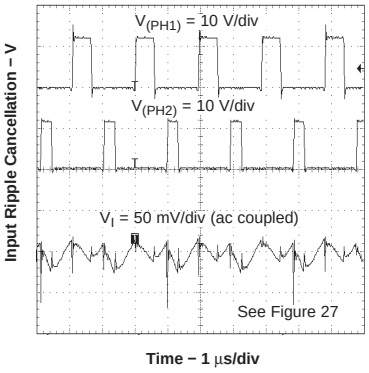


Figure 19.

MEASURED LOOP RESPONSE 100-µF POSCAP

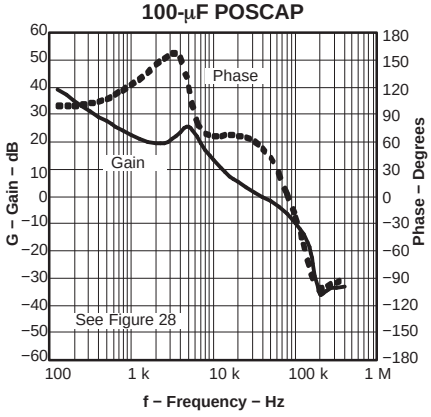


Figure 20.

MEASURED LOOP RESPONSE 2 × 180-µF SP CAPACITORS

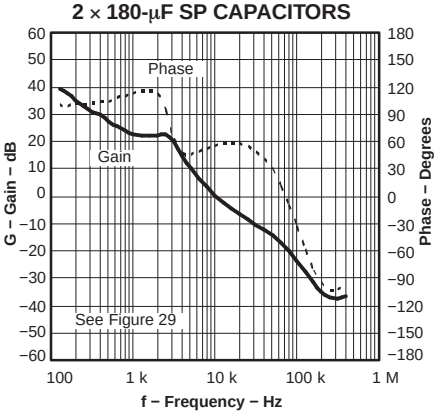


Figure 21.

MEASURED LOOP RESPONSE 330-µF OSCON

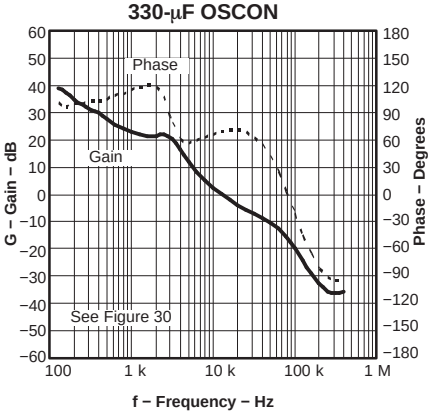


Figure 22.

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LAYOUT INFORMATION

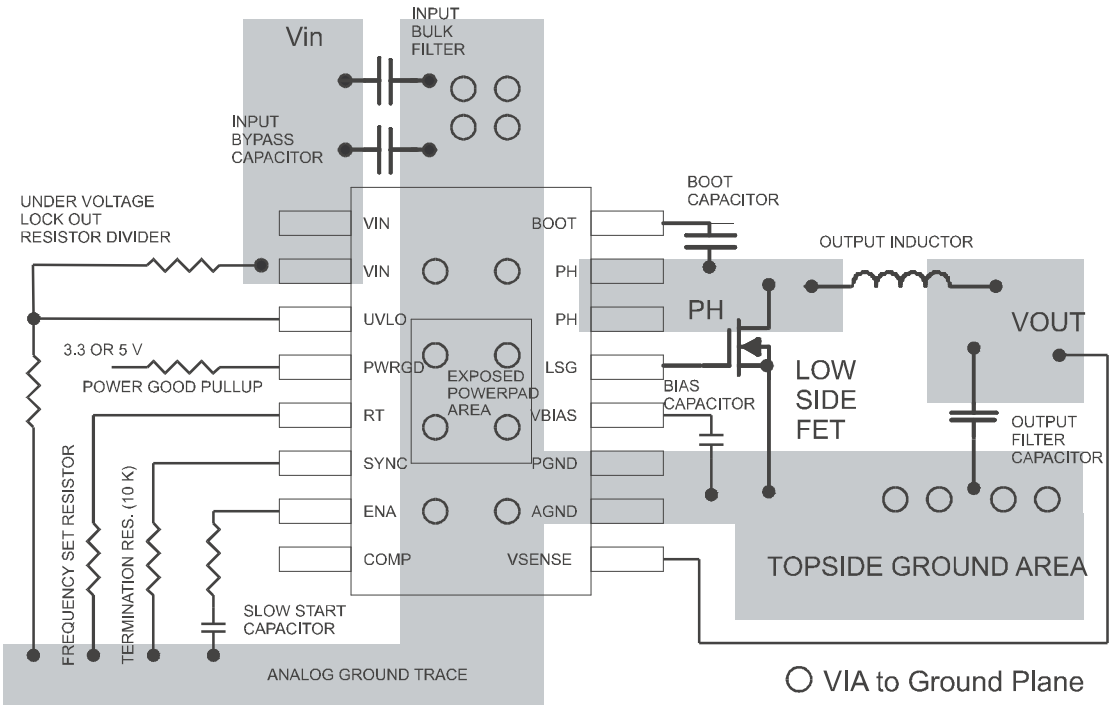


Figure 23. TPS5435x PCB Layout

PCB Layout

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low-ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS5435x ground pins. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric, and the optimum placement is closest to the VIN pins and the AGND and PGND pins. See Figure 23 for an example of a board layout. The AGND and PGND pins should be tied to the PCB ground plane at the pins of the IC. The source of the low-side MOSFET and the anode of the Schottky diode should be connected directly to the PCB ground plane. The PH pins should be tied together and routed to the drain of the low-side MOSFET or to the cathode of the external Schottky diode. Since the PH connection is the switching node, the MOSFET (or diode) should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The recommended conductor width from pins 14 and 15 is 0.050 in to 0.075 in of 1-oz copper. The length of the copper land pattern should be no more than 0.2 in.

For operation at full-rated load, the analog ground plane must provide adequate heat dissipating area. A 3-in × 3-in plane of copper is recommended, though not mandatory, dependent on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD package should be connected to the largest area available. Additional areas on the bottom or top layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD package to the analog ground-plane layer should be made using 0.013-in diameter vias to avoid solder wicking through the vias. Four vias should be in the PowerPAD area, with four additional vias outside the pad area and underneath the package. Additional vias beyond those recommended to enhance thermal performance should be included in areas not under the device package.

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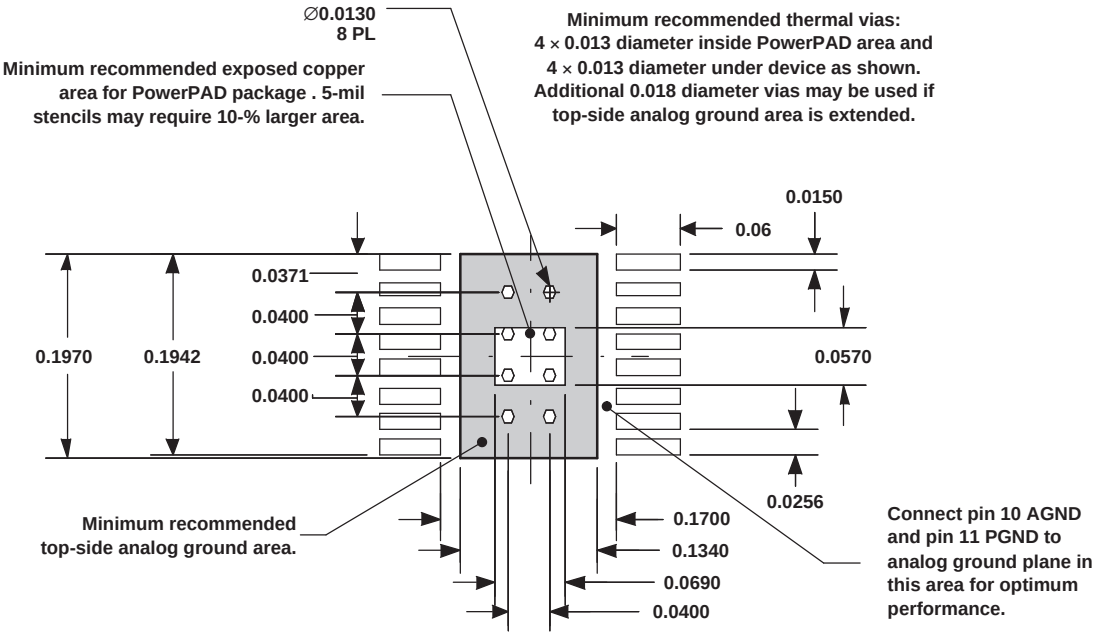


Figure 24. Thermal Considerations for PowerPAD™ Layout

APPLICATION INFORMATION

Figure 25 shows the schematic for a typical TPS54356 application. The TPS54356 can provide up to 3-A output current at a nominal output voltage of 3.3 V. For proper thermal performance, the exposed PowerPAD package underneath the device must be soldered down to the printed circuit board.

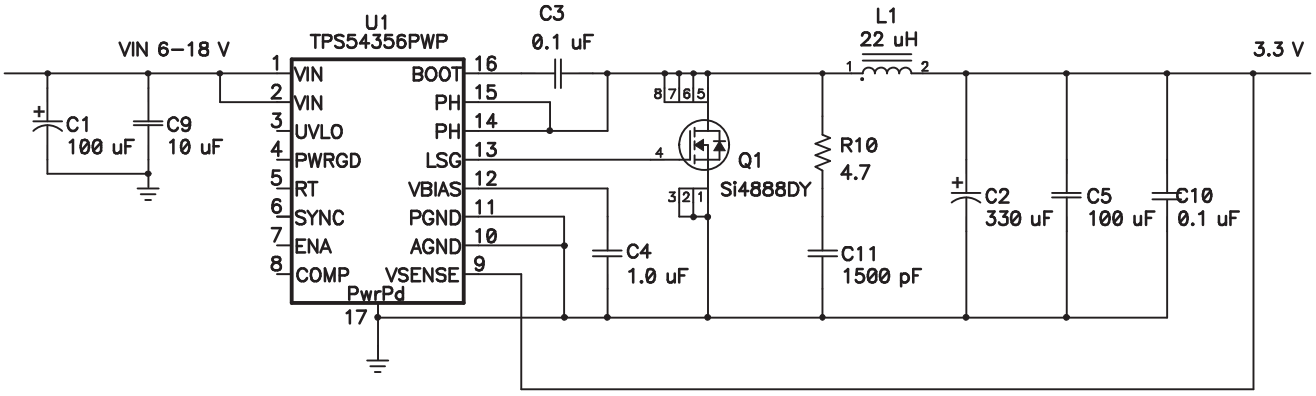


Figure 25. Application Circuit, 12 V to 3.3 V

Design Procedure

The following design procedure can be used to select component values for the TPS54356. Alternately, the SWIFT Designer Software may be used to generate a complete design. The SWIFT Designer Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

To begin the design process, a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

For this design example, use the following as the input parameters:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	6 V to 18 V
Output voltage	3.3 V
Input ripple voltage	300 mV
Output ripple voltage	10 mV
Output current rating	3 A
Operating frequency	500 kHz

Switching Frequency

The switching frequency is set using the RT pin. Grounding RT sets the PWM switching frequency to a default frequency of 250 kHz. Floating RT sets the PWM switching frequency to 500 kHz. By connecting a resistor from RT to AGND, any frequency in the range of 250 kHz to 700 kHz can be set. Use equation 9 to determine the proper value of RT.

$$\text{RT}\ (\text{k}\Omega) = \frac{46000}{f_S\ (\text{kHz}) - 35.9} \tag{9}$$

In this example circuit, RT is not connected and the switching frequency is set at 500 kHz.

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Input Capacitors

The TPS54356 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum value for the decoupling capacitor, C9, is 10 μF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. Additionally, some bulk capacitance may be needed, especially if the TPS54356 circuit is not located within about 2 in from the input voltage source. The value for this capacitor is not critical, but it also should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

This input ripple voltage can be approximated by equation 10:

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + (I_{OUT(MAX)} \times ESR_{(MAX)}) \quad (10)$$

Where:

$I_{OUT(MAX)}$ = Maximum load current

f_{SW}= Switching frequency

C_{BULK} = Bulk capacitor value

and ESR_{MAX} = Maximum series resistance of the bulk capacitor

The maximum RMS ripple current also needs to be checked. For worst-case conditions, this can be approximated by equation 11:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (11)$$

In this case, the input ripple voltage is 140 mV and the RMS ripple current is 1.5 A. The maximum voltage across the input capacitors is VIN max plus delta VIN/2. The chosen bulk and bypass capacitors are each rated for 25 V and the combined ripple current capacity is greater than 3 A, both providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Output Filter Components

Inductor Selection

To calculate the minimum value of the output inductor, use equation 12:

$$L_{(MIN)} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{sw}} \quad (12)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. For designs using low ESR output capacitors such as ceramics, use K_{IND} = 0.3. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.1 to keep the inductor ripple current small. The minimum inductor value is calculated to be 17.96 μH. The next-highest standard value is 22 μH, which is used in this design.

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be derived from equation 13:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{sw} \times 0.8}\right)^2} \quad (13)$$

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and the peak inductor current can be determined using equation 14:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times f_{sw}} \quad (14)$$

For this design, the RMS inductor current is 3.007 A and the peak inductor current is 3.15 A. The chosen inductor is a Coiltronics DR127-220 22 µH. It has a saturation current rating of 7.57 A and a RMS current rating of 4 A, easily meeting these requirements. A lesser-rated inductor could be used if less margin is desired. In general, inductor values for use with the TPS54356 are in the range of 6.8 µH to 47 µH.

Capacitor Requirements

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because, along with the inductor current, it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist.

Consider the relationship between the desired closed-loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed-loop crossover frequency at less than one-fifth of the switching frequency. With high switching frequencies such as the 500-kHz frequency of this design, internal circuit limitations of the TPS54356 limit the practical maximum crossover frequency to about 70 kHz. Additionally, the capacitor type and value must be chosen to work with the internal compensation network of the TPS5435x family of dc/dc converters. To allow for adequate phase gain in the compensation network, the LC corner frequency should be approximately one decade or so below the closed-loop crossover frequency. This limits the minimum capacitor value for the output filter to:

$$C_{OUT(MIN)} = \frac{1}{L_{OUT}} \times \left(\frac{K}{2\pi f_{CO}}\right)^2 \quad (15)$$

Where K is the frequency multiplier for the spread between f_{LC} and f_{CO}. K should be between 5 and 15, typically 10, for one decade difference. For a desired crossover of 20 kHz and a 22-µH inductor, the minimum value for the output capacitor is 288 µF. The selected output capacitor must be rated for a voltage greater than the desired output voltage, plus one-half the ripple voltage. Any derating amount also must be included. The maximum RMS ripple current in the output capacitor is given by equation 16:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{sw}}\right) \quad (16)$$

The calculated RMS ripple current is 156 mA in the output capacitors.

Choosing Capacitor Value

For this design example, a relatively large aluminum electrolytic capacitor is combined with a smaller-value ceramic capacitor. This combination provides a stable high-performance design at a relatively low cost. Also, by carefully choosing the capacitor values and ESRs, the design can be tailored to complement the internal compensation poles and zeros of the TPS54356.

These preconfigured poles and zeroes, internal to the TPS54356, limit the range of output filter configurations. A variety of capacitor values and types of dielectric are supported. There are a number of different ways to calculate the output filter capacitor value and ESR to work with the internal compensation network. This procedure outlines a relatively simple procedure that produces good results with an output filter consisting of a high-ESR dielectric capacitor in parallel with a low-ESR ceramic capacitor. SWIFT Designer Software is used for designs with unusually high closed-loop crossover frequencies, low value, low-ESR output capacitors such as ceramics, or if the designer is unsure about the design procedure.

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The TPS54356 contains a compensation network with the following nominal characteristics:

f_{INT} = 1.7 kHz

f_{Z1} = 2.5 kHz

f_{Z2} = 4.8 kHz

f_{P1} = 95 kHz

f_{P2} = 125 kHz

For a stable design, the closed-loop crossover frequency should be set less than one-fifth of the switching frequency, and the phase margin at crossover must be greater than 45 degrees. The general procedure outlined here produces results consistent with these requirements, without going into great detail about the theory of loop compensation.

In this case, the output filter LC corner frequency should be selected to be near the first compensation zero frequency, as described by equation 17:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT}C2}} \cong f_{Z1} \tag{17}$$

Placement of the LC corner frequency at f_{Z1} is not critical; it only needs to be close. For the design example, f_{LC} = 2 kHz.

Solving for C2 using equation 18:

$$C2 \cong \frac{1}{4\pi^2 f^2_{Z1} L_{OUT}} \tag{18}$$

The desired value for C2 is calculated as 184 µF. A close standard value of 330 µF is chosen, with a resulting LC corner frequency of 1.9 kHz. As shown, this value is not critical as long as it results in a corner frequency in the vicinity of f_{Z1}.

Next, when using a large ceramic capacitor in parallel with a high-ESR electrolytic capacitor, there is a pole in the output filter that should be at f_{Z2}, as shown in equation 19:

$$f_{P(ESR)} = \frac{1}{2\pi R_{(C2ESR)}C5} = f_{Z2} \tag{19}$$

Now, the actual C2 capacitor must be selected based on the ESR and the value of capacitor C5, so that the above equation is satisfied. In this example, the $R_{(C2ESR)}C5$ product should be 3.18×10^{-5}. From the available capacitors, by choosing a Panasonic EEVFKOJ331XP aluminum electrolytic capacitor with a nominal ESR of 0.34 Ω yields a calculated value for C5 of 98 µF. The closest standard value is 100 µF. As the actual ESR of the capacitor can vary by a large amount, this value also is not critical.

The closed-loop crossover frequency should be greater than f_{LC} and less than one-fifth of the switching frequency. Also, the crossover frequency should not exceed 70 kHz, as the error amplifier may not provide the desired gain. As stated previously, closed loop-crossover frequencies between 5 and 15 times f_{LC} work well. For this design, the crossover frequency can be estimated by:

$$f_{CO} = 1.125 \times 10^{-3} \times f_{P(ESR)} \times f_{LC} \tag{20}$$

This simplified equation is valid for this design because the output filter capacitors are mixed technology. Compare this result to the actual measured loop response plot of Figure 5. The measured closed-loop crossover frequency of 19.95 kHz differs from the calculated value because the actual output filter capacitor component parameters differed slightly from the specified data-sheet values.

Capacitor ESR and Output Ripple

The amount of output ripple voltage, as specified in the initial design parameters, is determined by the maximum ESR of the output capacitor and the input ripple current. The output ripple voltage is the inductor ripple current times the ESR of the output filter, so the maximum specified ESR as listed in the capacitor data sheet is given by equation 21:

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$$ESR_{(MAX)} = \left(\frac{V_{IN(MAX)} \times L_{OUT} \times f_{sw} \times 0.8}{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)} \right) \times \Delta V_{p-p(MAX)} \quad (21)$$

and the maximum ESR required is 33 mΩ. In this design, the aluminum electrolytic capacitor has an ESR of 0.340 mΩ, but it is in parallel with an ultra-low ESR ceramic capacitor of 2 mΩ maximum. The measured output ripple voltage for this design is approximately 4 mV_{p-p}, as shown in Figure 10.

Bias AND Bootstrap Capacitors

Every TPS54356 design requires a bootstrap capacitor, C3, and a bias capacitor, C4. The bootstrap capacitor must be 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT pin. The bias capacitor is connected between the VBIAS pin and AGND. The value should be 1 µF. Both capacitors should be high-quality ceramic types with X7R or X5R grade dielectric for temperature stability. They should be placed as close to the device connection pins as possible.

Low-Side FET

The TPS54356 is designed to operate using an external low-side FET, and the LSG pin provides the gate drive output. Connect the drain to the PH pin, the source to PGND, and the gate to LSG. The TPS54356 gate drive circuitry is designed to accommodate most common n-channel FETs that are suitable for this application. The SWIFT Designer Software can be used to calculate all the design parameters for low-side FET selection. There are some simplified guidelines that can be applied that produce an acceptable solution in most designs.

The selected FET must meet the absolute maximum ratings for the application:

- Drain-source voltage (VDSS) must be higher than the maximum voltage at the PH pin, which is V_{INMAX} + 0.5 V.
- Gate-source voltage (VGSS) must be greater than 8 V.
- Drain current (Id) must be greater than 1.1 × I_{OUTMAX}.
- Drain-source on resistance (RDSON) should be as small as possible; less than 30 mΩ is desirable. Lower values for RDSON result in designs with higher efficiencies. It is important to note that the low-side FET on time typically is longer than the high-side FET on time, so attention paid to low-side FET parameters can make a marked improvement in overall efficiency.
- Total gate charge (Q_g) must be less than 50 nC. Again, lower Q_g characteristics result in higher efficiencies.
- Additionally, check that the device chosen is capable of dissipating the power losses.

For this design, a Fairchild FDR6674A 30-V n-channel MOSFET is used as the low-side FET. This particular FET is designed specifically to be used as a low-side synchronous rectifier.

Power Good

The TPS54356 is provided with a power-good (PWRGD) output pin. This output is an open-drain output and is intended to be pulled up to a 3.3-V or 5-V logic supply. A 10-kΩ pullup resistor works well in this application. The absolute maximum voltage is 6 V, so care must be taken not to connect this pullup resistor to VIN if the maximum input voltage exceeds 6 V.

Snubber Circuit

R10 and C11 of the application schematic in Figure 25 comprise a snubber circuit. The snubber is included to reduce overshoot and ringing on the phase node when the internal high-side FET turns on. Since the frequency and amplitude of the ringing depends to a large degree on parasitic effects, it is best to choose these component values, based on actual measurements of any design layout. See literature number SLUP100 for more detailed information on snubber design.

Figure 26 shows an application where a clamp diode is used in place of the low-side FET. The TPS54352-7 incorporates an integrated pulldown FET so that the circuit remains operating in continuous mode during light load operation. A 3-A 40-V Schottky diode, such as the Motorola MBRS340T3 or equivalent, is recommended. See Figure 15, Figure 16, and Figure 17 for efficiency data and switching waveforms for this circuit.

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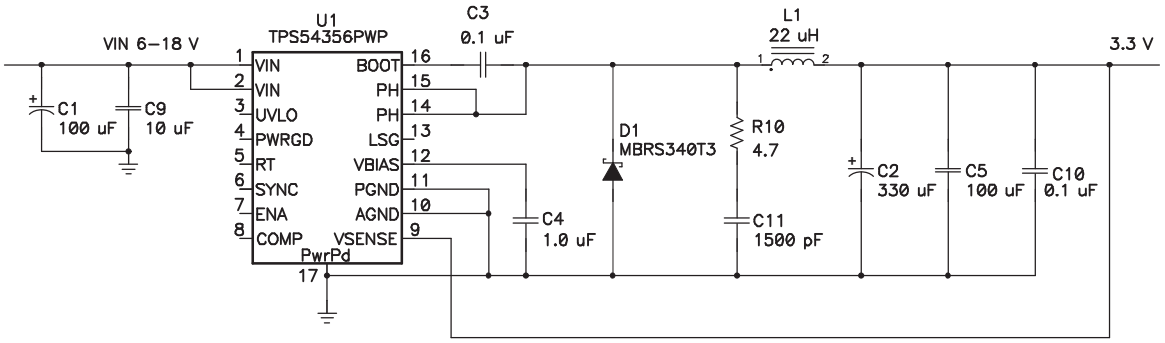


Figure 26. Power Supply With Schottky Diode

Figure 27 is an example of power-supply sequencing using a TPS54356 (U1) to generate an output of 3.3 V, and a TPS54354 (U2) to generate a 1.8-V output. These output voltages are typical I/O and core voltages for microprocessors and FPGAs. In the circuit, the 3.3-V supply is designed to power up first.

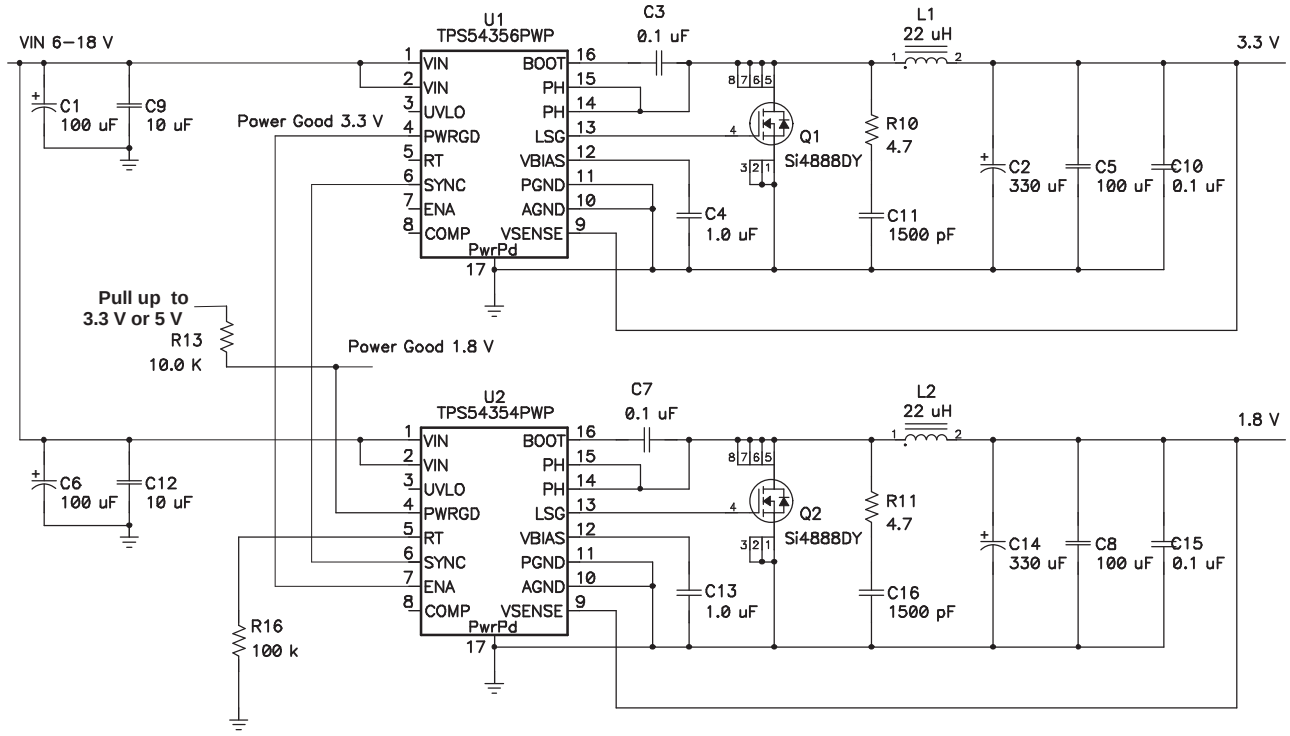


Figure 27. Power Supply With Sequencing

The PWRGD pin of U1 is tied to the ENA pin of U2 so that the 1.8-V supply starts to ramp up after the 3.3-V supply is within regulation. Figure 18 shows these start-up sequence waveforms.

Since the RT pin of U1 is floating, the SYNC pin is an output. This synchronization signal is fed the SYNC pin of U2. RT of U2 has a 110-kΩ resistor to ground, and SYNC for this device acts as an input. The 1.8-V supply operates synchronously with the 3.3-V supply, and their switching node rising edges are approximately 180 degrees out of phase, allowing for a reduction in the input voltage ripple. See Figure 19 for this waveform.

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Alternate Output Filter Designs

The previous design procedure example demonstrated a technique to design a 3.3-V power supply using both aluminum electrolytic and ceramic output filter capacitors. Other types of output filter capacitors are supported by the TPS5435x family of dc/dc converters. Figure 26, Figure 27, and Figure 28 show designs using other popular capacitor types.

In Figure 28, the TPS54356 is shown with a single 100-µF 6-V POSCAP as the output filter capacitor. C10 is a high-frequency bypass capacitor and does not enter into the design equations. The design procedure is similar to the previous example, except in the design of the output filter. In the previous example, the output filter LC corner was set at the first zero in the compensation network, while the second compensation zero was used to counteract the output filter pole caused by the interaction of the C2 capacitor ESR with C5. In this design example, the output LC corner frequency is to be set at the second zero frequency (f_{Z2}) of the internal compensation network, approximately 5 kHz, while the first zero is used to provide phase boost prior to the LC corner frequency.

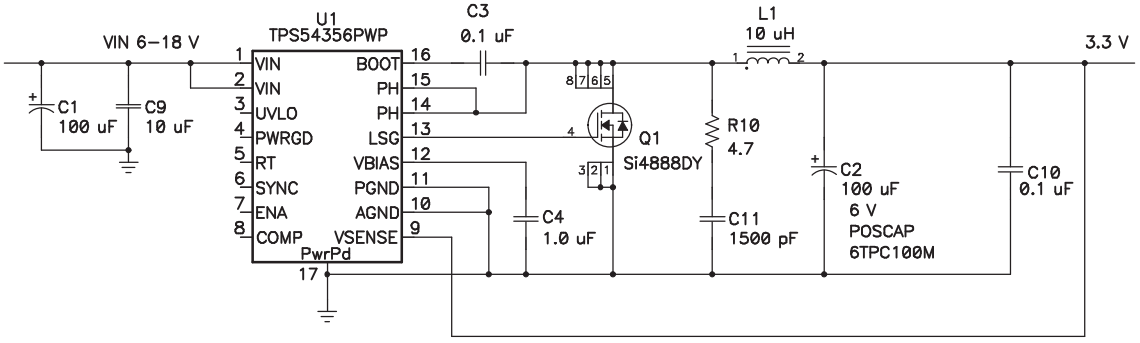


Figure 28. 3.3-V Power Supply With Sanyo POSCAP Output Filter Capacitor

Inductor Selection

Using equation 12 and a K_{IND} 0.2, the minimum inductor value required is 8.98 µH. The closest standard value, 10 µH, is selected. RMS and peak inductor currents are the same as calculated previously.

Capacitor Selection

With the inductor set at 10 µH and a desired corner frequency of 5 kHz, the output capacitor value is given by:

$$C2 = \frac{1}{4\pi^2 f_{z2}^2 L_{out}} = \frac{1}{4 \times \pi^2 \times 5000^2 \times 10^{-5}} = 101\ \mu F$$

Use 100 µF as the closest standard value.

Calculating the RMS ripple current in the output capacitor using equation 16 yields 156 mA. The POSCAP 6TPC100M capacitor selected is rated for 1700 mA. See the closed-loop response curve for this design in Figure 20.

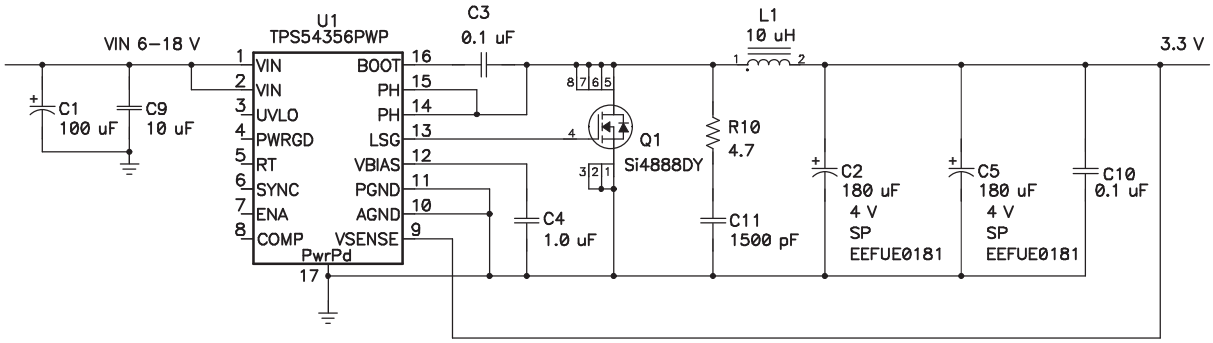


Figure 29. 3.3-V Power Supply With Panasonic SP Output Filter Capacitors

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In Figure 29, the TPS54356 is shown with two 180-mF 4-V special polymer dielectric output filter capacitors (C2 and C5). C10 is a high-frequency bypass capacitor and does not enter into the design equations. In the previous example, the output LC corner frequency is to be set at the second zero frequency f_{Z2} of the internal compensation network, approximately 5 kHz, while the first zero is used to provide phase boost prior to the LC corner frequency. The special polymer electrolytic capacitors used in this design require that the closed-loop crossover frequency be lowered due to the significantly lower ESR of this type of capacitor.

Inductor Selection

The inductor is the same 10-µH value as the previous example.

Capacitor Selection

To lower the closed-loop crossover, it is necessary to reduce the LC corner frequency below 5 kHz. Using a target value of 2500 Hz, the output capacitor value is given by:

$$C2 = \frac{1}{4\pi^2 f_{Z2}^2 L_{out}} = \frac{1}{4 \times \pi^2 \times 2500^2 \times 10^{-5}} = 405\ \mu F$$

Use 2 × 180 µF = 360 µF as a combination of standard values that is close to 405 µF.

The RMS ripple current in the output capacitor is the same as before. The selected capacitors are each 3.3 A. See the closed-loop response curve for this design in Figure 21.

In Figure 30, the TPS54356 is shown with a Sanyo OSCON output filter capacitor (C2). C10 is a high-frequency bypass capacitor and does not enter into the design equations. This design is identical to the previous example, except that a single OSCON capacitor of 330 µF is used for the calculated value of 405 µF. Compare the closed-loop response for this design in Figure 22 to the closed-loop response in Figure 21. Note that there is only a slight difference in the response and the general similarity in both the gain and phase plots. This is the expected result for these two similar output filters.

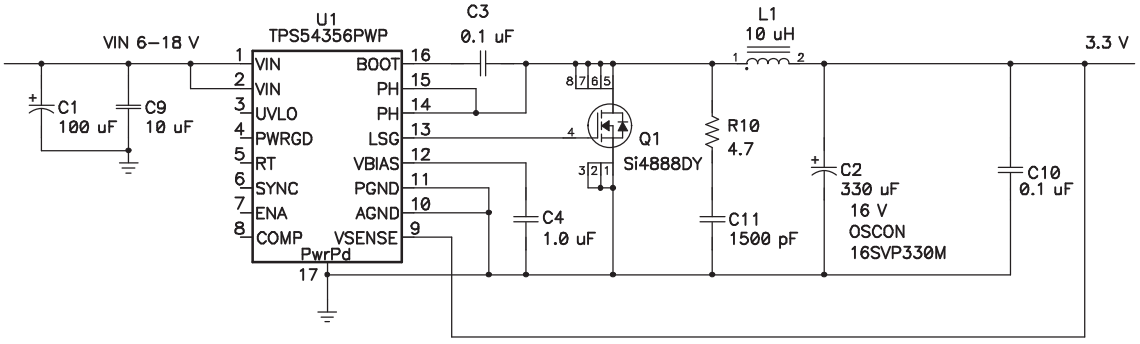


Figure 30. 3.3-V Power Supply With Sanyo OSCON Output Filter Capacitor

Many other additional output filter designs are possible. Use the SWIFT Designer Software to generate other designs or follow the general design procedures illustrated in this application section.

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MAXIMUM SWITCHING FREQUENCY
vs
INPUT VOLTAGE

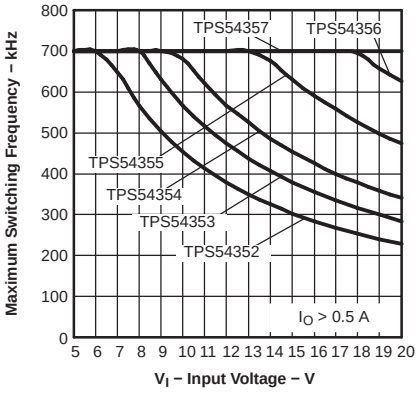


Figure 31.

RT RESISTANCE
vs
SWITCHING FREQUENCY

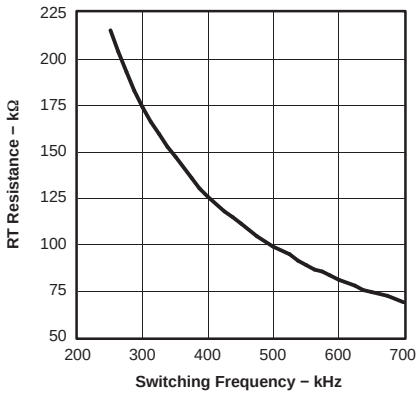


Figure 32.

VIN(UVLO) START AND STOP
vs
FREE-AIR TEMPERATURE

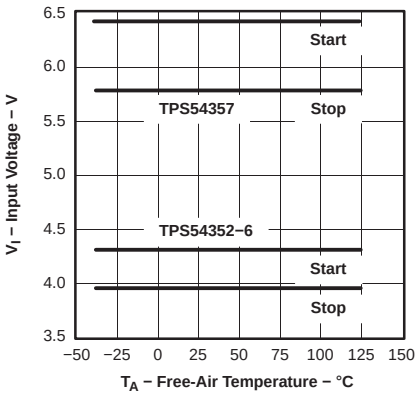


Figure 33.

ENABLED SUPPLY CURRENT
vs
INPUT VOLTAGE

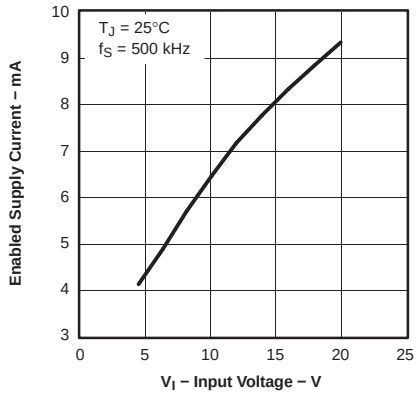


Figure 34.

DISABLED SUPPLY CURRENT
vs
INPUT VOLTAGE

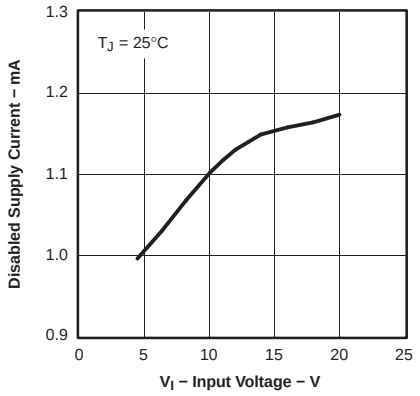


Figure 35.

BIAS VOLTAGE
vs
INPUT VOLTAGE

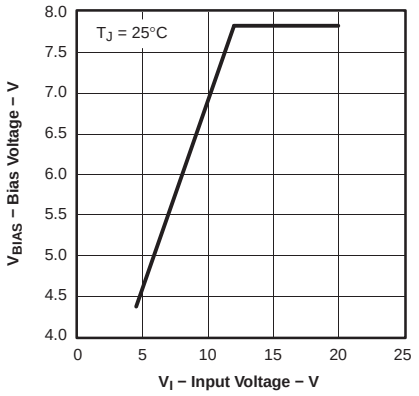


Figure 36.

POWER-GOOD THRESHOLD
vs
JUNCTION TEMPERATURE

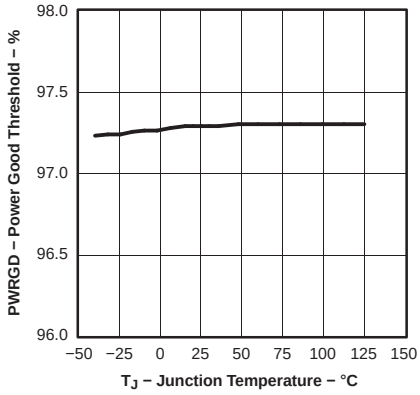


Figure 37.

INTERNAL VOLTAGE REFERENCE
vs
JUNCTION TEMPERATURE

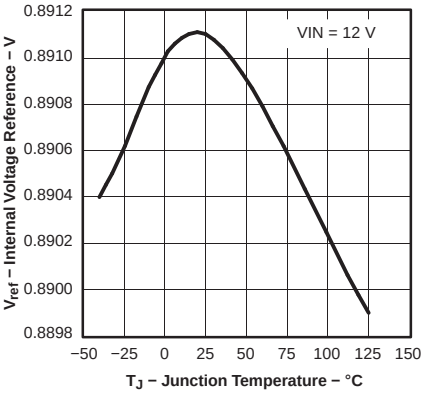


Figure 38.

CURRENT LIMIT
vs
INPUT VOLTAGE

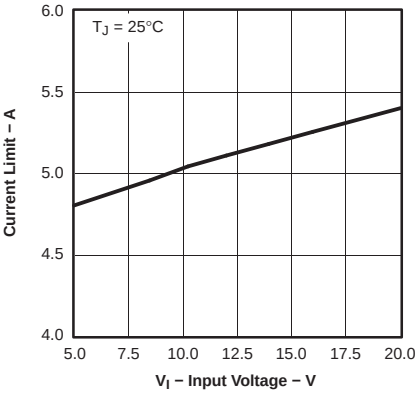


Figure 39.

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ON RESISTANCE
vs
JUNCTION TEMPERATURE

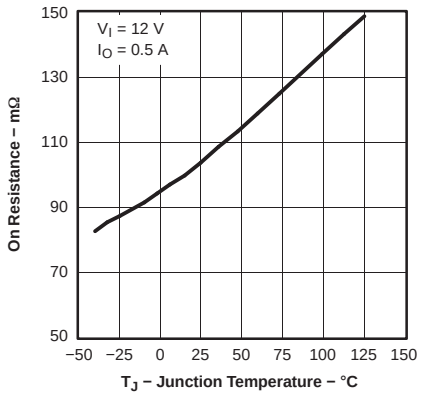


Figure 40.

PH VOLTAGE
vs
SINK CURRENT

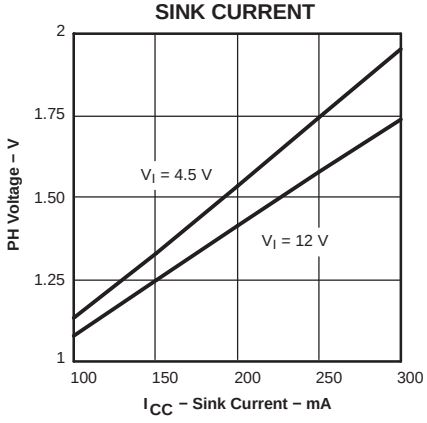


Figure 41.

SLOW-START CAPACITANCE
vs
TIME

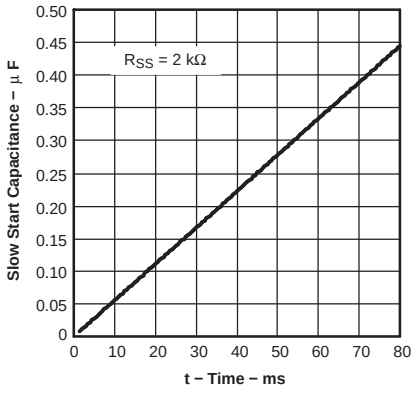


Figure 42.

POWER-GOOD DELAY
vs
SWITCHING FREQUENCY

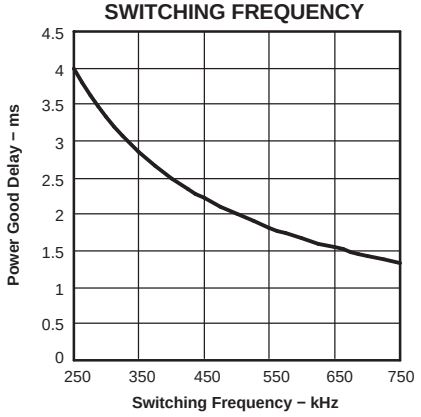


Figure 43.

HICCUP TIME
vs
SWITCHING FREQUENCY

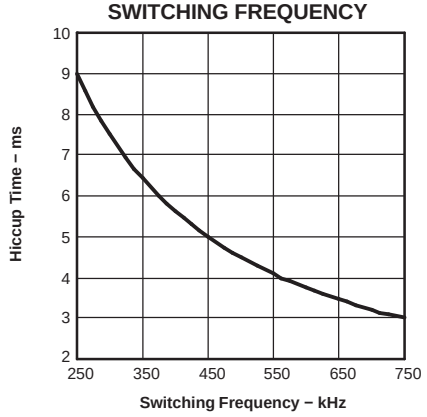


Figure 44.

INTERNAL SLOW START TIME
vs
SWITCHING FREQUENCY

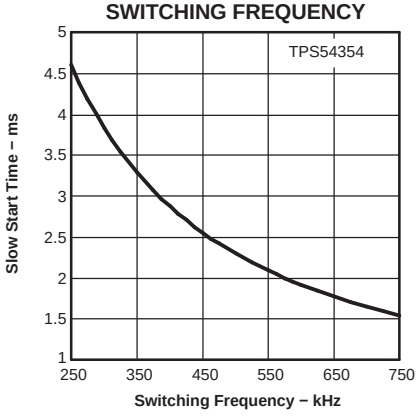


Figure 45.

FREE-AIR TEMPERATURE
vs
MAXIMUM OUTPUT CURRENT

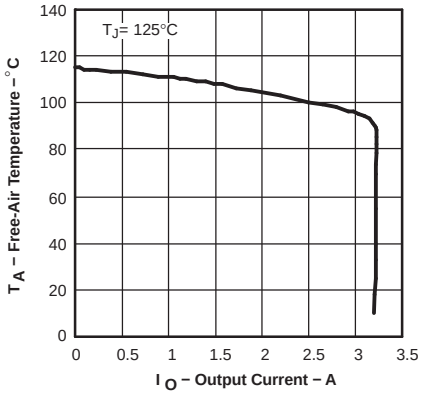


Figure 46.

MAXIMUM OUTPUT VOLTAGE
vs
INPUT VOLTAGE

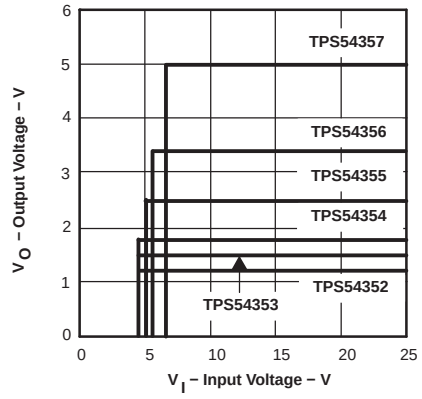


Figure 47.

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

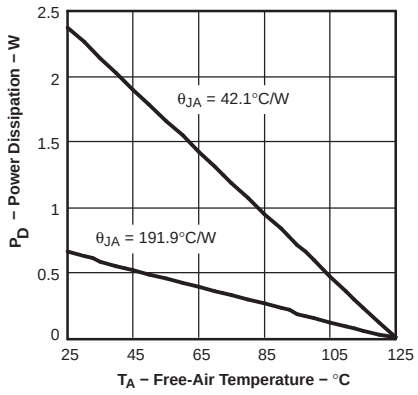
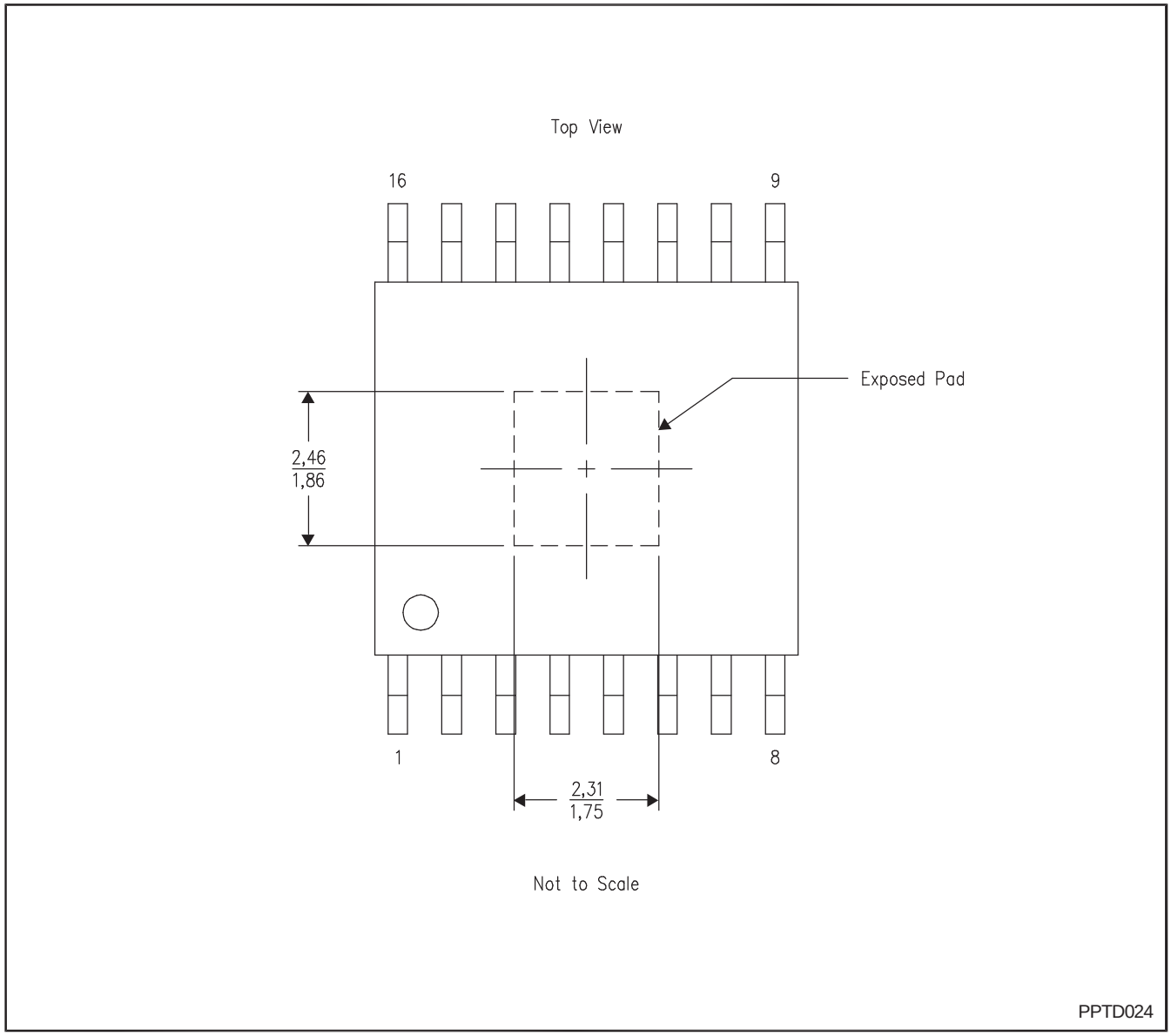


Figure 48.

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THERMAL PAD MECHANICAL DATA

PWP (R-PDSO-G16) **PowerPAD™ PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54354MPWPREP	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PMDM
TPS54354MPWPREP.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	PMDM
TPS54356MPWPREP	Obsolete	Production	HTSSOP (PWP) | 16	-	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54354-EP, TPS54356-EP :

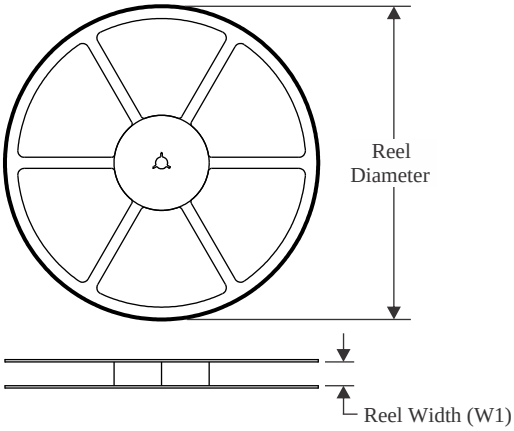
- Catalog : TPS54354, TPS54356

NOTE: Qualified Version Definitions:

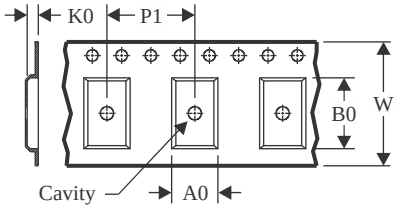
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

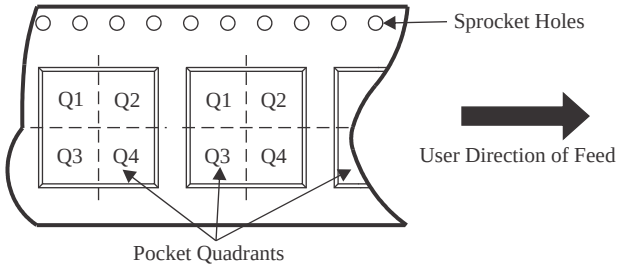


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

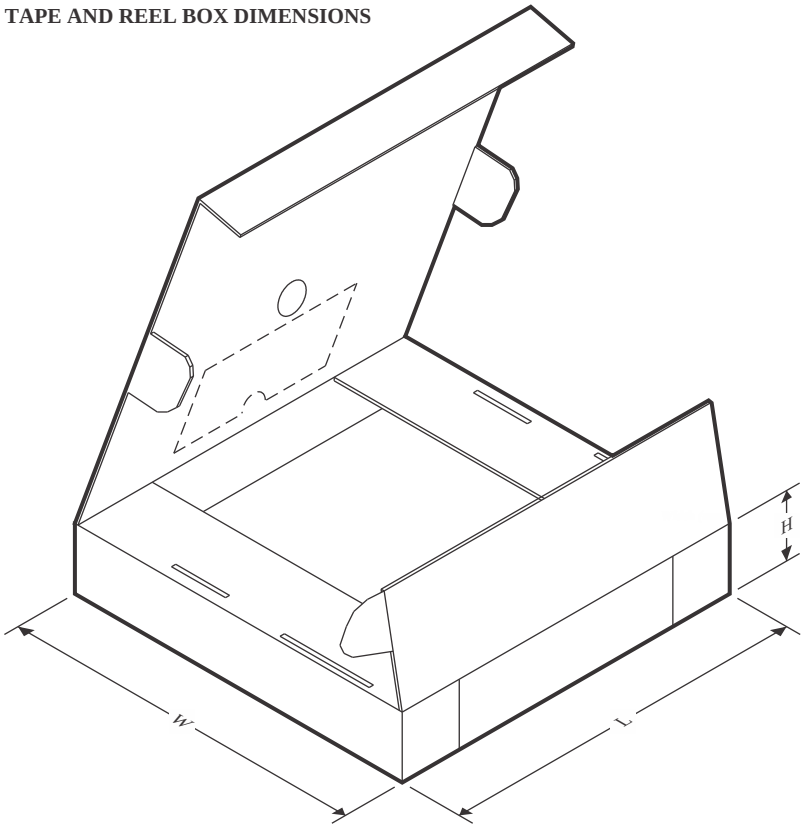
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54354MPWPREP	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

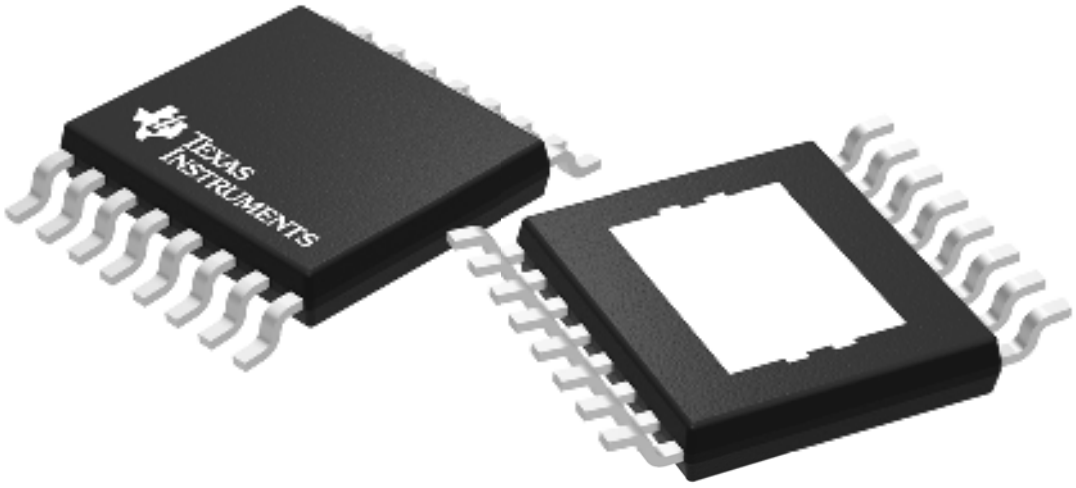


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54354MPWPREP	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073225-3/J

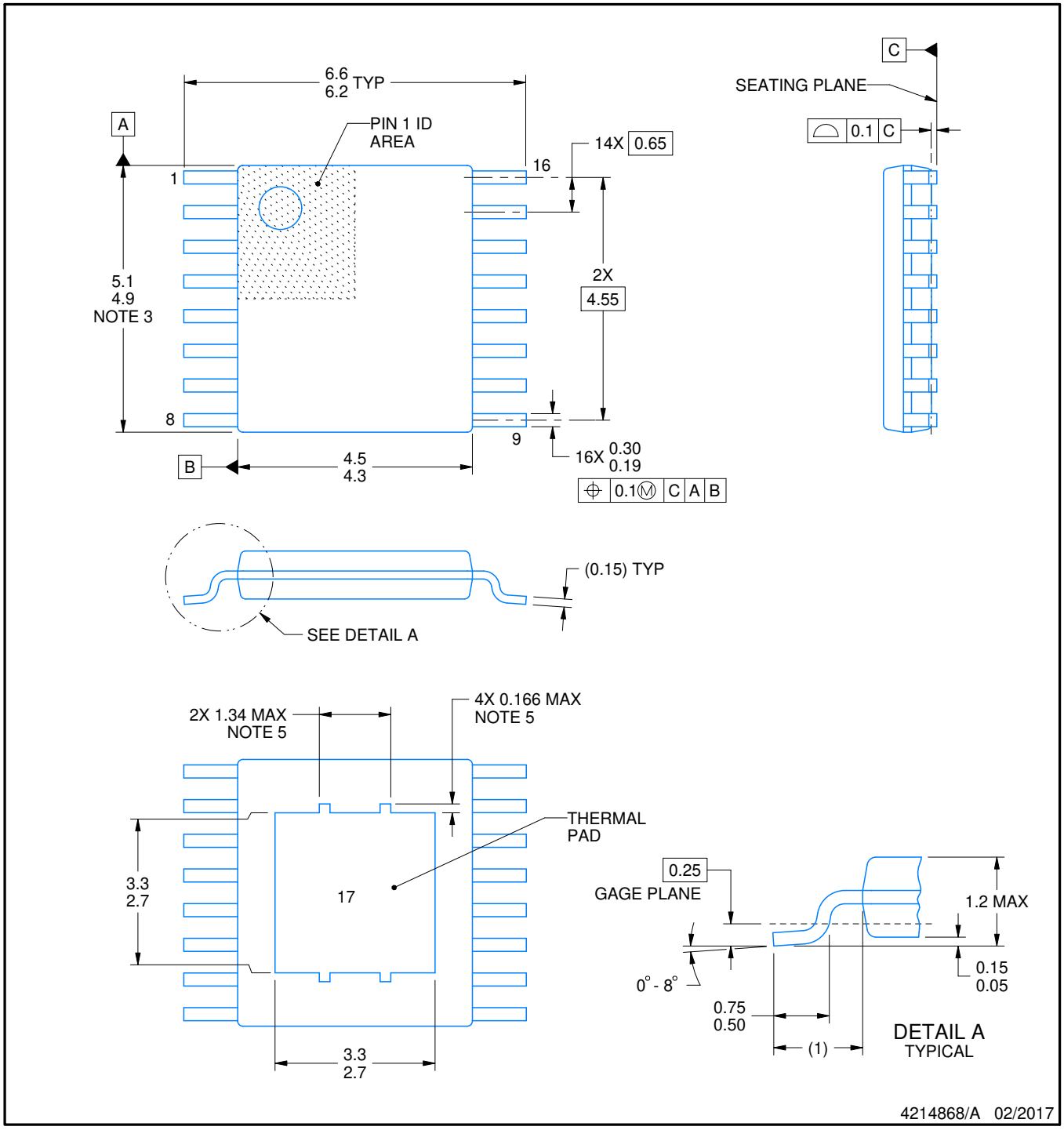


PACKAGE OUTLINE

PWP0016A

PowerPAD ™ HTSSOP - 1.2 mm max height

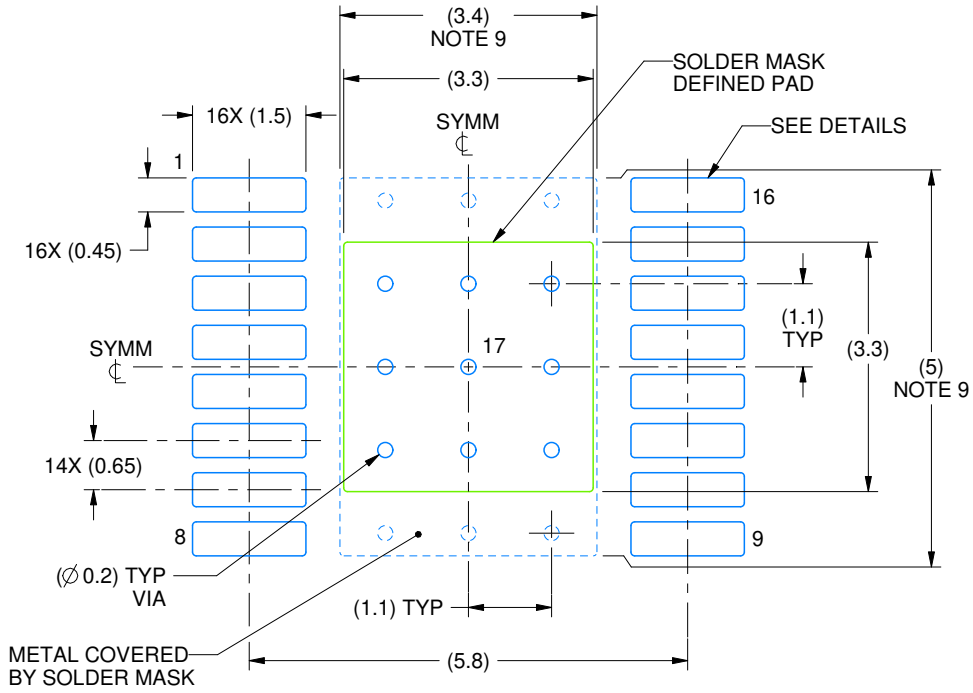
PLASTIC SMALL OUTLINE



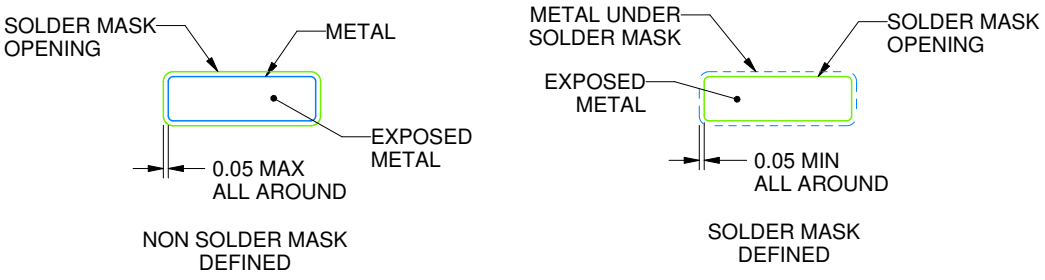
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

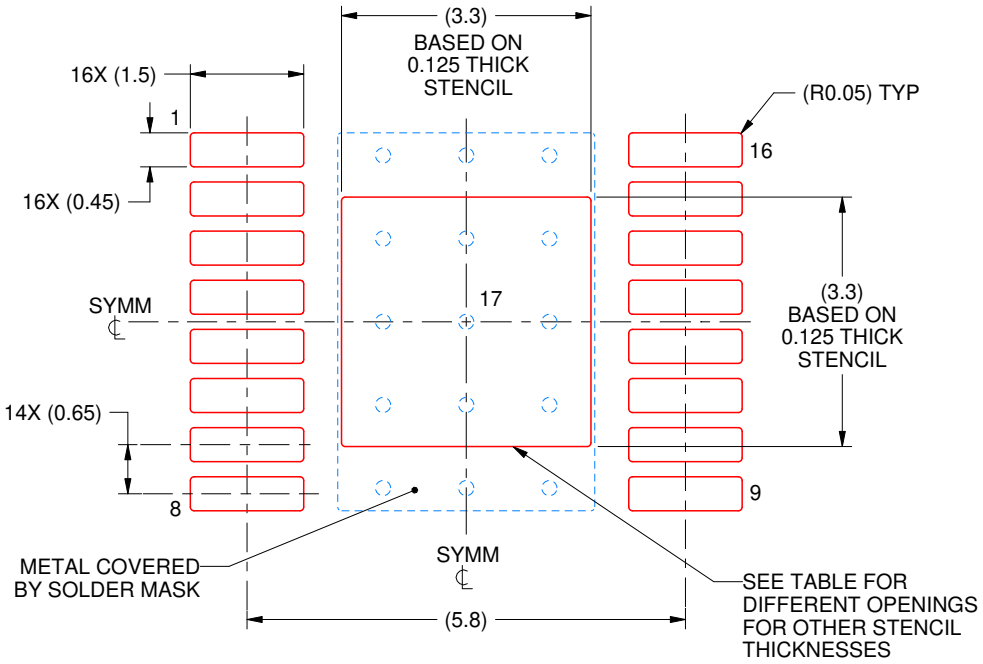


SOLDER MASK DETAILS
PADS 1-16

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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