

Typical Size
6,4 mm X 6,6 mm

3-A OUTPUT TRACKING/TERMINATION SYNCHRONOUS PWM SWITCHER WITH INTEGRATED FETs (SWIFT™)

FEATURES

- **Qualified for Automotive Applications**
- **Tracks Externally Applied Reference Voltage**
- **60-mΩ MOSFET Switches for High Efficiency at 3-A Continuous Output Source or Sink Current**
- **6% to 90% V_I Output Tracking Range**
- **Wide PWM Frequency: Fixed 350 kHz or Adjustable 280 kHz to 700 kHz**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Total Cost**

APPLICATIONS

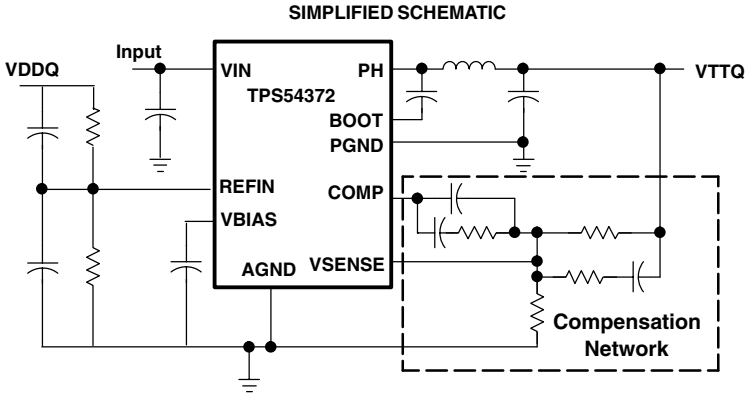
- **DDR Memory Termination Voltage**
- **Active Termination of GTL and SSTL High-Speed Logic Families**
- **DAC Controlled High Current Output Stage**
- **Precision Point of Load Power Supply**

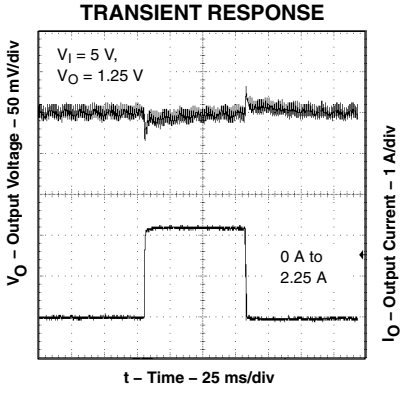
DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the TPS54372 low-input voltage high-output current synchronous-buck PWM converter integrates all required active components. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a status output to indicate valid operating conditions.

The TPS54372 is available in a thermally enhanced 20-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. Texas Instruments provides evaluation modules and the SWIFT designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

SIMPLIFIED SCHEMATIC





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD and SWIFT are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION†

T_J	REFIN VOLTAGE	PACKAGE‡	PART NUMBER
–40°C to 125°C	0.2 V to 1.75 V	Plastic HTSSOP (PWP)§	TPS54372QPWPRQ1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ The PWP package is available taped and reeled as indicated by the R suffix to the device type (i.e., TPS54372QPWPRQ1). See the application section of the data sheet for PowerPAD drawing and layout information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TPS54372
V_I	Input voltage range	VIN, ENA	–0.3 V to 7 V
		RT	–0.3 V to 6 V
		VSENSE, REFIN	–0.3 V to 4 V
		BOOT	–0.3 V to 17 V
V_O	Output voltage range	VBIAS, COMP, STATUS	–0.3 V to 7 V
		PH	–0.6 V to 6 V
I_O	Source current	PH	Internally limited
		COMP, VBIAS	6 mA
I_S	Sink current	PH	6 A
		COMP	6 mA
		ENA, STATUS	10 mA
	Voltage differential	AGND to PGND	±0.3 V
T_J	Operating virtual junction temperature range		–40°C to 150°C
T_{stg}	Storage temperature		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage	3		6	V
T_J	Operating junction temperature	–40		125	°C

DISSIPATION RATINGS(1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
20 Pin PWP with solder	26.0°C/W	3.85 W(3)	2.11 W	1.54 W
20 Pin PWP without solder	57.5°C/W	1.73 W	0.96 W	0.69 W

(1) For more information on the PWP package, see the Texas Instruments technical brief (SLMA002).
(2) Test board conditions:
1. 3” x 3”, four layers, thickness: 0.062”
2. 1.5 oz. copper traces located on the top of the PCB
3. 1.5 oz. copper ground plane on the bottom of the PCB
4. Ten thermal vias (see *Recommended Land Pattern* in the *Applications Section* of this data sheet)
(3) Maximum power dissipation may be limited by overcurrent protection.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE, VIN						
V_{IN}	Input voltage range		3		6	V
$I_{(Q)}$	Quiescent current	f_s = 350 kHz, RT open, PH pin open		6.2	9.6	mA
		f_s = 386 kHz, RT = 160 kΩ, PH pin open		8.4	12.8	
		Shutdown, ENA = 0 V		1	1.4	
UNDER VOLTAGE LOCK OUT						
	Start threshold voltage, UVLO			2.95	3	V
	Stop threshold voltage, UVLO		2.7	2.8		V
	Hysteresis voltage, UVLO			115		mV
	Rising and falling edge deglitch, UVLO(1)			2.5		µs
BIAS VOLTAGE						
	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.7	2.8	2.95	V
	Output current, VBIAS (2)				100	µA
REGULATION						
	Line regulation(1)(3)	I_L = 1.5 A, f_s = 350 kHz, T_J = 125°C			0.07	%/V
	Load regulation(1)(3)	I_L = 0 A to 3 A, f_s = 350 kHz, T_J = 125°C			0.03	%/A
OSCILLATOR						
	Internally set free running frequency	RT open	265	350	440	kHz
	Externally set free running frequency range	RT = 180 kΩ (1% resistor to AGND)(1)	252	280	308	kHz
		RT = 160 kΩ (1% resistor to AGND)	290	312	350	
		RT = 68 kΩ (1% resistor to AGND)(1)	663	700	762	
	Ramp valley(1)			0.75		V
	Ramp amplitude (peak-to-peak)(1)			1		V
	Minimum controllable on time(1)				200	ns
	Maximum duty cycle(1)		90%			
ERROR AMPLIFIER						
	Error amplifier open loop voltage gain	1 kΩ COMP to AGND(1)	90	110		dB
	Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(1)	3	5		MHz
	Error amplifier common mode input voltage range	Powered by internal LDO(1)	0		VBIAS	V
	Input bias current, VSENSE	VSENSE = V_{ref}		60	250	nA
	Output voltage slew rate (symmetric), COMP(1)		1	1.4		V/µs
PWM COMPARATOR						
	PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive(1)		70	85	ns
SLOW-START/ENABLE						
	Enable threshold voltage, ENA		0.82	1.2	1.4	V
	Enable hysteresis voltage, ENA(1)			0.03		V
	Falling edge deglitch, ENA(1)			2.5		µs
	Internal slow-start time(1)		2.6	3.35	4.1	ms
STATUS						
	Output saturation voltage, STATUS	I_{sink} = 2.5 mA		0.18	0.3	V
	Leakage current, STATUS	V_I = 3.6 V			1	µA

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 8.

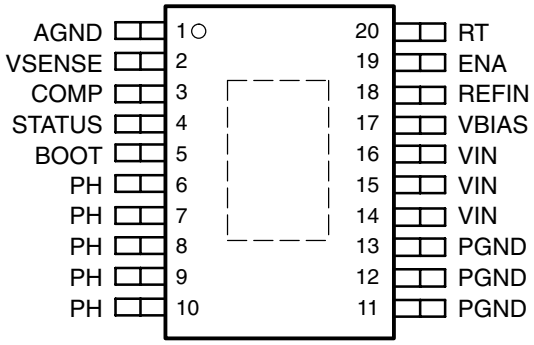
ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_I = 3 V to 6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
	Current limit	V_I = 3 V	4	6.5		A
		V_I = 6 V	4.5	7.5		
	Current limit leading edge blanking time(1)			100		ns
	Current limit total response time(1)			200		ns
THERMAL SHUTDOWN						
	Thermal shutdown trip point(1)		135	150	165	°C
	Thermal shutdown hysteresis(1)			10		°C
OUTPUT POWER MOSFETS						
$r_{DS(on)}$	Power MOSFET switches	V_I = 6 V(4)		59	88	mΩ
		V_I = 3 V(4)		85	136	

(1) Specified by design
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 8.
(4) Matched MOSFETs low-side $r_{DS(on)}$ production tested, high-side $r_{DS(on)}$ production tested.

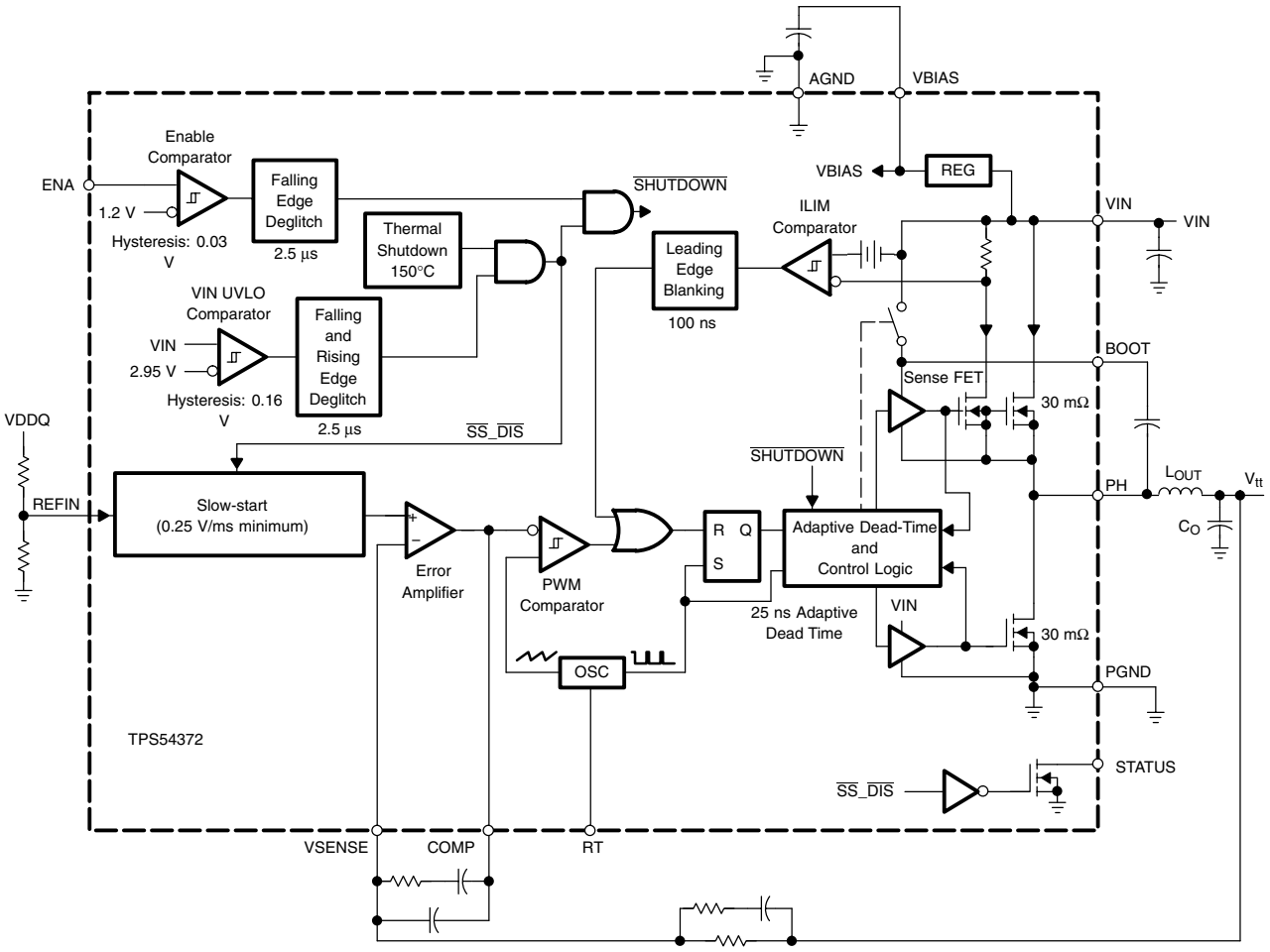
HTSSOP PowerPAD
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor and RT resistor. Connect the PowerPAD connection to AGND.
BOOT	5	Bootstrap output. 0.022-μF to 0.1-μF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect the frequency compensation network from COMP to VSENSE.
ENA	19	Enable input. Logic high enables oscillator, PWM control and MOSFET driver circuits. Logic low disables operation and places device in a low quiescent current state.
PGND	11–13	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6–10	Phase input/output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
RT	20	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency, f_S.
REFIN	18	External reference input. High impedance input to slow-start and error amplifier circuits.
STATUS	4	Open drain output. Asserted low when VIN < UVLO, VBIAS and internal reference are not settled or the internal shutdown signal is active. Otherwise, STATUS is high.
VBIAS	17	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1-μF to 1.0-μF ceramic capacitor.
VIN	14–16	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high-quality, low-ESR 10-μF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage compensation network/output divider.

INTERNAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

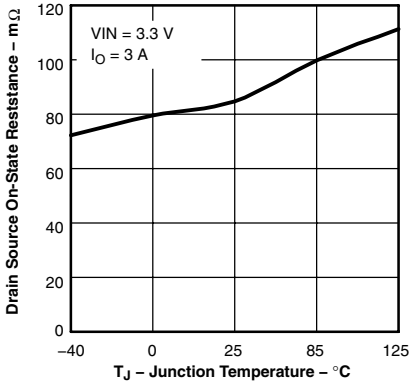


Figure 1

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

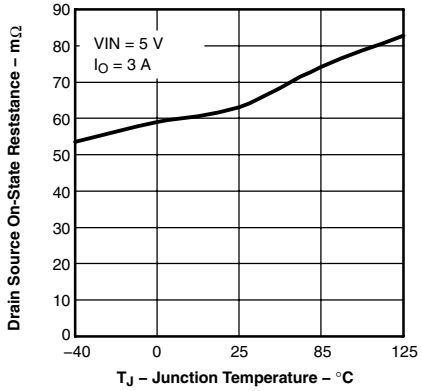


Figure 2

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

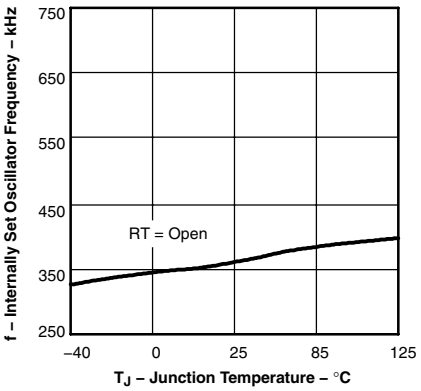


Figure 3

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

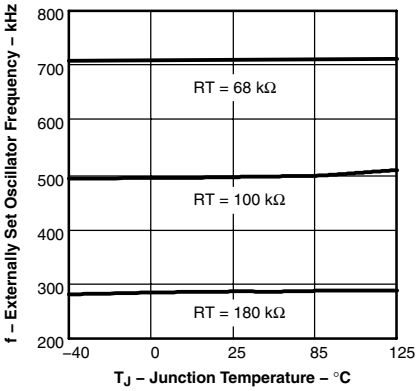


Figure 4

DEVICE POWER LOSSES vs LOAD CURRENT

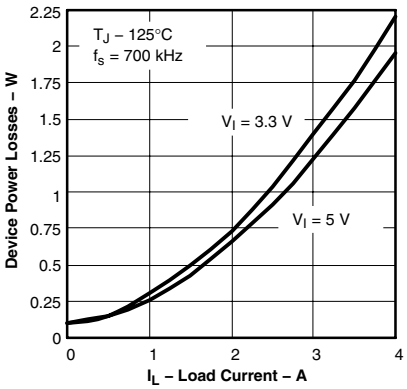


Figure 5

INTERNAL SLOW-START TIME vs JUNCTION TEMPERATURE

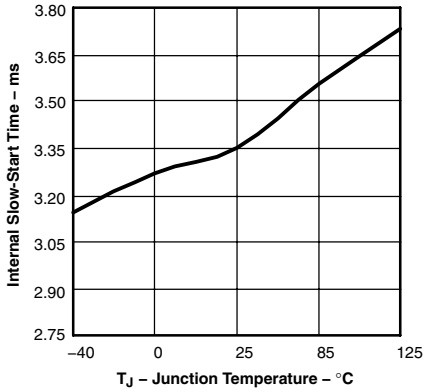


Figure 6

ERROR AMPLIFIER OPEN LOOP RESPONSE

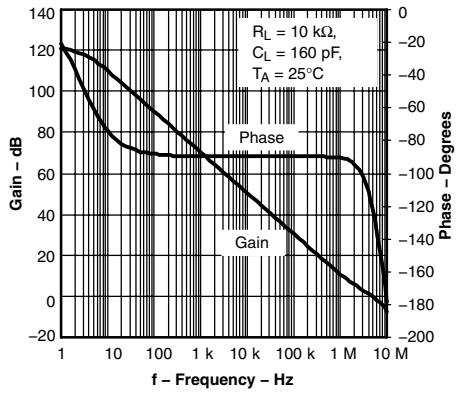


Figure 7

APPLICATION INFORMATION

Figure 8 shows the schematic diagram for a typical TPS54372 application. The TPS54372 (U1) can provide up to 3 A of output current at a nominal output voltage of one half of V_{DDQ} (typically 1.25 V). For proper operation, the PowerPAD underneath the integrated circuit TPS54372 is soldered directly to the printed-circuit board.

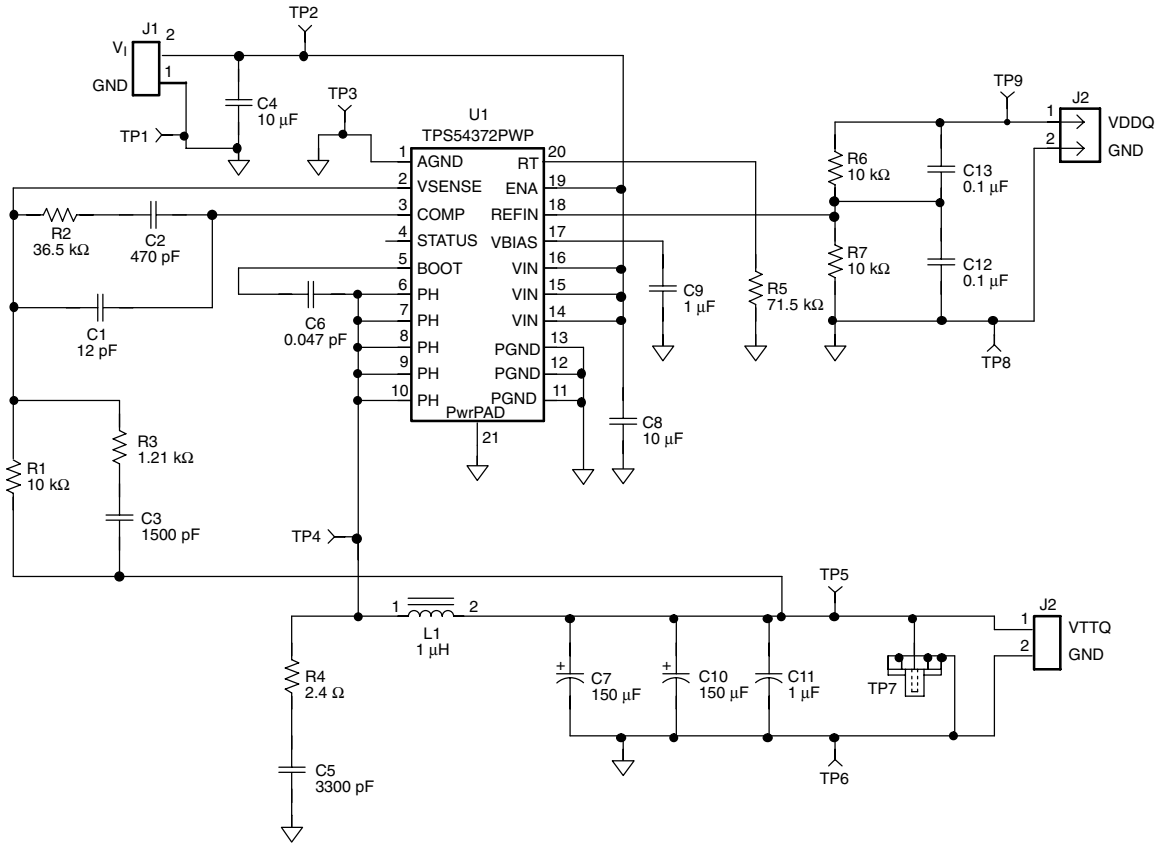


Figure 8. Application Circuit

COMPONENT SELECTION

The values for the components used in this design example were selected for good transient response and small PCB area. Special polymer capacitors are utilized in the output filter circuit. A small size, small value output inductor is also used. Compensation network components are chosen to maximize closed loop bandwidth and provide good transient response characteristics. Additional design information is available at www.ti.com.

INPUT VOLTAGE

The input voltage is a nominal 3.3 or 5 VDC. The input filter (C4) is a 10-µF ceramic capacitor (Taiyo Yuden). Capacitor C8, a 10-µF ceramic capacitor (Taiyo Yuden) that provides high frequency decoupling of the TPS54372 from the input supply, must be located as close as possible to the device. Ripple current is carried in both C4 and C8, and the return path to PGND should avoid the current circulating in the output capacitors C7, C10, and C11.

FEEDBACK CIRCUIT

The values for these components are selected to provide fast transient response times. Components R1 R2, R3, C1, C2, and C3 forms the loop compensation network for the circuit. For this design, a Type 3 topology is used. The transfer function of the feedback network is chosen to provide maximum closed loop gain available with open loop characteristics of the internal error amplifier. Closed loop crossover frequency is typically between 80 kHz and 125 kHz for input from 3 V to 6 V.

OPERATING FREQUENCY

In the application circuit, RT is grounded through a 71.5 kΩ resistor to select the operating frequency of 700 kHz. To set a different frequency, place a 68-kΩ to 180-kΩ resistor between RT (pin 20) and analog ground or leave RT floating to select the default of 350 kHz. The resistance can be approximated using the following equation:

$$R = \frac{500\ \text{kHz}}{\text{Switching Frequency}} \times 100\ [\text{k}\Omega] \quad (1)$$

OUTPUT FILTER

The output filter is composed of a 1-μH inductor and two 150-μF capacitors. The inductor is a low dc resistance (0.010 Ω) type, Vishay IHLP–2525CZ–01 1-μH, 8.5-A rated dc output. The capacitors used are 150 μF, 6.3-V special polymer types.

GROUNDING AND PowerPAD LAYOUT

The TPS54372 has two internal grounds (analog and power). Inside the TPS54372, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54372, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground areas are recommended. The analog ground area should be tied to the power ground area directly at the IC to reduce noise between the two grounds. The only components that should tie directly to the power ground area are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54372. The power ground areas as well as the powerpad mounting area should be tied to any internal ground planes using multiple vias. The layout of the TPS54372 evaluation module is representative of a recommended layout for a 2-layer board with the bottom layer representing the system ground plane. Documentation for the TPS54372 evaluation module can be found on the Texas Instruments web site under the TPS54372 product folder.

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Six vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the ten recommended that enhance thermal performance should be included in areas not under the device package.

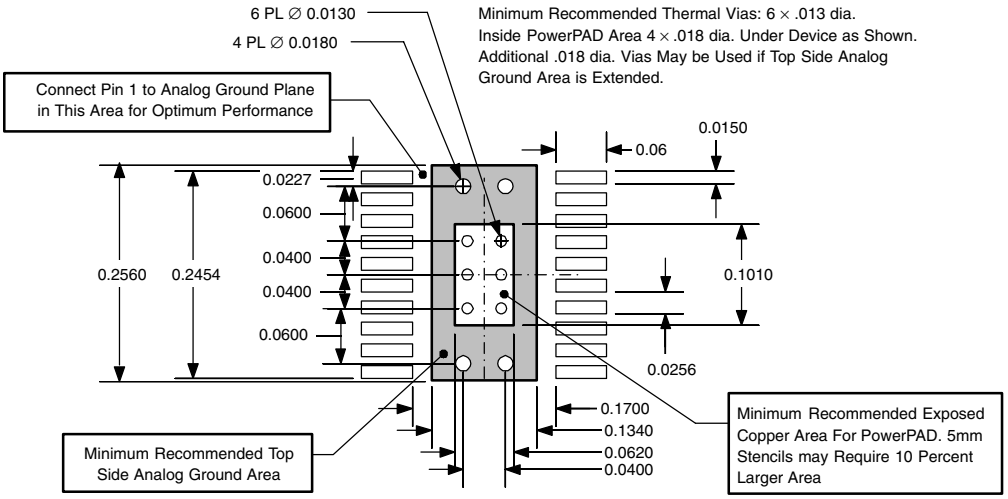


Figure 9. Recommended Land Pattern for 20-Pin PWP PowerPAD

PERFORMANCE GRAPHS

EFFICIENCY vs OUTPUT CURRENT

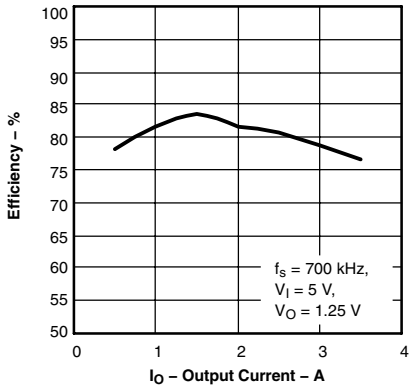


Figure 10

LOAD REGULATION vs OUTPUT CURRENT

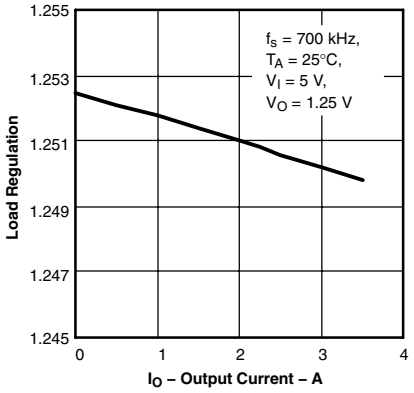


Figure 11

LINE REGULATION vs INPUT VOLTAGE

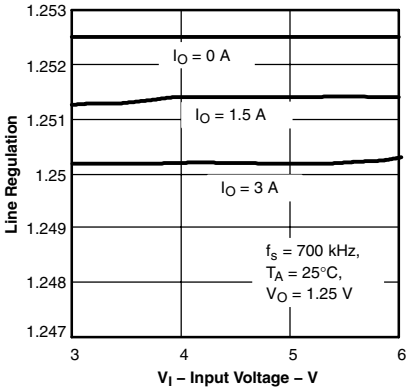


Figure 12

OUTPUT RIPPLE VOLTAGE

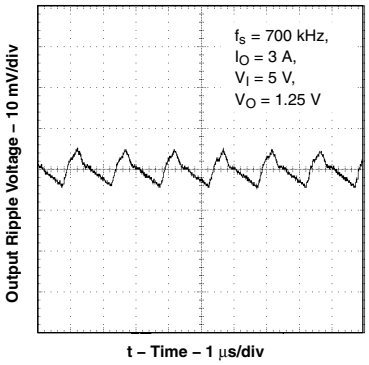


Figure 13

TRANSIENT RESPONSE

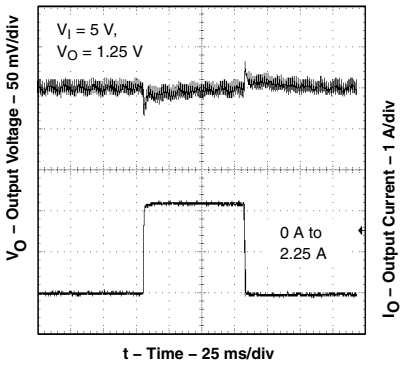


Figure 14

SLOW-START TIMING

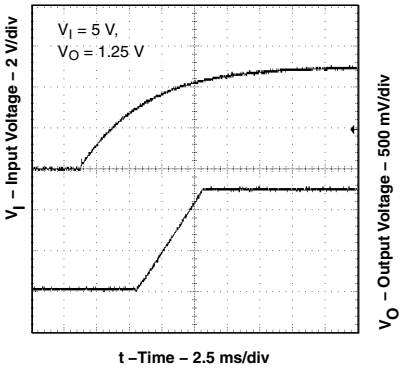


Figure 15

SOURCE-SINK TRANSIENT RESPONSE

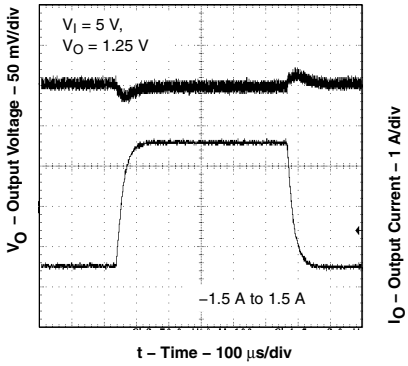
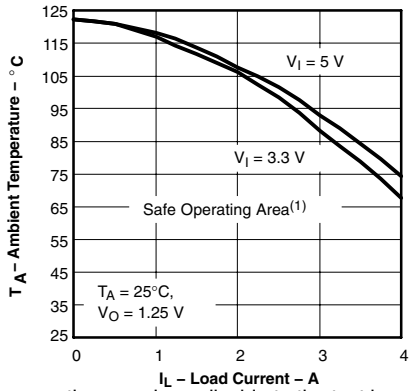


Figure 16

AMBIENT TEMPERATURE vs LOAD CURRENT



(1) Safe operating area is applicable to the test board conditions listed in the dissipation rating table section of this data sheet.

Figure 17

DETAILED DESCRIPTION

UNDERVOLTAGE LOCK OUT (UVLO)

The TPS54372 incorporates an undervoltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

ENABLE (ENA)

The enable pin, ENA, provides a digital control to enable or disable (shutdown) the TPS54372. An input voltage of 1.4 V or greater ensures the TPS54372 is enabled. An input of 0.82 V or less ensures the device operation is disabled. These are not standard logic thresholds, even though they are compatible with TTL outputs.

When ENA is low, the oscillator, slow-start, PWM control and MOSFET drivers are disabled and held in an initial state ready for device start-up. On an ENA transition from low to high, device start-up begins with the output starting from 0 V.

SLOW-START

The slow-start circuit provides start-up slope control of the output voltage to limit in-rush currents. The nominal internal slow-start rate is 0.25 V/ms with the minimum rate being 0.35 V/ms. When the voltage on REFIN rises faster than the internal slope or is present when device operation is enabled, the output rises at the internal rate. If the reference voltage on REFIN rises more slowly, then the output rises at approximately the same rate as REFIN.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND. External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be a useful as a reference voltage for external circuits.

VOLTAGE REFERENCE

The REFIN pin provides an input for a user supplied tracking voltage. Typically this input is one half of V_{DDQ}. The input range for this external reference is 0.2 V to 1.75 V. Above this level, the internal bandgap reference overrides the externally supplied reference voltage.

OSCILLATOR AND PWM RAMP

The oscillator frequency can be set to an internally fixed value of 350 kHz by leaving the RT pin unconnected (floating). If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor to the RT pin to ground. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\ [\text{kHz}] \qquad (2)$$

The following table summarizes the frequency selection configurations:

SWITCHING FREQUENCY	RT PIN
350 kHz, internally set	Float
Externally set 280 kHz to 700 kHz	R = 180 kΩ to 68 kΩ

ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the TPS54372 apart from most dc/dc converters. The user has a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54372 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the gate drive voltage to the low-side FET is below 2 V, while the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V. The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω. bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle by cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100 ns leading edge blanking circuit prevents false tripping of the current limit when the high-side switch is turning on. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal limit trip point. This sequence repeats until the fault condition is removed.

STATUS

The status pin is an open drain output that indicates when internal conditions are sufficient for proper operation. STATUS can be coupled back to a system controller or monitor circuit to indicate that the termination or tracking regulator is ready for start-up. STATUS is high impedance when the TPS54372 is operating or ready to be enabled.

STATUS is active low if any of the following occur:

- VIN < UVLO threshold
- VBIAS or internal reference have not settled.
- Thermal shutdown is active.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54372QPWPRQ1	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P54372Q1
TPS54372QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P54372Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54372-Q1 :

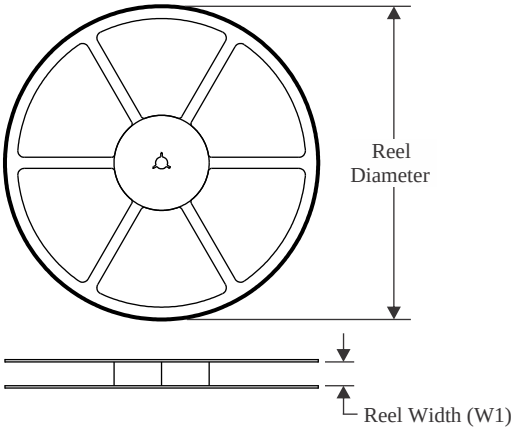
- Catalog : TPS54372

NOTE: Qualified Version Definitions:

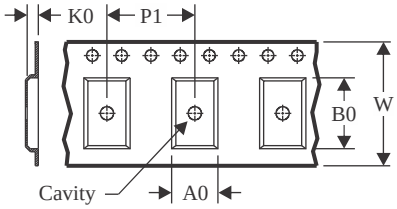
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

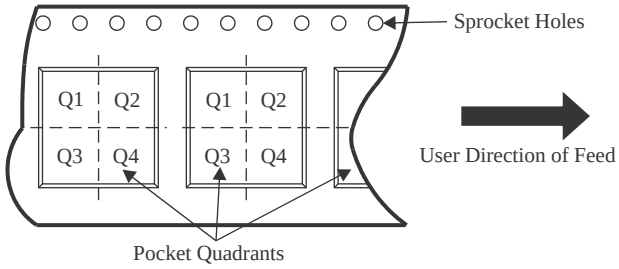


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

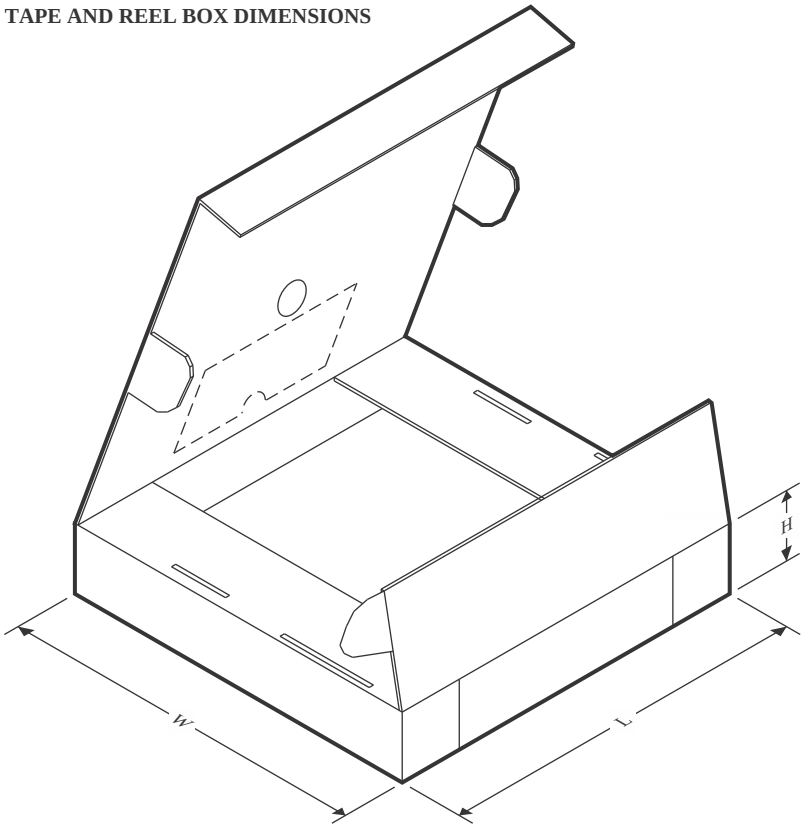
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54372QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54372QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

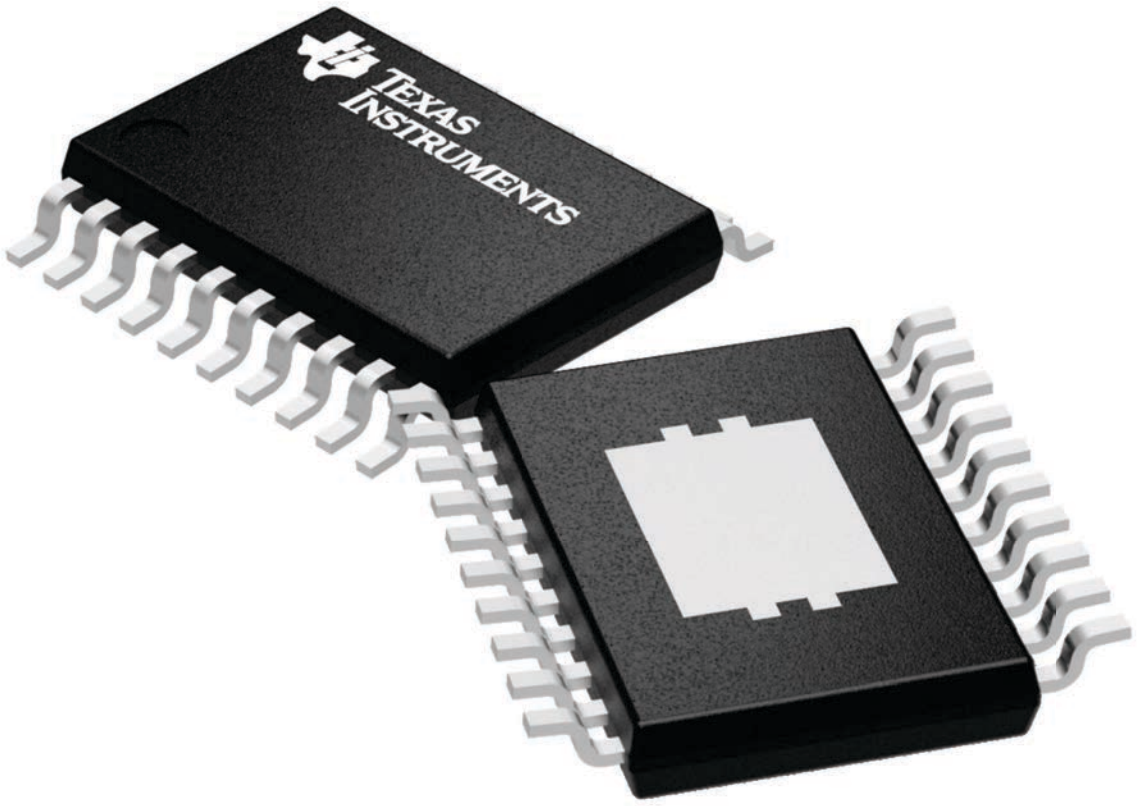
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

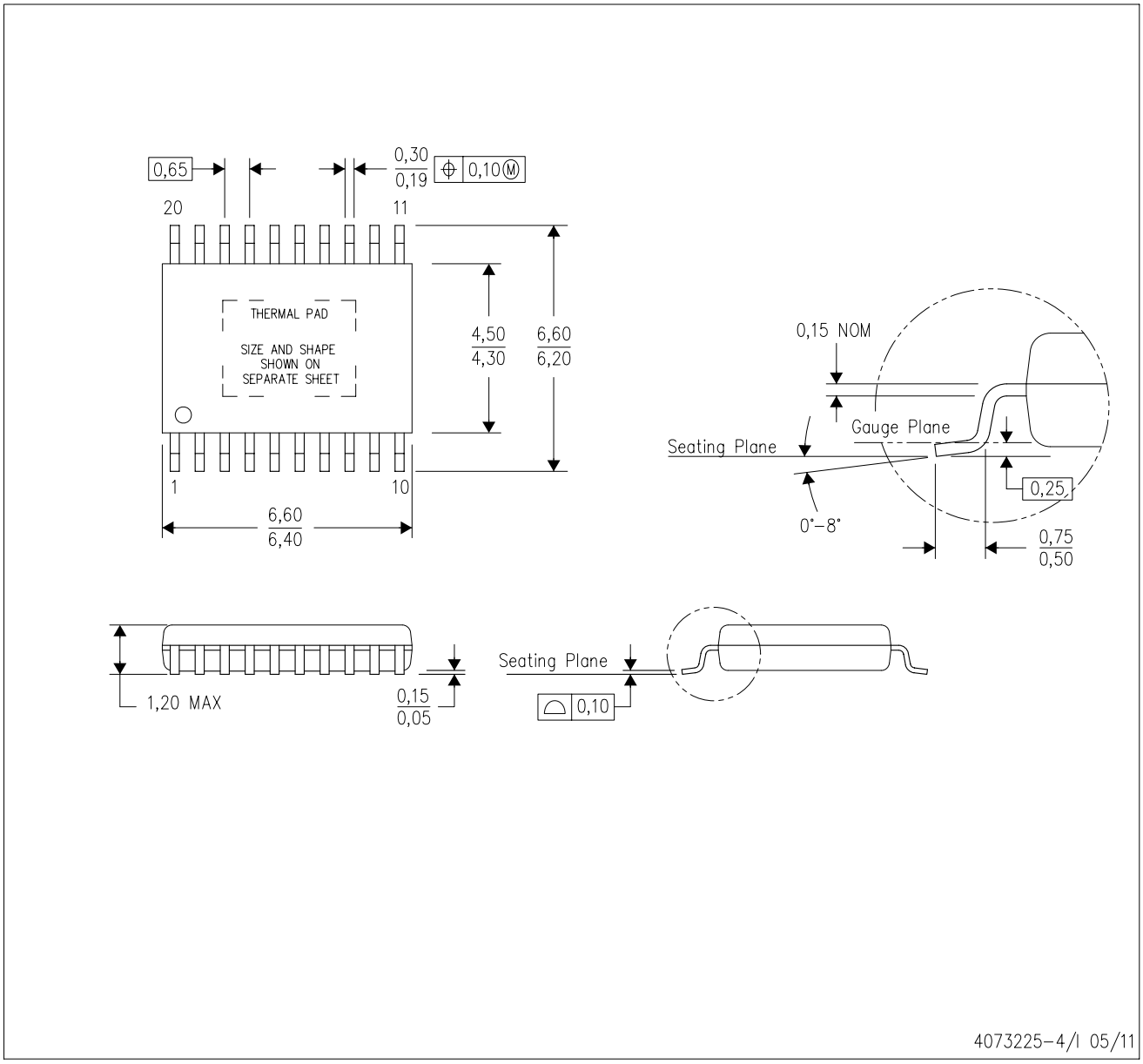
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

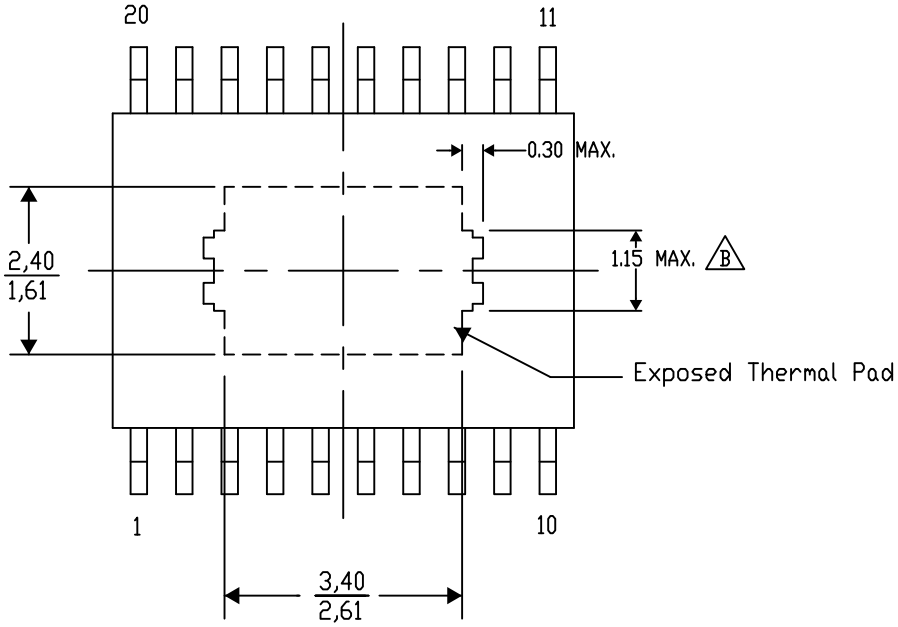
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

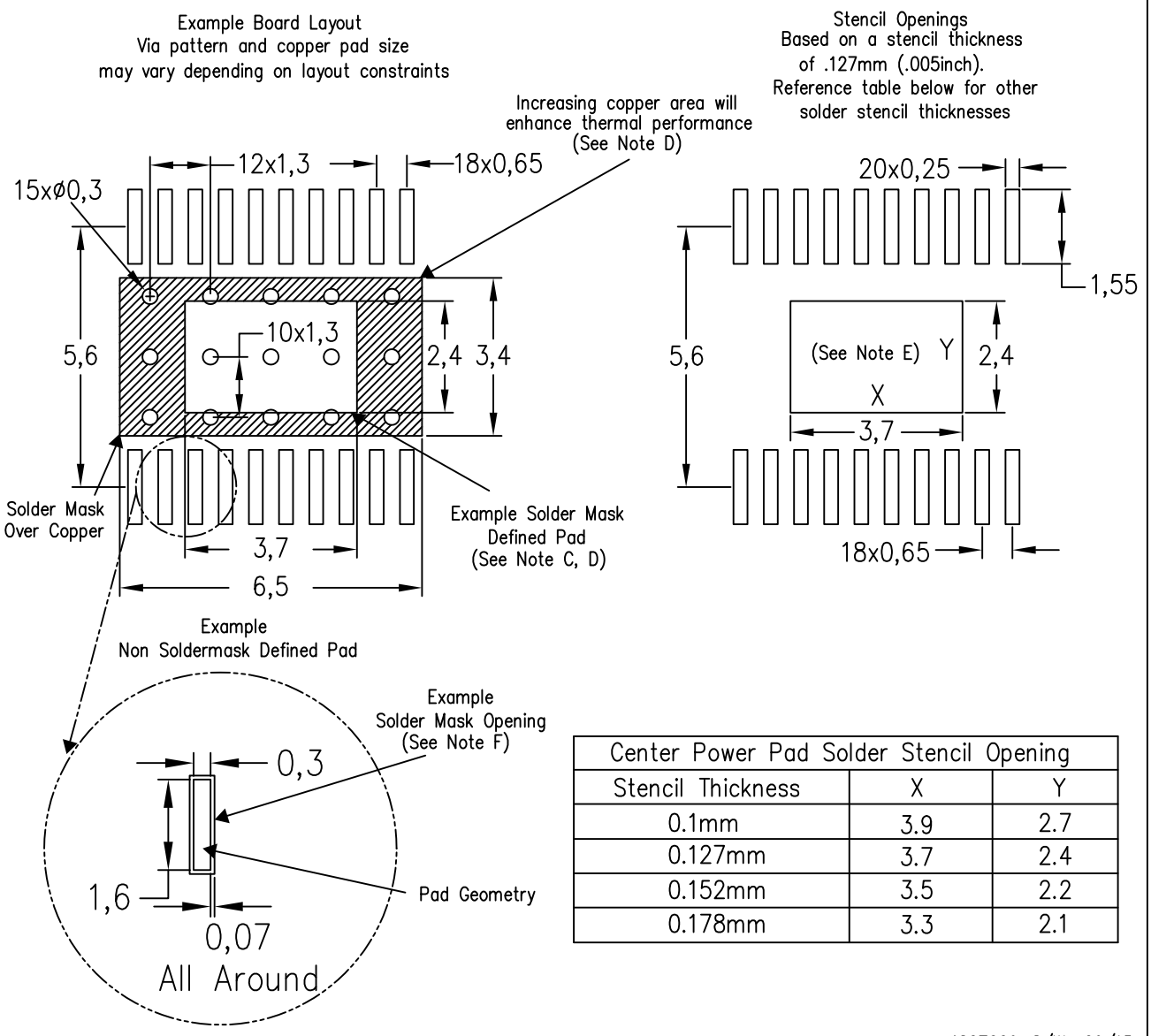
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025