TPS54478 2.95-V to 6-V Input, 4-A Synchronous Step-Down SWIFT™ Converter With Hiccup Current Limit

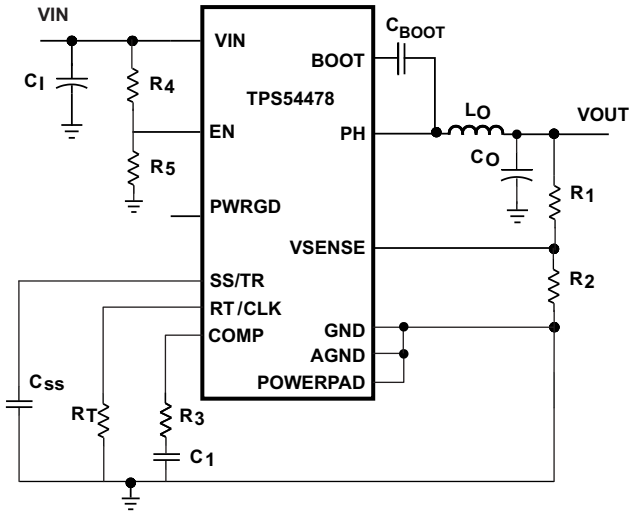
1 Features

- Two 30-mΩ (typical) MOSFETs for High Efficiency at 4-A Loads
- 200-kHz to 2-MHz Switching Frequency
- 0.6-V ± 1% Voltage Reference Over Temperature (–40°C to +150°C)
- Start-up With Prebiased Voltage
- Synchronizes to External Clock
- Adjustable Slow Start / Sequencing
- UV and OV Power-Good Output
- Cycle by Cycle Current Limit and Hiccup Current Protection
- Thermally Enhanced 3-mm × 3-mm 16-Pin WQFN (RTE)
- Pin Compatible to TPS54418
- Create a Custom Design Using the TPS54478 With the WEBENCH® Power Designer

2 Applications

- Low-Voltage, High-Density Power Systems
- Point-of-Load Regulation for High Performance DSPs, FPGAs, ASICs, and Microprocessors
- Broadband, Networking, and Optical Communications Infrastructure

Simplified Schematic



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3 Description

The TPS54478 device is a full featured 6-V, 4-A, synchronous step down current mode converter with two integrated MOSFETs.

The TPS54478 enables small designs by integrating the MOSFETs, implementing current mode control to reduce external component count, reducing inductor size by enabling up to 2-MHz switching frequency, and minimizing the IC footprint with a small 3-mm × 3-mm thermally enhanced WQFN package.

The TPS54478 provides accurate regulation for a variety of loads with an accurate ±1% voltage reference (V_{REF}) over temperature. Efficiency is maximized through the integrated 30-mΩ MOSFETs and 525-µA typical supply current. Using the enable pin, shutdown supply current is reduced to 2.5 µA by entering a shutdown mode.

Undervoltage lockout is internally set at 2.6 V, but can be increased by programming the threshold with a resistor network on the enable pin. The output voltage start-up ramp is controlled by the soft-start pin. An open-drain power-good signal indicates the output is within 93% to 107% of its nominal voltage.

Cycle-by-cycle current limit, hiccup overcurrent protection, and thermal shutdown protect the device during an overcurrent condition.

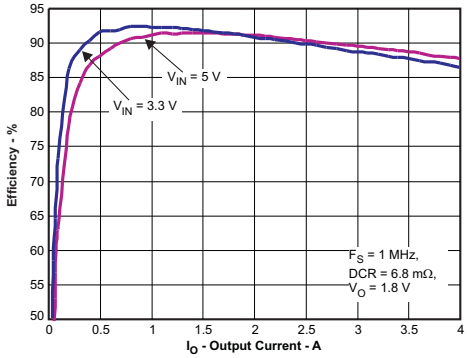
For more SWIFT™ documentation, see the TI website at www.ti.com/swift.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54478	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision A (November 2016) to Revision B **Page**

- Update title to include key features; add links for WEBENCH; delete link to SwitcherPro tool ... 1

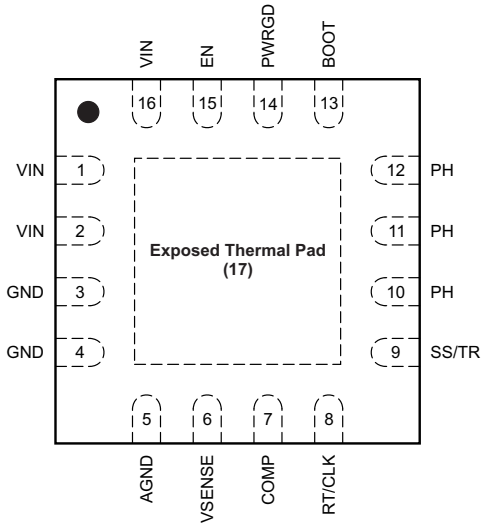
Changes from Original (June 2011) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table; see POA at the end of the datasheet. ... 1

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5 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	5	—	Analog Ground should be electrically connected to GND close to the device.
BOOT	13	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the BOOT UVLO, the output is forced to switch off until the capacitor is refreshed.
COMP	7	I/O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	I	Enable pin, internal pull-up current source. Pull below 1.21 V to disable. Float to enable. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors.
GND	3, 4	—	Power Ground. This pin should be electrically connected directly to the power pad under the IC.
PH	10, 11, 12	O	The source of the internal high side power MOSFET, and drain of the internal low side (synchronous) rectifier MOSFET.
PWRGD	14	O	An open drain output; asserts low if output voltage is low due to thermal shutdown, overcurrent, over/under-voltage or EN shut down.
RT/CLK	8	I	Resistor Timing or External Clock input pin.
SS/TR	9	I	Slow start and tracking. An external capacitor connected to this pin sets the output voltage rise time. The SS provides higer charge current when SS is below 0.15V, resulting in two slopes of the SS voltage. This pin can also be used for tracking.
Thermal Pad	17	—	GND pin should be connected to the exposed thermal pad for proper operation. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.
VIN	1, 2, 16	I	Input supply voltage, 2.95 V to 6 V.
VSENSE	6	I	Inverting node of the transconductance (gm) error amplifier.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	7	V
	EN	–0.3	7	
	BOOT		PH + 7	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	7	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	3.3	
Output voltage	BOOT-PH		7	V
	PH	–0.6	7	
	PH 10 ns Transient	–2	10	
Source current	EN		100	µA
	RT/CLK		100	
Sink current	COMP		100	µA
	PWRGD		10	mA
	SS/TR		100	µA
Junction Temperature, T_j		–40	150	°C
Storage Temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Electrical Characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per QSS 009-105 (JESD22-A114A)(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input Voltage Range	2.95		6	V
Output Current	0		4	A
Operating Junction Temperature Range, T_J	–40		150	°C

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6.4 Thermal Information

THERMAL METRIC[1][2][3]		TPS54478 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	50.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation may be limited by overcurrent protection
(3) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 150°C for best performance and long-term reliability. See power dissipation estimate in application section of this data sheet for more information.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		2.95		6.0	V
Input under voltage lockout threshold	No voltage hysteresis		2.6		V
Shutdown supply current	EN = 0 V, 25°C, 2.95 V ≤ VIN ≤ 6 V		0.7	2.5	µA
Quiescent Current - I_q	VSENSE = 0.7 V, VIN = 5 V, 25°C, RT = 78.7 kΩ		525	700	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.30		V
	Falling		1.21		
Input current	Enable threshold + 50 mV		–3.4		µA
	Enable threshold – 50 mV		–0.64		
VOLTAGE REFERENCE (VSENSE PIN)					
Voltage Reference	2.95 V ≤ VIN ≤ 6 V, –40°C <T_J < 150°C	0.594	0.600	0.606	V
MOSFET					
High side switch resistance	BOOT-PH = 5 V		30	60	mΩ
	BOOT-PH = 3.3 V		37	70	
Low side switch resistance	VIN = 5 V		30	60	mΩ
	VIN = 3.3 V		37	70	
ERROR AMPLIFIER					
Input current			7		nA
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		225		µmhos
Error amplifier transconductance (gm) during slow start	–2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V, Vsense = 0.4 V		77		µmhos
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±20		µA
COMP to Iswitch gm			14		A/V
CURRENT LIMIT					
Current limit threshold	VIN = 6V, Fs = 500 KHz	5.2	6.5	8.2	A
Cycles before entering hiccup			512		Cycles
Cycles of converter in off state during hiccup			16384		Cycles
Low side Fet reverse current limit			3.1		A
THERMAL SHUTDOWN					
Thermal shutdown			165		°C

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Electrical Characteristics (continued)

T_J = –40°C to 150°C, VIN = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hysteresis			15		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching frequency range using RT mode		200		2000	kHz
Switching frequency	$R_{(RT/CLK)}$ = 78.7 kΩ	400	500	600	kHz
Switching frequency range using CLK mode		300		2000	kHz
Minimum CLK pulse width		75			ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 78.7 kΩ		0.5		V
RT/CLK high threshold			1.6	2.2	V
RT/CLK low threshold		0.4	0.6		V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		75		ns
PLL lock in time	Measure at 500 kHz		14		µs
PH (PH PIN)					
Minimum On time	Measured at 50% points on PH, VIN = 5 V, I_{OUT} = 2 A		100		ns
	Measured at 50% points on PH, VIN = 5 V, I_{OUT} = 0 A		120		
Minimum Off time	Prior to skipping off pulses, VIN = 5 V, I_{OUT} = 2 A		110		ns
Rise Time	VIN = 5 V, 4 A		1.5		V/ns
Fall Time			1.5		
BOOT (BOOT PIN)					
BOOT Charge Resistance	VIN = 5 V		15		Ω
BOOT-PH UVLO	VIN = 2.95 V		2.2		V
SLOW START AND TRACKING (SS/TR PIN)					
SS voltage threshold (V_{SSTHR})			0.15		V
Charge Current	$V_{(SS/TR)} < V_{SSTHR}$		45		µA
	$V_{(SS/TR)} > V_{SSTHR}$		2.2		
SS/TR to VSENSE matching	$V_{(SS/TR)}$ = 0.3 V		65		mV
SS/TR to reference crossover	98% normal		0.86		V
SS/TR discharge voltage (Overload)	VSENSE = 0 V		2.5		mV
SS/TR discharge current (Overload)	VSENSE = 0 V, $V_{(SS/TR)}$ = 0.4 V		900		µA
SS discharge current (UVLO, EN, Thermal fault)	VIN = 5 V, V(SS) = 0.5 V		1.16		mA
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		93		% Vref
	VSENSE rising (Good)		95		
	VSENSE rising (Fault)		107		
	VSENSE falling (Good)		105		
Hysteresis	VSENSE falling		2		% Vref
Output high leakage	VSENSE = VREF, $V_{(PWRGD)}$ = 5.5 V		7		nA
On resistance	VIN = 2.95 V		56	120	Ω
Output low	$I_{(PWRGD)}$ = 3 mA		0.2	0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		1.2	1.6	V

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6.6 Typical Characteristics

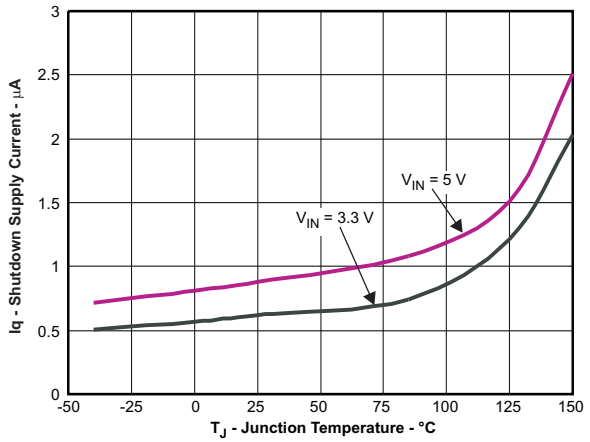


Figure 1. Shutdown Supply Current vs Temperature

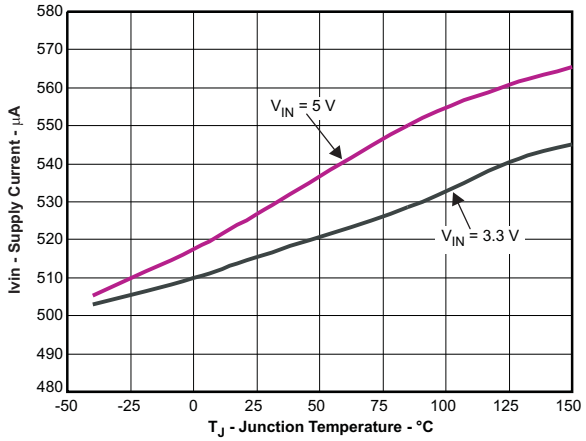


Figure 2. VIN Supply Current vs Temperature

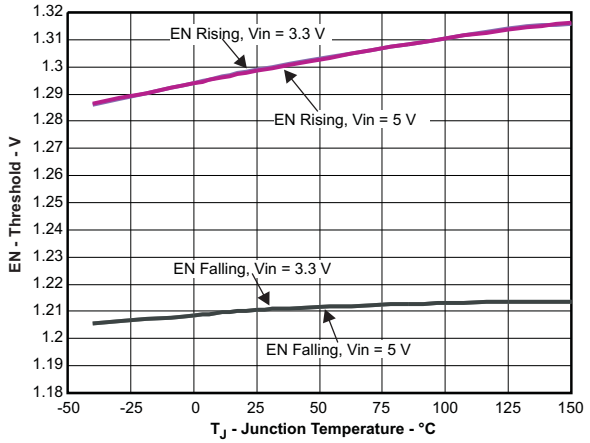


Figure 3. EN Pin Voltage vs Temperature

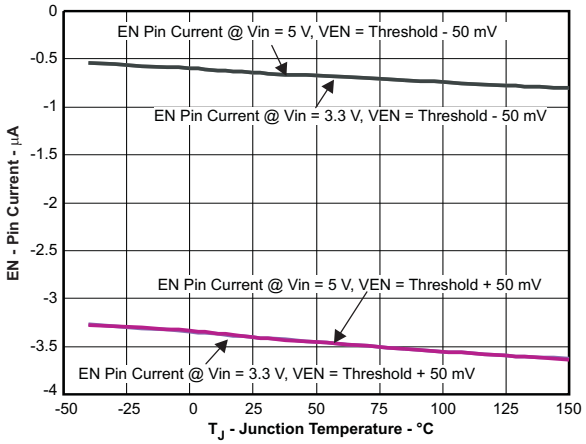


Figure 4. EN Pin Current vs Temperature

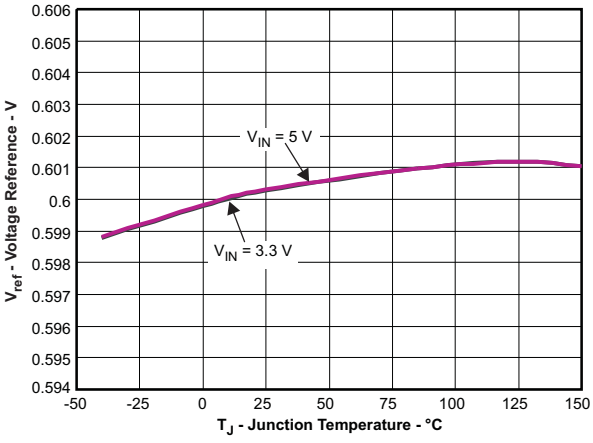


Figure 5. Voltage Reference vs Temperature

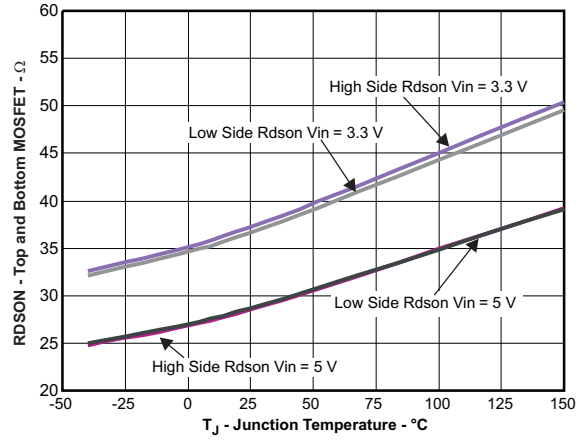


Figure 6. MOSFET Rdson vs Temperature

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Typical Characteristics (continued)

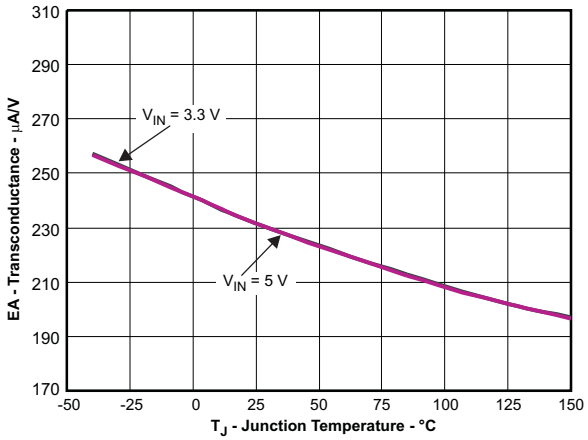


Figure 7. Transconductance vs Temperature

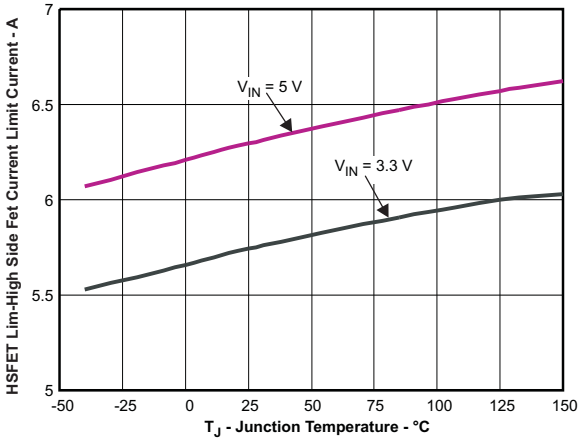


Figure 8. High Side FET Current Limit vs Temperature

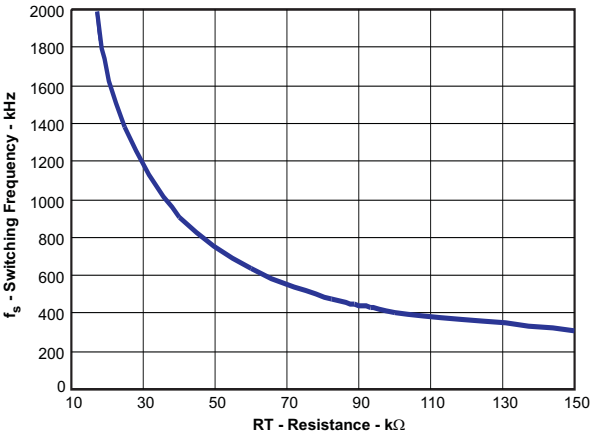


Figure 9. Switching Frequency vs RT Resistance

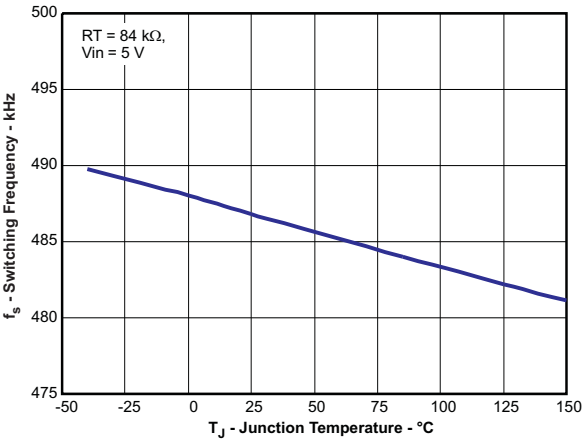


Figure 10. Switching Frequency vs Temperature

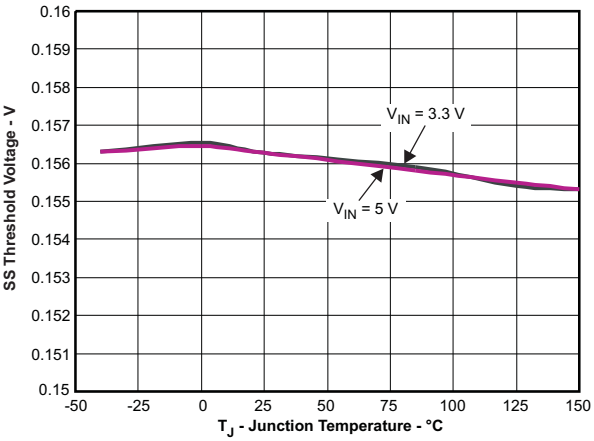


Figure 11. VSS Voltage Threshold V_{SSTHR} vs Temperature

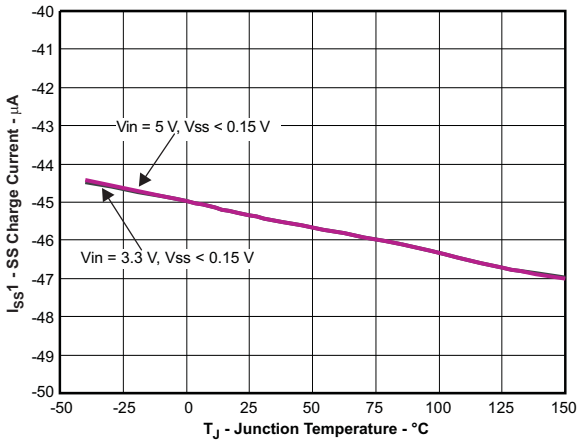


Figure 12. SS Charge Current vs Temperature

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Typical Characteristics (continued)

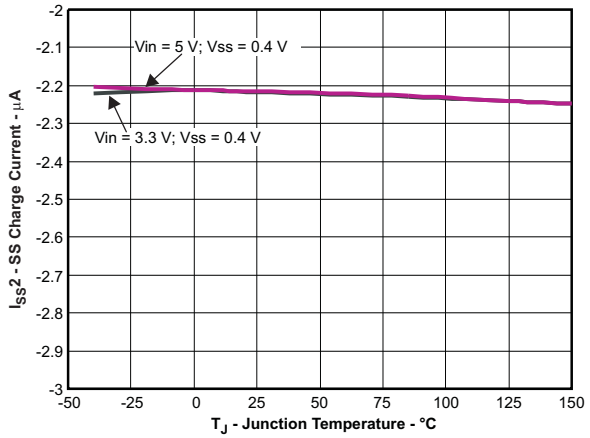


Figure 13. SS Charge Current vs Temperature

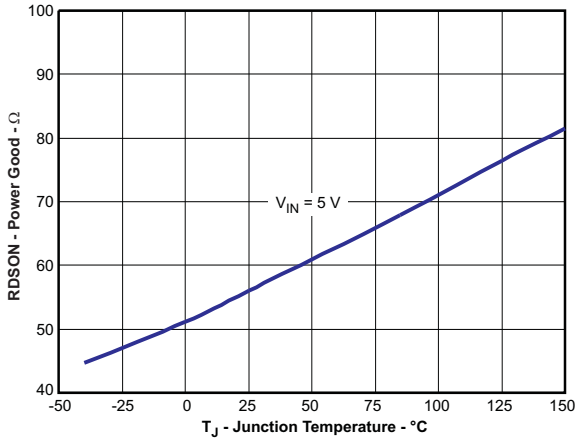


Figure 14. PWRGD Rdson vs Temperature

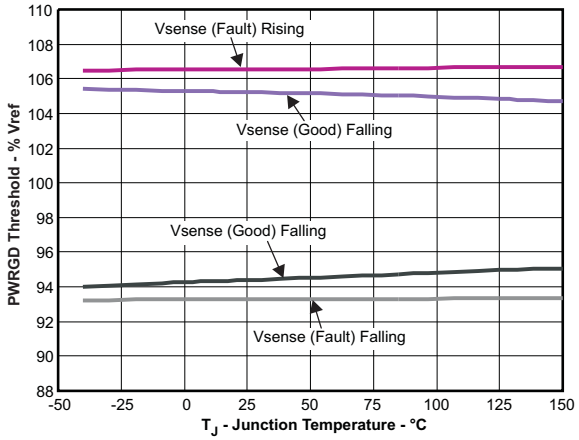


Figure 15. PWRGD Threshold vs Temperature

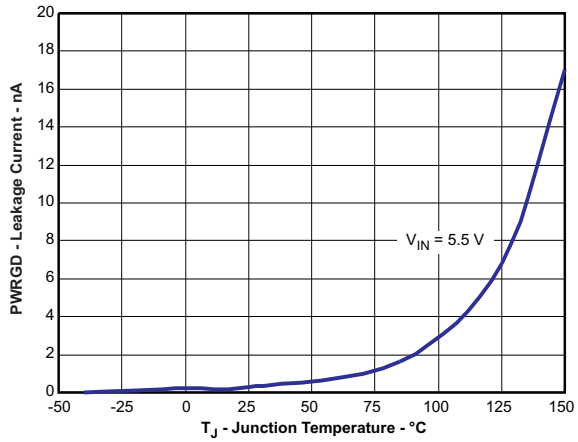


Figure 16. PWRGD Leakage Current vs Temperature

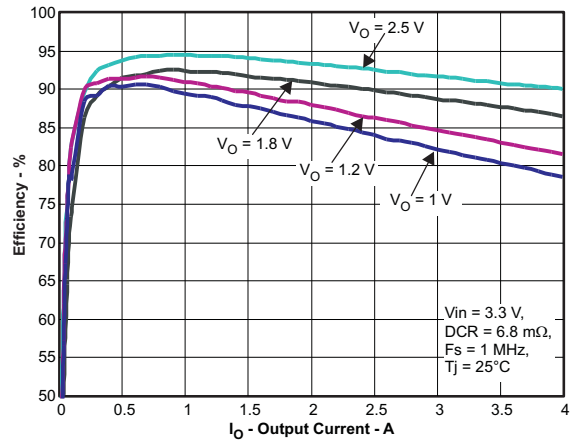


Figure 17. Efficiency vs Load Current

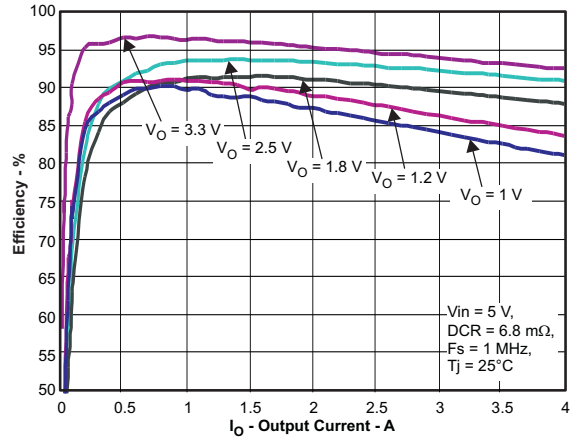


Figure 18. Efficiency vs Load Current

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Typical Characteristics (continued)

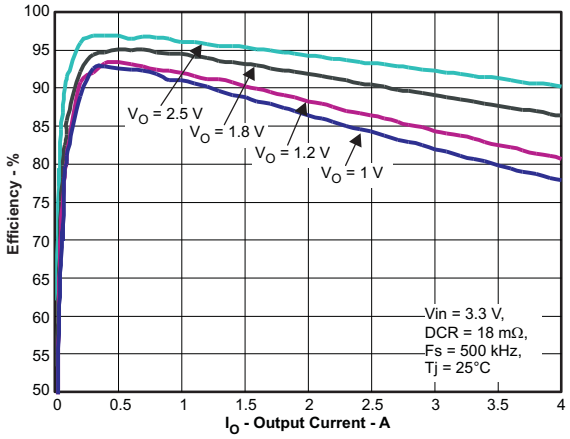


Figure 19. Efficiency vs Load Current

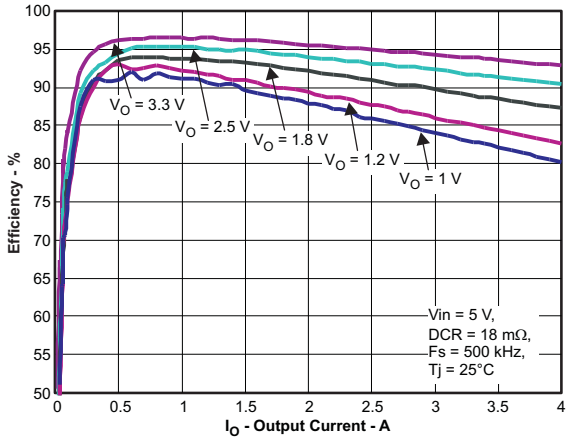


Figure 20. Efficiency vs Load Current

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7 Detailed Description

7.1 Overview

The TPS54478 is a 6-V, 4-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54478 has a typical default start up voltage of 2.6 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the pull up current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS54478 is typically 525 μA when not switching and under no load. When the device is disabled, the supply current is less than 2.5 μA.

The integrated 30 mΩ MOSFETs allow for high efficiency power supply designs with continuous output currents up to 4 amperes.

The TPS54478 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54478 to operate approaching 100%. The output voltage can be stepped down to as low as the 0.600 V reference.

TPS54478 features monotonic starup under pre-bias conditions. The low side Fet turns on for a very short time period every cycle before the output voltage reaches the pre-biased voltage. This ensures the boot cap has enough charge to turn on the top Fet when the output voltage reaches the pre-biased voltage.

The TPS54478 has a power good comparator (PWRGD) with 2% hysteresis.

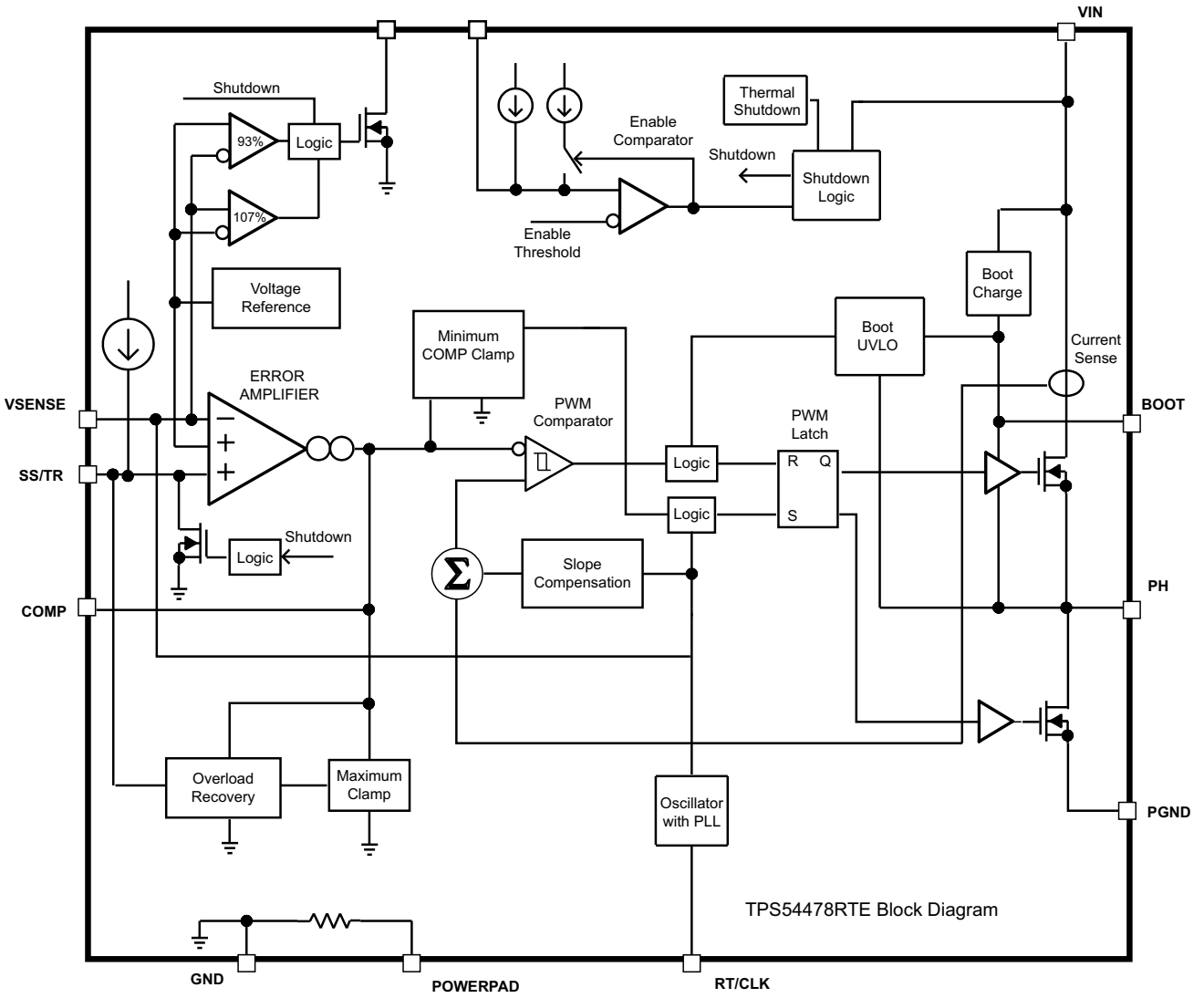
The TPS54478 minimizes excessive output overvoltage transients by taking advantage of the overvoltage power good comparator. When the regulated output voltage is greater than 107% of the nominal voltage, the overvoltage comparator is activated, and the high side MOSFET is turned off and masked from turning on until the output voltage is lower than 105%.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for slow start. The SS/TR pin is discharged before the output power up to ensure a repeatable restart after an overtemperature fault, UVLO fault or disabled condition. To optimize the output startup waveform, two levels of SS current are implemented. The first slope has more current so that the converter can get out of the region requiring small minimum ON time.

To reduce the power dissipation of TPS54478 during overcurrent event, the hiccup protection is implemented beyond the cycle-by-cycle protection. Thermal shutdown prevents the overheat damage of the device.

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7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54478 uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

7.3.2 Slope Compensation and Output Current

The TPS54478 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

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Feature Description (continued)

7.3.3 Bootstrap Voltage (BOOT) and Low Dropout Operation

The TPS54478 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve drop out, the TPS54478 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.2 V. The high side MOSFET is turned off using an UVLO circuit, allowing for the low side MOSFET to conduct when the voltage from BOOT to PH drops below 2.2 V. Since the supply current sourced from the BOOT pin is very low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is very high.

7.3.4 Error Amplifier

The TPS54478 has a transconductance amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.600 V voltage reference. The transconductance of the error amplifier is 225 μA/V during normal operation. When the voltage of VSENSE pin is below 0.600 V and the device is regulating using the SS/TR voltage, the gm is typically greater than 77 μA/V, but less than 225 μA/V. The frequency compensation components are placed between the COMP pin and ground.

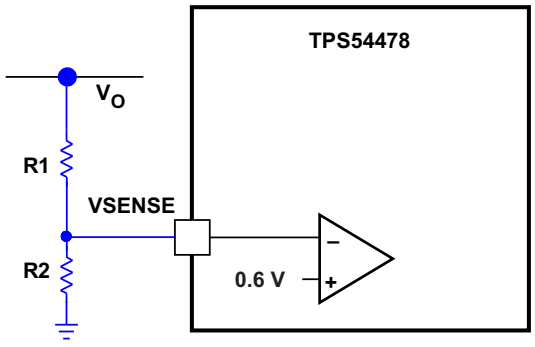
7.3.5 Voltage Reference

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature-stable bandgap circuit. The bandgap and scaling circuits produce 0.600 V at the non-inverting input of the error amplifier.

7.3.6 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 20 kΩ for the R1 resistor and use the Equation 1 to calculate R2. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.6\ V}{V_O - 0.6\ V} \right) \quad (1)$$



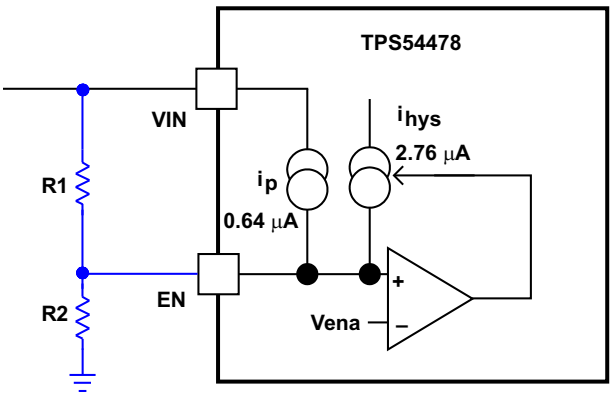
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Figure 21. Voltage Divider Circuit

Feature Description (continued)

7.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54478 is disabled when the VIN pin voltage falls below 2.6 V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 22 to adjust the input voltage UVLO by using two external resistors. It is recommended to use the EN resistors to set the UVLO falling threshold (V_{STOP}) above 2.6 V. The rising threshold (V_{START}) should be set to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pull-up current source that provides the default condition of the TPS54478 operating when the EN pin floats. Once the EN pin voltage exceeds 1.30 V, an additional 2.76 μA of hysteresis is added. When the EN pin is pulled below 1.21 V, the 2.76 μA is removed. This additional current facilitates input voltage hysteresis.



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Figure 22. Adjustable Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (3)$$

Where I_h = 2.76 μA, I_p = 0.64 μA, $V_{ENRISING}$ = 1.30 V, $V_{ENFALLING}$ = 1.21 V

7.3.8 Slow Start / Tracking Pin

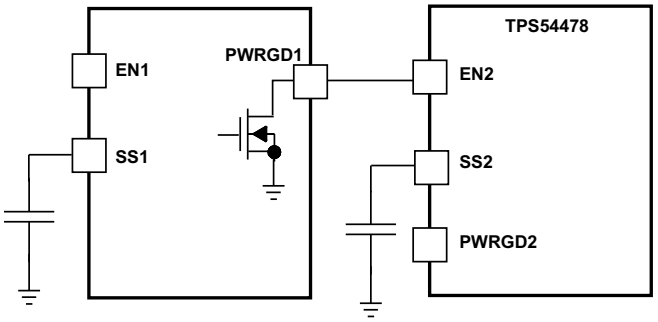
The TPS54478 regulates to the lower of the SS/TR pin and the internal reference voltage. A capacitor on the SS/TR pin to ground implements a slow start time. Before the SS pin reaches the voltage threshold V_{SSTHR}, the charge current is about 45 μA. The TPS54478 internal pull-up current source of 2.2 μA charges the external slow start capacitor after the SS pin voltage exceeds V_{SSTHR}. Equation 4 calculates the required slow start capacitor value where Tss is the desired slow start time in ms and Css is the required capacitance in nF.

$$Css(nF) = 3 \times Tss(mS) \quad (4)$$

If during normal operation, the VIN goes below the UVLO, EN pin pulled below 1.21 V, or a thermal shutdown event occurs, the TPS54478 stops switching. When the VIN goes above UVLO, EN is released or pulled high, or a thermal shutdown is exited, then SS/TR is discharged to below 65 mV before reinitiating a powering up sequence. The VSENSE voltage will follow the SS/TR pin voltage with a 65mV offset up to 90% of the internal voltage reference. When the SS/TR voltage is greater than 90% of the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference.

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Feature Description (continued)



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Figure 23. Sequential Start-Up Sequence

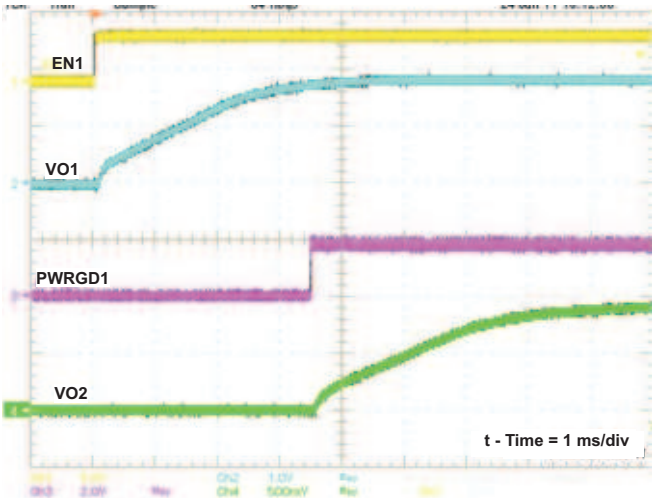
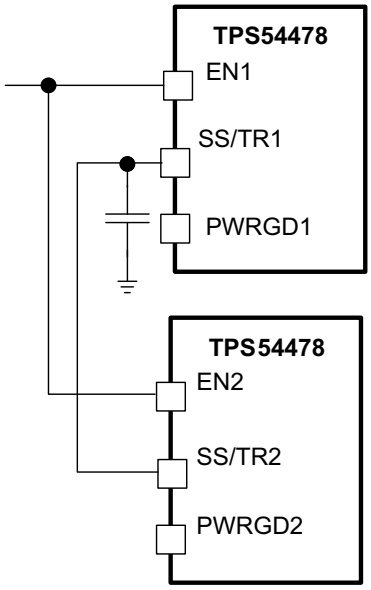


Figure 24. Sequential Startup using EN and PWRGD



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Figure 25. Schematic for Ratio-metric Start-Up Sequence

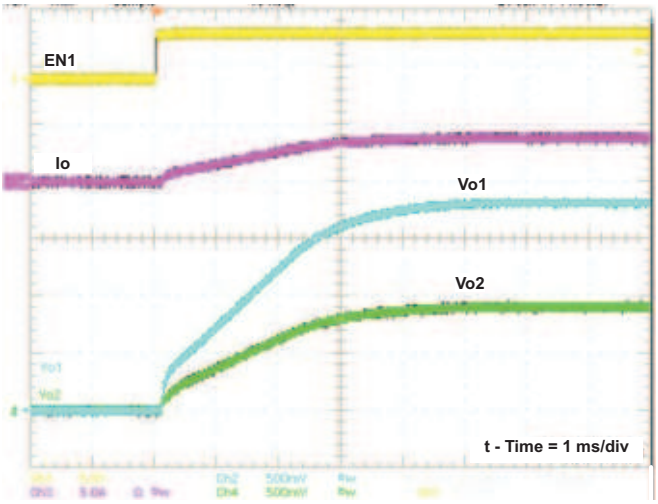


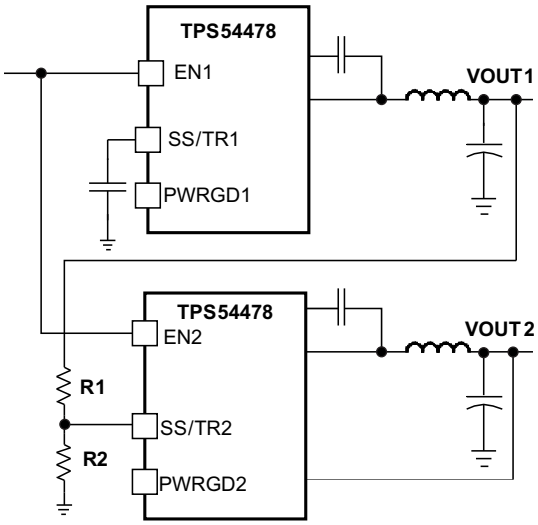
Figure 26. Ratio-metric Startup

Simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 27 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 5 and Equation 6, the tracking resistors can be calculated. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset) in the slow start circuit and the offset created by the pullup current source (Iss) and tracking resistors, the Vssoffset and Iss are included as variables in the equations. As the SS/TR voltage becomes more than 85% of the nominal reference voltage the Vssoffset becomes larger as the slow start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage needs to be greater than 0.86 V for a complete handoff to the internal voltage reference as shown in Figure 28.

Feature Description (continued)

$$R1 = \frac{Vout2}{Vref} \times \frac{Vssoffset}{Iss} \quad (5)$$

$$R2 = \frac{Vref \times R1}{Vout2 - Vref} \quad (6)$$



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Figure 27. Simultaneous Startup Sequence

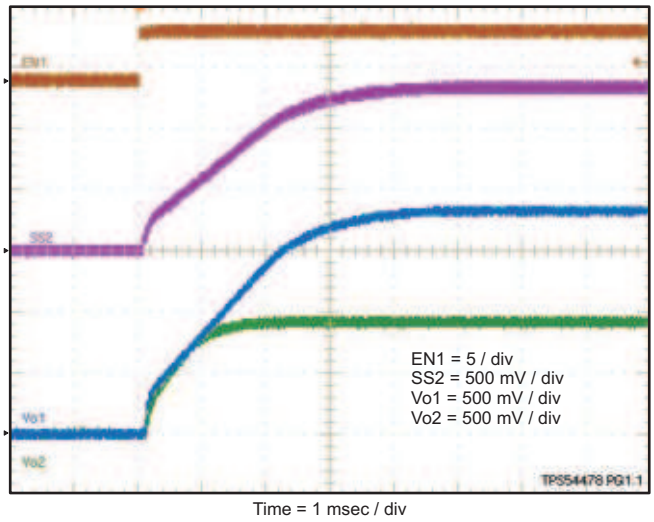


Figure 28. Simultaneous Start-Up using Coupled SS/TR Pins

7.3.9 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54478 is adjustable over a wide range from 200 kHz to 2000 kHz by placing a maximum of 150 kΩ and minimum of 16 kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in Figure 5 or Equation 7.

$$RT\ (k\Omega) = \frac{90066}{Fs(kHz)^{1.135}} \quad (7)$$

$$Fs(kHz) = \frac{23439}{RT(k\Omega)^{0.8813}} \quad (8)$$

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage and minimum controllable on time should be considered.

The minimum controllable on time is typically 100 ns at full current load and 120 ns at no load, and limits the maximum operating input voltage or output voltage.

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Feature Description (continued)

7.3.10 Overcurrent Protection

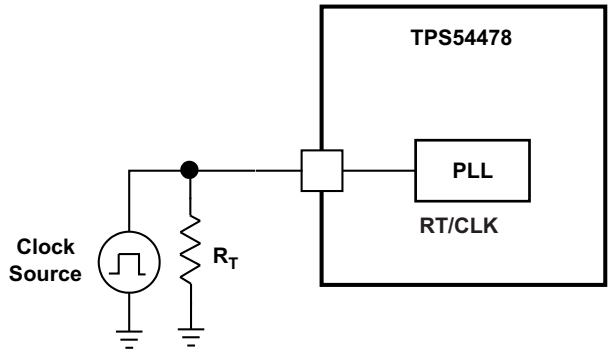
The TPS54478 implements current mode control which uses the COMP pin voltage to turn off the high side MOSFET and turn on the low side MOSFET on a cycle by cycle basis. Each cycle the switch current and the COMP pin voltage are compared, when the peak switch current intersects the COMP voltage the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit. When the OCP reaches 512 cycles, the converter enters hiccup mode in which no switching action happens for about 16000 cycles. This helps the reduction of the power consumption during the over current event.

7.3.11 START-UP into Prebiased Output

The TPS54478 features monotonic startup into pre-biased output. The low side FET turns on for a very short time period every cycle before the output voltage reaches the pre-biased voltage. This ensures the boot cap has enough charge to turn on the top FET when the output voltage reaches the pre-biased voltage. The TPS54478 also implements low side current protection by detecting the voltage over the low side MOSFET. When the converter sinks current through its low side FET is more than 3.1 A, the control circuit will turn the low side FET off. Due to the implemented prebias function, the low side Fet reverse current protection should not be reached, but it provides another layer of protection in the undesired events such as oscillation induced by load.

7.3.12 Synchronize Using the RT/CLK Pin

The RT/CLK pin is used to synchronize the converter to an external system clock. See Figure 29. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on time of at least 75ns. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to the frequency set by the resistor. The square wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V typically. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of the PH is synchronized to the falling edge of RT/CLK pin.



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Figure 29. Synchronizing to a System Clock

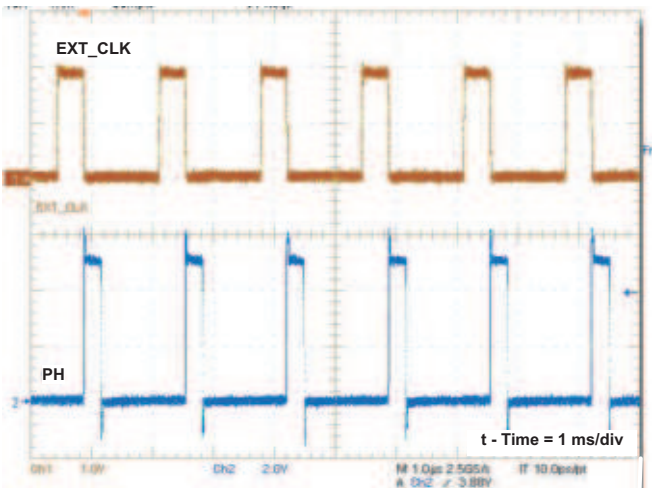


Figure 30. Plot of Synchronizing to System Clock

7.3.13 Power Good (PWRGD Pin)

The PWRGD pin output is an open drain MOSFET. The output is pulled low when the VSENSE voltage enters the fault condition by falling below 93% or rising above 107% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 95% or falls below 105% of the internal voltage reference the PWRGD output MOSFET is turned off. It is recommended to use a pull-up resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 6 V or less. The PWRGD is in a valid state once the VIN input voltage is greater than 1.6 V.

Feature Description (continued)

7.3.14 Overvoltage Transient Protection

The TPS54478 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold which is 107% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold the high side MOSFET is allowed to turn on the next clock cycle.

7.3.15 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 150°C, the device reinitiates the power up sequence by discharging the SS pin to below 65 mV. The thermal shutdown hysteresis is 15°C.

7.3.16 Small Signal Model for Loop Response

Figure 31 shows an equivalent model for the TPS54478 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response without slope compensation effect. The error amplifier is a transconductance amplifier with a gm of 225 μA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R0 and capacitor Co model the open loop gain and frequency response of the amplifier. The 1-mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

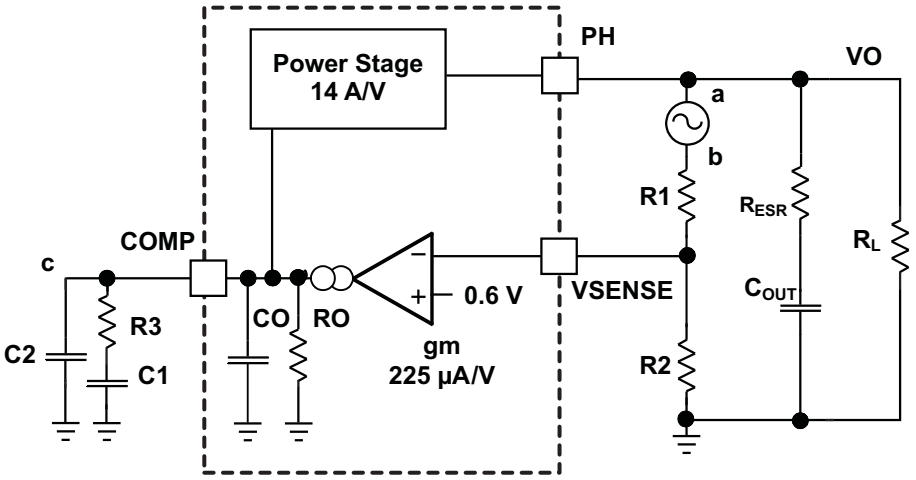


Figure 31. Small Signal Model for Loop Response Without Slope Comp Effect

7.3.17 Simple Small Signal Model for Peak Current Mode Control

Figure 31 is a simple small signal model that can be used to understand how to design the frequency compensation without slope compensation effect. The TPS54478 power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 9 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 31) is the power stage transconductance. The gm for the TPS54478 is 14 A/V. The low frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in Equation 10. As the load current increases and decreases, the low frequency gain decreases and increases,

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Feature Description (continued)

respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current (see Equation 11). The combined effect is highlighted by the dashed line in the right half of Figure 32. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

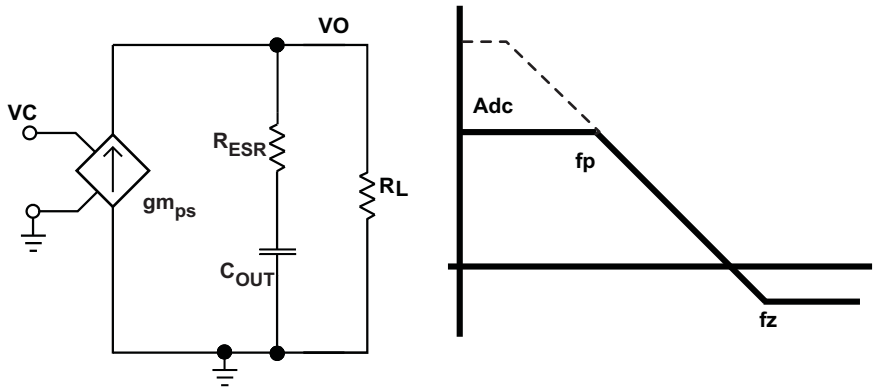


Figure 32. Simple Small Signal Model and Frequency Response for Peak Current Mode Control without Slope Comp Effect

$$\frac{vo}{vc} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \quad (9)$$

$$Adc = gm_{ps} \times R_L \quad (10)$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (11)$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (12)$$

7.3.18 Small Signal Model for Frequency Compensation

The TPS54478 uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in Figure 33. The Type 2 circuits are most likely implemented in high bandwidth power supply designs using low ESR output capacitors. In Type 2A, one additional high frequency pole is added to attenuate high frequency noise.

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Feature Description (continued)

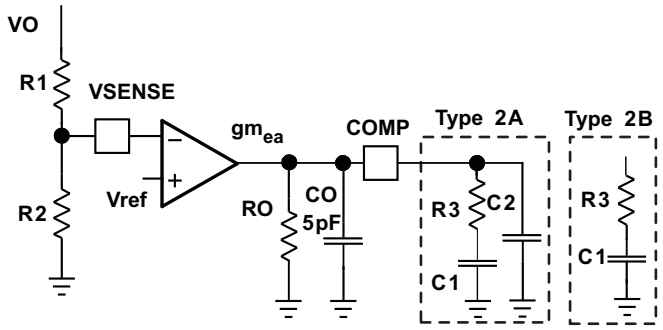


Figure 33. Type-II of Frequency Compensation

The design guidelines for TPS54478 loop compensation are addressed in the *Application Information* section with more details. The approach is to run the Pspice model first to find the accurate response of the power stage with slope compensation effect. The compensation network is then designed based on the desired crossover frequency. The crossover frequency and phase margin are more closer to the measured results when the slope compensation effect is included.

For type-II compensation, the modulator pole, fpmod, and the esr zero, fz1 can be calculated using Equation 13 and Equation 14. Derating the output capacitor (C_{OUT}) is needed if the output voltage is a high percentage of the capacitor rating. Use the capacitor manufacturer information to derate the capacitor value. Use Equation 15 and Equation 16 to estimate a starting point for the crossover frequency, fc. Equation 15 is the geometric mean of the modulator pole and the esr zero and Equation 16 is the mean of modulator pole and the switching frequency. Use the lower value of Equation 15 or Equation 16 as the maximum crossover frequency.

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \tag{13}$$

$$fz\ mod = \frac{1}{2\pi \times Resr \times Cout} \tag{14}$$

$$f_C = \sqrt{fp\ mod \times fz\ mod} \tag{15}$$

$$f_C = \sqrt{fp\ mod \times \frac{fsw}{2}} \tag{16}$$

The type-III compensation is recommended to achieve higher crossover frequency by introducing extra phase lift. By adding a small capacitor C3 in parallel with R1, one-pair of zero and pole is generated as given by Equation 17 and Equation 18. The *Application Information* section provides step-by-step design guidelines for Type-III compensation with the effect of slope compensation included.

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Feature Description (continued)

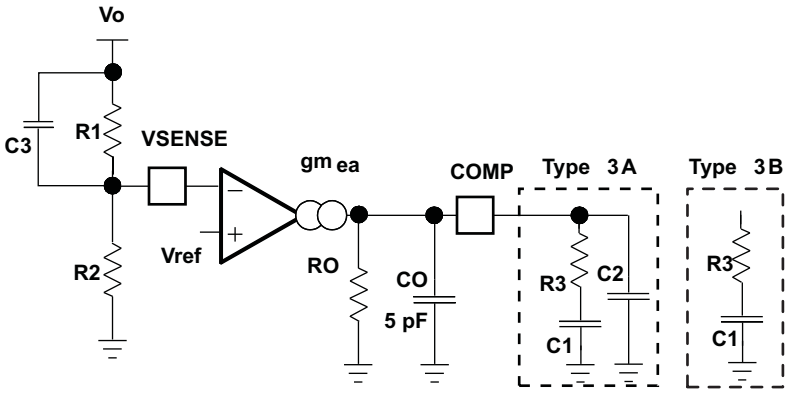


Figure 34. Type-III of Frequency Compensation

$$fz = \frac{1}{2\pi \times R1 \times C3} \quad (17)$$

$$fp = \frac{1}{2\pi \times (R1 // R2) \times C3} \quad (18)$$

7.4 Device Functional Modes

7.4.1 PWM Operation

TPS54478 is a synchronous buck converter. Normal operation occurs when V_{IN} is above 2.95 V and the SS/ENA pins is high to enable the device.

7.4.2 Standby Operation

TPS54478 can be placed in standby when the SS/ENA pin is set low, disabling the device.

7.5 Programming

7.5.1 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins. The sequential method can be implemented using an open drain or collector output of a power on reset pin of another device. Figure 23 shows the sequential method. The PWRGD is coupled to the EN pin on the TPS54478 which enables the second power supply once the primary supply reaches regulation.

Ratio-metric start up can be accomplished by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow start time the pull up current source must be doubled in Equation 4. The ratio metric method is illustrated in Figure 25.

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8 Application and Implementation

NOTE

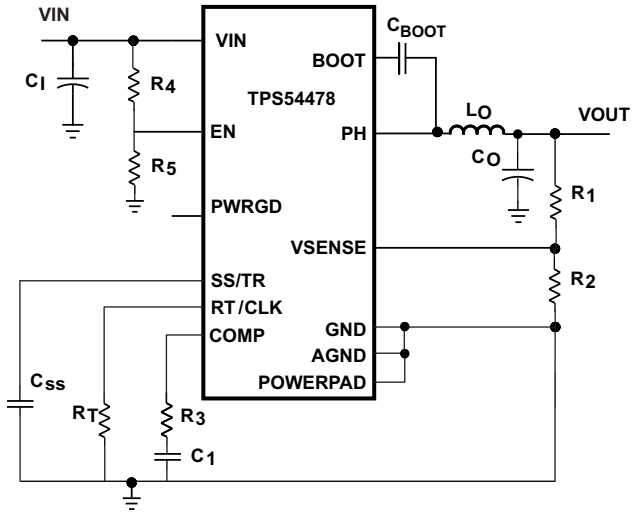
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPS54478 is a synchronous buck converter. It can convert an input voltage of 2.95 V to 6 V to a lower voltage. Maximum output current is 4 A.

8.2 Typical Application

The schematic diagram for this design example is shown in Figure 36. The component reference designators of this schematic are used for the equations in *Detailed Design Procedure*.



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Figure 35. Typical Application

8.2.1 Design Requirements

This example details the design of a high frequency switching regulator design using ceramic output capacitors. This design is available as the TPS54478EVM-037 (PWR037) evaluation module (EVM). A few parameters must be known in order to start the design process. These parameters are typically determined on the system level. For this example, start with the following known parameters:

Table 1. Design Parameters

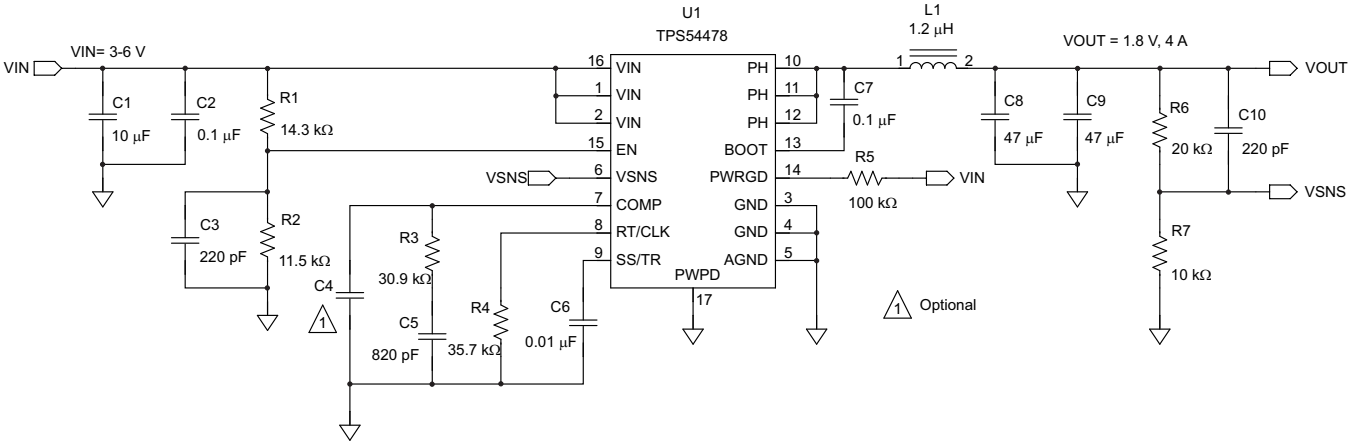
DESIGN PARAMETER	EXAMPLE VALUE
Output Voltage	1.8 V
Transient Response 1 A to 3.0 A load step	ΔVout = 3%
Maximum Output Current	4 A
Input Voltage	3 V to 6 V, 5 V nominal
Output Voltage Ripple	< 30 mV p-p
Switching Frequency (Fsw)	1000 kHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, choose the highest switching frequency possible since this produces the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the converter's performance. The converter is capable of running from 300 kHz to 2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 1 MHz is selected to achieve both a small solution size and a high efficiency operation. Using Equation 7, R4 is calculated to be 35.4 kΩ. A standard 1% 35.7 kΩ value was chosen in the design.



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Figure 36. High Frequency, 1.8 V Output Power Supply Design with Adjusted UVLO

8.2.2.2 Output Inductor Selection

The inductor selected works for the entire TPS54478 input voltage range. To calculate the value of the output inductor, use Equation 19. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use K_{IND} = 0.3 and the inductor value is calculated to be 1.05 µH. For this design, a nearest standard value was chosen: 1.2 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 21 and Equation 22.

For this design, the RMS inductor current is 4.01 A and the peak inductor current is 4.53 A. The chosen inductor is a Coilcraft XAL5030-122ME. It has a saturation current rating of 11.8 A (20% inductance loss) and a RMS current rating of 8.7 A (20 °C temperature rise). The series resistance is 6.78 mΩ typical.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \quad (19)$$

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \quad (20)$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw} \right)^2} \quad (21)$$

$$ILpeak = Iout + \frac{Iripple}{2} \quad (22)$$

8.2.2.3 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 23 shows the minimum output capacitance necessary to accomplish this.

For this example, the transient load response is specified as a 3% change in Vout for a load step from 1 A (25% load) to 3 A (75% load). For this example, ΔIout = 3 – 1 = 2.0 A and ΔVout = 0.03 × 1.8 = 0.054 V. Using these numbers gives a minimum capacitance of 74.1 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 24 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 24 yields 4.4 uF.

$$Co > \frac{2 \times \Delta Iout}{fsw \times \Delta Vout} \quad (23)$$

where

- ΔIout is the change in output current, *f*sw is the regulators switching frequency and ΔVout is the allowable change in the output voltage.

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \quad (24)$$

Equation 25 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 25 indicates the ESR should be less than 28.6 mΩ. In this case, the ESR of the ceramic capacitor is much less than 28.6 mΩ.

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, two 47 µF 10 V X5R ceramic capacitors with 3 mΩ of ESR are used. The estimated capacitance after derating is 2 x 45 µF = 90 µF.

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Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. Equation 26 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 26 yields 303 mA.

$$Resr < \frac{Voripple}{Iripple} \tag{25}$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \tag{26}$$

8.2.2.4 Input Capacitor

The TPS54478 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54478. The input ripple current can be calculated using Equation 27.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 10 V voltage rating is required to support the maximum input voltage. For this example, one 10 µF and one 0.1 µF 10 V capacitors in parallel have been selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 28. Using the design example values, Ioutmax = 4 A, Cin = 10 µF, Fsw = 1 MHz, yields an input voltage ripple of 99 mV and a rms input ripple current of 1.95 A.

$$Icirms = Iout \times \sqrt{\frac{Vout}{Vinmin} \times \frac{(Vinmin - Vout)}{Vinmin}} \tag{27}$$

$$\Delta Vin = \frac{Ioutmax \times 0.25}{Cin \times fsw} \tag{28}$$

8.2.2.5 Slow Start Capacitor

The slow start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54478 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow start capacitor value can be calculated using Equation 29. For the example circuit, the slow start time is not too critical since the output capacitor value is 2 x 47 µF which does not require much current to charge to 1.8 V. The example circuit has the slow start time set to an arbitrary value of 3.33 ms which requires a 10 nF capacitor.

$$C6(nF) = 3 \cdot Tss(mS) \tag{29}$$

8.2.2.6 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

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8.2.2.7 Output Voltage and Feedback Resistors Selection

For the example design, 10.0 kΩ was selected for R7. Using Equation 30, R6 is calculated as 20.0 kΩ. The nearest standard 1% resistor is 20.0 kΩ.

$$R6 = R7 \cdot \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{30}$$

Due to the internal design of the TPS54478, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.6 V. Above 0.6 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by Equation 31:

$$Voutmin = Ontimemin \times Fsmax \times (Vinmax - Ioutmin \times RDSmin) - Ioutmin \times (RL + RDSmin) \tag{31}$$

where

- Voutmin = minimum achievable output voltage
- Ontimemin = minimum controllable on-time (100 ns typical. 120 ns no load)
- Fsmax = maximum switching frequency including tolerance
- Vinmax = maximum input voltage
- Ioutmin = minimum load current
- RDSmin = minimum high-side MOSFET on resistance (see *Electrical Characteristics*)
- RL = series resistance of output inductor

There is also a maximum achievable output voltage which is limited by the minimum off time. The maximum output voltage is given by Equation 32:

$$Voutmax = Vin \times \left(1 - \frac{Offtimemax}{ts}\right) - Ioutmax \times (RDSmax + RI) - (0.7 - Ioutmax \times RDSmax) \times \left(\frac{tdead}{ts}\right) \tag{32}$$

where

- Voutmax = maximum achievable output voltage
- Vin = minimum input voltage
- Offtimemax = maximum off time (180 ns typical for adequate margin)
- ts = 1/Fs
- Ioutmax = maximum current
- RDSmax = maximum high-side MOSFET on resistance (see *Electrical Characteristics*)
- RI = DCR of the inductor
- tdead = dead time (40 ns)

8.2.2.8 Compensation

There are several possible methods to design closed loop compensation for dc/dc converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at -20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and starts to fall one decade above the modulator pole frequency reaching a minimum of -90 degrees one decade above the modulator pole frequency. The modulator pole is a simple pole shown in Equation 33.

$$F_{PMOD} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot R_{OUT}} \tag{33}$$

For the TPS54478 most circuits will have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics will deviate from the ideal approximations. The phase loss of the power stage will now approach -180 degrees, making compensation more difficult. The power stage transfer function can be solved but it is a tedious hand calculation that does not lend itself to simple approximations. It is best to use Pspice or TINA-TI to accurately model the power stage gain and phase so that a

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reliable compensation circuit can be designed. That is the technique used in this design procedure. Using the pspice model of SLVM279 apply the values calculated previously to the output filter components of L1, C9, and C10. Set Rload to the appropriate value. For this design, L1 = 1.2 µH. C8 and C9 use the derated capacitance value of 45 µF, and the ESR is set to 3 mΩ. The Rload resistor is 1.8 / 4 = 450 mΩ. Now the power stage characteristic can be plotted as shown in Figure 37.

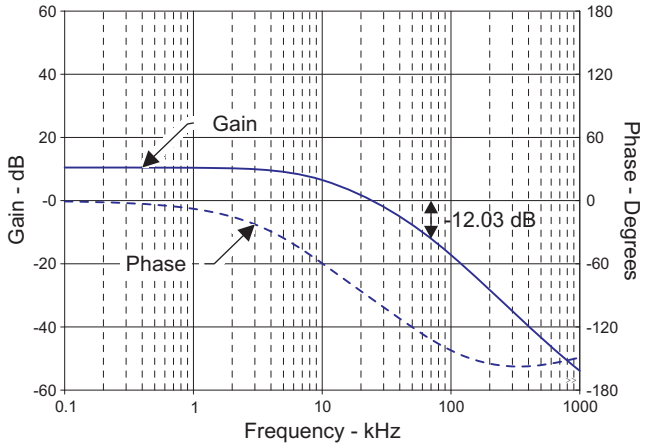


Figure 37. Power Stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 70 kHz. From the power stage gain and phase plots, the gain at 70 kHz is -12.03 dB and the phase is -131.86 degrees. For 60 degrees of phase margin, additional phase boost from a feed forward capacitor in parallel with the upper resistor of the voltage set point divider will be required. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. The required value of R3 can be calculated from Equation 34.

$$R3 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{EA}} \cdot \sqrt{\frac{V_{out}}{V_{REF}}} \tag{34}$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 70 kHz. The required value for C5 is given by Equation 35.

$$C5 = \frac{1}{2 \cdot \pi \cdot R3 \cdot \frac{F_{CO}}{10}} \tag{35}$$

To maximize phase gain the high frequency pole is not implemented and C4 is not populated. The pole can be useful to offset the ESR of aluminum electrolytic output capacitors. If desired the value for C4 can be calculated from Equation 36.

$$C4 = \frac{1}{2 \cdot \pi \cdot R3 \cdot F_P} \tag{36}$$

For maximum phase boost, the pole frequency F_P will typically be one decade above the intended crossover frequency F_{CO}.

The feed forward capacitor C10, is used to increase the phase boost at crossover above what is normally available from Type II compensation. It places an additional zero/pole pair located at Equation 37 and Equation 38.

$$F_Z = \frac{1}{2 \cdot \pi \cdot C10 \cdot R6} \tag{37}$$

$$F_P = \frac{1}{2 \cdot \pi \cdot C10 \cdot R6 \,||\, R7} \tag{38}$$

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This zero and pole pair is not independent. Once the zero location is chosen, the pole is fixed as well. For optimum performance, the zero and pole should be located symmetrically about the intended crossover frequency. The required value for C10 can calculated from Equation 39.

$$C10 = \frac{1}{2 \cdot \pi \cdot R6 \cdot F_{CO} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (39)$$

For this design the calculated values for the compensation components are R3 = 30.6 kΩ ,C5 = 736 pF and C10 = 197 pF. Using standard values, the compensation components are R3 = 30.9 kΩ ,C5 = 820 pF and C10 = 220 pF.

8.2.3 Application Curves

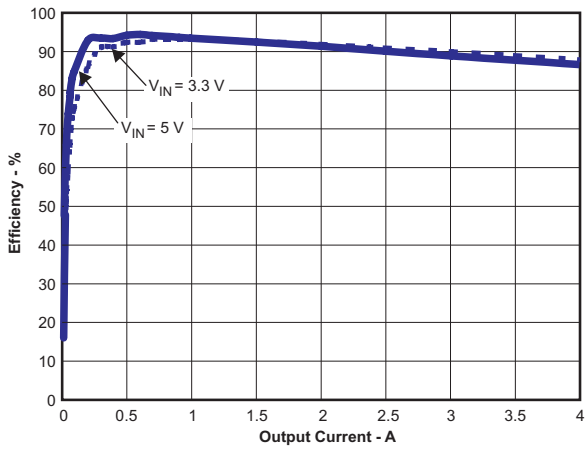


Figure 38. Efficiency vs Load Current

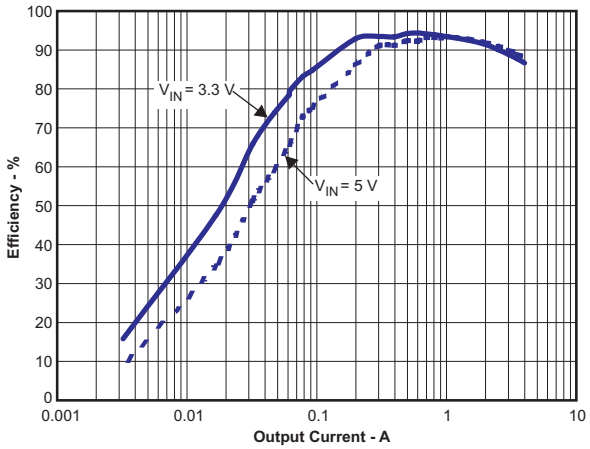
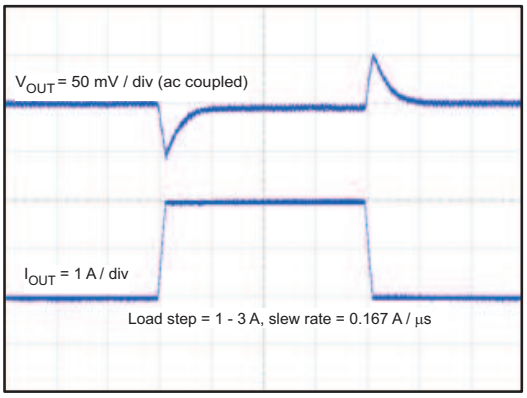
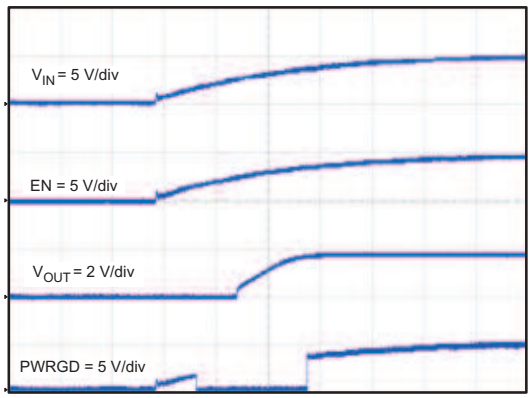


Figure 39. Efficiency vs Load Current



Time = 100 µs/div

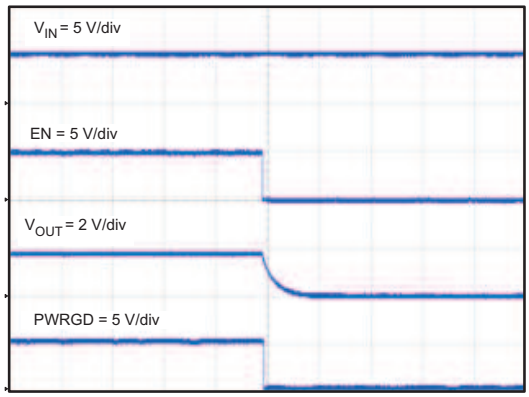
Figure 40. Transient Response, 2 A Step



Time = 2 ms/div

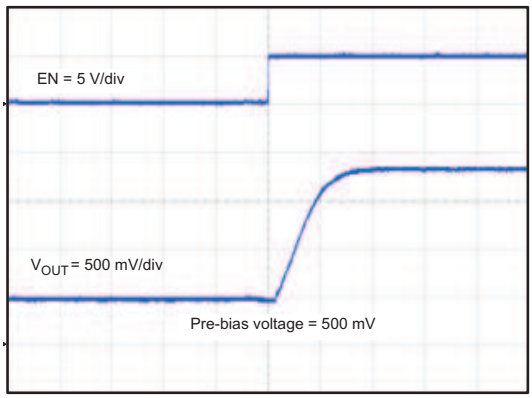
Figure 41. Power Up VOUT, VIN

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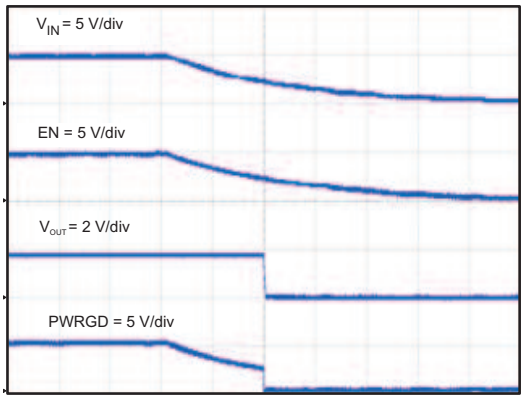
Time = 2 ms/div

Figure 42. Power Up VOUT, EN



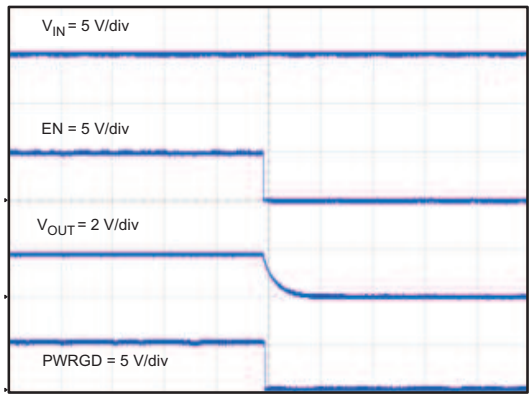
Time = 2 msec / div

Figure 43. Power Up into Prebias Voltage



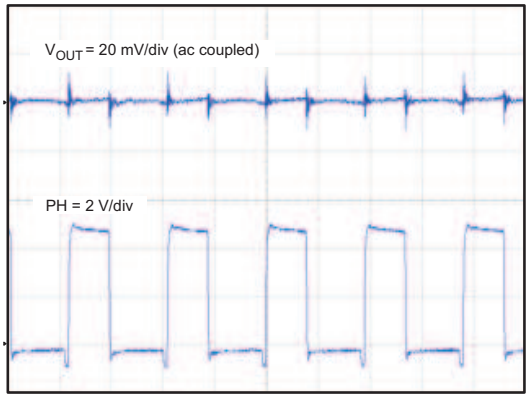
Time = 2 ms/div

Figure 44. Power Down VOUT, VIN



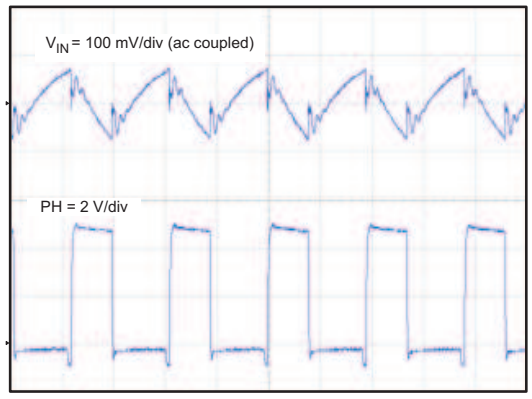
Time = 2 ms/div

Figure 45. Power Down VOUT, EN



Time = 500 ns/div

Figure 46. Output Ripple, I_{OUT} = 4 A



Time = 500 ns/div

Figure 47. Input Ripple, I_{OUT} = 4 A

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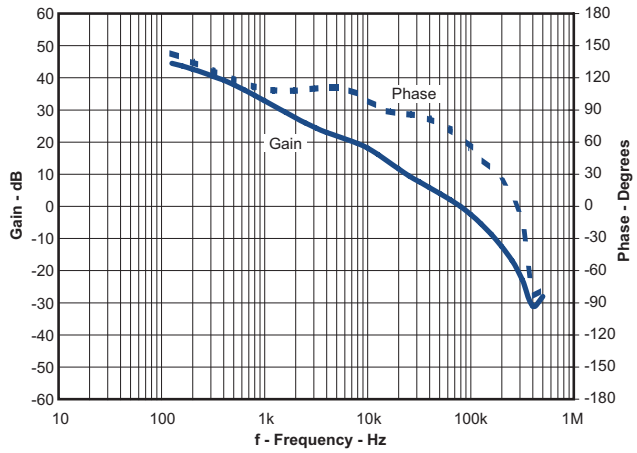


Figure 48. Closed Loop Response, V_{IN} = 5 V, I_{OUT} = 4 A

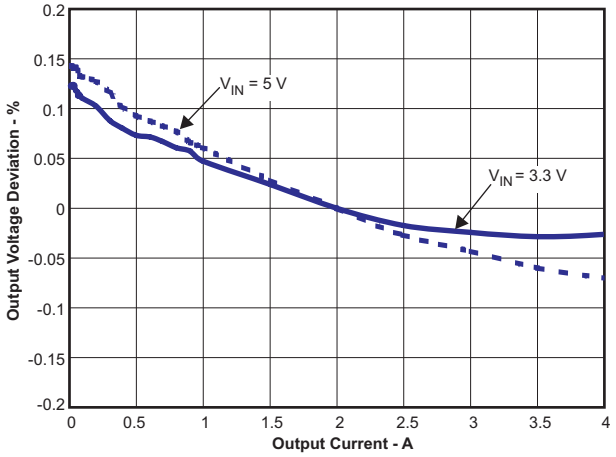


Figure 49. Output Voltage Regulation vs Load Current

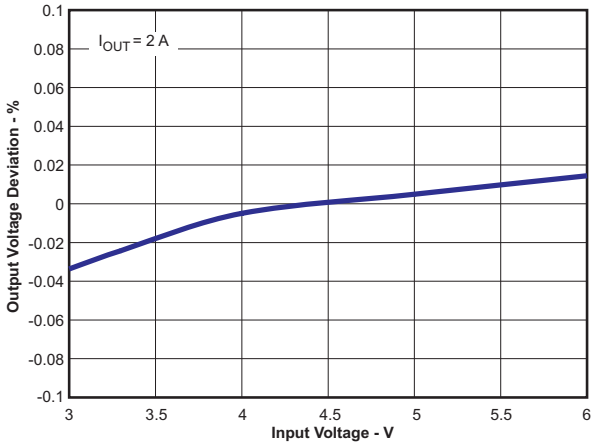
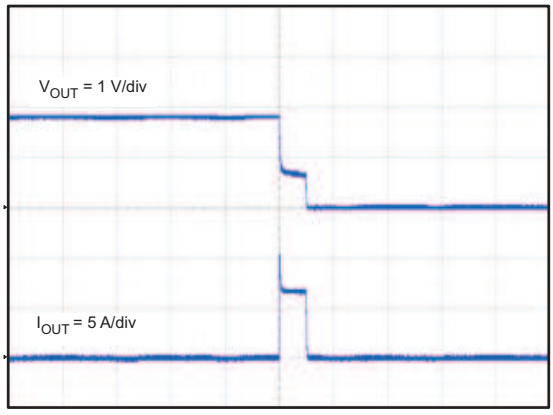
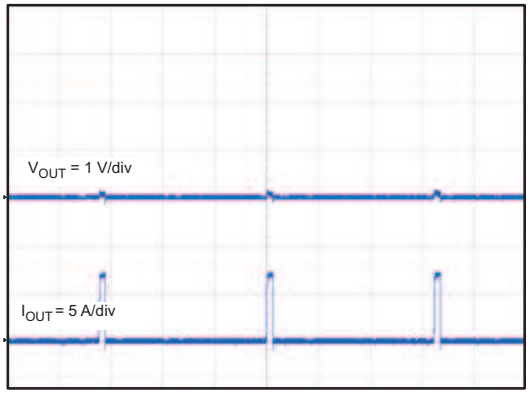


Figure 50. Output Voltage Regulation vs Input Voltage



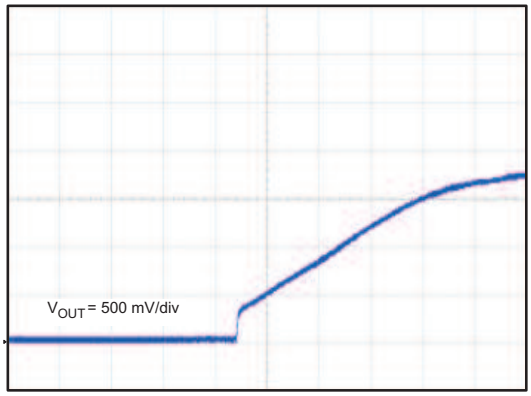
Time = 1 ms/div

Figure 51. Hiccup Mode Current Limit



Time = 5 ms/div

Figure 52. Hiccup Mode Current Limit



Time = 500 µs/div

Figure 53. Start Up Characteristic

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 2.95 V and 6 V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

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10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. Care should be taken to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 54 for a PCB layout example. The GND pins and AGND pin should be tied directly to the power pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors. For operation at full rated load, the top side ground area along with any additional internal ground planes must provide adequate heat dissipating area.

Locate the input bypass capacitor as close to the IC as possible. The PH pin should be routed to the output inductor. Since the PH connection is the switching node, the output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation components, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace as shown. The RT/CLK pin is particularly sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

10.2 Layout Example

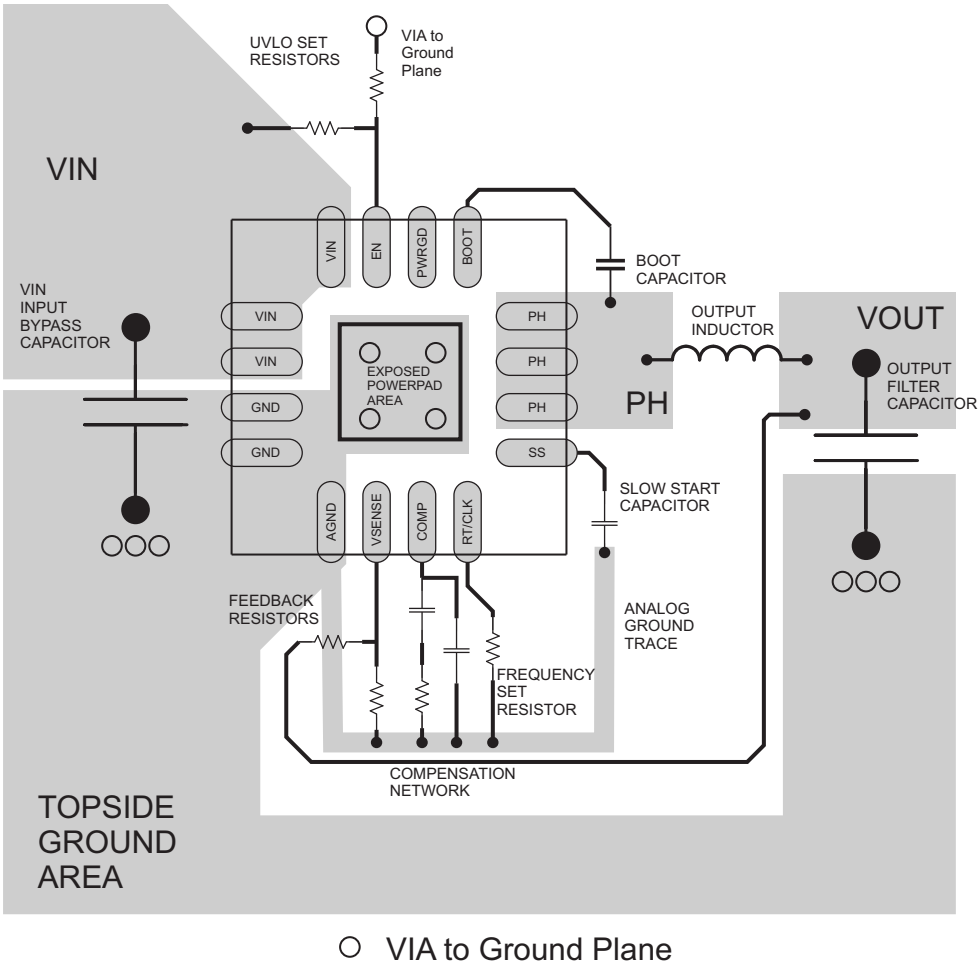


Figure 54. PCB Layout Example

10.3 Power Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous conduction mode (CCM) operation. The power dissipation of the IC (Ptot) includes conduction loss (Pcon), dead time loss (Pd), switching loss (Psw), gate drive loss (Pgd) and supply current loss (Pq).

$$Pcon = Io^2 \times R_{DS_on_Temp}$$

$$Pd = f_{sw} \times Io \times 0.7 \times 40 \times 10^{-9}$$

$$Psw = 1/2 \times V_{in} \times Io \times f_{sw} \times 7 \times 10^{-9}$$

$$Pgd = 2 \times V_{in} \times f_{sw} \times 6 \times 10^{-9}$$

$$Pq = V_{in} \times 525 \times 10^{-6}$$

Where:

I_O is the output current (A).
$R_{DS_on_Temp}$ is the on-resistance of the high-side MOSFET with given temperature (Ω).
V_{in} is the input voltage (V).
f_{sw} is the switching frequency (Hz).

So

$$Ptot = Pcon + Pd + Psw + Pgd + Pq$$

For given T_A,

$$T_J = T_A + Rth \times Ptot$$

For given T_{JMAX} = 150°C

$$T_{Amax} = T_{Jmax} - Rth \times Ptot$$

Where:

Ptot is the total device power dissipation (W).
T_A is the ambient temperature (°C).
T_J is the junction temperature (°C).
Rth is the thermal resistance of the package (°C/W).
T_{JMAX} is maximum junction temperature (°C).
T_{AMAX} is maximum ambient temperature (°C).

There are additional power losses in the regulator circuit due to the inductor AC and DC losses and trace resistance that impact the overall efficiency of the regulator.

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11 Device and Documentation Support

11.1 Device Support

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11.1.2 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54478 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- For SWIFT™ documentation, see the TI website at www.ti.com/swift
- *TPS54478EVM-037 4-A, SWIFT™ Regulator Evaluation Module* User's Guide (SLVU470)

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11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54478RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54478
TPS54478RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54478
TPS54478RTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54478
TPS54478RTET.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54478
TPS54478RTETG4	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54478
TPS54478RTETG4.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54478

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

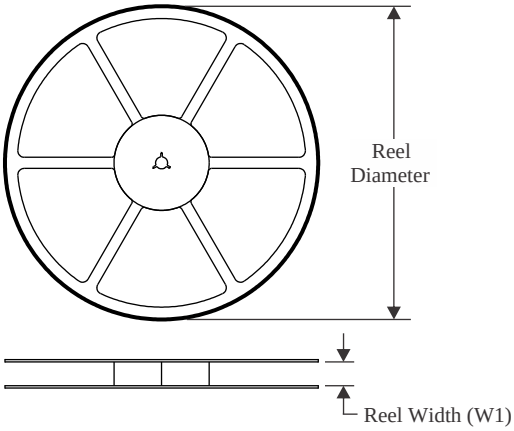
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

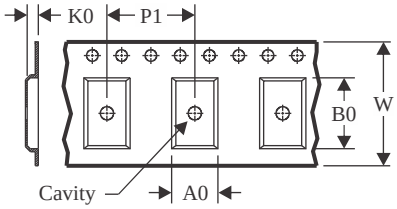
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

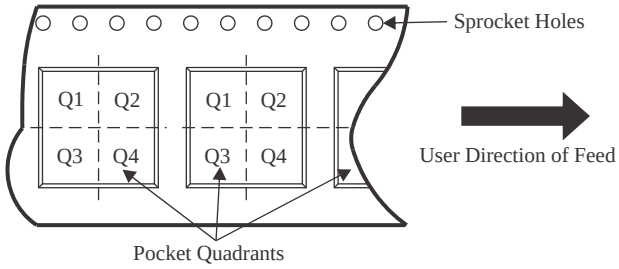


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

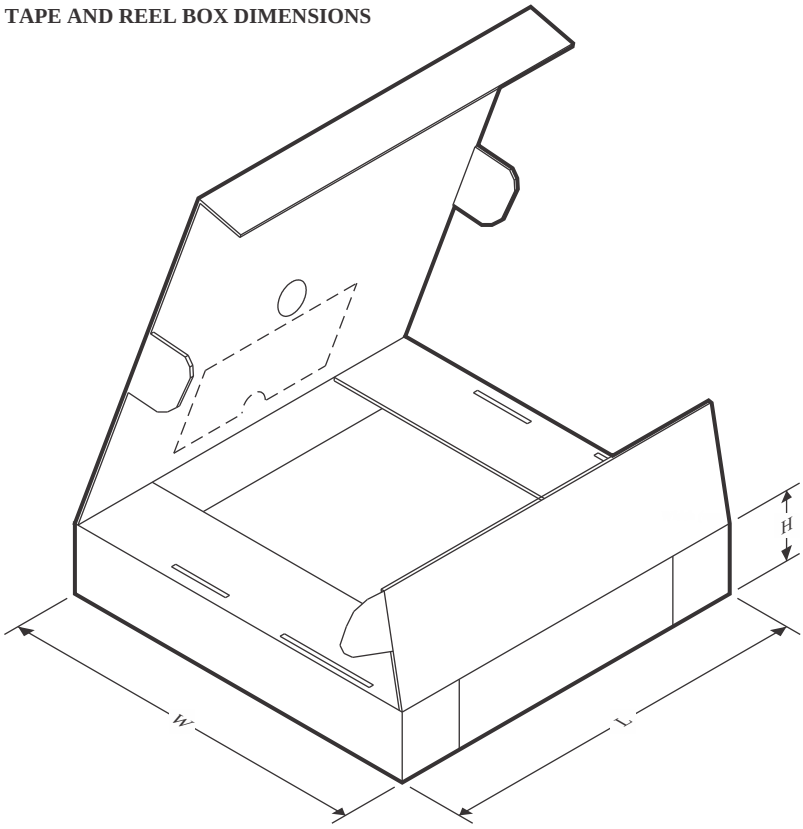
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54478RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54478RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54478RTETG4	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54478RTER	WQFN	RTE	16	3000	353.0	353.0	32.0
TPS54478RTET	WQFN	RTE	16	250	213.0	191.0	35.0
TPS54478RTETG4	WQFN	RTE	16	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

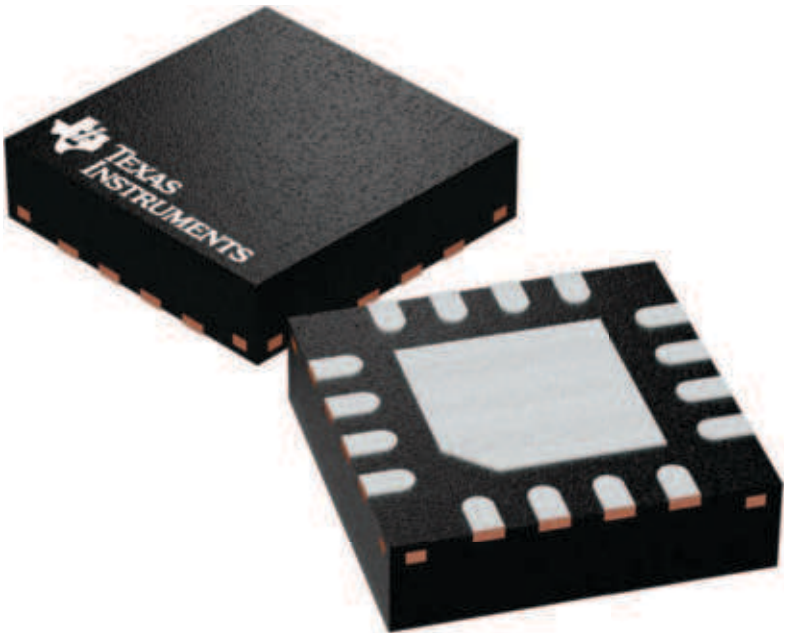
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



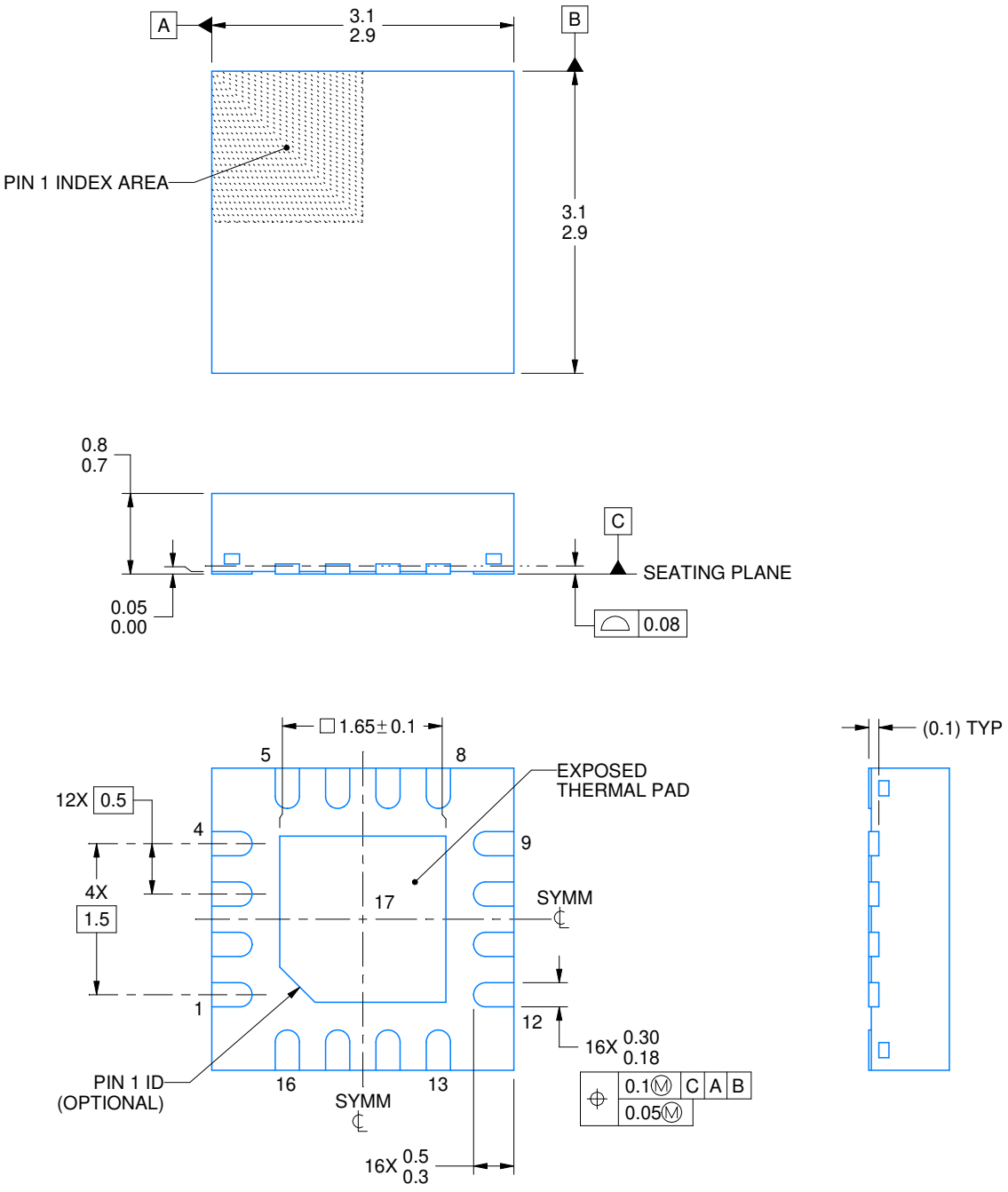
4225944/A

RTE0016F

PACKAGE OUTLINE

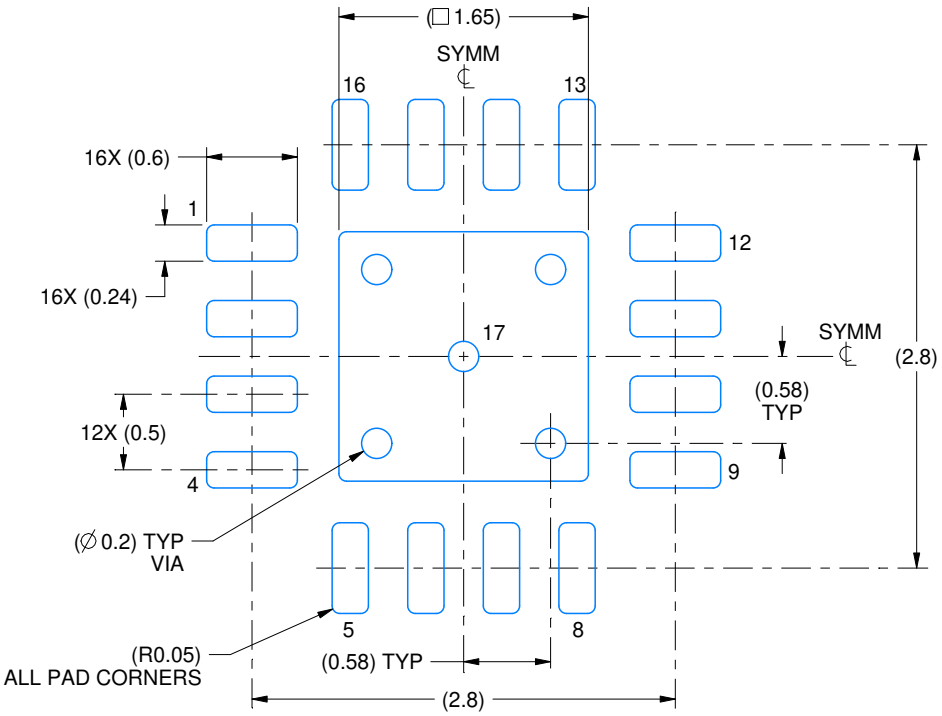
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

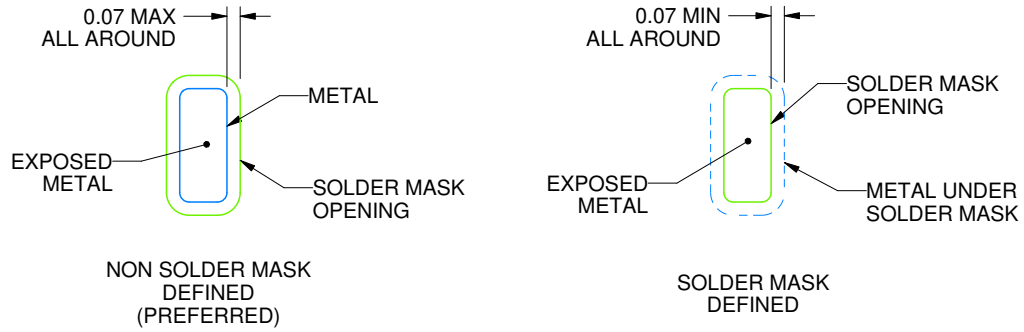


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

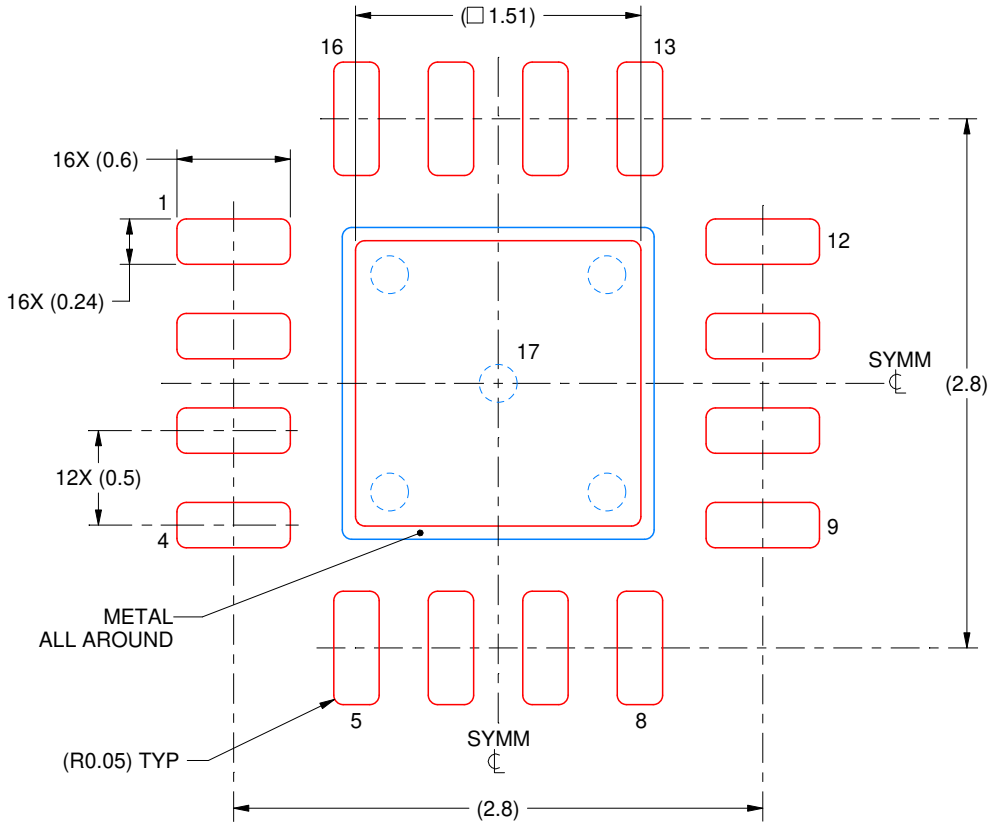


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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