3-V TO 6-V INPUT, 6-A OUTPUT TRACKING SYNCHRONOUS BUCK PWM SWITCHER WITH INTEGRATED FETs (SWIFT™) FOR SEQUENCING

Check for Samples: TPS54680-EP

FEATURES

- **Power Up/Down Tracking For Sequencing**
- **30-mΩ, 12-A Peak MOSFET Switches for High Efficiency at 6-A Continuous Output Source or Sink Current**
- **Wide PWM Frequency: Fixed 350 kHz or Adjustable 280 kHz to 700 kHz**
- **Power Good and Enable**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Integrated Solution Reduces Board Area and Component Count**

APPLICATIONS

- **Low-Voltage, High-Density Distributed Power Systems**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors Requiring Sequencing**
- **Broadband, Networking and Optical Communications Infrastructure**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Rated From –55°C to 125°C**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

DESCRIPTION

As a member of the SWIFT™ family of dc/dc regulators, the TPS54680 low-input voltage high-output current synchronous buck PWM converter integrates all required active components. Using the TRACKIN pin with other regulators, simultaneous power up and down are easily implemented. Included on the substrate with the listed features are a true, high performance, voltage error amplifier that enables maximum performance and flexibility in choosing the output filter L and C components; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally or externally set slow-start circuit to limit inrush currents; and a power good output useful for processor/logic reset.

The TPS54680 is available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

ORDERING INFORMATION(1)

T_J	OUTPUT VOLTAGE	PACKAGE	PART NUMBER	VID NUMBER
–40°C to 125°C	0.9 V to 3.3 V	Plastic HTSSOP (PWP)(2)	TPS54680QPWPREP	V62/04641-01XE
–55°C to 125C	0.9 V to 3.3 V	Plastic HTSSOP (PWP)(2)	TPS54680MPWPREP	V62/04641-02XE
			TPS54680MPWPEP	V62/04641-02XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) See the application section of the data sheet for PowerPAD drawing and layout information.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

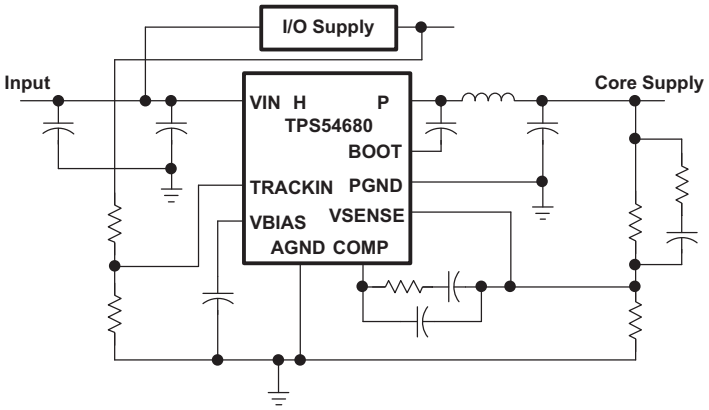
SWIFT, PowerPAD are trademarks of Texas Instruments.

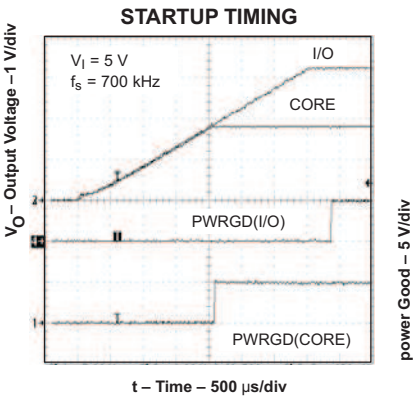
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS54680-EP	UNIT
Input voltage range, V_I	VIN, ENA	–0.3 V to 7 V	V
	RT	–0.3 V to 6 V	
	VSENSE, TRACKIN	–0.3 V to 4V	
	BOOT	–0.3 V to 17 V	
Output voltage range, V_O	VBIAS, COMP, PWRGD	–0.3 V to 7 V	V
	PH	–0.6 V to 10 V	
Source curren, I_O	PH	Internally Limited	
	COMP, VBIAS	6	mA
Sink current, I_S	PH	12	A
	COMP	6	mA
	ENA, PWRGD	10	
Voltage differential	AGND to PGND	±0.3	V
Operating virtual junction temperature range, T_J		–55 to 150	°C
Storage temperature, T_{stg}(2)		–65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, V_I	3		6	V

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THERMAL INFORMATION

THERMAL METRIC[1]		TPS54680 PWP 28 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	36.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	15.5	
θ_{JB}	Junction-to-board thermal resistance[4]	13.1	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.4	
ψ_{JB}	Junction-to-board characterization parameter[6]	12.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPS54680Q			TPS54680M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY VOLTAGE, VIN									
	Input voltage range, VIN		3.0		6.0	3.0		6.0	V
$I_{(Q)}$	Quiescent current	f_s = 350 kHz, RT open, PH pin open		11	15.8		11	15.8	mA
		f_s = 500 kHz, RT = 100 kΩ, PH pin open		16	23.5		16	23.5	
		Shutdown, ENA = 0 V		1	1.4		1	1.4	
UNDER VOLTAGE LOCK OUT									
	Start threshold voltage, UVLO			2.95	3.0		2.95	3.0	V
	Stop threshold voltage, UVLO		2.70	2.80		2.70	2.80		V
	Hysteresis voltage, UVLO		0.14	0.16		0.093	0.16		V
	Rising and falling edge deglitch, UVLO[1]			2.5			2.5		µs
BIAS VOLTAGE									
	Output voltage, VBIAS	$I_{(VBIAS)}$ = 0	2.70	2.80	2.90	2.70	2.80	2.90	V
	Output current, VBIAS[2]				100			100	µA
CUMULATIVE REFERENCE									
V_{ref}	Accuracy		0.882	0.891	0.900	0.879	0.891	0.900	V
REGULATION									
	Line regulation[1][3]	I_L = 3 A, f_s = 350 kHz, T_J = 85°C			0.04			0.04	%/V
		I_L = 3 A, f_s = 550 kHz, T_J = 85°C			0.04			0.04	
	Load regulation[1][3]	I_L = 0 A to 6 A, f_s = 350 kHz, T_J = 85°C			0.03			0.03	%/A
		I_L = 0 A to 6 A, f_s = 550 kHz, T_J = 85°C			0.03			0.03	

(1) Specified by design from -40°C to 85°C.
(2) Static resistive loads only
(3) Specified by the circuit used in Figure 10

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TPS54680Q			TPS54680M			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY VOLTAGE, VIN								
OSCILLATOR								
Internally set – free running frequency	RT open	280	350	450	244	350	450	kHz
Externally set – free running frequency range	RT = 180 kΩ (1% resistor to AGND)	252	280	308	252	280	320	kHz
	RT = 100 kΩ (1% resistor to AGND)	460	500	540	432	500	540	
	RT = 68 kΩ (1% resistor to AGND)	663	700	762	656	700	762	
Ramp valley(4)			0.75			0.75		V
Ramp amplitude (peak-to-peak)(4)			1			1		V
Minimum controllable on time(4)				200			230	ns
Maximum duty cycle		90			90			%
ERROR AMPLIFIER								
Error amplifier open loop voltage gain	1 kΩ COMP to AGND(4)	90	110		90	110		dB
Error amplifier unity gain bandwidth	Parallel 10 kΩ, 160 pF COMP to AGND(4)	3	5		3	5		MHz
Error amplifier common mode input voltage range	Powered by internal LDO(4)	0		VBIAS	0		VBIAS	V
Input bias current, VSENSE	VSENSE = V_{ref}		60	250		60	300	nA
Output voltage slew rate (symmetric), COMP		1	1.4			1.4		V/µs
PWM COMPARATOR								
PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime)	10-mV overdrive(4)		70	85		70	85	ns
ENABLE								
Enable threshold voltage, ENA		0.82	1.20	1.40	0.82	1.20	1.40	V
Enable hysteresis voltage, ENA			0.03			0.03		V
Falling edge deglitch, ENA(4)			2.5			2.5		µs
Leakage current, ENA	V_I = 5.5 V			1			1.6	µA
POWER GOOD								
Power good threshold voltage	VSENSE falling		90			90		%V_{ref}
Power good hysteresis voltage(4)			3			3		%V_{ref}
Power good falling edge deglitch(4)			35			35		µs
Output saturation voltage, PWRGD	$I_{(sink)}$ = 2.5 mA		0.18	0.3		0.18	0.3	V
Leakage current, PWRGD	V_I = 5.5 V			1			1	µA
CURRENT LIMIT								
Current limit trip point	V_I = 3 V Output shorted(4)	7.2	10		6.5	10		A
	V_I = 6 V Output shorted(4)	10	12		6.6	12		
Current limit leading edge blanking time			100			100		ns
Current limit total response time			200			200		ns
THERMAL SHUTDOWN								
Thermal shutdown trip point(4)		135	150	165	135	150	165	°C
Thermal shutdown hysteresis(4)			10			10		°C

(4) Specified by design from -40°C to 85°C.

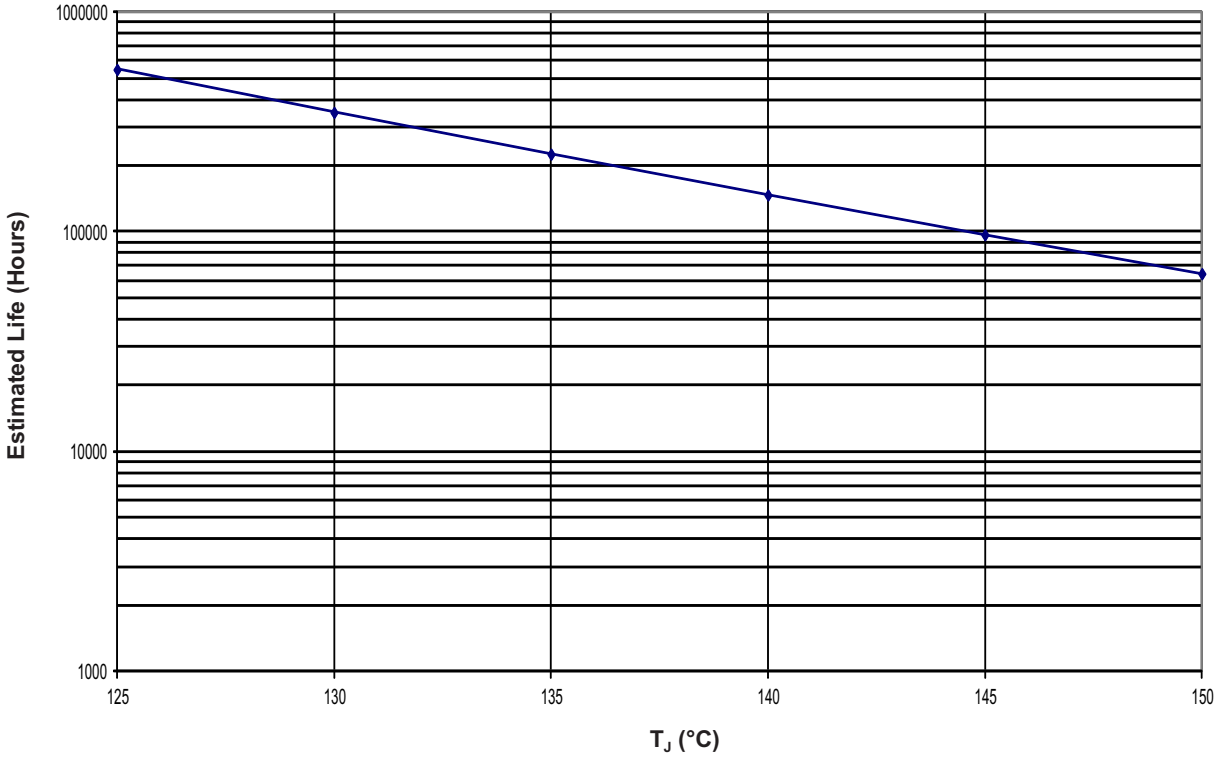
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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TPS54680Q			TPS54680M			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY VOLTAGE, VIN								
OUTPUT POWER MOSFETS								
$r_{DS(on)}$ Power MOSFET switches	V_I = 6 V(5)		26	47		26	47	mΩ
	V_I = 3 V(5)		36	65		36	65	
TRACKIN								
Input offset, TRACKIN	V_{SENSE} = TRACKIN = 0.75 V	–2.5		2.5	–2.5		2.5	mV
Input voltage range, TRACKIN	See (6)	0		V_{ref}	0		V_{ref}	V

(5) Matched MOSFETs low-side $r_{DS(on)}$ production tested, high-side $r_{DS(on)}$ specified by design
(6) Specified by design from -40°C to 85°C.



A. See datasheet for absolute maximum and minimum recommended operating conditions.

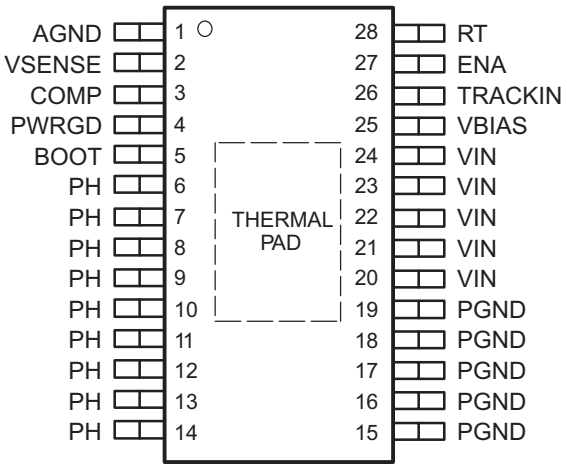
B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. TPS54680-EP Wirebond Life Derating Chart

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PWP PACKAGE
(TOP VIEW)

PWP PACKAGE
(TOP VIEW)

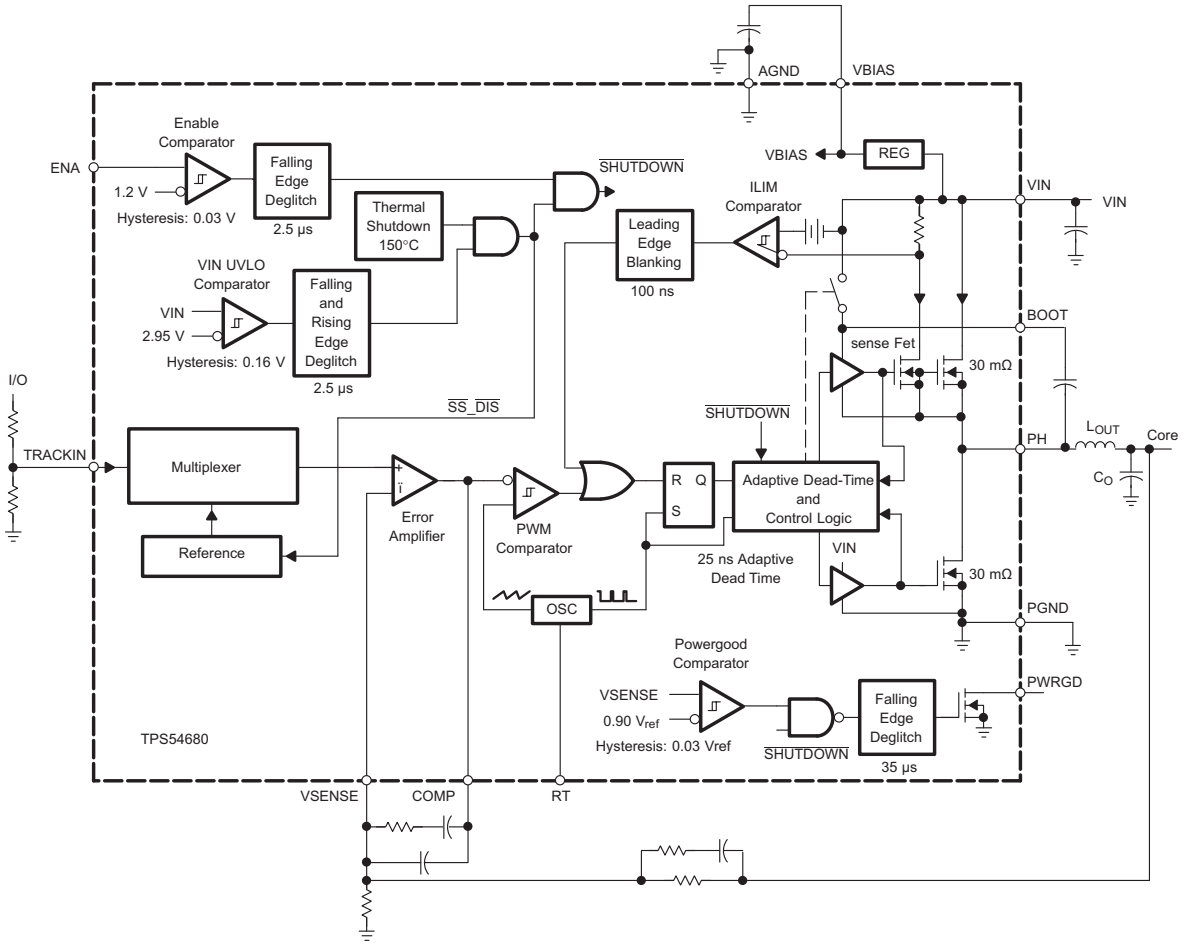


TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground. Return for compensation network/output divider, slow-start capacitor, VBIAS capacitor, RT resistor. Connect PowerPAD to AGND.
BOOT	5	Bootstrap output. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-side FET driver.
COMP	3	Error amplifier output. Connect frequency compensation network from COMP to VSENSE
ENA	27	Enable input. Logic high enables oscillator, PWM control and MOSFET driver circuits. Logic low disables operation and places device in low quiescent current state.
PGND	15–19	Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. A single point connection to AGND is recommended.
PH	6–14	Phase output. Junction of the internal high-side and low-side power MOSFETs, and output inductor.
PWRGD	4	Power good open drain output. High when VSENSE ≥ 90% Vref, otherwise PWRGD is low.
RT	28	Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency.
TRACKIN	26	External reference input. High impedance input to internal reference/multiplexer and error amplifier circuits.
VBIAS	25	Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1-µF to 1.0-µF ceramic capacitor.
VIN	20–24	Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low-ESR 10-µF ceramic capacitor.
VSENSE	2	Error amplifier inverting input. Connect to output voltage through compensation network/output divider.

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INTERNAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

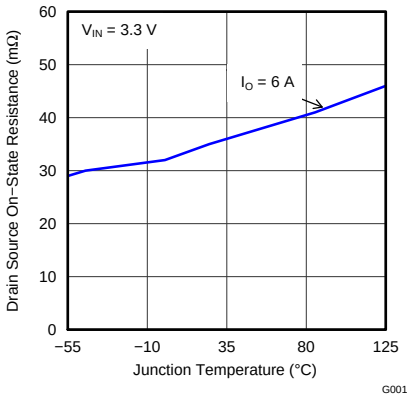


Figure 2.

DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

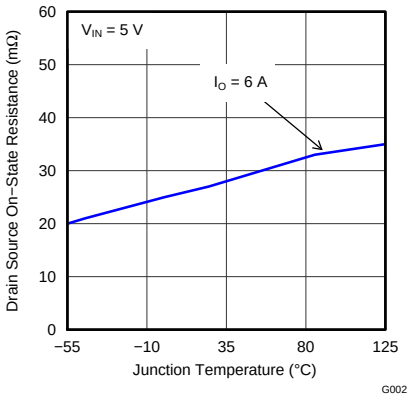


Figure 3.

INTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

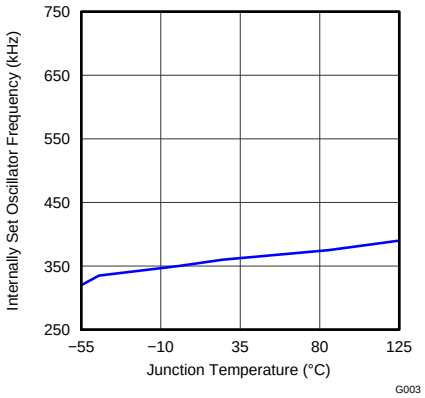


Figure 4.

EXTERNALLY SET OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

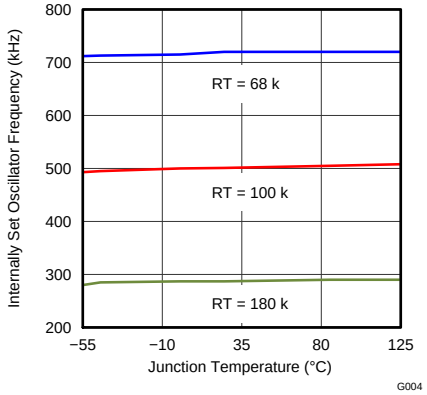


Figure 5.

VOLTAGE REFERENCE vs JUNCTION TEMPERATURE

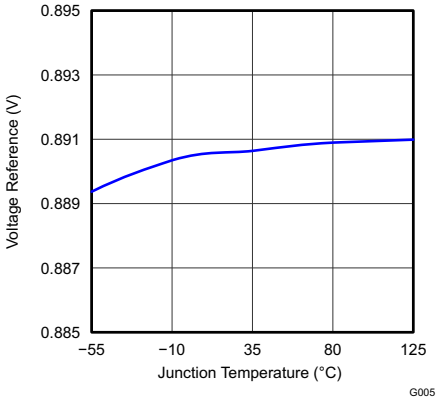


Figure 6.

DEVICE POWER LOSSES AT T_J = 125°C vs LOAD CURRENT

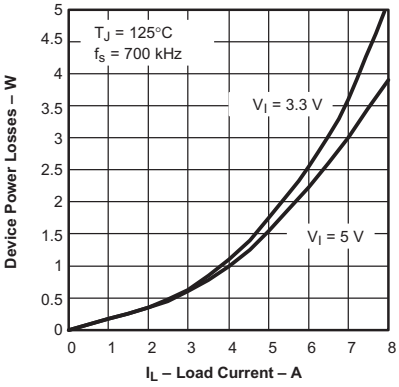


Figure 7.

OUTPUT VOLTAGE REGULATION vs INPUT VOLTAGE

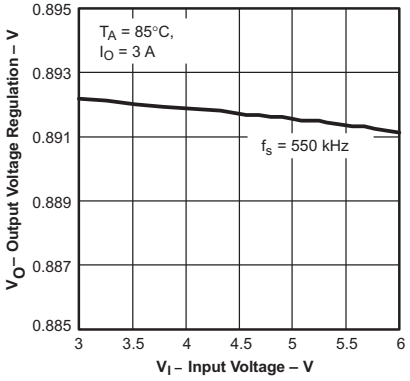


Figure 8.

ERROR AMPLIFIER vs OPEN LOOP RESPONSE

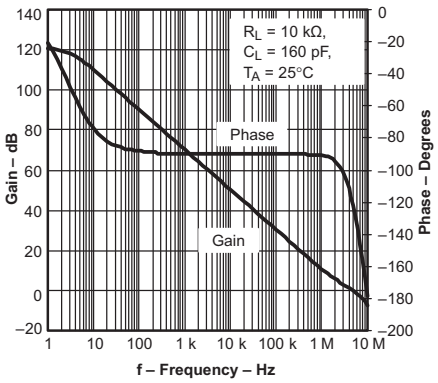


Figure 9.

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APPLICATION INFORMATION

Figure 10 shows the schematic diagram for a typical TPS54680 application. The TPS54680 (U1) can provide greater than 6 A of output current at a nominal output voltage of 1.8 V. For proper thermal performance, the exposed thermal PowerPAD underneath the integrated circuit package must be soldered to the printed-circuit board. To provide power up tracking, the enable of the I/O supply should be used. If the I/O enable is not used to power up, then devices with similar undervoltage lockout thresholds need to be implemented to ensure power up tracking. To ensure power down tracking, the enable pin should be used.

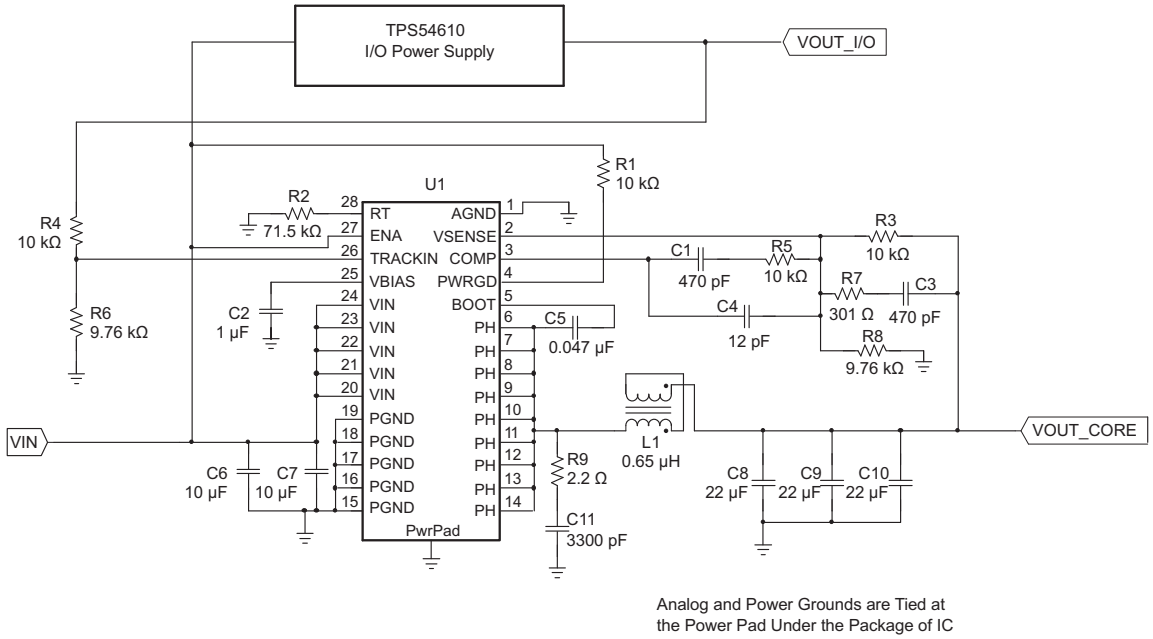


Figure 10. Application Circuit

COMPONENT SELECTION

The values for the components used in this design example were selected for low output ripple voltage and small PCB area. Additional design information is available at www.ti.com.

INPUT FILTER

The input voltage is a nominal 5 Vdc. The input filter C6 is a 10-µF ceramic capacitor (Taiyo Yuden). C7 also a 10-µF ceramic capacitor (Taiyo Yuden) provides high frequency decoupling of the TPS54680 from the input supply and must be located as close as possible to the device. Ripple current is carried in both C6 and C7, and the return path to PGND must avoid the current circulating in the output capacitors C8, C9, and C10.

FEEDBACK CIRCUIT

The values for these components have been selected to provide low output ripple voltage. The resistor divider network of R3 and R8 sets the output voltage for the circuit at 1.8 V. R3, along with R7, R5, C1, C3, and C4 form the loop compensation network for the circuit. For this design, a Type 3 topology is used.

OPERATING FREQUENCY

In the application circuit, the 350 kHz operation is selected by leaving RT open. Connecting a 180 kΩ to 68 kΩ resistor between RT (pin 28) and analog ground can be used to set the switching frequency to 280 kHz to 700 kHz. To calculate the RT resistor, use the equation below:

$$R = \frac{500\,\text{kHz}}{\text{Switching Frequency}} \times 100\,[\text{k}\Omega] \quad (1)$$

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OUTPUT FILTER

The output filter is composed of a 0.65-µH inductor and 3 x 22-µF capacitor. The inductor is a low dc resistance (0.017 Ω) type, Pulse Engineering PA0227. The capacitors used are 22-µF, 6.3 V ceramic types with X5R dielectric. The feedback loop is compensated so that the unity gain frequency is approximately 75 kHz.

GROUNDING AND POWERPAD LAYOUT

The TPS54680 has two internal grounds (analog and power). Inside the TPS54680, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. The PowerPAD must be tied directly to AGND. Noise injected between the two grounds can degrade the performance of the TPS54680, particularly at higher output currents. However, ground noise on an analog ground plane can also cause problems with some of the control and bias signals. Therefore, separate analog and power ground planes are recommended. These two planes must tie together directly at the IC to reduce noise between the two grounds. The only components that must tie directly to the power ground plane are the input capacitor, the output capacitor, the input voltage decoupling capacitor, and the PGND pins of the TPS54680. The layout of the TPS54680 evaluation module is representative of a recommended layout for a 4-layer board. Documentation for the TPS54680 evaluation module can be found on the Texas Instruments web site under the TPS54680 product folder. See the TPS54680 EVM user's guide.

LAYOUT CONSIDERATIONS FOR THERMAL PERFORMANCE

For operation at full rated load current, the analog ground plane must provide an adequate heat dissipating area. A 3-inch by 3-inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD must be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available must be used when 6 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer must be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Eight vias must be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the twelve recommended that enhance thermal performance must be included in areas not under the device package.

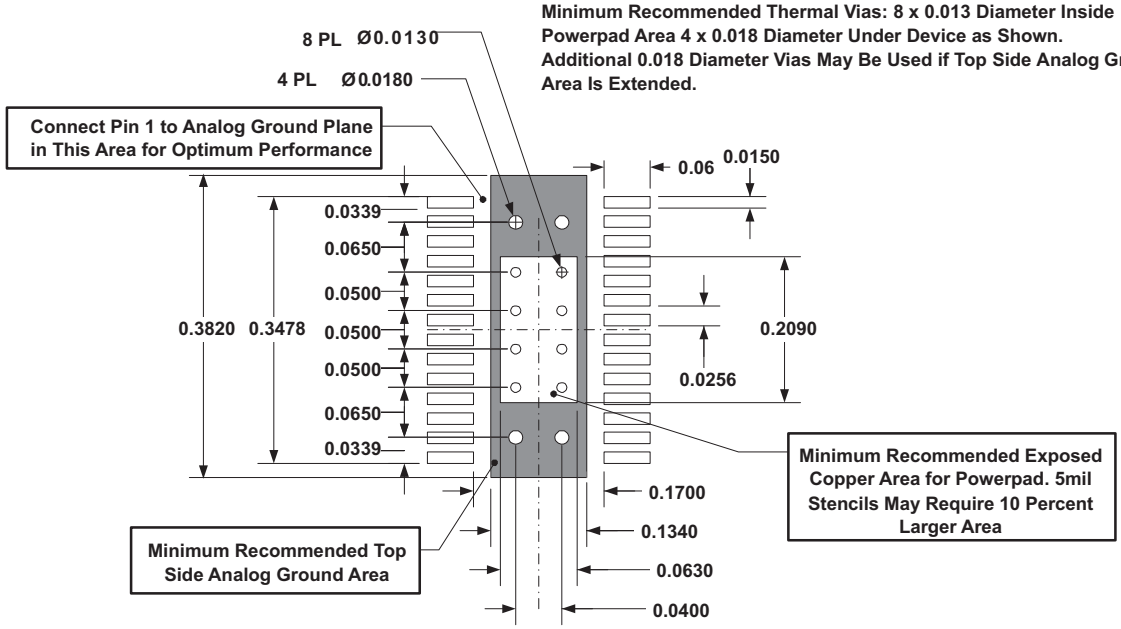


Figure 11. Recommended Land Pattern for 28-Pin PWP PowerPAD

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PERFORMANCE GRAPHS (1)

EFFICIENCY vs OUTPUT CURRENT

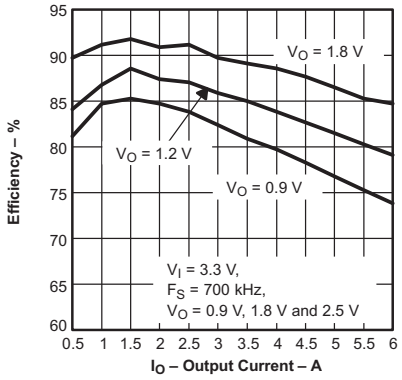


Figure 12.

LOAD REGULATION vs OUTPUT CURRENT

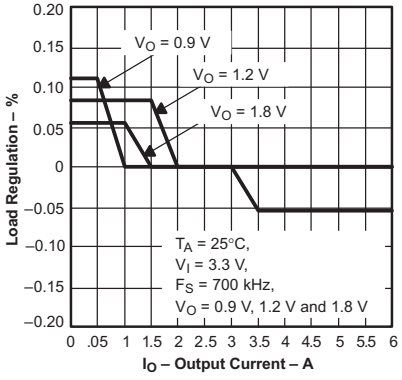


Figure 13.

LINE REGULATION vs INPUT VOLTAGE

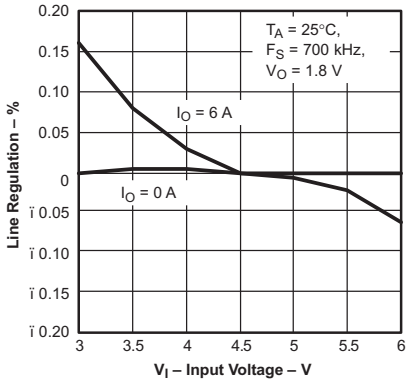


Figure 14.

LOOP RESPONSE

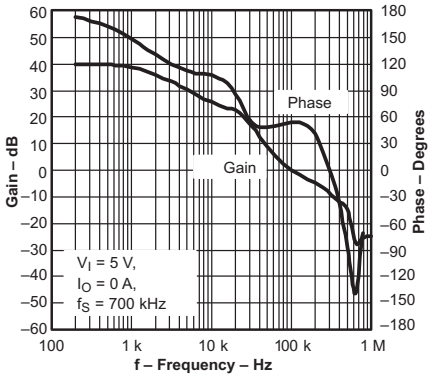


Figure 15.

AMBIENT TEMPERATURE vs LOAD CURRENT

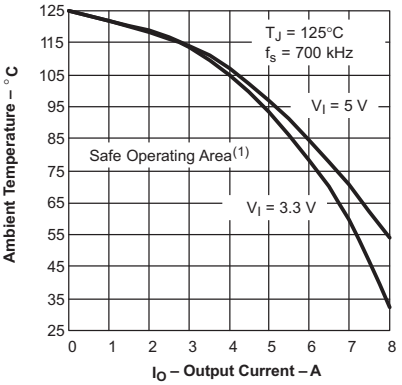


Figure 16.

OUTPUT AND INPUT RIPPLE

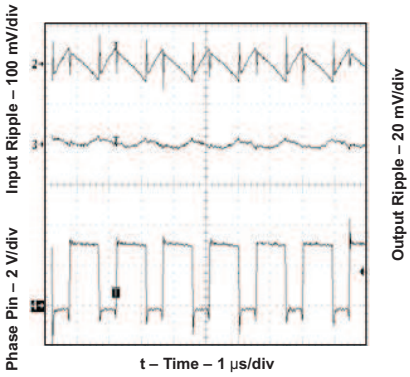


Figure 17.

LOAD TRANSIENT RESPONSE

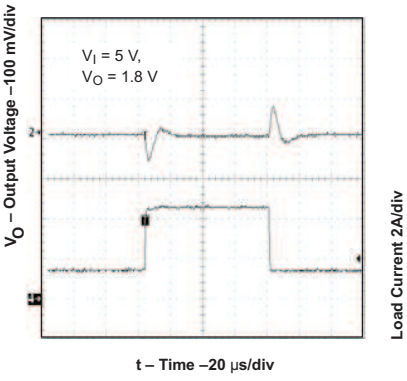


Figure 18.

STARTUP TIMING

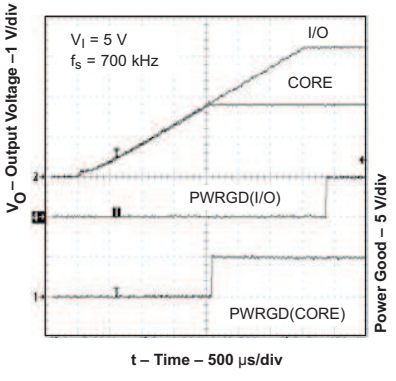


Figure 19.

POWER DOWN TIMING

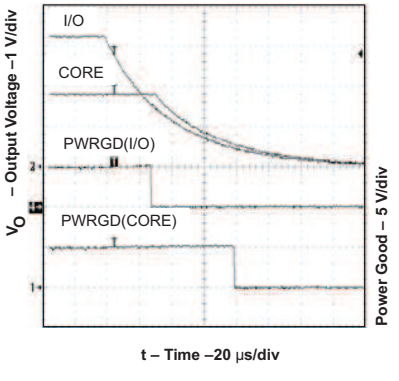


Figure 20.

(1) Safe operating area is applicable to the test board conditions in the Dissipation Ratings

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Figure 21 shows the schematic diagram for a power supply tracking design using a TPS2034 high side power switch and a TPS54680 device. The TPS2034 power switch ensures the I/O voltage is not applied to the load before U1 has enough bias voltage to operate and generate the core voltage.

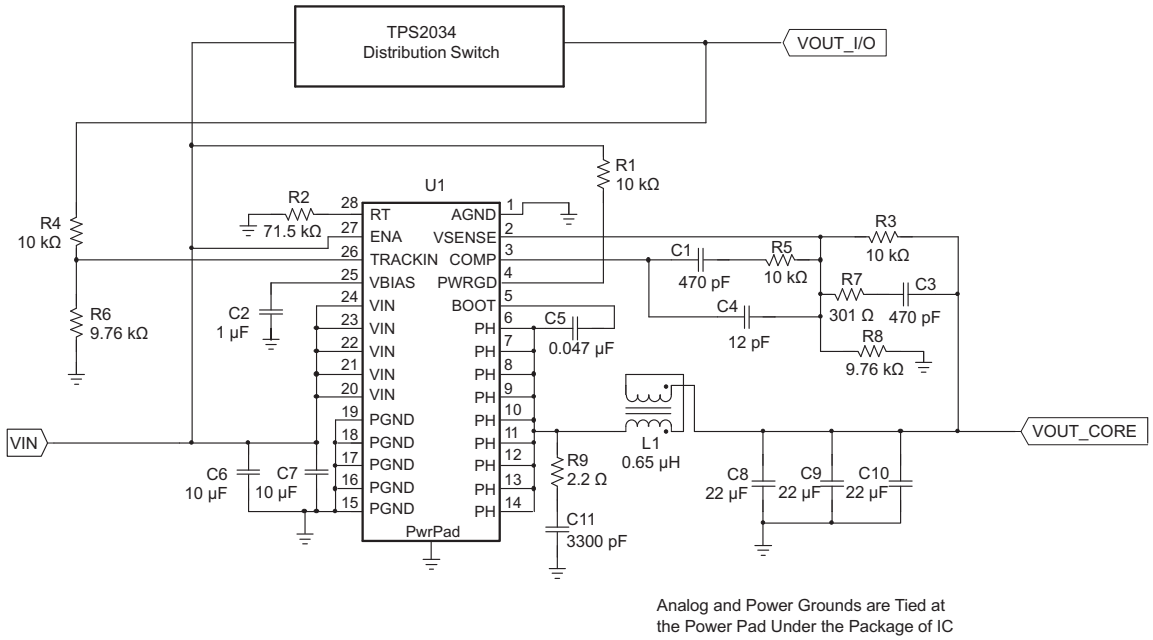


Figure 21. 3.3-V Small Size, High Frequency Design

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LOAD TRANSIENT RESPONSE

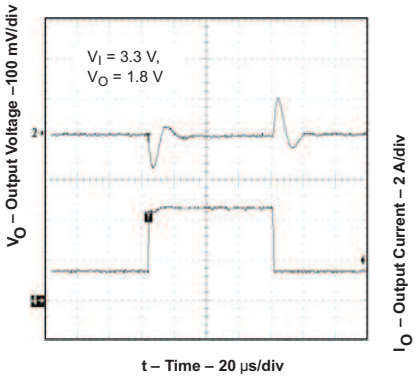


Figure 22.

EFFICIENCY vs OUTPUT CURRENT

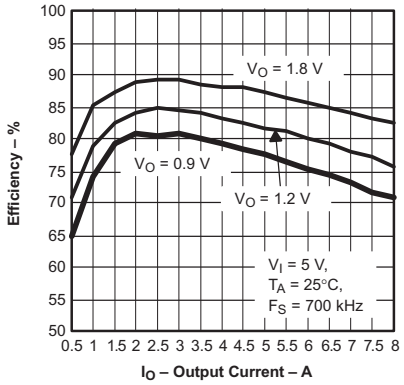


Figure 23.

LOAD REGULATION vs OUTPUT CURRENT

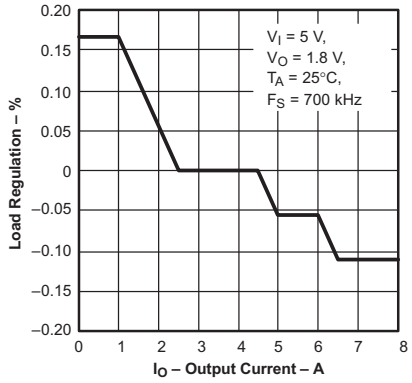


Figure 24.

LINE REGULATION vs INPUT VOLTAGE

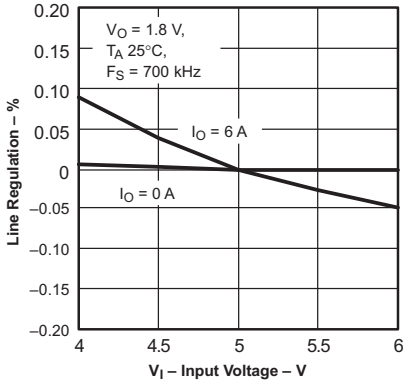


Figure 25.

LOOP RESPONSE

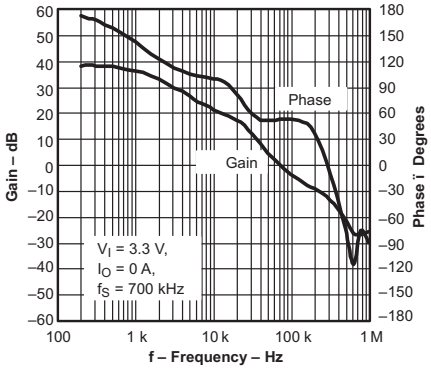


Figure 26.

AMBIENT TEMPERATURE vs LOAD CURRENT

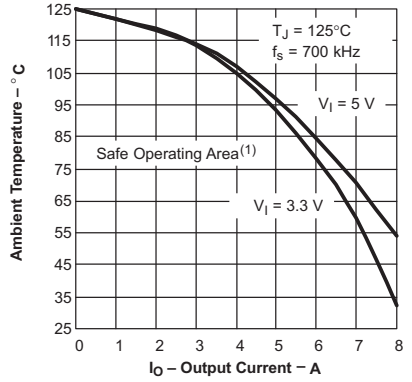


Figure 27.

OUTPUT AND INPUT RIPPLE

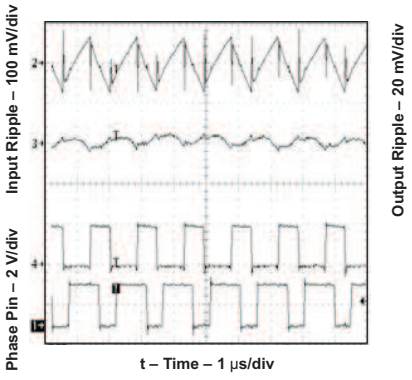


Figure 28.

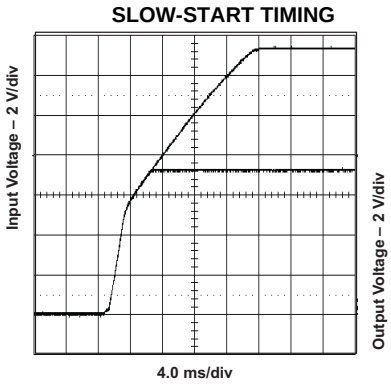


Figure 29.

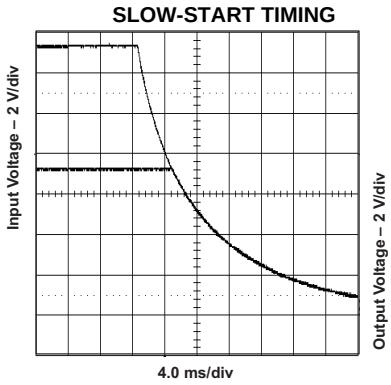


Figure 30.

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DETAILED DESCRIPTION

UNDERVOLTAGE LOCK OUT (UVLO)

The TPS54680 incorporates an under voltage lockout circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit reduce the likelihood of shutting the device down due to noise on VIN.

TRACKIN/INTERNAL SLOW-START

The internal slow-start circuit provides start-up slope control of the output voltage. The nominal internal slow-start rate is 25 V/ms. When the voltage on TRACKIN rises faster than the internal slope or is present when device operation is enabled, the output rises at the internal rate. If the reference voltage on TRACKIN rises more slowly, then the output rises at about the same rate as TRACKIN.

Once the voltage on the TRACKIN pin is greater than the internal reference of 0.891 V, the multiplexer switches the noninverting node to the high precision reference.

ENABLE (ENA)

The enable pin, ENA, provides a digital control enable or disable (shut down) for the TPS54680. An input voltage of 1.4 V or greater ensures that the TPS54680 is enabled. An input of 0.82 V or less ensures that device operation is disabled. These are not standard logic thresholds, even though they are compatible with TTL outputs.

When ENA is low, the oscillator, slow-start, PWM control and MOSFET drivers are disabled and held in an initial state ready for device start-up. On an ENA transition from low to high, device start-up begins with the output starting from 0 V.

VBIAS REGULATOR (VBIAS)

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor must be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.70 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

VOLTAGE REFERENCE

The voltage reference system produces a precise Vref signal by scaling the output of a temperature stable bandgap circuit. During manufacture, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure adds to the high precision regulation of the TPS54680, since it cancels offset errors in the scale and error amplifier circuits.

OSCILLATOR AND PWM RAMP

The oscillator frequency is set internally to 350 kHz. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 to 700 kHz by connecting a resistor between the RT pin and AGND. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND:

$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\,[\text{kHz}] \quad (2)$$

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SWITCHING FREQUENCY	RT PIN
350 kHz, internally set	Float
Externally set 280 kHz to 700 kHz	R = 180 kΩ to 68 kΩ

ERROR AMPLIFIER

The high performance, wide bandwidth, voltage error amplifier sets the TPS54680 apart from most dc/dc converters. The user is given the flexibility to use a wide range of output L and C filter components to suit the particular application needs. Type 2 or type 3 compensation can be employed using external compensation components.

PWM CONTROL

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch. Once the PWM latch is reset, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as VREF. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54680 is capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and low-side FET turns on to decrease the energy in the output inductor and consequently the output current. This process is repeated each cycle in which the current limit comparator is tripped.

DEAD-TIME CONTROL AND MOSFET DRIVERS

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. While the low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 2 V.

The high-side and low-side drivers are designed with 300-mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and an internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

OVERCURRENT PROTECTION

The cycle-by-cycle current limiting is achieved by sensing the current flowing through the high-side MOSFET and comparing this signal to a preset overcurrent threshold. The high side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100-ns leading edge blanking circuit prevents the current limit from false tripping. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

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THERMAL SHUTDOWN

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown automatically when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit.

Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously; starting up by control of the soft-start circuit, heating up due to the fault condition, and then shutting down upon reaching the thermal shutdown trip point. This sequence repeats until the fault condition is removed.

POWER-GOOD (PWRDG)

The power good circuit monitors for under voltage conditions on VSENSE. If the voltage on VSENSE is 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold or ENA is low, or a thermal shutdown occurs. When VIN ≥ UVLO threshold, ENA ≥ enable threshold, and VSENSE > 90% of V_{ref}, the open drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of V_{ref} and a 35 µs falling edge deglitch circuit prevent tripping of the power good comparator due to high frequency noise.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54680MPWPEP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54680M
TPS54680MPWPEP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54680M
TPS54680MPWPREP	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54680M
TPS54680MPWPREP.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54680M
TPS54680QPWPREP	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54680EP
TPS54680QPWPREP.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54680EP
V62/04641-01XE	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54680EP
V62/04641-02XE	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54680M
V62/04641-02XE-T	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54680M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54680-EP :

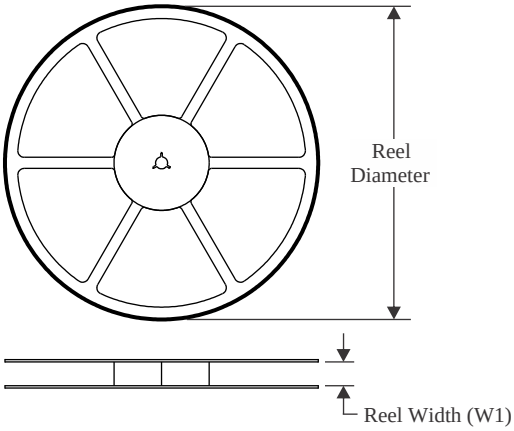
- Catalog : TPS54680

NOTE: Qualified Version Definitions:

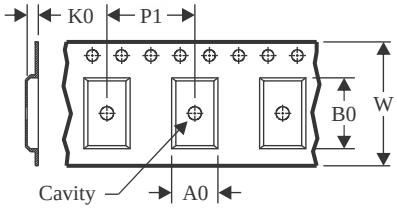
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

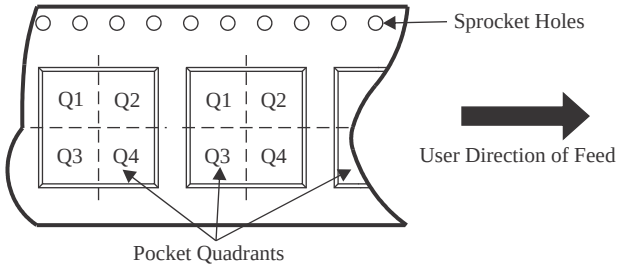


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

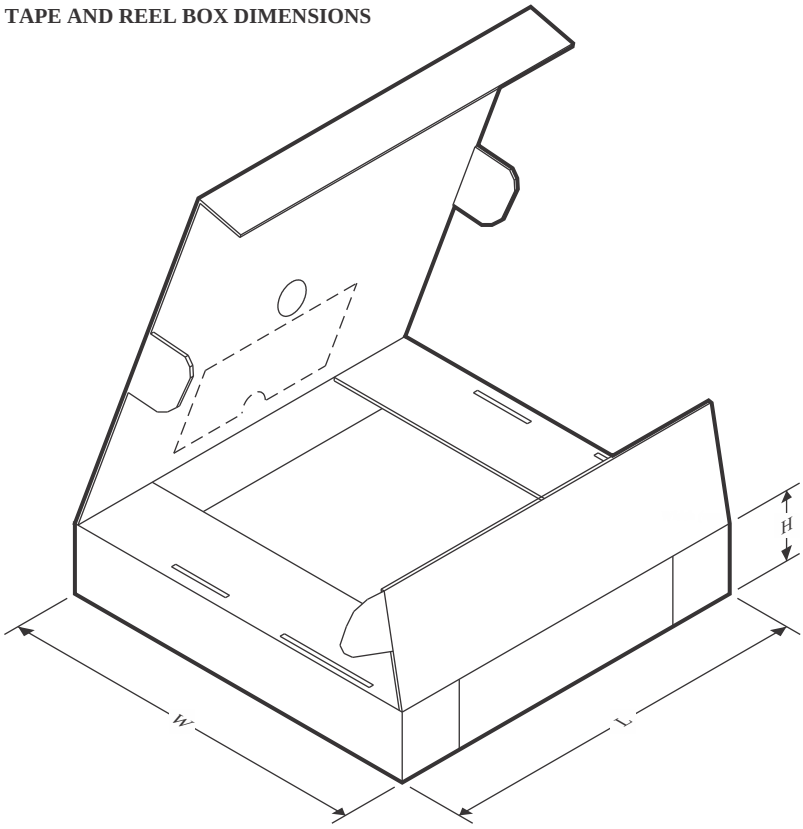
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54680MPWPREP	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS54680QPWPREP	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

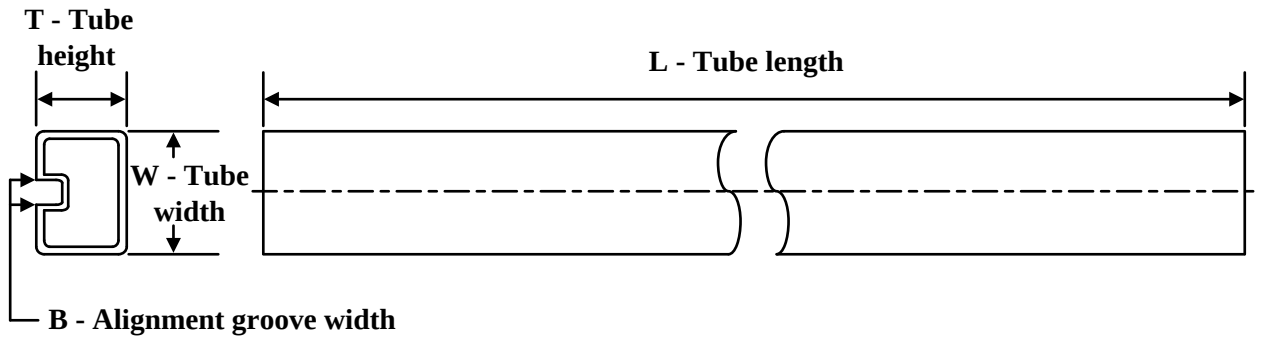
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54680MPWPREP	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPS54680QPWPREP	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54680MPWPEP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPS54680MPWPEP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5
V62/04641-02XE-T	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

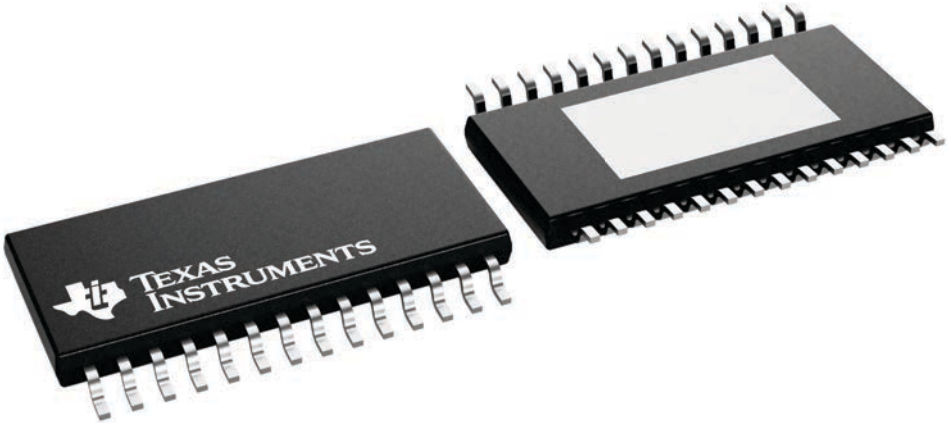
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

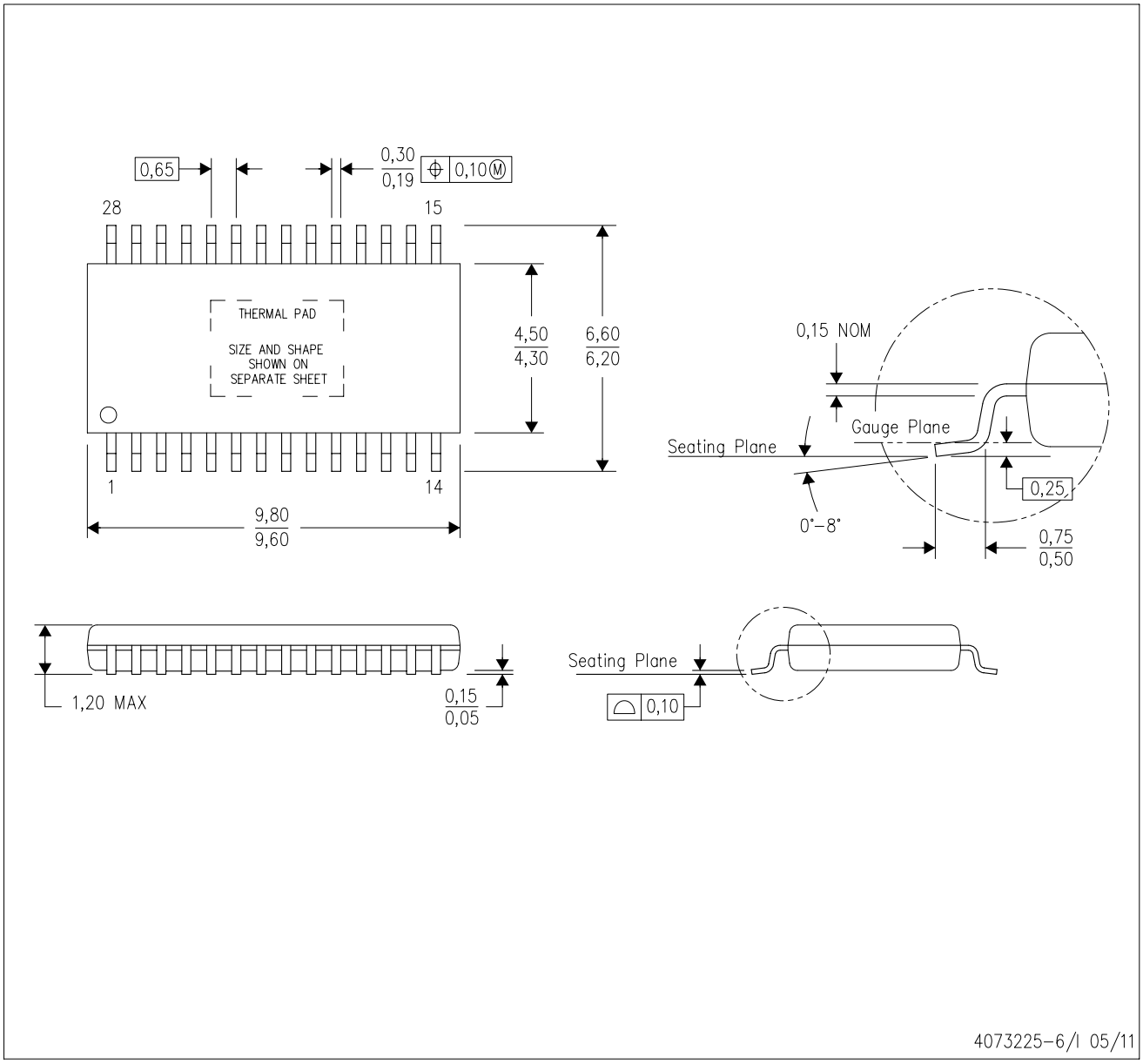
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

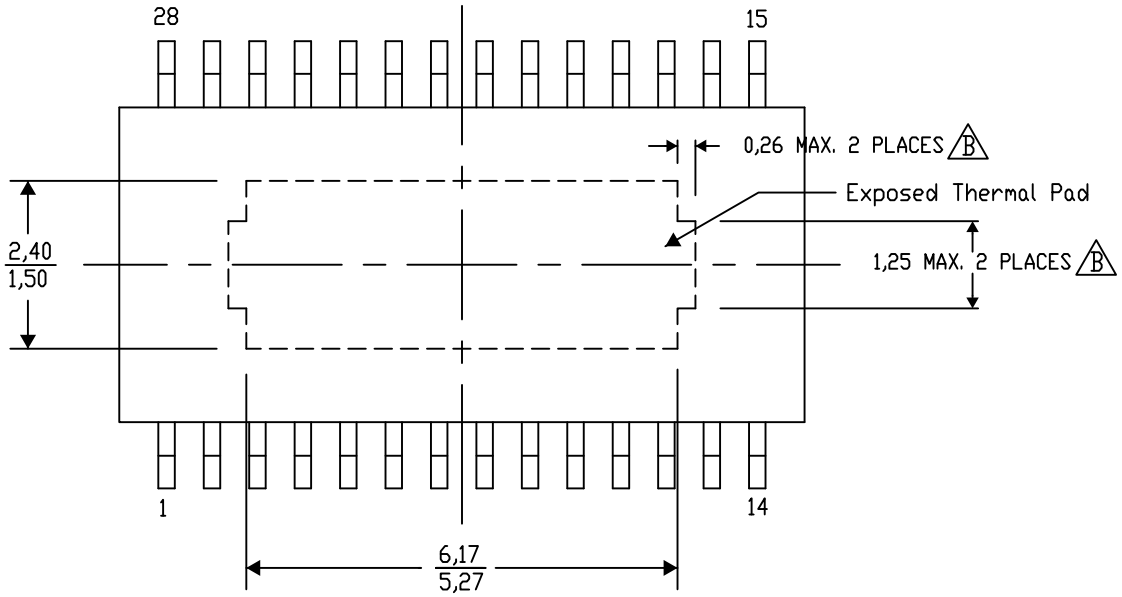
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

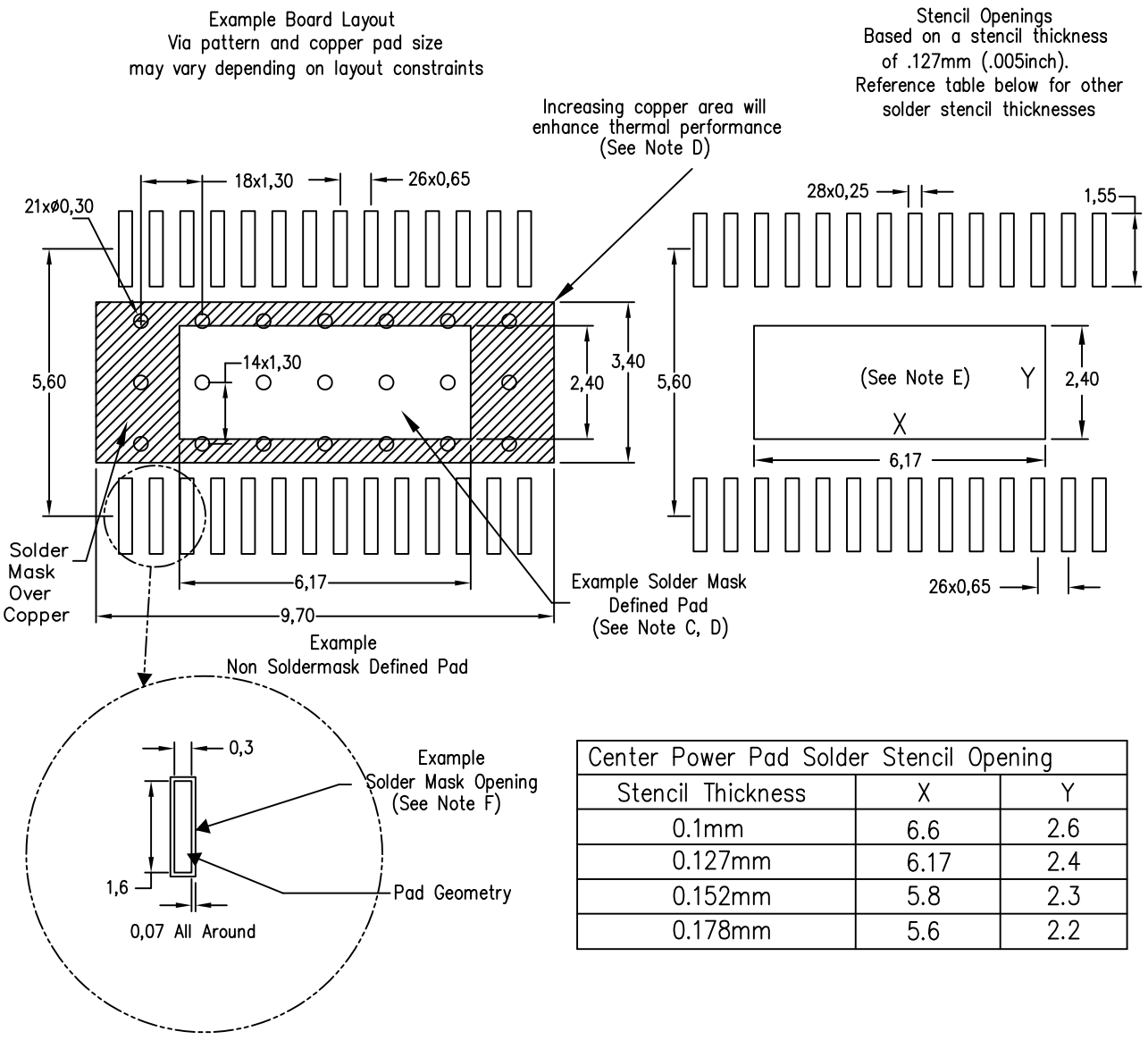
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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