TEXAS INSTRUMENTS

TPS62231-Q1, TPS622314-Q1

SLVSB63A – DECEMBER 2011 – REVISED MARCH 2016

TPS62231x-Q1 3-MHz Ultra-Small Step-Down Converter in 1 × 1.5 SON Package

1 Features

- Qualified for Automotive Applications
- Up to 3.8-MHz Switch Frequency
- Up to 94% Efficiency
- Output Peak Current up to 500 mA
- Excellent AC and Transient Load Regulation
- High PSRR (up to 90 dB)
- Small External Output-Filter Components 1 µH and 4.7 µF
- V_{IN} range from 2.05 V to 6 V
- Optimized Power Save Mode For Low Output-Ripple Voltage
- Forced PWM Mode Operation
- Typical 22-µA Quiescent Current
- 100% Duty Cycle for Lowest Dropout
- Small 1 × 1.5 × 0.6-mm^3 SON Package
- 12-mm^2 Minimum Solution Size
- Supports 0.6-mm Maximum Solution Height
- Soft Start With 100-µs (Typical) Start-Up Time

2 Applications

- Advanced Driver-Assistance System (ADAS)
  - Front Camera, Rear View Camera
  - Surround View
  - Blind-Spot Monitoring
- Automotive Telematics, eCall, and Tolling
- Space-Optimized Automotive and Industrial Power Systems

3 Description

The TPS6223x-Q1 device family is a high-frequency, synchronous step-down DC-DC converter ideal for space-optimized automotive and industrial applications. The device supports up to 500-mA output current and allows the use of tiny and low-cost chip inductors and capacitors.

With a wide input-voltage range of 2.05 V to 6 V, the device can be powered by a preregulated voltage rail or Li-Ion batteries with extended voltage range. Two different fixed-output voltage versions are available at 1.5 V and 1.8 V.

The TPS6223x-Q1 series features switch frequency up to 3.8 MHz. At medium to heavy loads, the converter operates in PWM mode and automatically enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range.

Because of its excellent PSRR and AC load regulation performance, the device is also suitable to replace linear regulators to obtain better power conversion efficiency.

The Power Save Mode in TPS6223x-Q1 reduces the quiescent current consumption down to 22 µA during light load operation. It is optimized to achieve very low output voltage ripple even with small external component and features excellent AC load regulation.

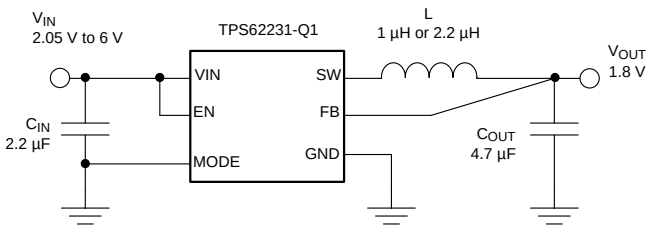
For noise-sensitive applications, the device can be forced to PWM Mode operation over the entire load range by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS6223x-Q1 is available in a 1-mm × 1.5-mm^2 6-pin SON package.

Device Information[1]

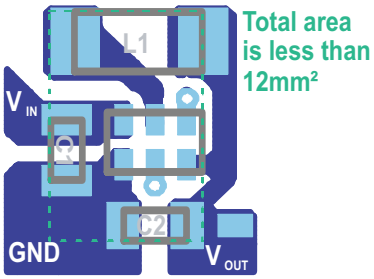
PART NUMBER	OUTPUT VOLTAGE	FREQUENCY
TPS62231-Q1	1.8 V	3 MHz
TPS622314-Q1	1.5 V	3 MHz

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



Small PCB Layout Size



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

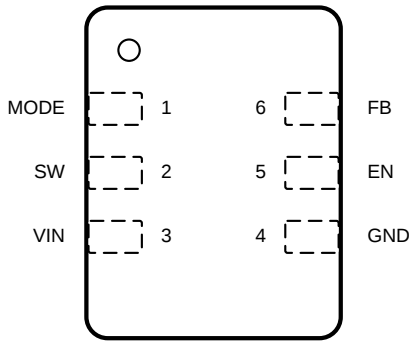
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2011) to Revision A	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed the *Applications* list	1
• Deleted the *Ordering Information* table	1
• Deleted references to devices and voltage options that are not available as automotive grade	1
• Added minimum and maximum recommended values for output inductance and output capacitance in the *Recommended Operating Conditions* table for clarity	4
• Deleted the *Dissipation Ratings* table and added a more detailed *Thermal Information* table	4
• Deleted the *Parameter Measurement Information* section	7

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5 pPin Configuration and Functions

DRY Package
6-Pin SON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	MODE	IN	When the MODE pin is high, the device is forced to operate in PWM mode. When the MODE pin is low, the power save mode is enabled with automatic transition from PFM (pulse frequency mode) to PWM (pulse width modulation) mode. This pin must be terminated.
2	SW	OUT	This pin is the switch pin and is connected to the internal MOSFET switches. Connect the inductor to this pin.
3	VIN	PWR	V_{IN} power supply pin.
4	GND	PWR	GND supply pin.
5	EN	IN	This is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
6	FB	IN	Feedback pin for the internal regulation loop. Connect this pin directly to the output capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Voltage at VIN and SW pin(2)	–0.3	7	V
	Voltage at EN, MODE pin(2)	–0.3	(V_{IN} + 0.3) ≤7	V
	Voltage at FB pin(2)	–0.3	3.6	V
	Peak output current	internally limited		A
	Power dissipation	Internally limited		
T_J	Maximum operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Machine Model (MM)	200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

operating ambient temperature T_A = –40 to 105°C (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
Supply voltage, V_{IN}[2]			2.05		6	V
Effective output inductance			0.7	1 or 2.2	4.3	µH
Effective output capacitance			2	4.7	15	µF
Recommended minimum supply voltage	$V_{OUT} \le (V_{IN} – 1\ V)$[3]	500-mA maximum I_{OUT}[4]		3	3.6	V
		350-mA maximum I_{OUT}[4]		2.5	2.7	
	$V_{OUT} \le 1.8$ V	60-mA maximum output current[4]			2.05	
Operating junction temperature, T_J			–40		125	°C
Ambient temperature, T_A			–40		105	°C

(1) In applications where high power dissipation, poor package thermal resistance, or both are present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} \times P_{D(max)})$.
(2) The minimum required supply voltage for start-up is 2.05 V. The device is functional down to the falling UVLO (undervoltage lockout) threshold.
(3) For a voltage difference between minimum V_{IN} and V_{OUT} of ≥ 1 V
(4) Typical value applies for T_A = 25°C, maximum value applies for T_A = 105°C with $T_J \le 125$°C, PCB layout needs to support proper thermal performance.

6.4 Thermal Information

THERMAL METRIC[1]		TPS62231x-Q1 DRY (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	294.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	166.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	166.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	159.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, EN = V_{IN}, MODE = GND, T_A = –40°C to 105°C(1), C_{IN} = 2.2 µF, L = 2.2 µH, C_{OUT} = 4.7 µF, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range(2)			2.05		6	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA. PFM mode enabled (MODE = 0) device not switching			22	40	µA
		I_{OUT} = 0 mA. PFM mode enabled (MODE = 0) device switching, V_{IN} = 3.6 V, V_{OUT} = 1.2 V			25		µA
		I_{OUT} = 0 mA. Switching with no load (MODE/DATA = V_{IN}), PWM operation, V_{OUT} = 1.8 V, L = 2.2 µH			3		mA
I_{SD}	Shutdown current	EN = GND(3)			0.1	1	µA
UVLO	Undervoltage-lockout threshold	Falling			1.8	1.9	V
		Rising			1.9	2.05	V
ENABLE, MODE THRESHOLD							
$V_{IH\ TH}$	Threshold for detecting high EN, MODE	2.05 V ≤ V_{IN} ≤ 6 V , rising edge			0.8	1	V
$V_{IL\ TH\ HYS}$	Threshold for detecting low EN, MODE	2.05 V ≤ V_{IN} ≤ 6 V , falling edge		0.4	0.6		V
I_{IN}	Input bias Current, EN, MODE	EN, MODE = GND or V_{IN} = 3.6 V			0.01	0.5	µA
POWER SWITCH							
$R_{DS(ON)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V, T_{Jmax} = 105°C; $R_{DS(ON)}$ max value			600	850	mΩ
	Low-side MOSFET on-resistance	V_{IN} = 3.6 V, T_{Jmax} = 105°C; $R_{DS(ON)}$ max value			350	480	mΩ
I_{LIMF}	Forward current-limit MOSFET high side	V_{IN} = 3.6 V, open loop		690	850	1050	mA
	Forward current-limit MOSFET low side	V_{IN} = 3.6 V, open loop		550	840	1220	mA
T_{SD}	Thermal shutdown	Increasing junction temperature			150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature			20		°C
CONTROLLER							
t_{ONmin}	Minimum on time	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, Mode = high, I_{OUT} = 0 mA			135		ns
t_{OFFmin}	Minimum off time				40		ns
OUTPUT							
V_{REF}	Internal reference voltage				0.70		V
V_{OUT}	Output voltage accuracy(4)	V_{IN} = 3.6 V, Mode = GND, device operating in PFM Mode, I_{OUT} = 0 mA			0%		
		V_{IN} = 3.6 V, MODE = V_{IN}, I_{OUT} = 0 mA	T_A = 25°C	–2%		2%	
			T_A = –40°C to 105°C	–2.5%		2.5%	
	DC output voltage load regulation	PWM operation, Mode = V_{IN} = 3.6 V, V_{OUT} = 1.8 V			0.001		%/mA
	DC output voltage line regulation	I_{OUT} = 0 mA, Mode = V_{IN}, 2.05 V ≤ V_{IN} ≤ 6 V			0		%/V
t_{Start}	Start-up time	Time from active EN to V_{OUT} = 1.8 V, V_{IN} = 3.6 V, 10-Ω load			100		µs
I_{LK_SW}	Leakage current into SW pin	V_{IN} = V_{OUT} = V_{SW} = 3.6 V, EN = GND(5)			0.1	0.5	µA

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} \times P_{D(max)})$.
(2) The minimum required supply voltage for start-up is 2.05 V. The device is functional down to the falling UVLO (undervoltage lockout) threshold
(3) Shutdown current into VIN pin, includes internal leakage
(4) $V_{IN} = V_O + 1$ V
(5) The internal resistor divider network is disconnected from FB pin.

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6.6 Typical Characteristics

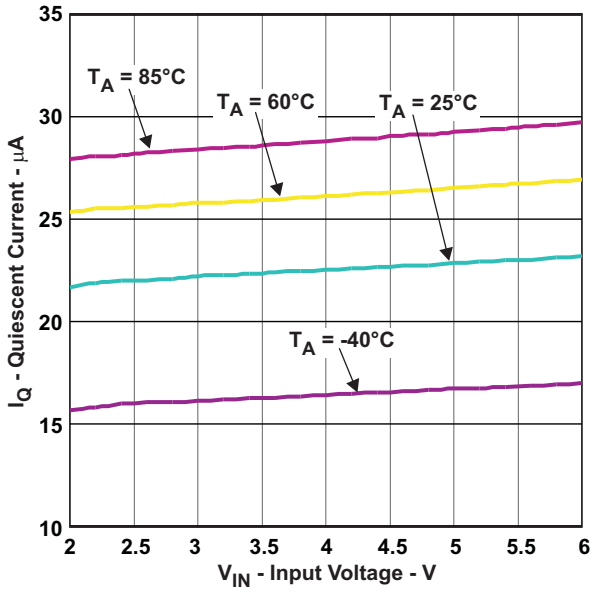


Figure 1. Quiescent Current I_Q vs Ambient Temperature (T_A)

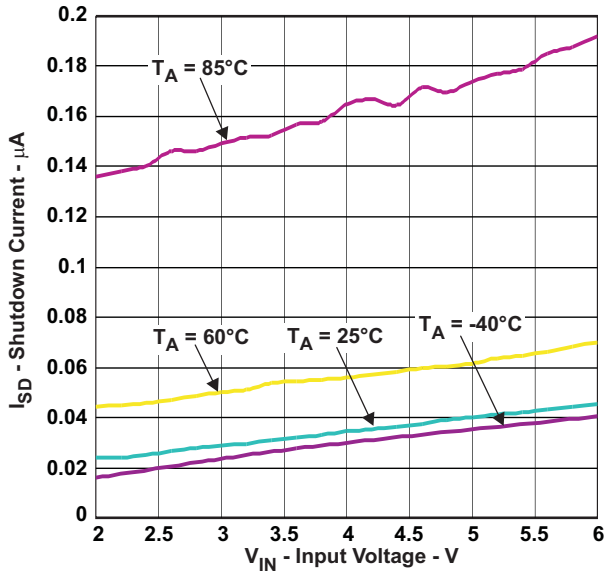


Figure 2. Shutdown Current I_{SD} vs Ambient Temperature (T_A)

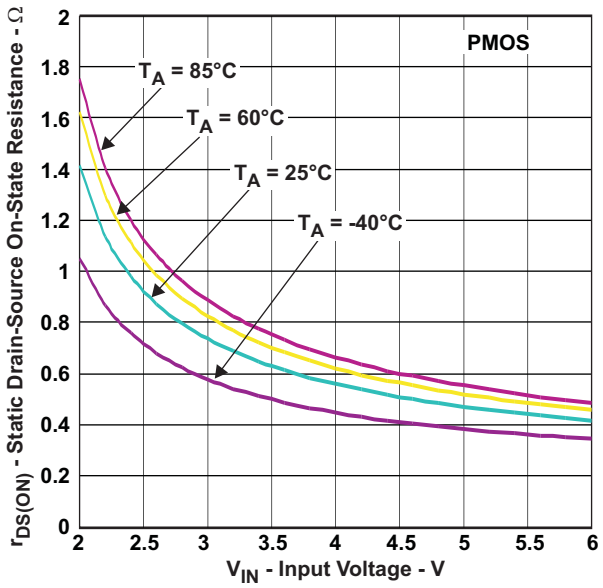


Figure 3. PMOS $R_{DS(ON)}$ vs Supply Voltage V_{IN} and Ambient Temperature (T_A)

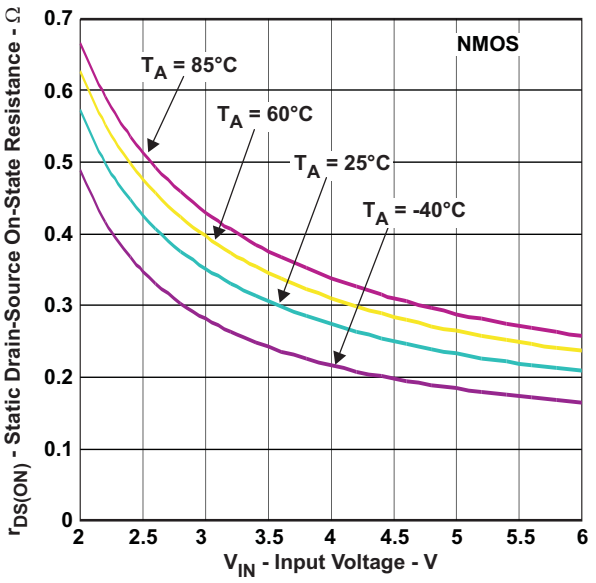


Figure 4. NMOS $R_{DS(ON)}$ vs Supply Voltage V_{IN} and Ambient Temperature (T_A)

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7 Detailed Description

7.1 Overview

The TPS6223x-Q1 synchronous step-down converter family of devices includes a unique, hysteretic PWM-controller scheme which enables switch frequencies over 3 MHz, excellent transient and AC load regulation, and operation with cost-competitive external components.

The controller topology supports forced PWM mode as well as power save mode operation. power save mode operation reduces the quiescent current consumption down to 22 µA and ensures high conversion efficiency at light loads by skipping switch pulses. In forced PWM mode, the device operates on a quasi-fixed frequency, avoids pulse skipping, and allows filtering of the switch noise by external filter components. The actual switching frequency depends on the input voltage, output voltage, device mode, and actual load current.

The TPS6223x-Q1 family of devices offers fixed output-voltage options featuring smallest solution size by using only three external components.

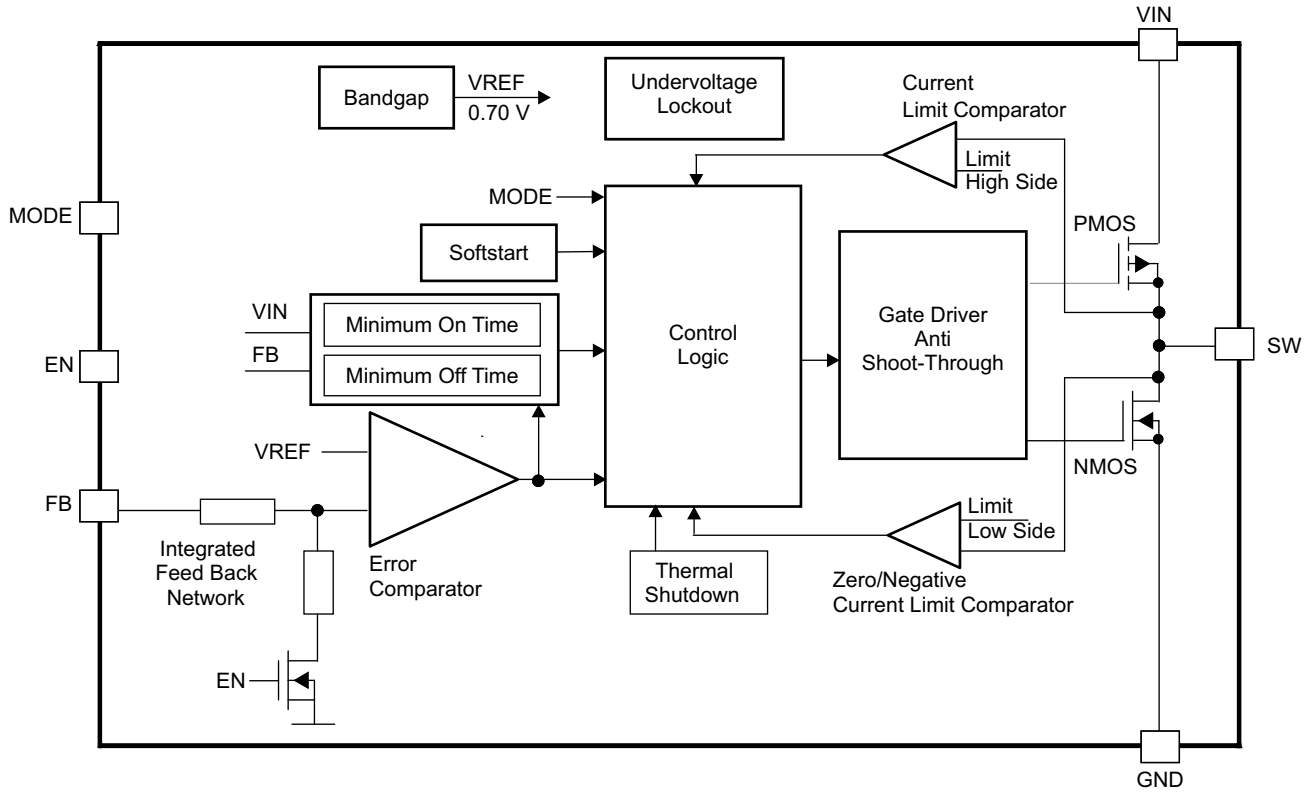
The internal switch-current limit of 850 mA (typical) supports output currents of up to 500 mA, depending on the operating condition.

A significant advantage of TPS6223x-Q1 family of devices compared to other hysteretic PWM controller topologies is excellent DC and AC load regulation capability in combination with low output-voltage ripple over the entire load range which makes this device well suited for audio and RF applications.

When the output voltage falls below the threshold of the error comparator, a switch pulse is initiated, and the high-side switch is turned on. This switch remains on until a minimum on time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high-side switch-current limit. When the high-side switch turns off, the low-side switch rectifier is turned on and the inductor current ramps down until the high side switch turns on again or the inductor current reaches zero.

In forced PWM mode operation, the negative inductor current is allowed to enable continuous conduction mode even at no load condition.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

The undervoltage-lockout (UVLO) circuit prevents the device from misoperation at low input voltages. This circuit prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6223x-Q1 family of devices has an UVLO threshold set to 1.8 V (typical). Fully-functional operation is permitted for the input voltage down to the falling UVLO-threshold level. The converter starts operation again when the input voltage crosses the rising UVLO-threshold level.

7.3.2 Enable and Shutdown

The device starts operation when the EN pin is set high and starts up with the soft-start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of 0.1 µA (typical). In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off.

The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails.

7.3.3 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical), the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues operation when the junction temperature falls below the thermal shutdown hysteresis.

7.4 Device Functional Modes

7.4.1 Soft Start

The device has an internal soft-start circuit that controls the ramp up of the output voltage and limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system generates a monotonic ramp up of the output voltage and reaches the nominal output voltage which is typically 100 µs after EN pin was pulled high.

If the output voltage does not reach the target value by this time, such as in the case of heavy load, the converter then operates in a current limit mode set by the switch-current limits.

The device is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.4.2 Power Save Mode

Connecting the MODE pin to GND enables the automatic PWM mode and power save mode operation. The converter operates in quasi-fixed frequency PWM mode at moderate to heavy loads and in the PFM (pulse frequency modulation) mode during light loads, which maintains high efficiency over a wide-load current range. In PFM mode, the device starts to skip switch pulses and generates only single pulses with an on time of t_{ONmin}. The PFM Mode frequency depends on the load current and the external inductor and output capacitor values. The PFM mode of the device is optimized for low output-voltage ripple if small external components are used. Even at low output currents, the PFM frequency is above the audible noise spectrum and makes this operation mode suitable for audio applications.

Use Equation 1 to estimate the on time t_{ONmin}.

$$t_{ONmin} = \frac{V_{OUT}}{V_{IN}} \times 260 \text{ ns}$$

where

- t_{ON} = High-side switch on time (ns)
- V_{OUT}= Output voltage (V)

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Device Functional Modes (continued)

- V_{IN}= Input voltage (V) (1)

Therefore, use Equation 2 to calculate the approximate peak inductor current in PFM mode.

$$I_{LPFMpeak} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ONmin}$$

where

- $I_{LPFMpeak}$ = PFM inductor peak current (mA)
- L = Inductance (µH) (2)

Use Equation 3 to estimate the transition from PFM into PWM mode and from PWM into PFM.

$$I_{OUT_PFM/PWM} = 0.5 \times I_{LPFMpeak}$$

where

- $I_{OUT_PFM/PWM}$ = Output current for transition from PFM to PWM mode and transition from PWM to PFM mode (mA) (3)

7.4.3 Forced PWM Mode

Pulling the MODE pin high forces the converter to operate in a continuous-conduction PWM mode even at light load currents. The advantage is that the converter operates with a quasi-fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads.

For additional flexibility, switch from power save mode to forced PWM mode during operation. This switching allows for efficient power management by adjusting the operation of the converter to the specific system requirements.

7.4.4 100% Duty-Cycle Low-Dropout Operation

The device starts to enter 100% duty-cycle mode when the input voltage comes close to the nominal output voltage. To maintain the output voltage, the high-side switch is turned on 100% for one or more cycles.

With further decreasing V_{IN}, the high-side MOSFET switch is turned on completely. In this case the converter offers a low input-to-output voltage difference which is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range.

Use Equation 4 to calculate the minimum input voltage to maintain regulation which is dependent on the load current and output voltage.

$$V_{IN}min = V_{OUT}max + I_{OUT}max \times \left(R_{DS(on)}max + R_L\right)$$

where

- V_{OUT}max = nominal output voltage plus maximum output-voltage tolerance
- I_{OUT}max = maximum output current plus inductor ripple current
- $R_{DS(on)}$max = maximum P-channel switch RDSon
- R_L = DC resistance of the inductor (4)

7.4.5 Short-Circuit Protection

The device integrates a high-side and low-side MOSFET current limit to protect the device against heavy load or short circuit. The current in the switches is monitored by current-limit comparators. When the current in the P-channel MOSFET reaches the current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on to ramp down the current in the inductor. The high-side MOSFET switch can only turn on again when the current in the low-side MOSFET switch has decreased below the threshold of the current-limit comparator.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS6223x-Q1 family of devices is a high-frequency, synchronous, step-down DC-DC converter providing switch frequencies up to 3.8 MHz.

8.2 Typical Application

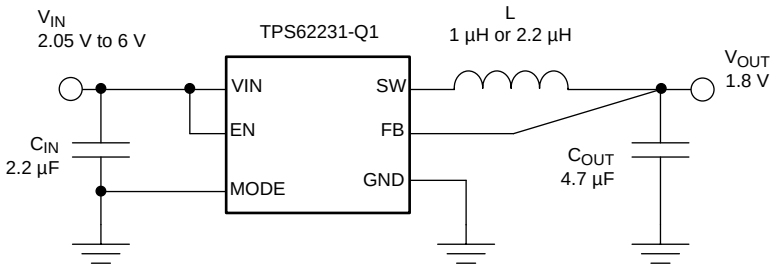


Figure 5. TPS62231-Q1 1.8-V Output

8.2.1 Design Requirements

The device operates over an input voltage range of 2.05 V to 6 V. The TPS62231-Q1 device has a fixed output voltage of 1.8 V (typical) and the TPS622314-Q1 device has a fixed output voltage of 1.5 V (typical). The device is easy to use and requires just three external components; however, the selection of external components and PCB layout must comply with the design guidelines to achieve the specified performance.

8.2.2 Detailed Design Procedure

8.2.2.1 Output Filter Design (Inductor and Output Capacitor)

The device is optimized to operate with effective inductance values in the range of 0.7 µH to 4.3 µH and with effective output capacitance in the range of 2 µF to 15 µF. The internal compensation is optimized to operate with an output filter of L = 1 µH or 2.2 µH and C_{OUT} = 4.7 µF. Larger or smaller inductor and capacitor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *Checking Loop Stability* section.

8.2.2.2 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple, and the efficiency. The selected inductor must be rated for DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT}. Use Equation 5 to calculate the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 6. This rating is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (5)$$

where

- L = Inductor value
- f = Switching frequency

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Typical Application (continued)

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- I_{Lmax} = Maximum inductor current
- ΔI_L = Peak-to-peak inductor ripple current (6)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (essentially the quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, use care when selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 1 lists the inductor series from different suppliers that have been used with the TPS6223x-Q1 converters. These components must be verified and validated to determine whether the component is suitable for the end application.

Table 1. List of inductors

INDUCTANCE (µH)	DIMENSIONS (mm^3)	INDUCTOR TYPE	SUPPLIER
1	2.5 × 2 × 1.2	LQM2HPN1R0MJ0	Murata
2.2	2 × 1.2 × 0.55	LQM21PN2R2	Murata
1 or 2.2	2 × 1.2 × 1	KSLI2012 series	Hitachi Metal

8.2.2.3 Output Capacitor Selection

The unique hysteretic PWM control scheme of the TPS6223x-Q1 device allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents the converter operate in power save mode and the output voltage ripple is dependent on the output capacitor value and the PFM peak inductor current. Higher output capacitor values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM Mode.

8.2.2.4 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications a 2.2-µF to 4.7-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering. Because a ceramic capacitor loses up to 80% of the initial capacitance at 5 V, TI recommends using 4.7-µF input capacitors for input voltages greater than 4.5 V.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 2 lists some tested input and output capacitors. These components must be verified and validated to determine whether the component is suitable for the end application.

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Table 2. List of Capacitor

CAPACITANCE (µF)	SIZE	CAPACITOR TYPE	SUPPLIER
2.2	0402	GRM155R60J225	Murata
4.7	0402	AMK105BJ475MV	Taiyo Yuden
4.7	0402	GRM155R60J475	Murata
4.7	0402	CL05A475MQ5NRNC	Samsung
4.7	0603	GRM188R60J475	Murata

8.2.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look at the following signals from a steady-state perspective:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These signals are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty-cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout, L-C combination, or both.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turnon of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ × ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_{OUT} to the steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing that helps judge the stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis must occur over the input voltage range, load current range, and temperature range.

8.2.3 Application Curves

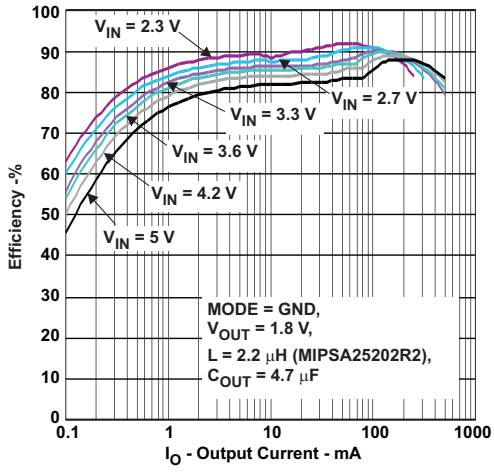


Figure 6. Efficiency: PFM and PWM Mode, 1.8-V Output Voltage

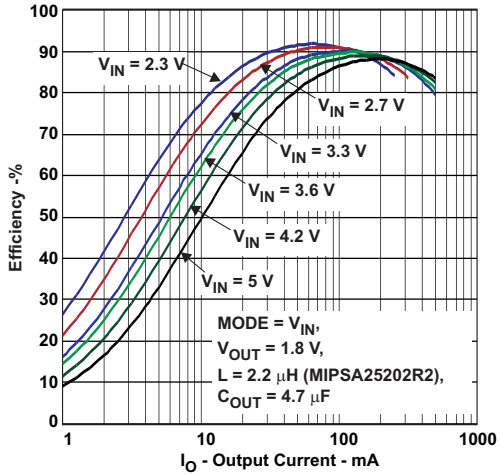


Figure 7. Efficiency: Forced PWM Mode, 1.8-V Output Voltage

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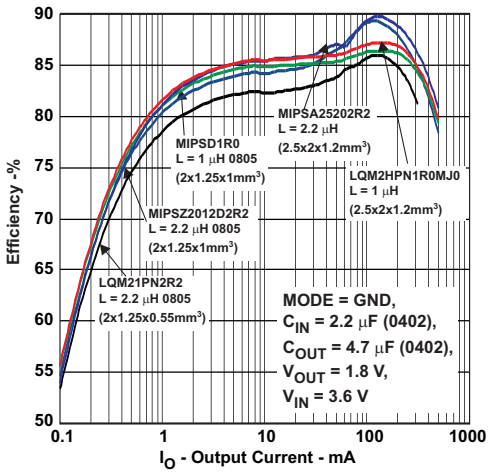


Figure 8. Comparison Efficiency vs Inductor Value and Size

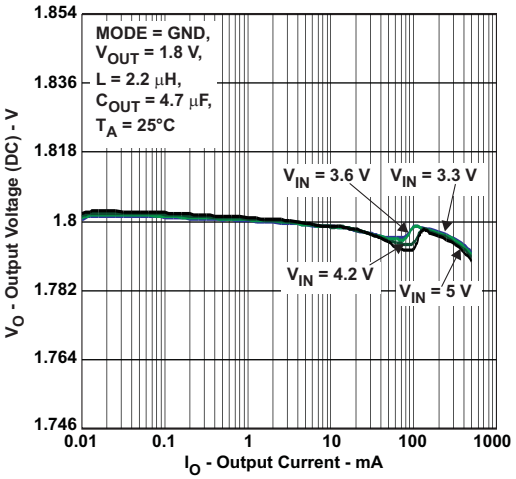


Figure 9. 1.8-V Output-Voltage Accuracy, PFM and PWM Mode

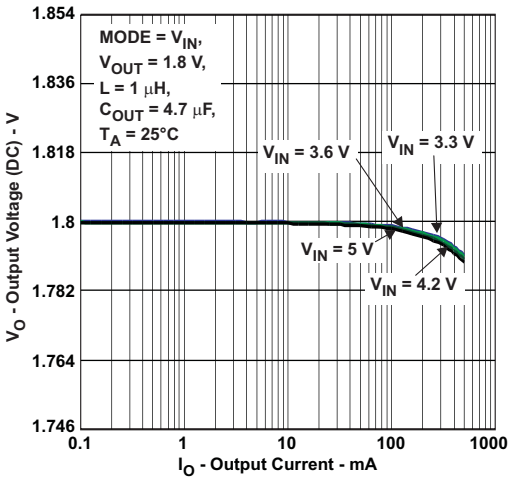


Figure 10. 1.8-V Output-Voltage Accuracy, Forced PWM Mode

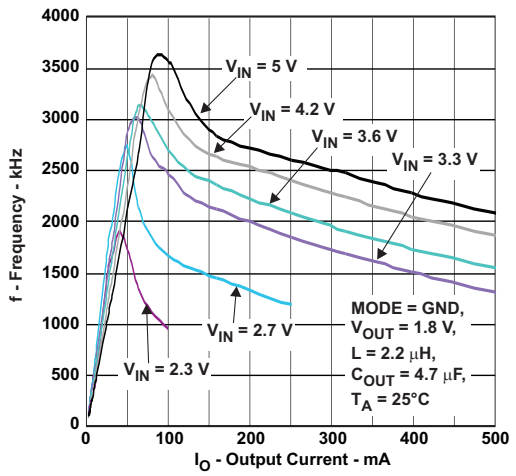


Figure 11. Switching Frequency vs Output Current, 1.8-V Output Voltage, Mode = GND

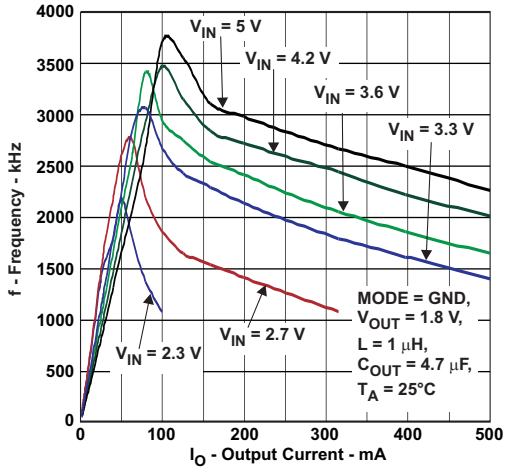


Figure 12. Switching Frequency vs Output Current, 1.8-V Output Voltage, Mode = GND

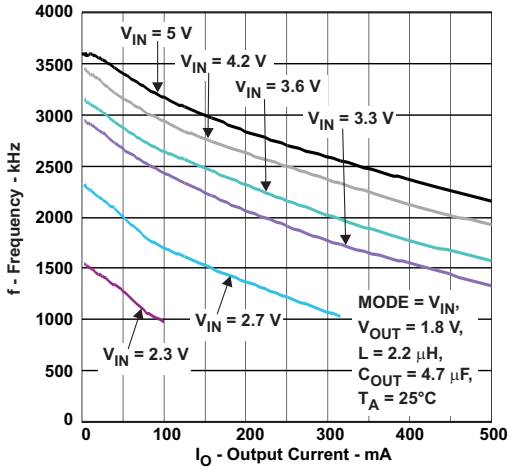


Figure 13. Switching Frequency vs Output Current, 1.8-V Output Voltage, Mode = V_{IN}

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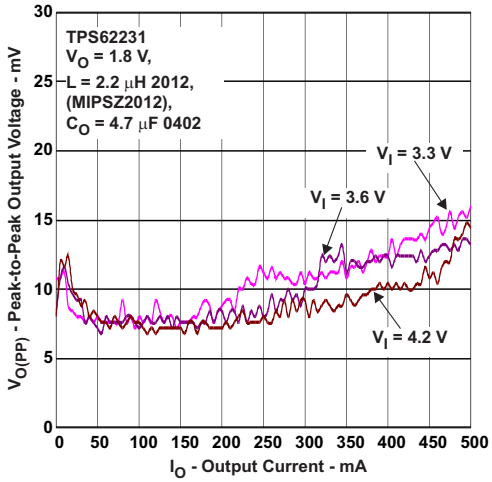


Figure 14. TPS62231-Q1: Output Voltage, Peak-to-Peak vs Output Current

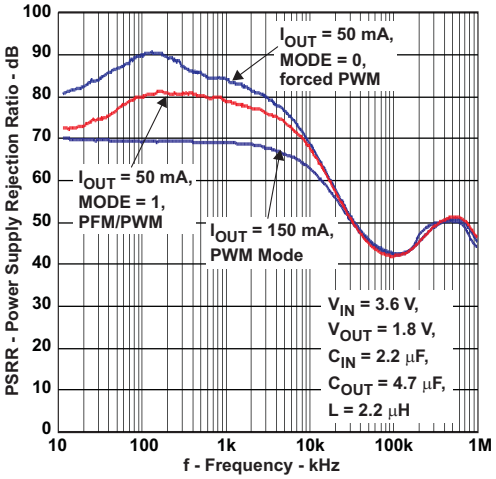


Figure 15. TPS62231-Q1 1.8-V PSRR

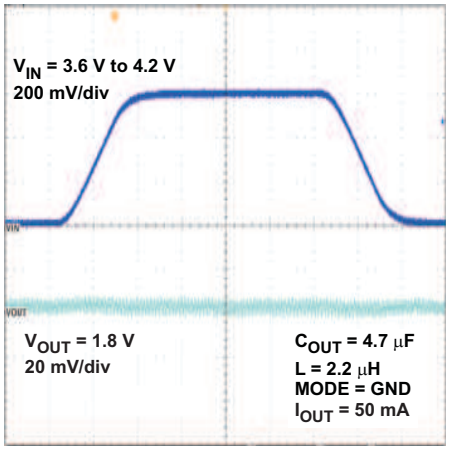


Figure 16. Line Transient Response: PFM Mode

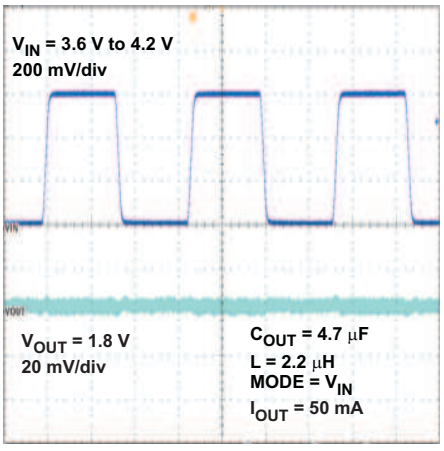


Figure 17. Line Transient Response: PWM Mode

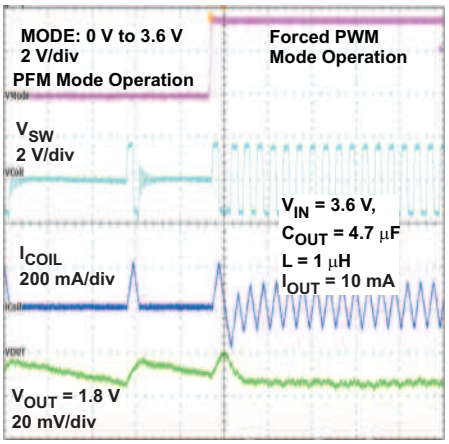


Figure 18. Mode Transition: PFM and Forced PWM Mode

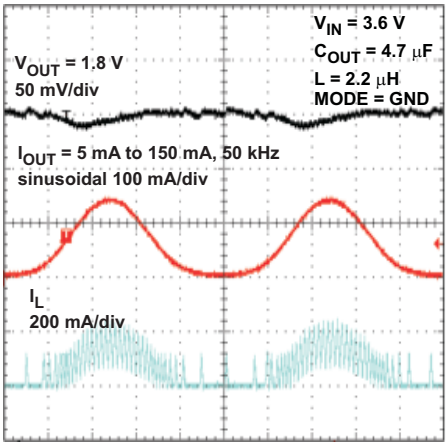


Figure 19. AC Load-Regulation Performance: 1.8-V V_{OUT}, PFM Mode

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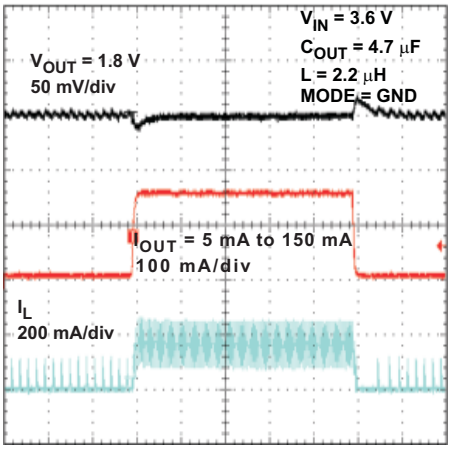


Figure 20. Load Transient Response: 5m A to 150 mA, PFM to PWM Mode, V_{OUT} 1.8 V

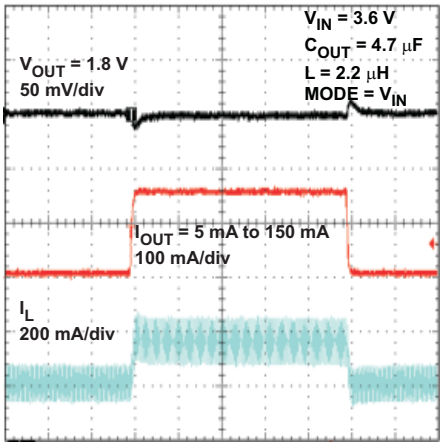


Figure 21. Load Transient Response: 5 mA to 150 mA, Forced PWM Mode, V_{OUT} 1.8 V

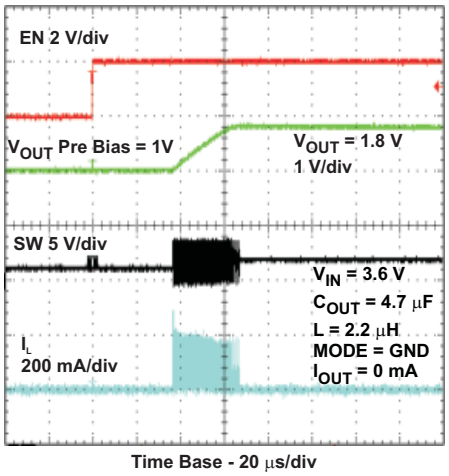


Figure 22. Startup in 1-V Pre-biased Output

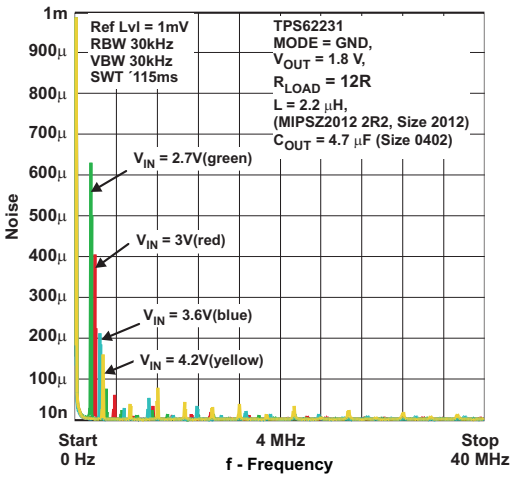


Figure 23. TPS62231-Q1: Spurious Output Noise, 12R Load

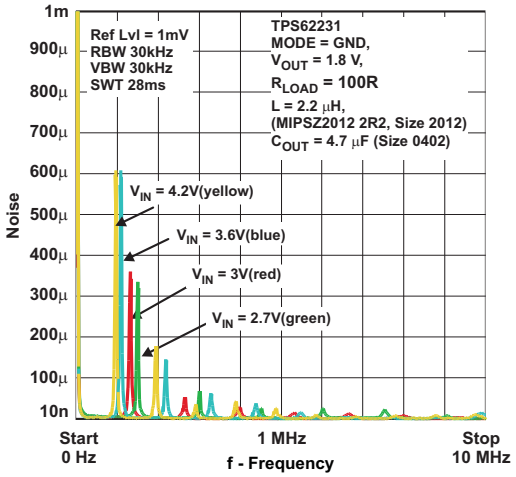


Figure 24. TPS62231-Q1: Spurious Output Noise, 100R Load

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9 Power Supply Recommendations

The TPS6223x-Q1 family of devices has no special requirements for the input power supply. The output current of the input power supply must to be rated according to the supply voltage, output voltage, and output current of the TPS6223x-Q1 family of devices.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Use care when designing the board layout to get the specified performance. If the layout is not done carefully, the regulator could show poor line regulation, load regulation, stability issues, and EMI problems. Providing a low-inductance, low-impedance ground path is critical. Therefore, use wide and short traces for the main current paths. Place the input capacitor as close as possible to the IC pins as well as the inductor and output capacitor.

Use a common power GND node and a different node for the Signal GND to minimize the effects of ground noise. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. Connect the FB line to the output capacitor and route the line away from noisy components and traces (for example, SW line).

10.2 Layout Example

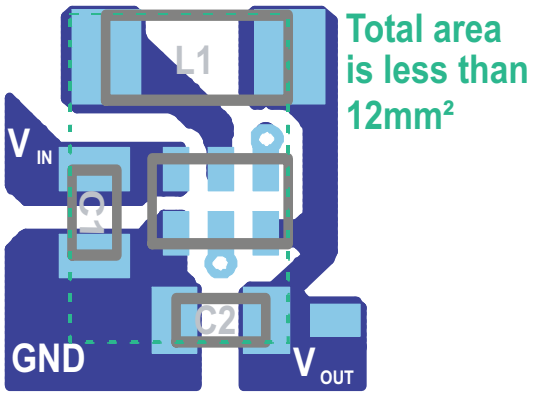


Figure 25. Recommended PCB Layout for TPS6223x-Q1

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Basic Calculation of a Buck Converter's Power Stage*, SLVA477
- *QFN/SON PCB Attachment*, SLUA271
- *Performing Accurate PFM Mode Efficiency Measurements*, SLVA236

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62231-Q1	Click here	Click here	Click here	Click here	Click here
TPS622314-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS622314TDRYRQ1	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	14
TPS622314TDRYRQ1.A	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	14
TPS62231TDRYRQ1	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	31
TPS62231TDRYRQ1.A	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	31

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

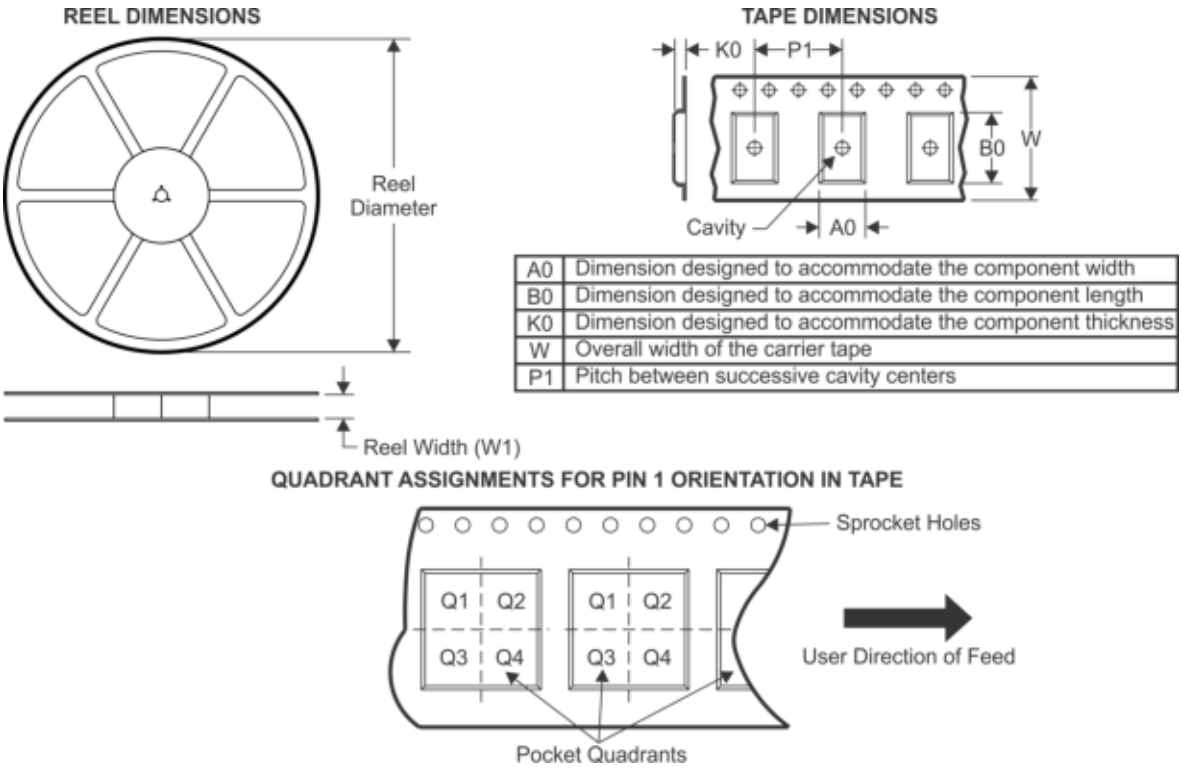
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

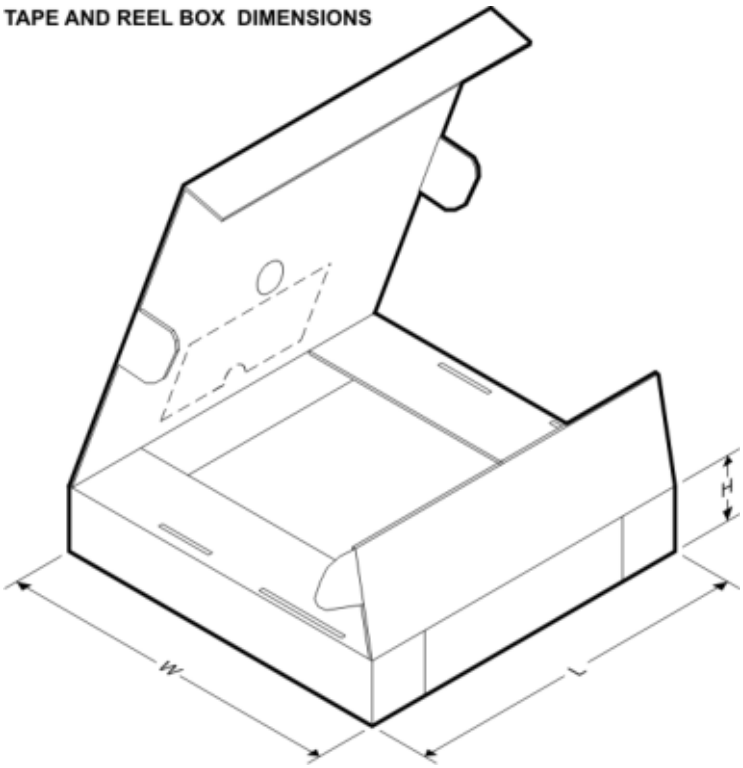


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS622314TDRYRQ1	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1
TPS62231TDRYRQ1	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS622314TDRYRQ1	SON	DRY	6	5000	213.0	191.0	35.0
TPS62231TDRYRQ1	SON	DRY	6	5000	213.0	191.0	35.0

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



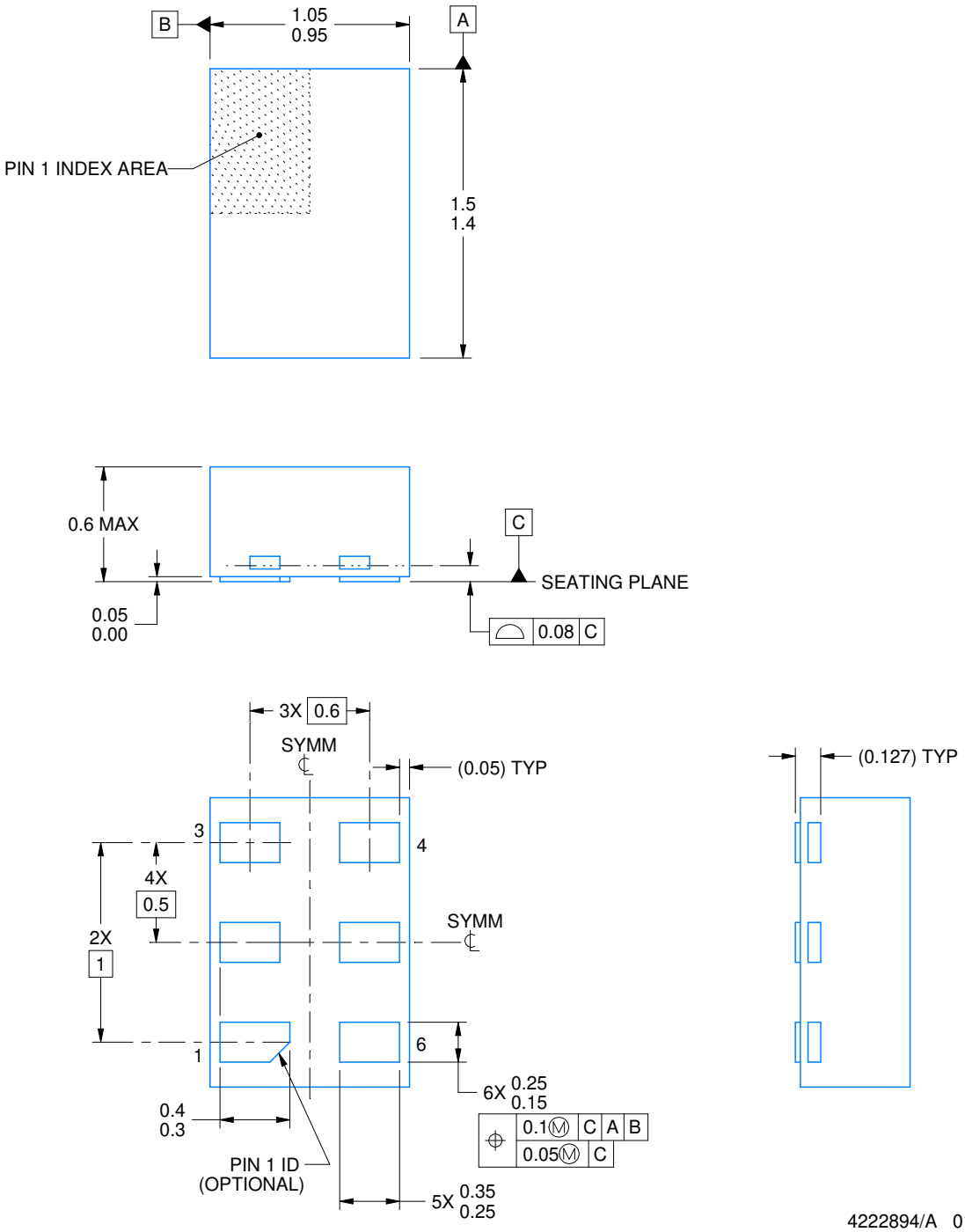
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRY0006A

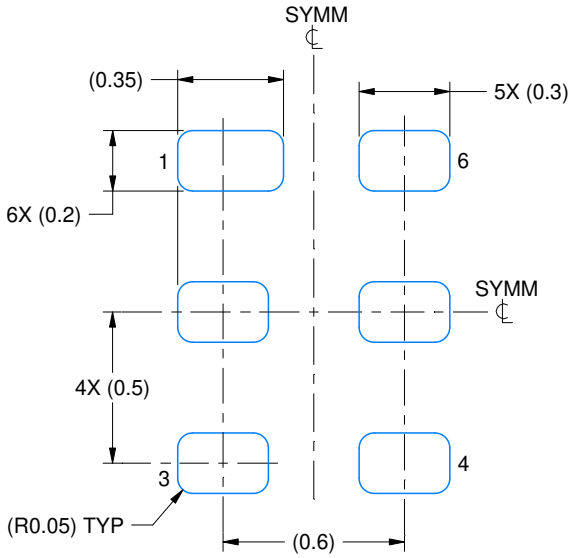
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

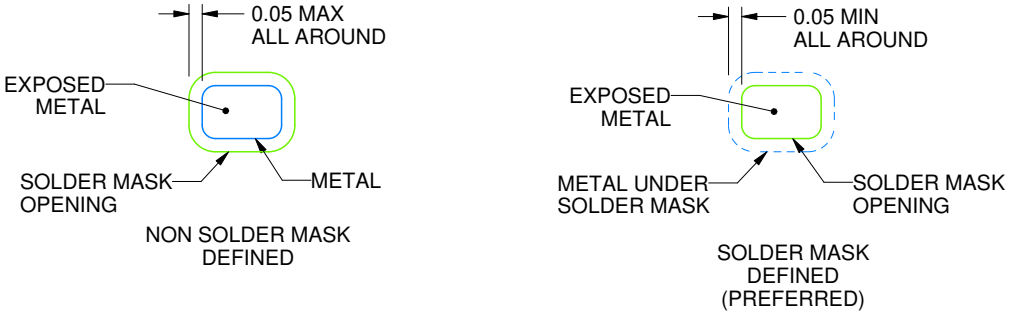


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

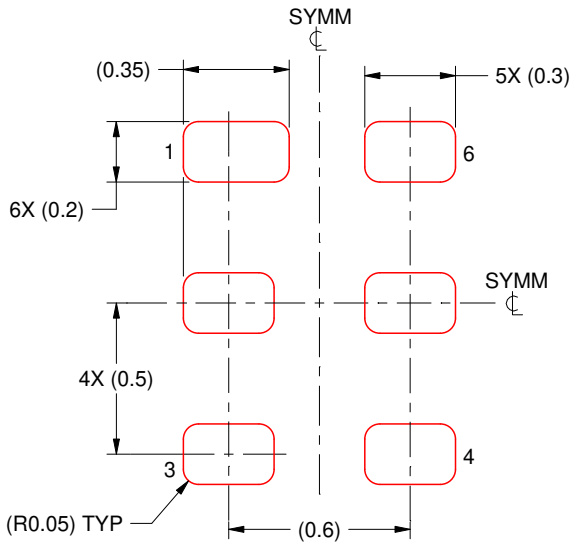
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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