TPS799-Q1 Automotive, 200-mA, Low Quiescent Current, Ultra-Low Noise, High PSRR, Low Dropout, Linear Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade –40°C to +125°C, T_A
- 200-mA low-dropout (LDO) regulator with enable (EN)
- Low I_Q: 40 µA
- Multiple output voltage versions available:
  - Fixed outputs of 1.2 V to 4.5 V
  - Adjustable outputs from 1.2 V to 6.5 V
- High PSRR: 66 dB at 1 kHz, 51 db at 10 kHz
- Ultra-low noise: 29.5 μV_{RMS}
- Fast start-up time: 45 µs
- Stable with a low ESR, 2-µF (typical) output capacitance
- Excellent load and line transient response
- 2% overall accuracy (load, line, and temperature)
- Very low dropout: 100 mV
- Thin SOT-23 and 2-mm × 2-mm WSON-6 packages

2 Applications

- Infotainment and clusters
- Advanced driver assistance systems

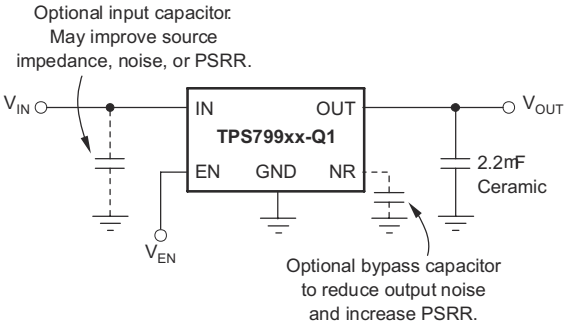
3 Description

The TPS799-Q1 low-dropout (LDO) low-power linear regulator offers excellent AC performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40-µA (typical) ground current. The TPS799-Q1 is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a dropout voltage of 100 mV (typical) at a 200-mA output. The TPS799-Q1 uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations. The device is fully specified from T_J = –40°C to +125°C and is offered in low-profile, thin SOT-23 and 2-mm × 2-mm WSON packages, designed for wireless handsets and WLAN cards.

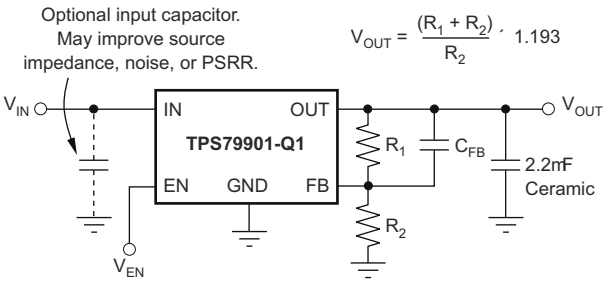
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS799-Q1	DRV (WSON, 6)	2 mm × 2 mm
	DDC (SOT-23, 5)	2.9 mm × 2.8 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit Fixed Voltage Versions



Typical Application Circuit Adjustable Voltage Version

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2015) to Revision G (June 2023)	Page
• Changed *SON* to *WSON* throughout document	1
• Changed automotive-specific *Features* bullet	1
• Added DRV (WSON) pinout to *Pin Configuration and Functions* section	3
• Changed *Layout Example* figure	13

Changes from Revision E (January 2012) to Revision F (March 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added High PSRR: 51 db at 10 kHz	1

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5 Pin Configuration and Functions

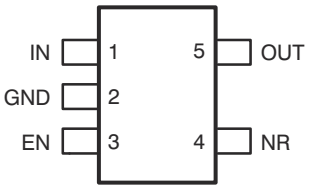


Figure 5-1. DDC Package, 5-Pin SOT-23 (Top View)

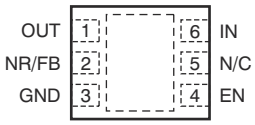


Figure 5-2. DRV Package, 6-Pin WSON (Top View)

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOT-23	WSON		
EN	3	4	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	—	2	I	Adjustable version only; this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	2	3, Pad	—	Ground. The pad must be tied to GND.
IN	1	6	I	Input supply.
N/C	—	5	—	Not internally connected. This pin must either be left open or tied to GND.
NR	4	2	—	Fixed-voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal band gap. This capacitor allows output noise to be reduced to very low levels.
OUT	5	1	O	Output of the regulator. A small capacitor (total typical capacitance ≥ 2 µF ceramic) is needed from this pin to ground to ensure stability.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	7	V
	Enable, V_{EN}	–0.3	V_{IN} + 0.3	V
	V_{OUT}	–0.3	V_{IN} + 0.3	V
	Peak output current	Internally limited		
	Continuous total power dissipation	See *Thermal Information*		
Temperature	Junction, T_J	–55	150	°C
	Storage junction, T_{stg}	–55	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		6.5	V
I_{OUT}	Output current	0.5		200	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS799-Q1		UNIT
		DRV (SON)	DDC (SOT-23)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.2	178.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	70.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	145.9	73.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.4	74.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

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6.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901-Q1, V_{OUT} = 3 V; typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		6.5	V
V_{FB}	Internal reference (TPS79901-Q1)			1.169	1.193	1.217	V
V_{OUT}	Output voltage range (TPS79901-Q1)			V_{FB}		6.5 – V_{DO}	V
V_{OUT}	Output accuracy	Nominal, T_J = 25°C		–1%		1%	
	Output accuracy(1)	Over V_{IN}, I_{OUT}, temperature, V_{OUT} + 0.3 V ≤ V_{IN} ≤ 6.5 V, 500 µA ≤ I_{OUT} ≤ 200 mA		–2%	±1%	2%	
ΔV_{OUT}%/ ΔV_{IN}	Line regulation(1)	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	500 µA ≤ I_{OUT} ≤ 200 mA			0.002		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(NOM)}$ – 0.1 V)	V_{OUT} < 3.3 V	I_{OUT} = 200 mA		100	175	mV
		V_{OUT} ≥ 3.3 V			90	160	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		200	400	600	mA
I_{GND}	Ground pin current	500 µA ≤ I_{OUT} ≤ 200 mA			40	60	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V, 2.7 V ≤ V_{IN} ≤ 6.5 V			0.15	1	µA
I_{FB}	Feedback pin current (TPS79901-Q1)			–0.5		0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.85 V, V_{OUT} = 2.85 V, C_{NR} = 0.01 µF, I_{OUT} = 100 mA	f = 100 Hz		70		dB
			f = 1 kHz		66		
			f = 10 kHz		51		
			f = 100 kHz		38		
V_N	Output noise voltage BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	C_{NR} = 0.01 µF			10.5 V_{OUT}		μV_{RMS}
		C_{NR} = none			94 V_{OUT}		
T_{STR}	Start-up time	V_{OUT} = 2.85 V, R_L = 14 Ω, C_{OUT} = 2.2 µF	C_{NR} = 0.001 µF		45		µs
			C_{NR} = 0.047 µF		45		
			C_{NR} = 0.01 µF		50		
			C_{NR} = none		50		
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1	µA
TSD	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		
T_J	Operating junction temperature			–40		125	°C
V_{UVLO}	Undervoltage lockout	V_{IN} rising		1.9	2.2	2.65	V
$V_{UVLO,hys}$	Hysteresis	V_{IN} falling			70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater.
(2) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.8 V because minimum V_{IN} = 2.7 V.

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6.6 Typical Characteristics

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901-Q1, V_{OUT} = 3 V; typical values are at T_J = 25°C

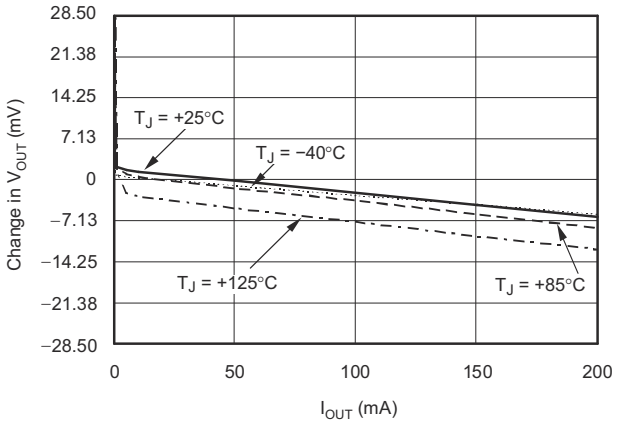


Figure 6-1. Load Regulation

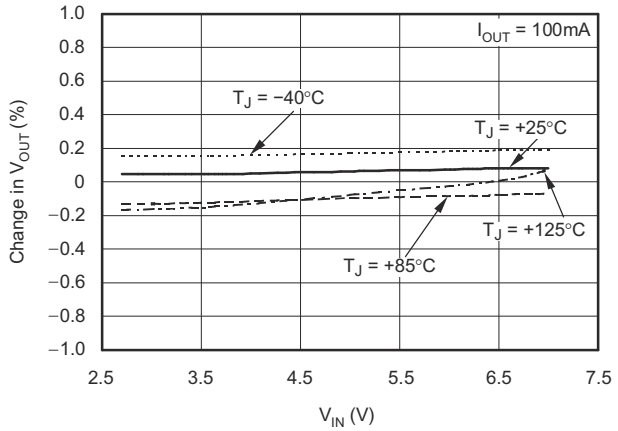


Figure 6-2. Line Regulation

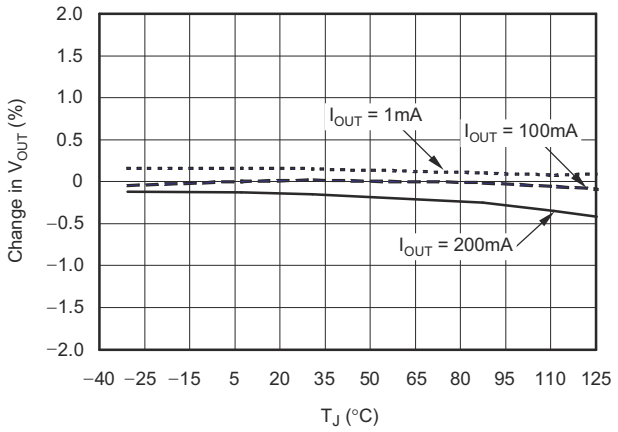


Figure 6-3. Output Voltage vs Junction Temperature

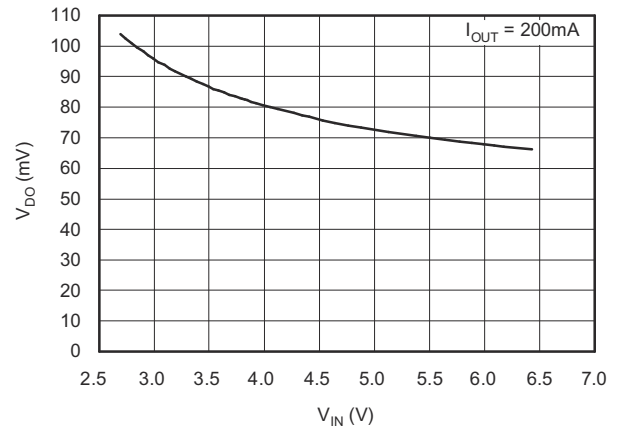


Figure 6-4. TPS79901-Q1 Dropout vs Input Voltage

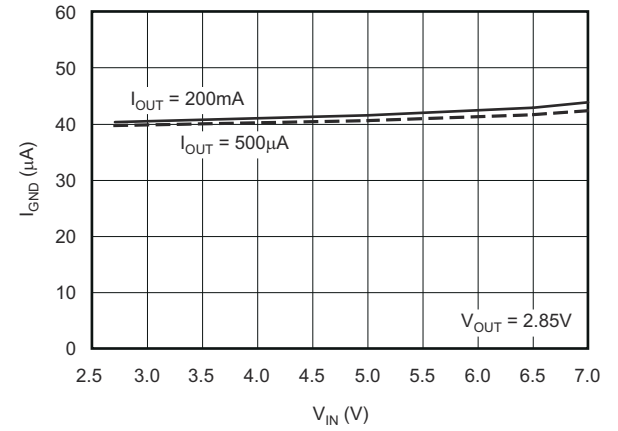


Figure 6-5. Ground Pin Current vs Input Voltage

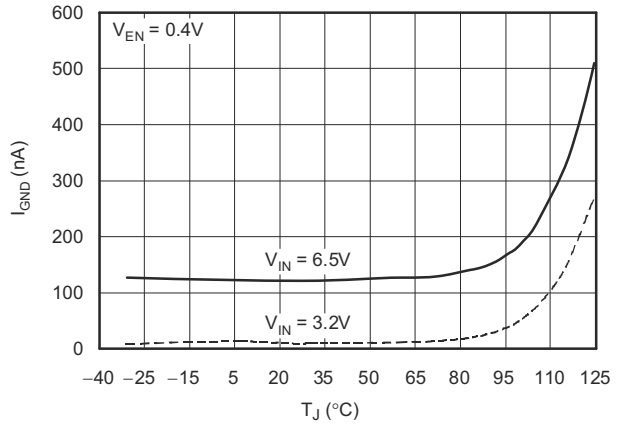


Figure 6-6. Ground Pin Current (Disabled) vs Junction Temperature

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6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, and C_{NR} = 0.01 µF (unless otherwise noted); for TPS79901-Q1, V_{OUT} = 3 V; typical values are at T_J = 25°C

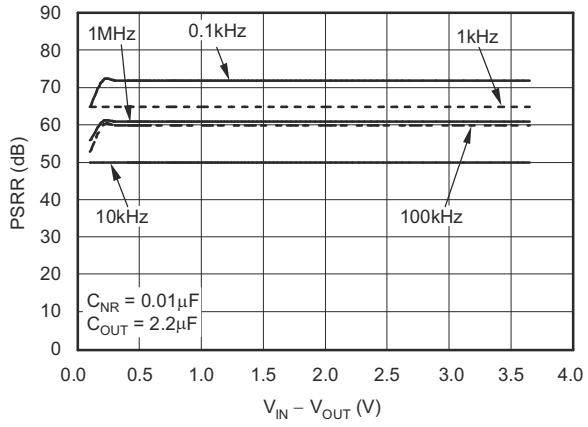


Figure 6-7. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}, I_{OUT} = 1 mA

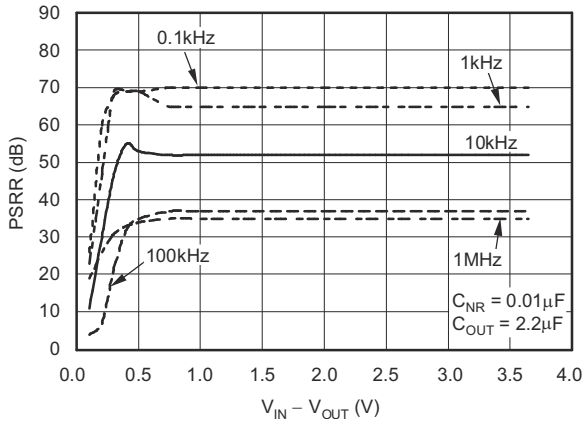


Figure 6-8. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}, I_{OUT} = 100 mA

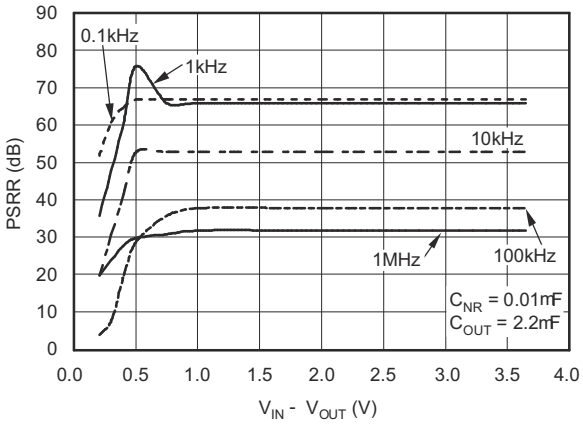


Figure 6-9. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}, I_{OUT} = 200 mA

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7 Detailed Description

7.1 Overview

The TPS799-Q1 low-dropout (LDO) regulator combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current make this device optimal for portable applications. All versions have thermal and overcurrent protection, and are fully specified from –40°C to +125°C.

The TPS799-Q1 also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device. If voltage at the output overshoots 5% from the nominal value, a pulldown resistor reduces the voltage to normal operating conditions, as illustrated in the *Functional Block Diagrams*.

7.2 Functional Block Diagrams

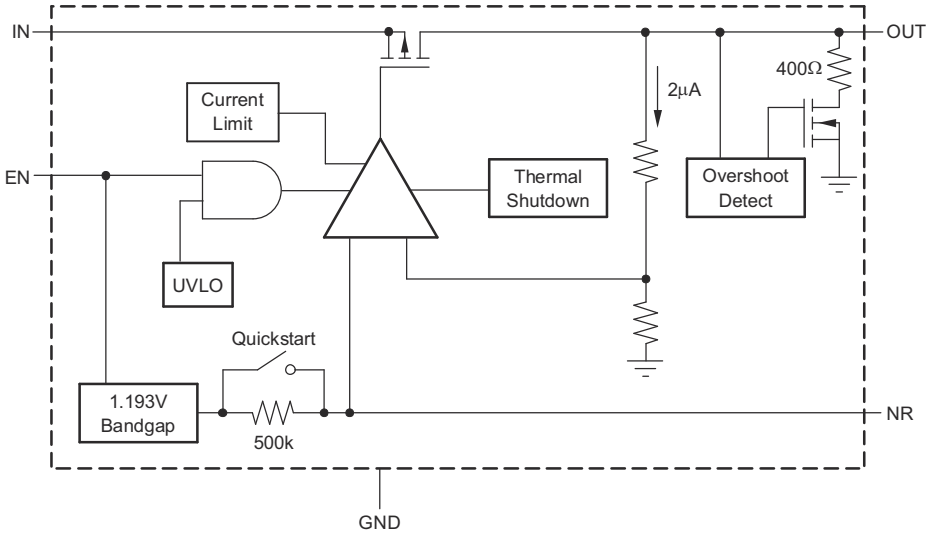


Figure 7-1. Fixed-Voltage Version

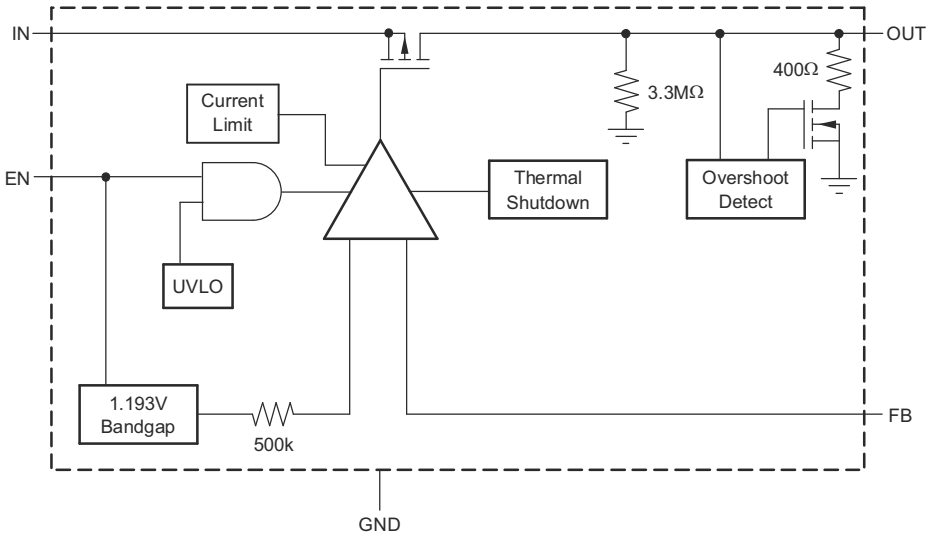


Figure 7-2. Adjustable-Voltage Version

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7.3 Feature Description

7.3.1 Internal Current Limit

The TPS799-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device must not be operated in current limit for extended periods of time.

The PMOS pass transistor in the TPS799-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting can be appropriate.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.3 Dropout Voltage

The TPS799-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS, ON}$ of the PMOS pass transistor. Because the PMOS transistor behaves like a resistor in dropout, V_{DO} scales approximately with output current.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 6-7 through Figure 6-9 in the *Typical Characteristics* section.

7.3.4 Start-Up

Fixed voltage versions of the TPS799-Q1 use a quick-start circuit to fast-charge the noise-reduction capacitor, C_{NR}, if present (see Figure 7-1). This circuit allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

For the fastest start-up, apply V_{IN} first, then drive the enable pin (EN) high. If EN is tied to IN, start-up is somewhat slower. The quick-start switch is closed for approximately 135 µs. To ensure that C_{NR} is fully charged during the quick-start time, a 0.01 µF or smaller capacitor must be used.

7.3.5 Undervoltage Lockout (UVLO)

The TPS799-Q1 uses a UVLO circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that the circuit typically ignores undershoot transients on the input if they are less than 50-µs duration.

7.4 Device Functional Modes

Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 150 nA, nominal.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS799-Q1 LDO regulator combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). Fixed-voltage versions provide a noise reduction pin to bypass noise generated by the band-gap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at start-up. The combination of high performance and low ground current also make the TPS799-Q1 designed for portable applications. All versions have thermal and overcurrent protection and are fully specified from –40°C to +125°C.

Figure 8-1 shows the basic circuit connections for fixed-voltage model. Figure 8-2 gives the connections for the adjustable output version (TPS79901-Q1). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 8-2. Sample resistor values for common output voltages are shown in Figure 8-2.

8.2 Typical Application

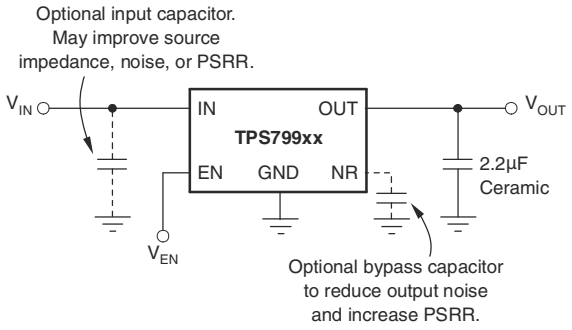


Figure 8-1. Typical Application Circuit for Fixed-Voltage Version

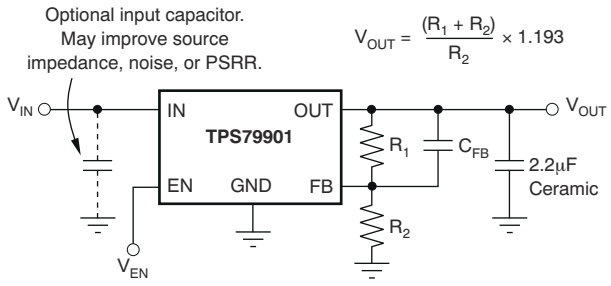


Figure 8-2. Typical Application Circuit for Adjustable-Voltage Version

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8.2.1 Design Requirements

Select the desired device based on the output voltage. Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor can be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor can be necessary to ensure stability.

The TPS799-Q1 is designed to be stable with standard ceramic capacitors of values 2.2 µF or larger. X5R and X7R type capacitors are best as they have minimal variation in value and ESR over temperature. Maximum ESR must be <1 Ω.

8.2.2.2 Feedback Capacitor Requirements (TPS79901-Q1 Only)

The feedback capacitor, C_{FB}, shown in Figure 8-2 is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value from 3 pF to 1 nF can be used. Fixed-voltage versions have an internal 30-pF feedback capacitor that is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5 pF must be used to ensure fast start-up; values above 47 pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901-Q1 device is stable in unity-gain configuration (OUT tied to FB) without C_{FB}.

8.2.2.3 Output Noise

In most LDOs, the band gap is the dominant noise source. If a noise-reduction capacitor (C_{NR}) is used with the TPS799-Q1, the band gap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2 µA of divider current has the same noise performance as a fixed-voltage version. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with C_{NR} = 0.01 µF, total noise is approximately given by Equation 1:

$$V_N = \frac{10.5\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

The adjustable version of the TPS79901-Q1 device does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the previous recommendations.

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increase duration of the transient response. In the adjustable version, adding C_{FB} between OUT and FB improves stability and transient response. The transient response of the TPS799-Q1 is enhanced by an active pulldown that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pulldown device behaves like a 350-Ω resistor to ground.

8.2.2.5 Minimum Load

The TPS799-Q1 is stable and well behaved with no output load. To meet the specified accuracy, a minimum load of 500 µA is required. Below 500 µA at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown to turn on. The output pulldown limits voltage drift to 5% typically, but ground current

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can increase by approximately 50 µA. In typical applications, the junction cannot reach high temperatures at light loads because there is no appreciable dissipated power. The specified ground current is valid at no load, in most applications.

8.2.3 Application Curve

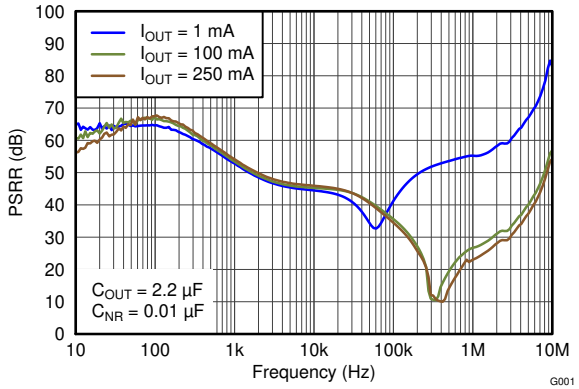


Figure 8-3. Power-Supply Rejection Ratio vs Frequency

8.3 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

8.4.1.2 Thermal Consideration

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage from overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799-Q1 is designed to protect against overload conditions. This circuitry was not intended to replace proper heat sinking. Continuously running the TPS799-Q1 into thermal shutdown degrades device reliability.

8.4.1.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal*

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Information table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

8.4.1.4 Package Mounting

Solder pad footprint recommendations for the TPS799-Q1 are available from the TI web site at www.ti.com.

8.4.2 Layout Example

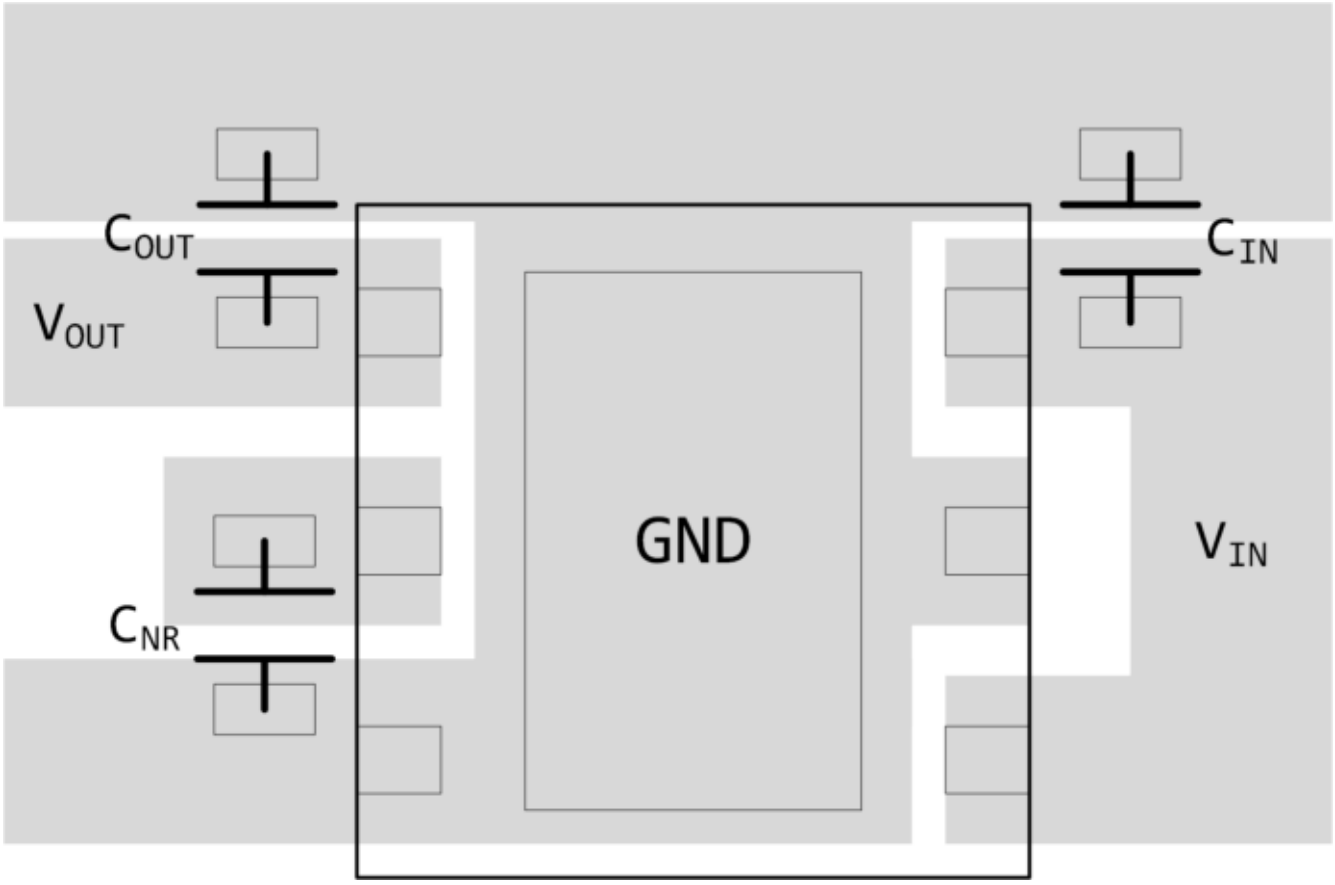


Figure 8-4. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *TPS799xxEVM-105 User's Guide*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS79901QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CFA
TPS79901QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CFA
TPS79912QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAV
TPS79912QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAV
TPS79915QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFC
TPS79915QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFC
TPS79915QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAQ
TPS79915QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAQ
TPS79918QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEW
TPS79918QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEW
TPS79925QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFM
TPS79925QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFM
TPS79927QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFD
TPS79927QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFD
TPS79927QDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFK
TPS79927QDRVRQ1.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFK
TPS79933QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PSEQ
TPS79933QDDCRQ1.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PSEQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS799-Q1 :

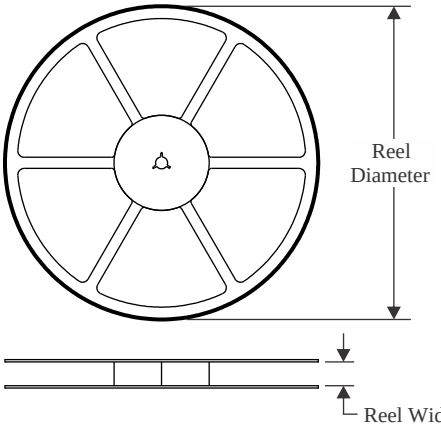
- Catalog : TPS799

NOTE: Qualified Version Definitions:

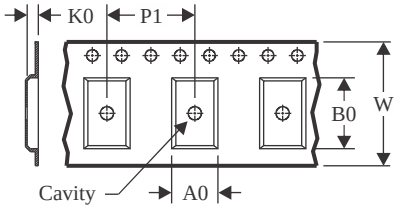
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

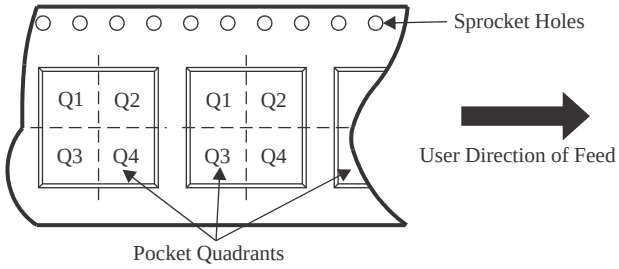


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

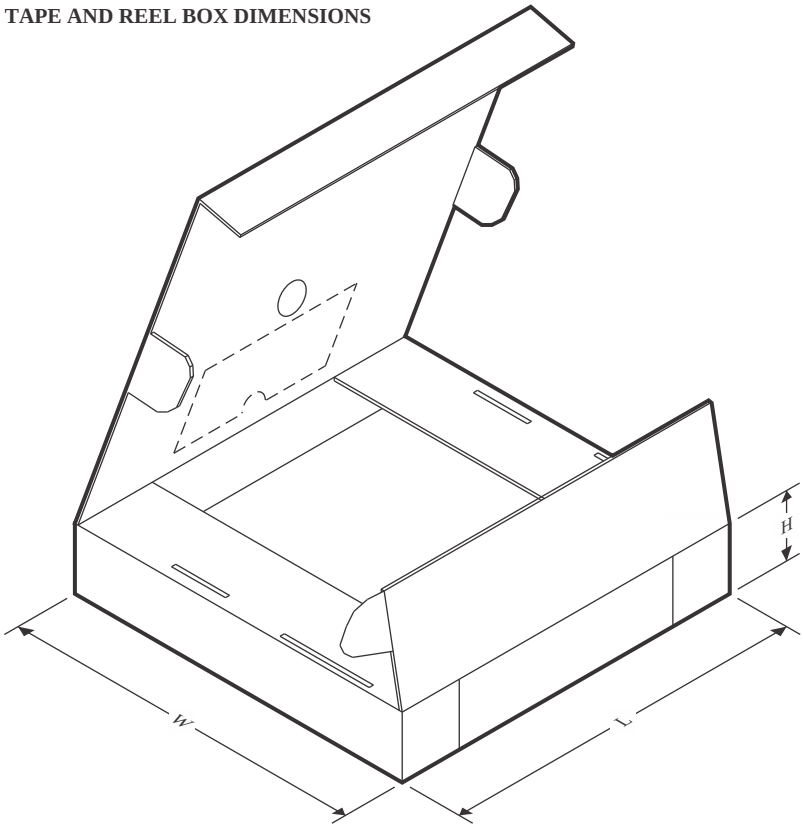
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79901QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79912QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79915QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79915QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79918QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79925QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79933QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



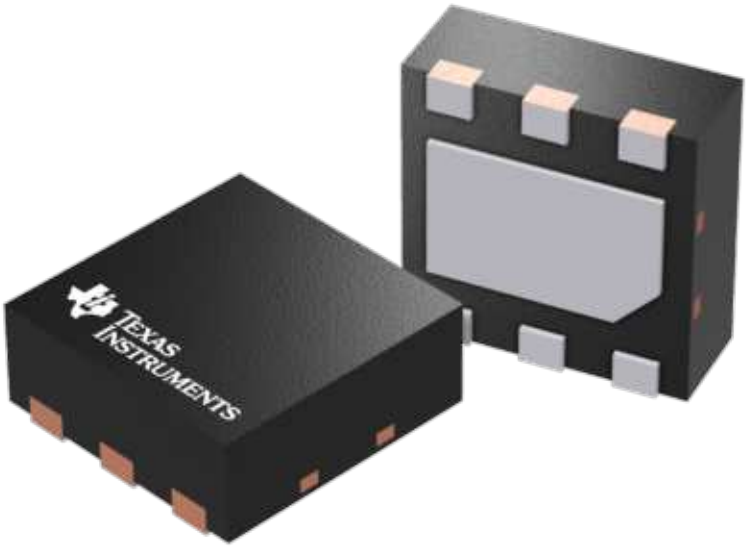
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79901QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS79912QDRVRQ1	WSON	DRV	6	3000	213.0	191.0	35.0
TPS79915QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79915QDRVRQ1	WSON	DRV	6	3000	213.0	191.0	35.0
TPS79918QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79925QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79927QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79927QDRVRQ1	WSON	DRV	6	3000	213.0	191.0	35.0
TPS79933QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0

GENERIC PACKAGE VIEW

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



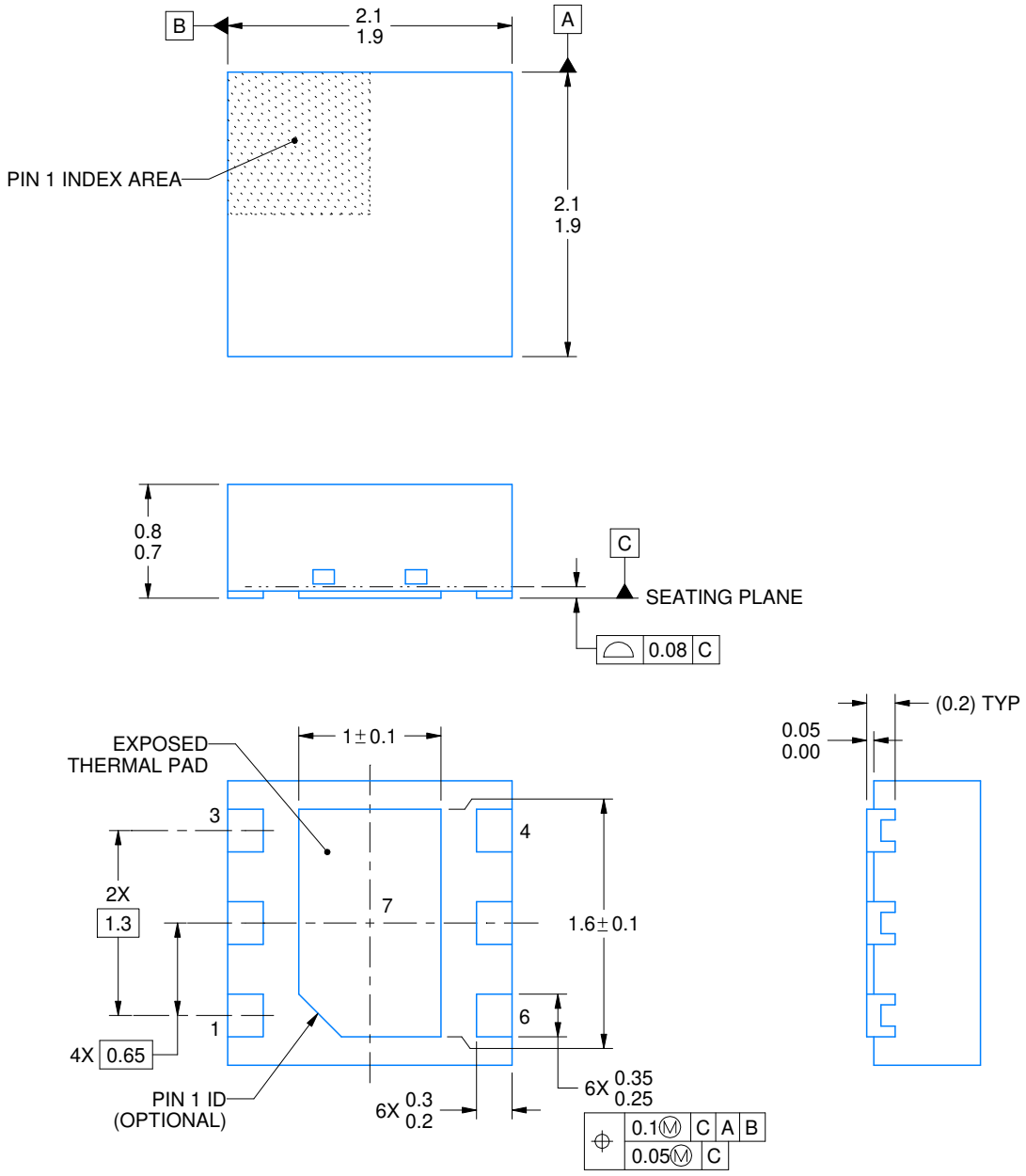
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

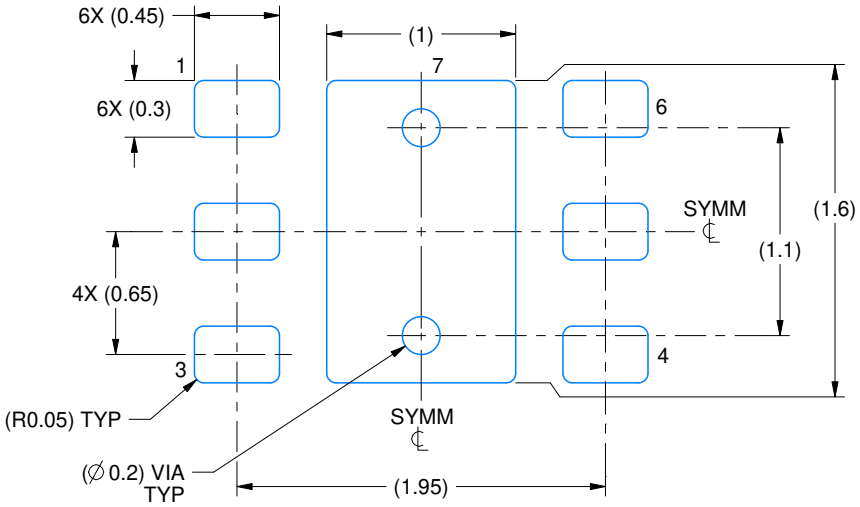
PLASTIC SMALL OUTLINE - NO LEAD



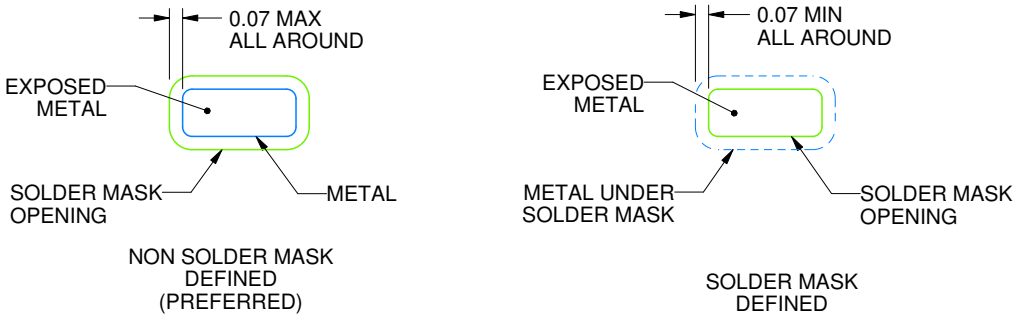
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

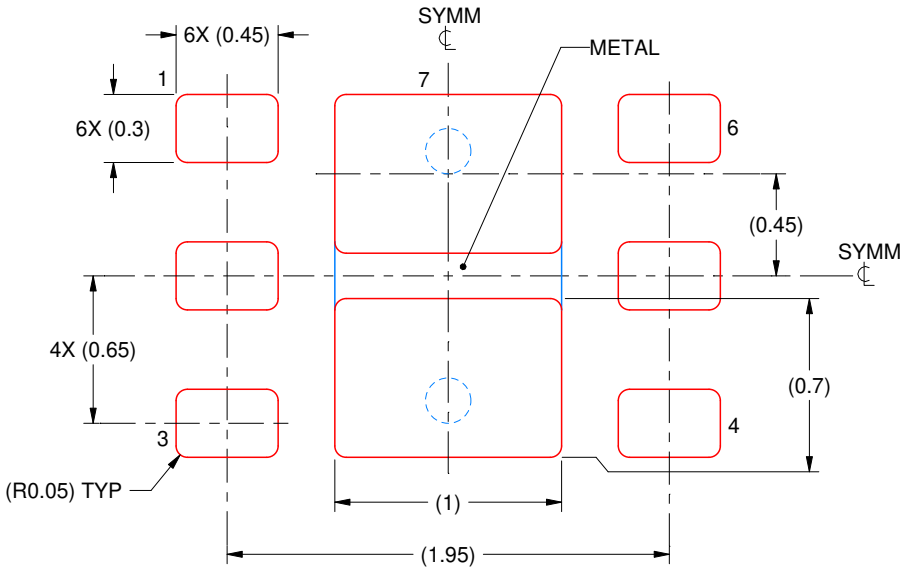


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

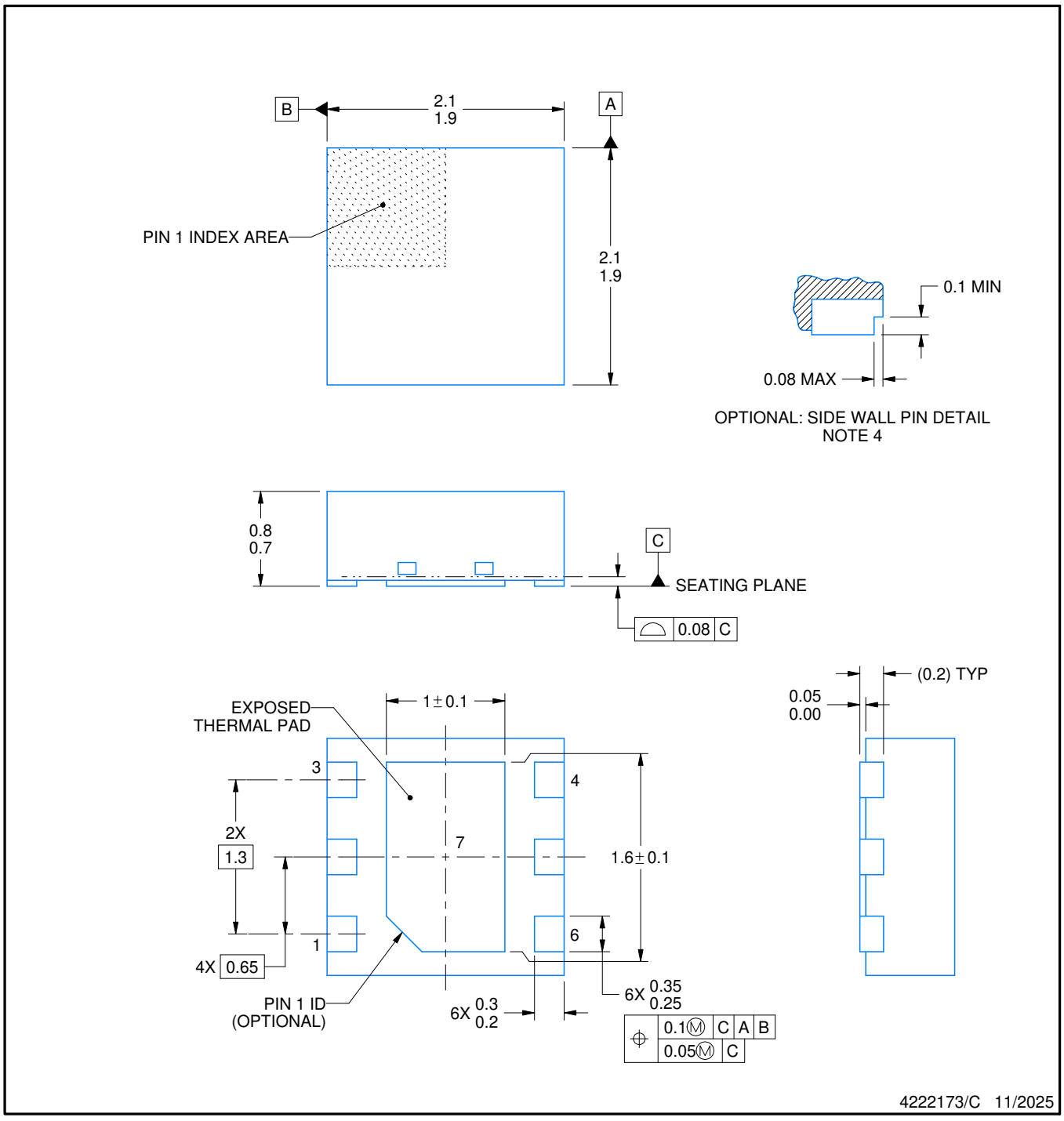
DRV0006A



PACKAGE OUTLINE

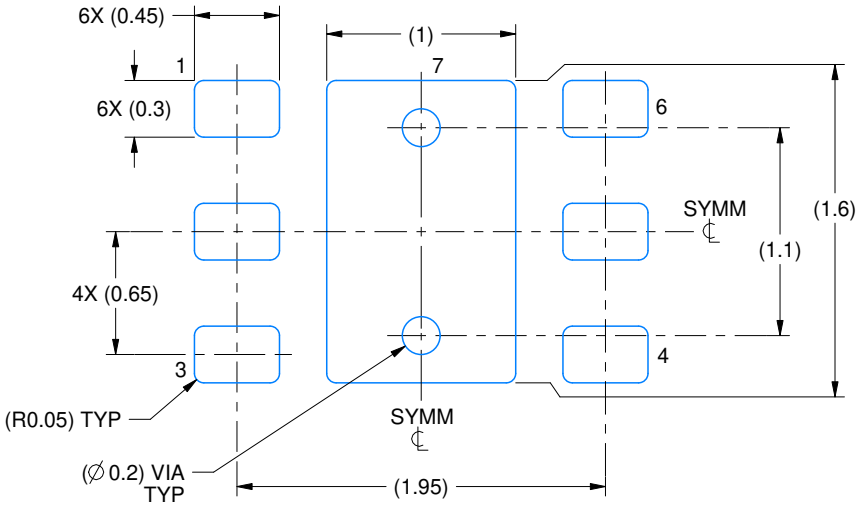
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

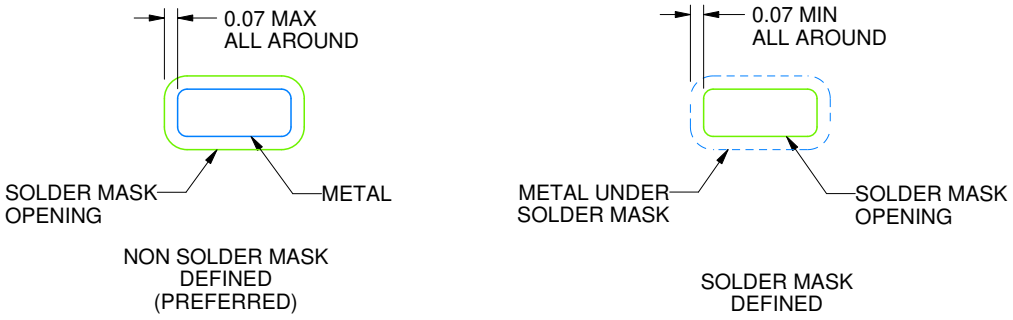


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

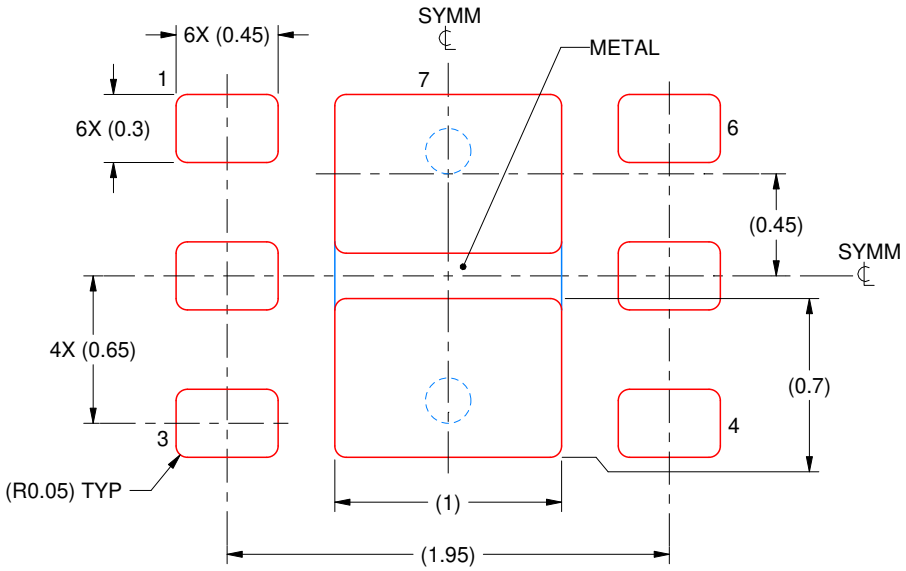


SOLDER MASK DETAILS

4222173/C 11/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

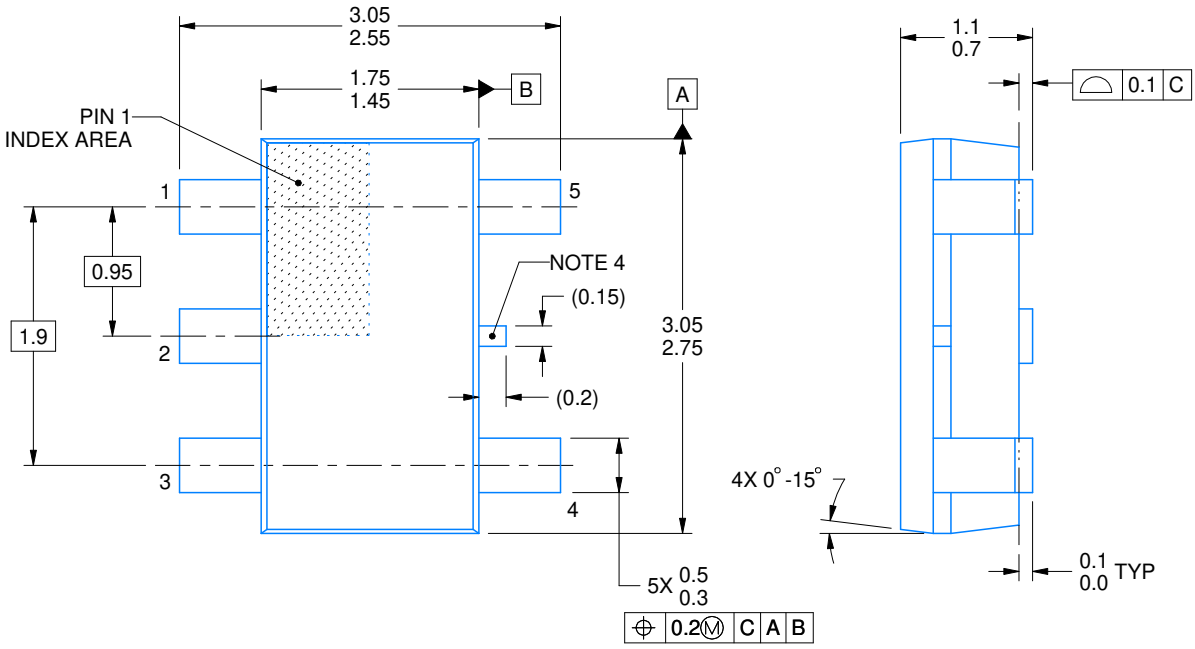
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

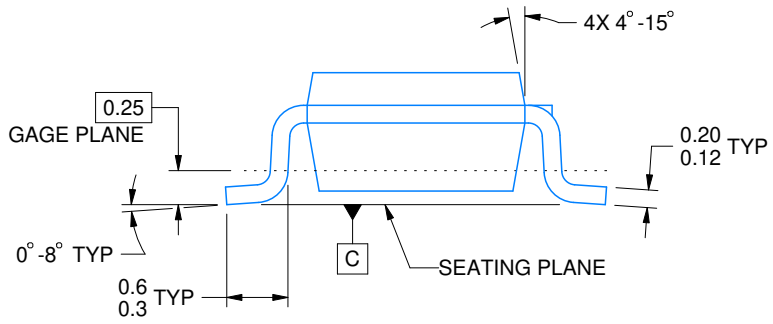
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

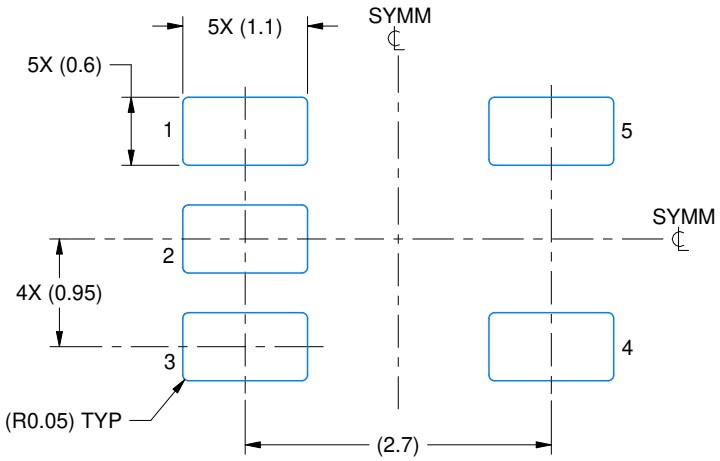




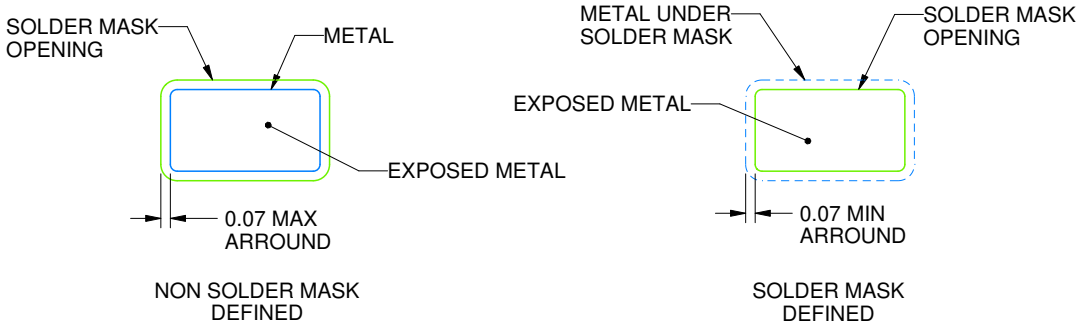
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

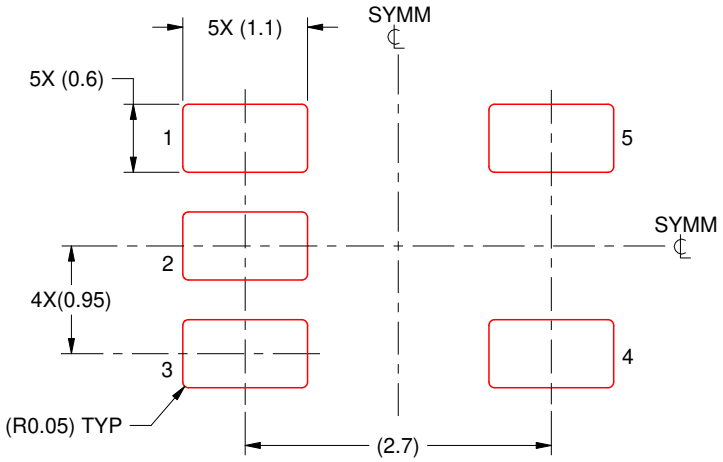


SOLDERMASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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