TRS3243E 3-V to 5.5-V Multichannel RS-232 Line Driver or Receiver With ±15-kV IEC ESD Protection

1 Features

- Single-chip and single-supply interface for IBM™ PC/AT™ serial port
- ESD Protection for RS-232 bus pins
  - ±15-kV Human-body model (HBM)
  - ±8-kV IEC61000-4-2, Contact discharge
  - ±15-kV IEC61000-4-2, Air-gap discharge
- Meets or exceeds requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates with 3-V to 5.5-V V_{CC} supply
- Always-active noninverting receiver output (ROUT2B)
- Designed to transmit at a data rate up to 500 kbit/s
- Low standby current: 1 µA typical
- External capacitors: 4 × 0.1 µF
- Accepts 5-V logic input with 3.3-V supply
- Designed to be interchangeable with industry standard '3243E devices
- Serial-mouse driveability
- Auto-powerdown feature to disable driver outputs when no valid RS-232 signal is sensed
- Package options include plastic small-outline (DW), shrink small-outline (DB), and thin shrink small-outline (PW)

2 Applications

- Battery-powered systems
- Personel electronics
- Notebooks
- Laptops
- Palmtop PCs
- Hand-held equipment

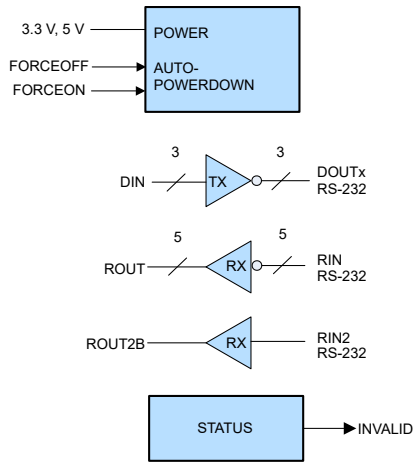
3 Description

The TRS3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port used in an IBM PC/AT, or compatible. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/µs driver output slew rate.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TRS3243E	SSOP (DB)	10.20 mm × 5.30 mm
	SOIC (DW)	17.90 mm x 7.50mm
	TSSOP (PW)	9.70 mm x 4.40 mm
	VQFN (RHB)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Revision History....2
5 Pin Configuration and Functions....3
6 Specifications....6
6.1 Absolute Maximum Ratings....6
6.2 ESD Ratings....6
6.3 ESD Ratings - IEC Specifications....6
6.4 Recommended Operating Conditions....7
6.5 Thermal Information....7
6.6 Electrical Characteristics....8
6.7 Switching Characteristics....9
7 Parameter Measurement Information....10
8 Detailed Description....13
8.1 Overview....13
8.2 Functional Block Diagram....13
8.3 Device Functional Modes....14
9 Application and Implementation....15
9.1 Typical Application....15
10 Device and Documentation Support....18
10.1 Receiving Notification of Documentation Updates....18
10.2 Support Resources....18
10.3 Trademarks....18
10.4 Electrostatic Discharge Caution....18
10.5 Glossary....18
11 Mechanical, Packaging, and Orderable Information....18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2022) to Revision E (December 2022) **Page**

- Changed Table 9-1 to match revision C of the data sheet. V_{CC} column: 3 V ± 5.5 V to: 3 V to 5.5 V and C1 column value: 0.47 µF to: 0.047 µF 15

Changes from Revision C (September 2011) to Revision D (October 2022) **Page**

- Deleted the *Ordering Information* table....1
- Added *Device Information* table, *Pin Configuration and Functions* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Changed the front page image from Block Diagram to Simplified Circuit....1
- Added the *ESD Ratings - IEC Specifications* table....6
- Changed the I_{CC} Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the *Electrical Characteristics* 8

Changes from Revision B (July 2009) to Revision C (September 2011) **Page**

- Deleted "VALID RIN RS-232 LEVEL" from INPUTS....14
- Deleted "ROUT2B is active" RECEIVER STATUS and combined ROUT outputs....14
- Added table "ROUT2B and $\overline{\text{INVALID}}$ Outputs" defining truth for ROUT2B and INVALID outputs. 14

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5 Pin Configuration and Functions

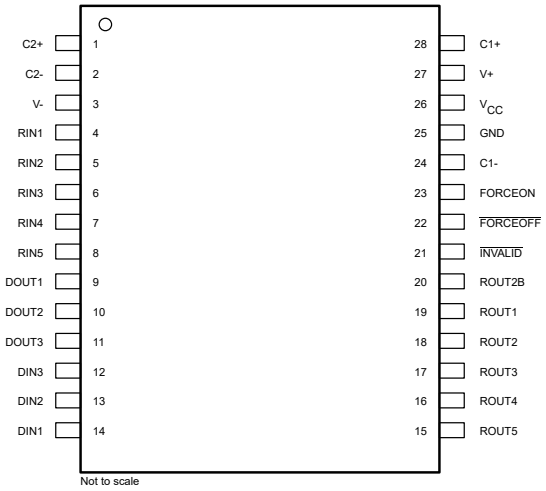


Figure 5-1. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP) (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-		Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	$\overline{\text{INVALID}}$	O	Invalid Output Pin
22	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V_{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor

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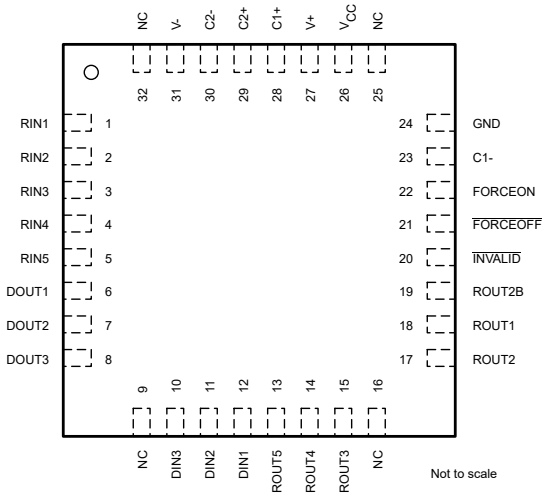


Figure 5-2. RHB Package, 32 Pin (VQFN)
(Top View)

Table 5-2. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RIN1	I	RS-232 receiver inputs
2	RIN2		
3	RIN3		
4	RIN4		
5	RIN5		
6	DOUT1	O	RS-232 driver outputs
7	DOUT2		
8	DOUT3		
9	NC	—	Not connected internally
10	DIN3	I	Driver inputs
11	DIN2		
12	DIN1		
13	ROUT5	O	Receiver outputs
14	ROUT4		
15	ROUT3		
16	NC	—	Not connected internally
17	ROUT2	O	Receiver outputs
18	ROUT1		
19	ROUT2B	O	Always-active noninverting receiver output
20	$\overline{\text{INVALID}}$	O	Invalid Output Pin
21	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
22	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
23	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
24	GND	—	Ground
25	NC	—	Not connected internally
26	V_{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage

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Table 5-2. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor
29	C2+	—	
30	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
31	V-	—	Negative charge pump output voltage
32	NC	—	Not connected internally

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.3	6	V
V+	Positive output supply voltage(2)		–0.3	7	V
V–	Negative output supply voltage(2)		0.3	–7	V
V+ – V–	Output supply voltage difference(2)			13	V
V_I	Input voltage	Driver ($\overline{\text{FORCEOFF}}$, FORCEON)	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage	Driver	–13.2	13.2	V
		Receiver ($\overline{\text{INVALID}}$)	–0.3	V_{CC} + 0.3	
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

				VALUE	UNIT
Driver Section					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) Driver output pins		±15,000	V
Receiver Section					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Receiver input pins	±15,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
Driver Section					
$V_{(ESD)}$	Electrostatic discharge	IEC61000-4-2, Air-Gap Discharge(1)	Driver outputs pins	±15	kV
		IEC61000-4-2, Contact Discharge(1)		±8	
Receiver Section					
$V_{(ESD)}$	Electrostatic discharge	IEC61000-4-2, Air-Gap Discharge(1)	Receiver input pins	±15	kV
		IEC61000-4-2, Contact Discharge(1)		±8	

(1) For the DB, PW and RHB package only: A minimum of 1-µF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating

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6.4 Recommended Operating Conditions

See Figure 9-1 (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		TRS3243EC	0		70	°C
			TRS3243EI	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.5 Thermal Information

THERMAL METRIC(1)		VQFN (RHB) 32 PINS	TSSOP (PW) 28 PINS	SOIC (DW) 28 PINS	DB (SSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	70.3	59.0	76.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.9	21.0	28.8	35.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.6	29.2	30.3	37.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.3	7.8	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.6	28.8	30.0	37.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.1	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 9-1)[2]

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
I_I	Input leakage current	$\overline{FORCEOFF}$, FORCEON				±0.01	±1	µA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC} For DB, PW and RHB package			0.3	1.2	mA
		Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC} For DW package			0.3	1	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND			1	10	µA
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded, All DIN are grounded			1	10	µA
DRIVER SECTION								
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND			5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND			–5	–5.4		V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA			±5			V
I_{IH}	High-level input current	V_I = V_{CC}				±0.01	±1	µA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	µA
V_{hys}	Input hysteresis						±1	V
I_{OS}	Short-circuit output current[3]	V_{CC} = 3.6 V,	V_O = 0 V				±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V					
r_O	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND,	V_O = ±12 V,	V_{CC} = 0 to 5.5 V			±25	µA
RECEIVER SECTION								
V_{OH}	High-level output voltage	I_{OH} = –1 mA			V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA					0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V				1.6	2.4	V
		V_{CC} = 5 V				1.9	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V			0.6	1.1		V
		V_{CC} = 5 V			0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)					0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{FORCEOFF}$ = 0 V				±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V or ±25 V			3	5	7	kΩ
AUTO-POWERDOWN SECTION								
$V_{IT+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}					2.7	V
$V_{IT–(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			–2.7			V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			–0.3		0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = -1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			V_{CC} – 0.6			V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}					0.4	V

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

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6.7 Switching Characteristics

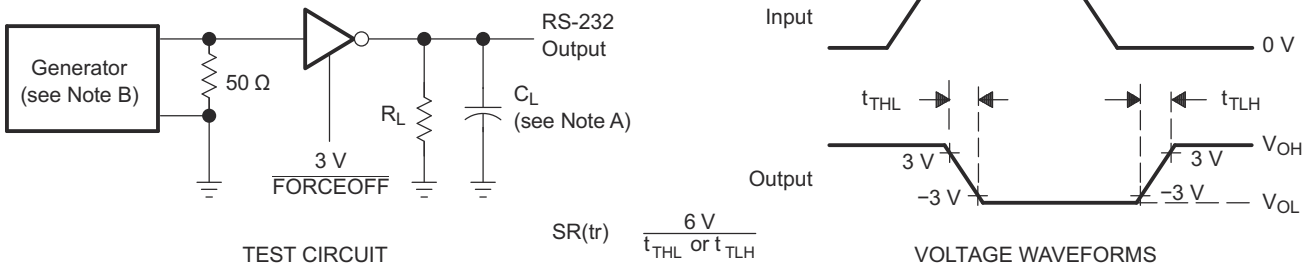
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 9-1) (2)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER SECTION							
	Maximum data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ See Figure 1	250	500		kbit/s
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See Figure 2		100		ns
SR(tr)	Slew rate, transition region (see Figure 1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ, PRR = 250 kbit/s	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	
RECEIVER SECTION							
t_{PLH}	Propagation delay time, low-to high-level output	C_L = 150 pF, See Figure 7-2			150		ns
t_{PHL}	Propagation delay time, high-to low-level output				150		ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 7-3			200		ns
t_{dis}	Output disable time				200		ns
$t_{sk(p)}$	Pulse skew(3)	See Figure 7-2			50		ns
AUTO-POWERDOWN SECTION							
t_{valid}	Propagation delay time, low-to high-level output	V_{CC} = 5 V			1		µs
$t_{invalid}$	Propagation delay time, high-to low-level output	V_{CC} = 5 V			30		µs
t_{en}	Supply enable time	V_{CC} = 5 V			100		µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V + 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

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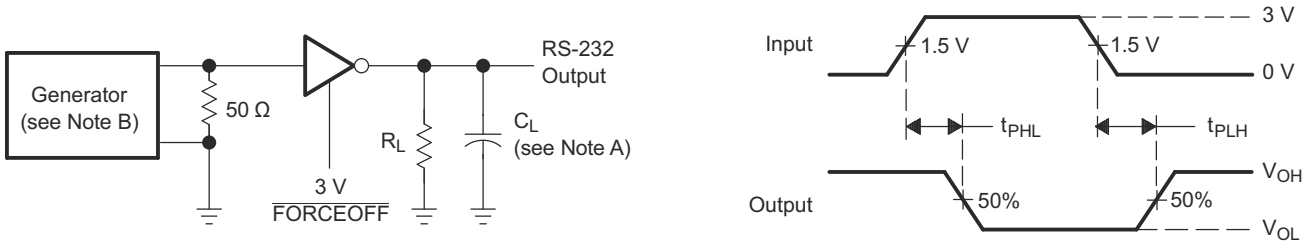
7 Parameter Measurement Information



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A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

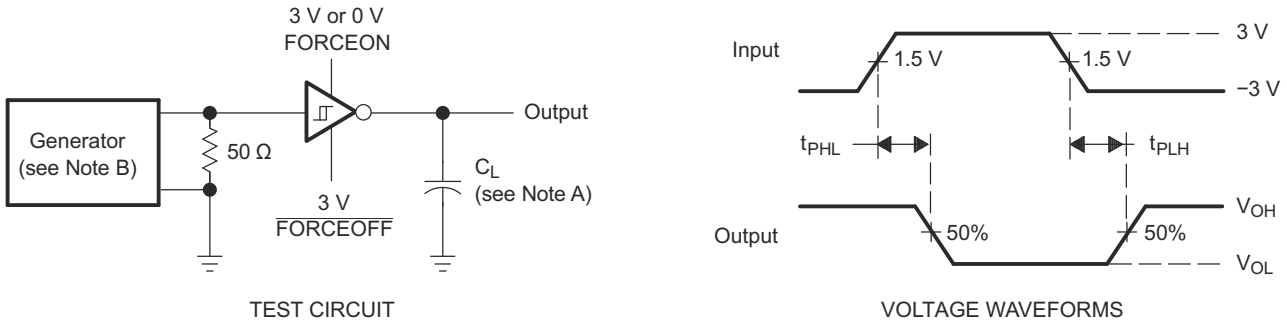
Figure 7-1. Driver Slew Rate



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A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 7-2. Driver Pulse Skew

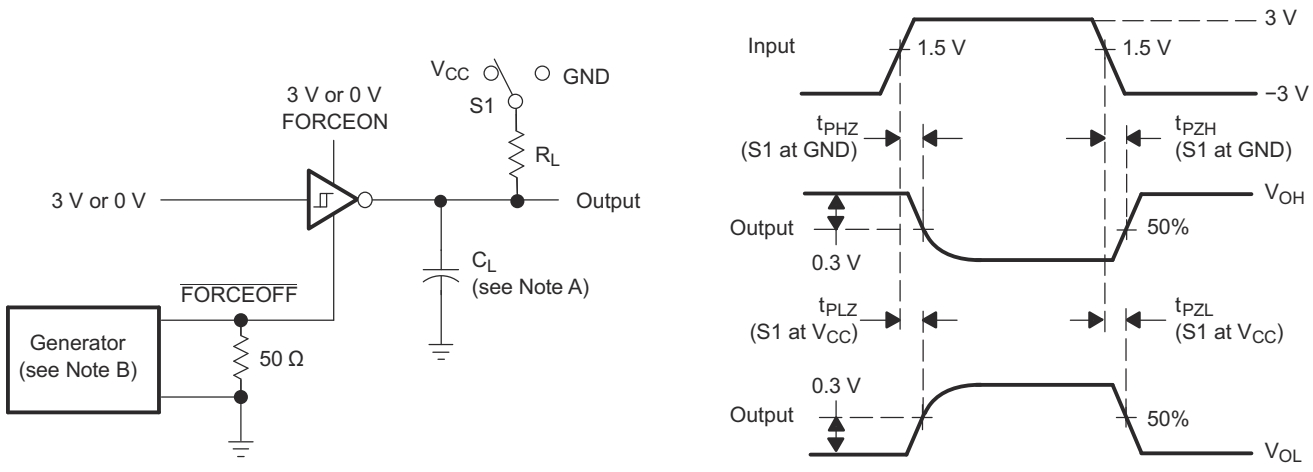


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A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 7-3. Receiver Propagation Delay Times

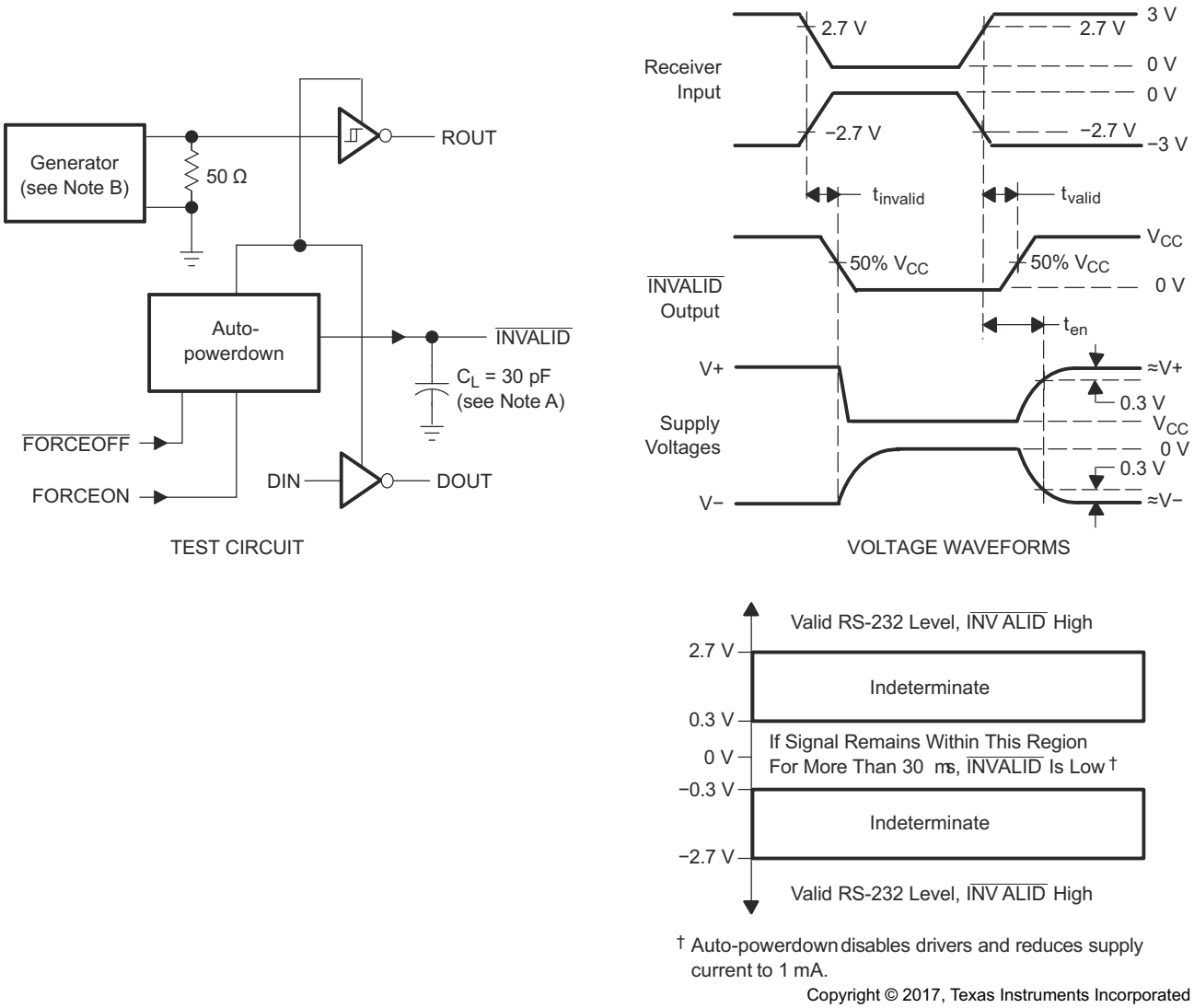
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A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 7-4. Receiver Enable And Disable Times



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A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 7-5. $\overline{\text{INVALID}}$ Propagation Delay Times And Supply Enabling Time

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8 Detailed Description

8.1 Overview

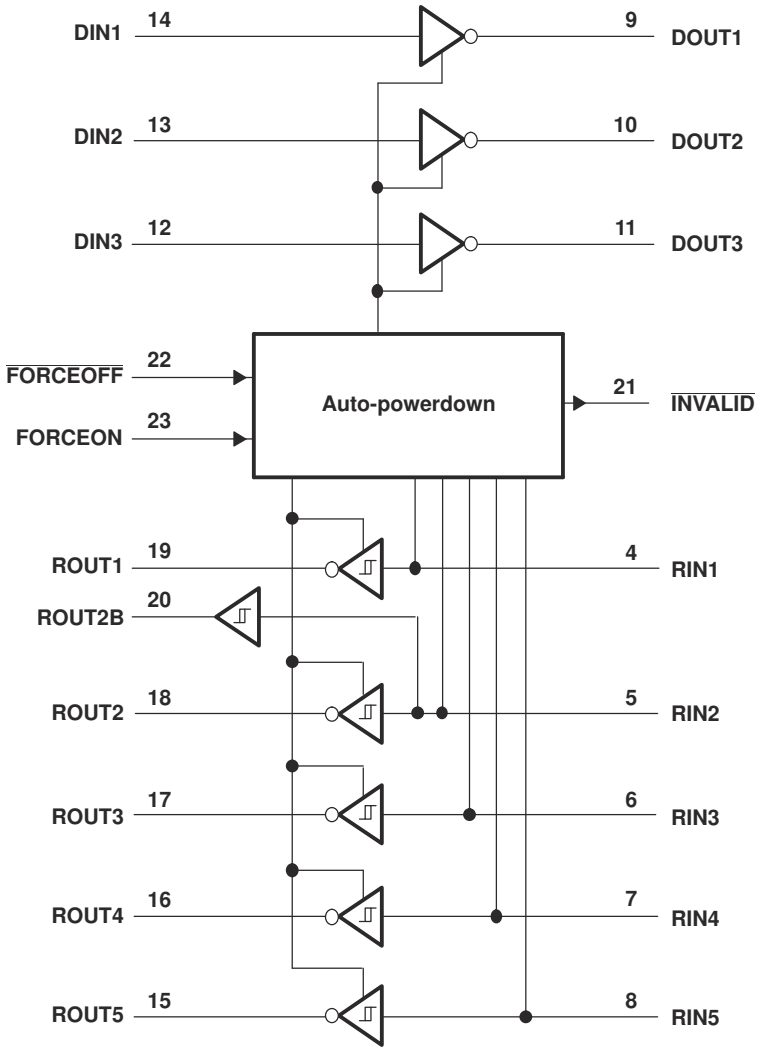
Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 µA.

Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs. Refer to Figure 7-5 for receiver input levels.

The TRS3243E is characterized for operation from 0°C to 70°C. The TRS3243EI is characterized for operation from –40°C to +85°C.

8.2 Functional Block Diagram



Logic Diagram (Positive Logic)

8.3 Device Functional Modes

Table 8-1 through Table 8-3 show the device functional modes.

Table 8-1. Each Driver

INPUTS(1)				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
X	L	H	No	Z	Powered off by auto-powerdown feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 8-2. Each Receiver

INPUTS(1)			OUTPUT	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation with auto-powerdown disabled/enabled
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Table 8-3. ROUT2B And Outputs $\overline{\text{INVALID}}$

INPUTS(1)				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
Yes	L	X	X	H	L	Always active
Yes	H	X	X	H	H	
Yes	Open	X	X	H	L	
No	Open	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

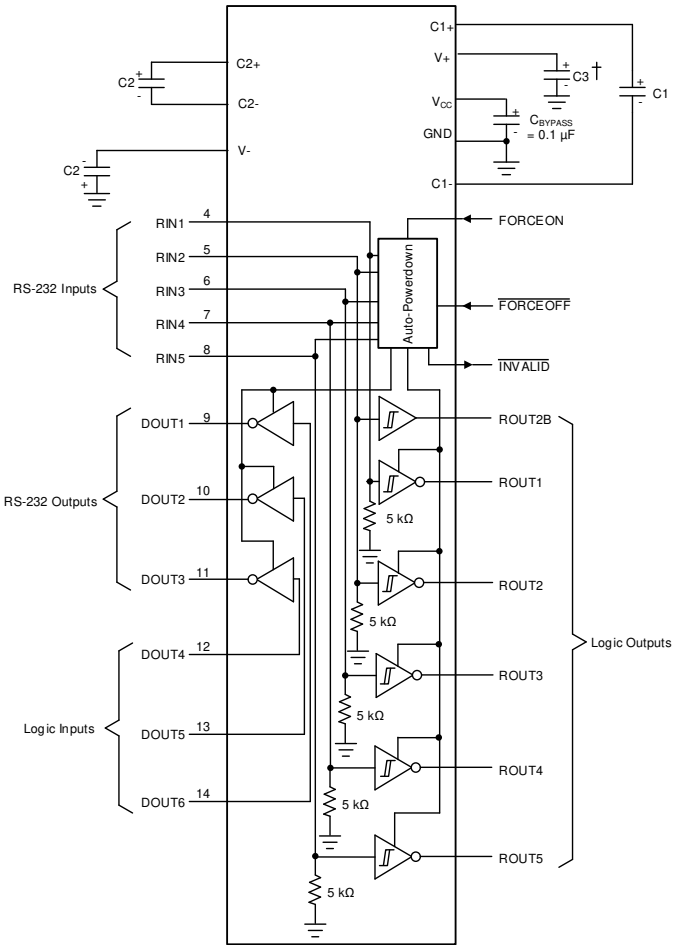
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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Application



A. C3 can be connected to V_{CC} or GND.
B. Resistor values shown are nominal.
C. Nonpolarized ceramic capacitors are acceptable. If using polarized tantalum or electrolytic capacitors, connect them as shown.

Figure 9-1. Typical Operating Circuit and Capacitor Values

Table 9-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

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9.1.1 Detailed Design Procedure

9.1.1.1 ESD Protection

TI TRS3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV in all states: normal operation, shutdown, and powered down. The TRS3243E devices are designed to continue functioning properly after an ESD occurrence without any latchup.

The TRS3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

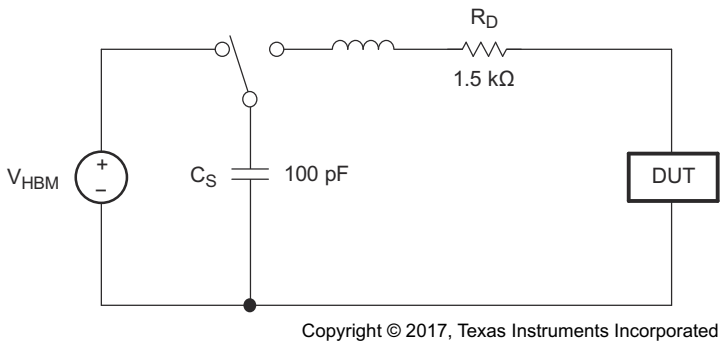
- ±15-kV Human-Body Model (HBM)
- ±15-kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- ±8-kV IEC61000-4-2, Contact Discharge

9.1.1.2 ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

9.1.1.3 Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 9-2, while Figure 9-3 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-kΩ resistor.



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Figure 9-2. HBM ESD Test Circuit

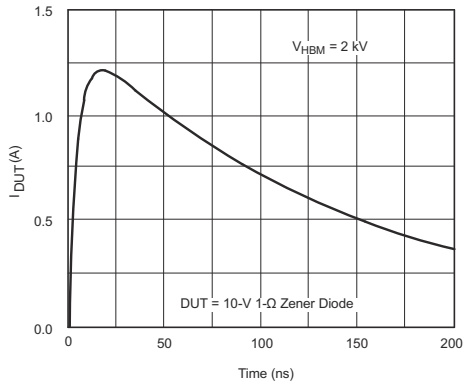


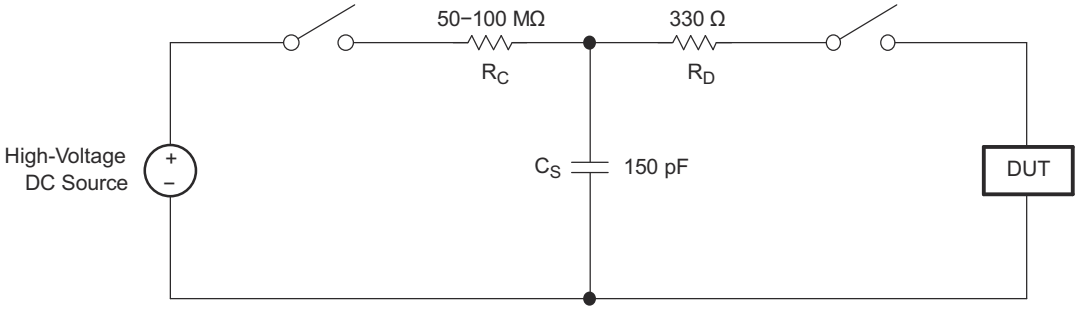
Figure 9-3. Typical HBM Current Waveform

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9.1.1.4 IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The TRS3243E is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

Figure 9-4 shows the IEC61000-4-2 model, and Figure 9-5 shows the current waveform for the corresponding ±8-kV contact-discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding ±15-kV (Level 4) air-gap discharge test involves approaching the DUT with an already energized probe.



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Figure 9-4. Simplified IEC61000-4-2 ESD Test Circuit

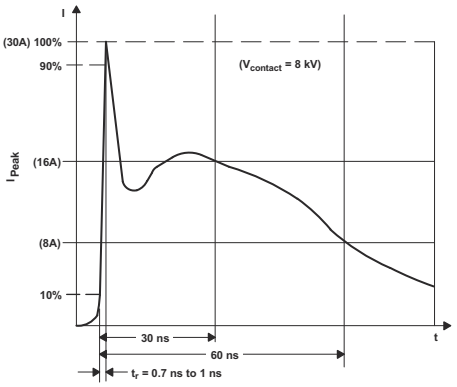


Figure 9-5. Typical Current Waveform Of IEC61000-4-2 ESD Generator

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

IBM™ and PC/AT™ are trademarks of International Business Machines Corporation.
TI E2E™ is a trademark of Texas Instruments.
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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS3243ECDB	Obsolete	Production	SSOP (DB) | 28	-	-	Call TI	Call TI	0 to 70	TRS3243EC
TRS3243ECDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC
TRS3243ECDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC
TRS3243ECDW	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	0 to 70	TRS3243EC
TRS3243ECDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC
TRS3243ECDWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC
TRS3243ECPW	Obsolete	Production	TSSOP (PW) | 28	-	-	Call TI	Call TI	0 to 70	RS43EC
TRS3243ECPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC
TRS3243ECPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC
TRS3243ECRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	RS43EC
TRS3243ECRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	RS43EC
TRS3243EIDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDBRG4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDBRG4.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDW	Obsolete	Production	SOIC (DW) | 28	-	-	Call TI	Call TI	-40 to 85	TRS3243EI
TRS3243EIDWR	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIDWR.A	Active	Production	SOIC (DW) | 28	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI
TRS3243EIPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI
TRS3243EIPWR.A	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI
TRS3243EIRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI
TRS3243EIRHBR.A	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI
TRS3243EIRHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

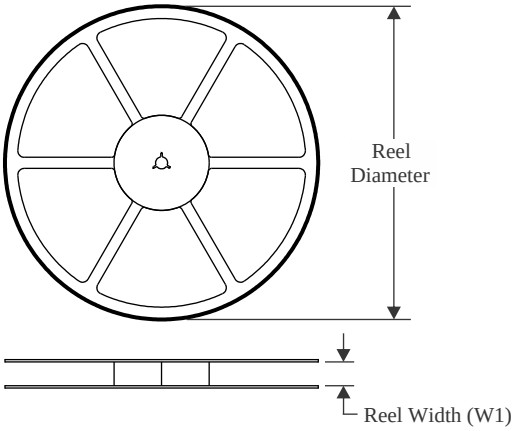
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

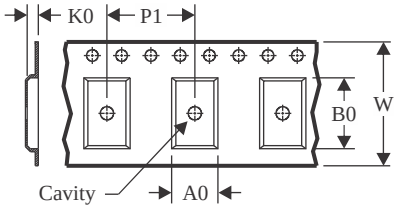
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

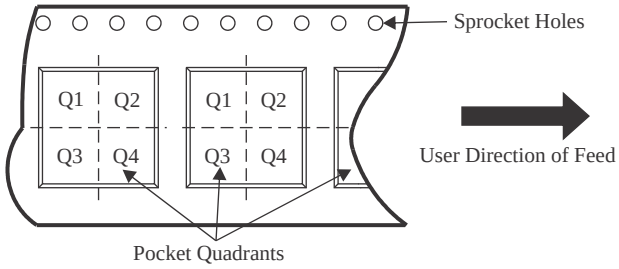


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

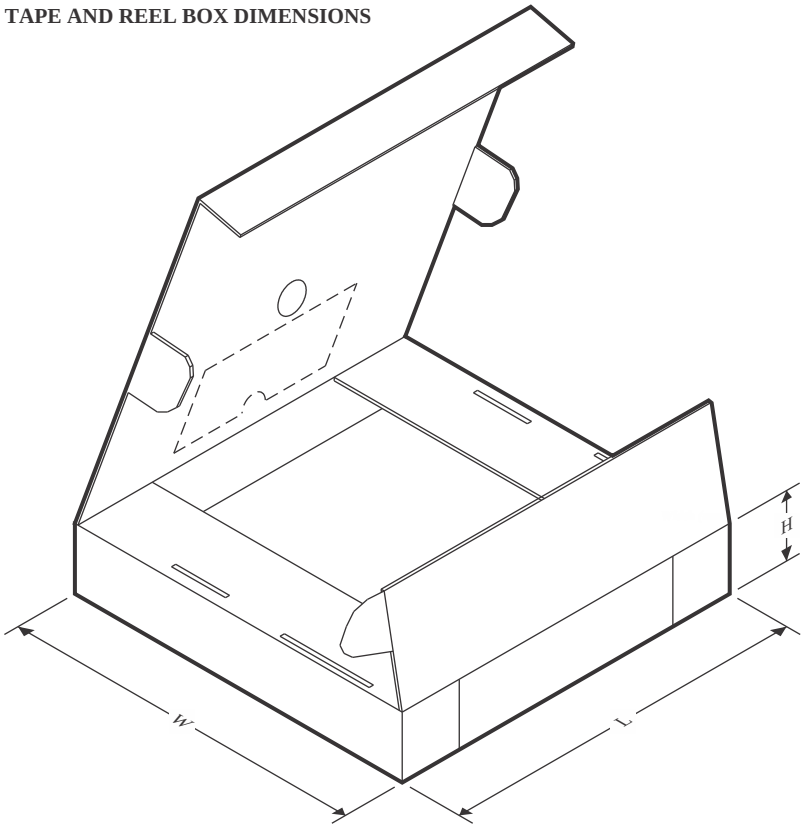
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3243ECDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TRS3243ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243ECPWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TRS3243ECRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TRS3243EIDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TRS3243EIDBRG4	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TRS3243EIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TRS3243EIRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

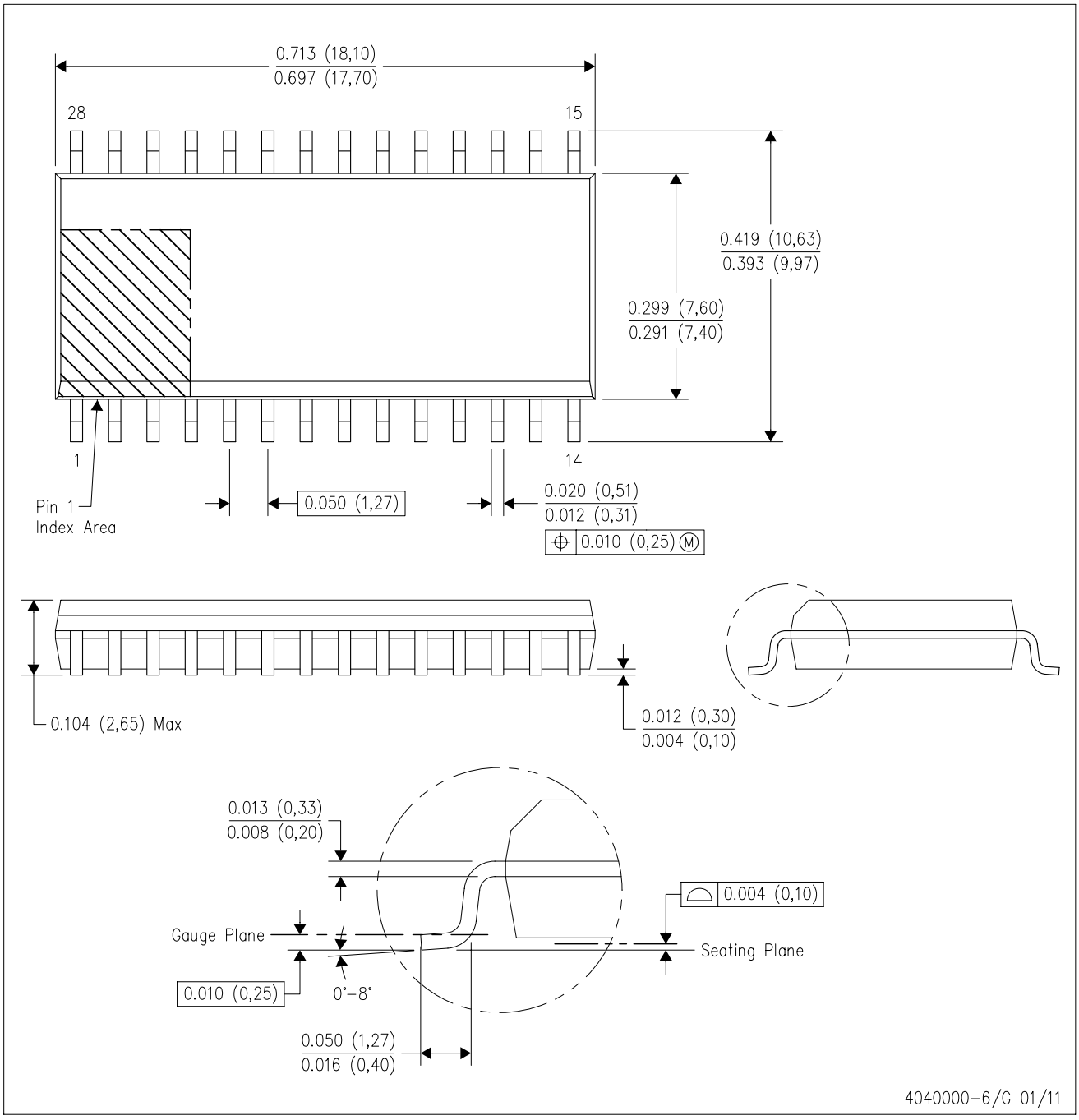
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

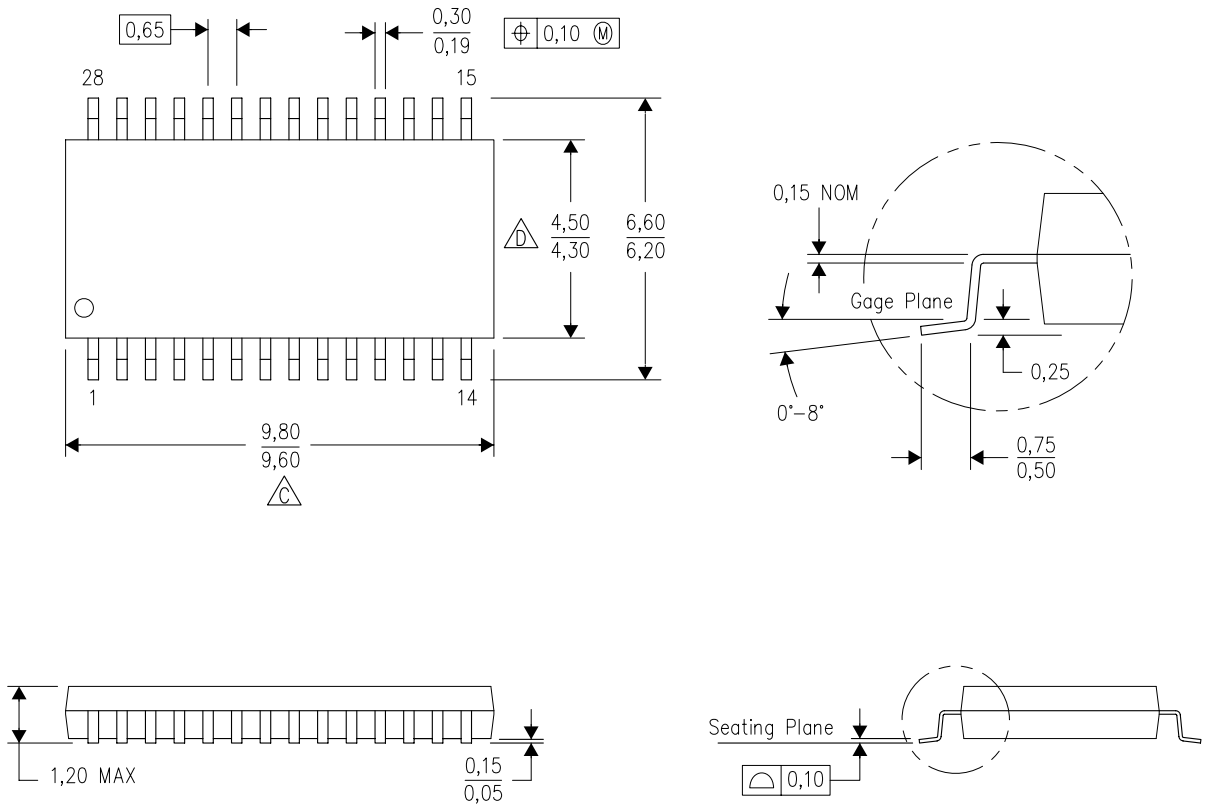
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3243ECDBR	SSOP	DB	28	2000	353.0	353.0	32.0
TRS3243ECDWR	SOIC	DW	28	1000	350.0	350.0	66.0
TRS3243ECPWR	TSSOP	PW	28	2000	353.0	353.0	32.0
TRS3243ECRHBR	VQFN	RHB	32	3000	360.0	360.0	36.0
TRS3243EIDBR	SSOP	DB	28	2000	353.0	353.0	32.0
TRS3243EIDBRG4	SSOP	DB	28	2000	353.0	353.0	32.0
TRS3243EIDWR	SOIC	DW	28	1000	350.0	350.0	66.0
TRS3243EIPWR	TSSOP	PW	28	2000	353.0	353.0	32.0
TRS3243EIRHBR	VQFN	RHB	32	3000	360.0	360.0	36.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

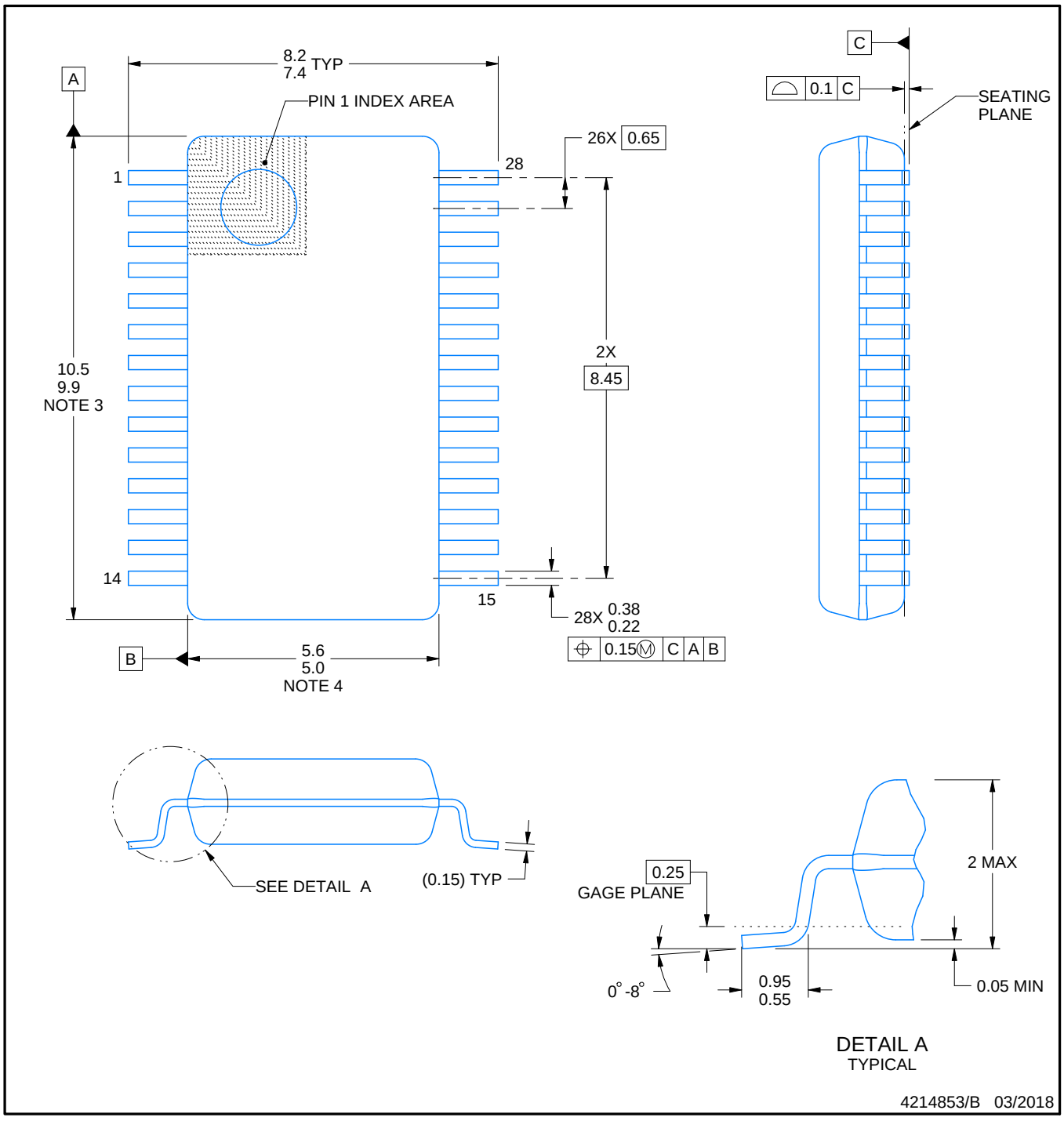
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PACKAGE OUTLINE

DB0028A

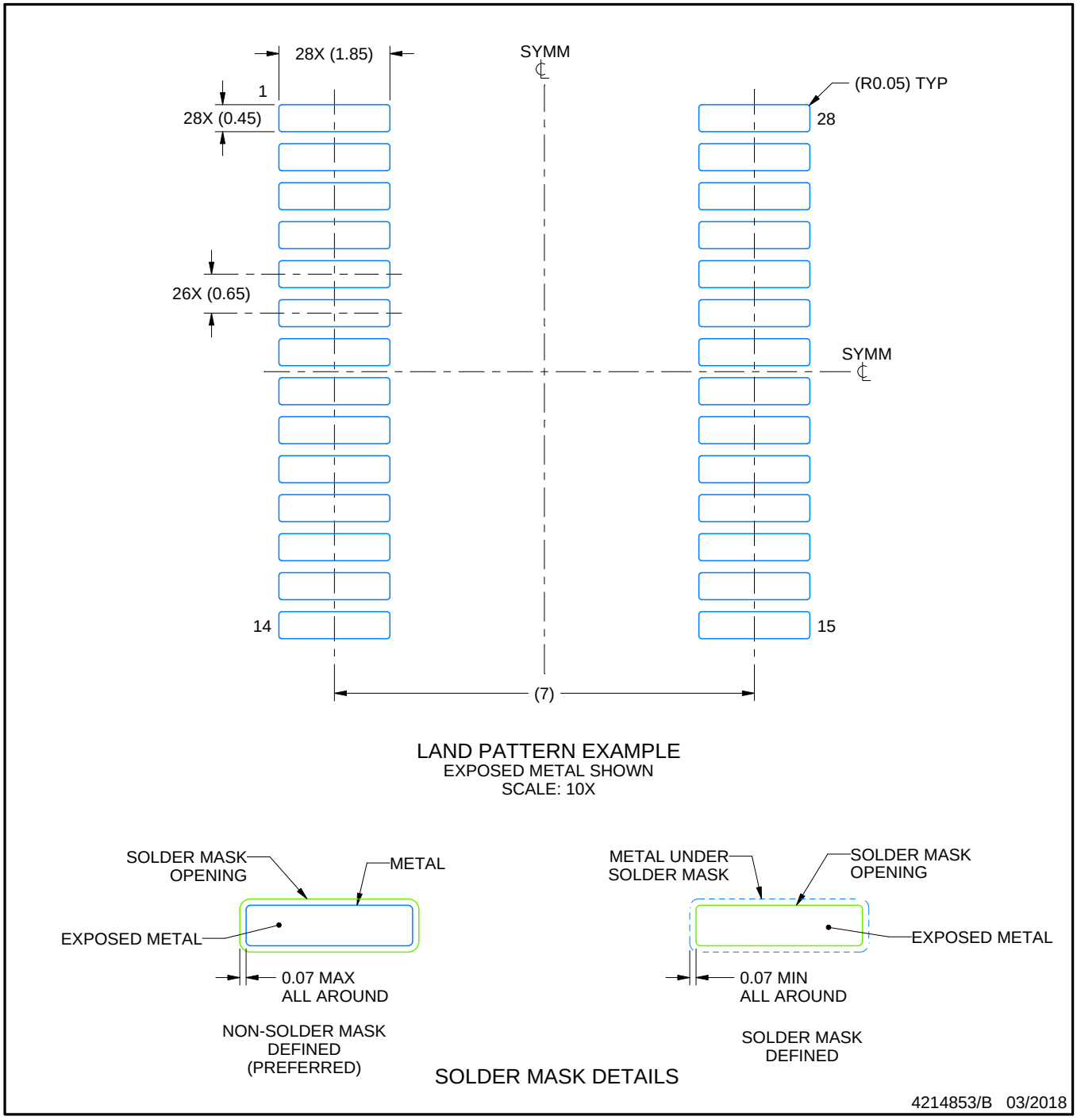
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



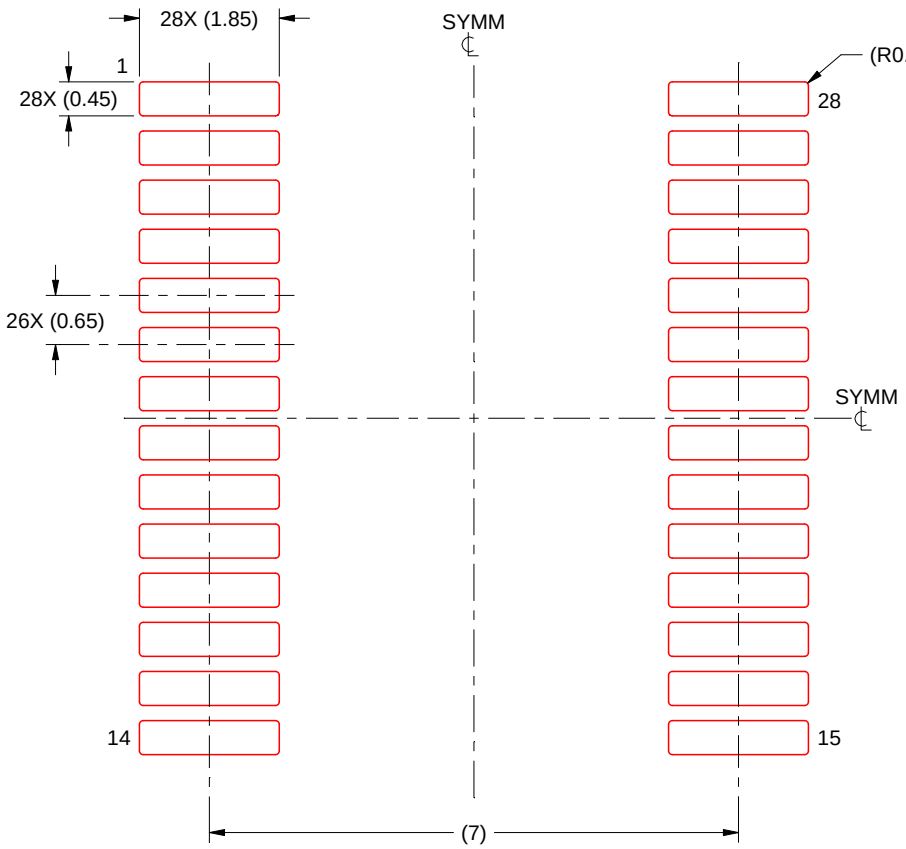
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

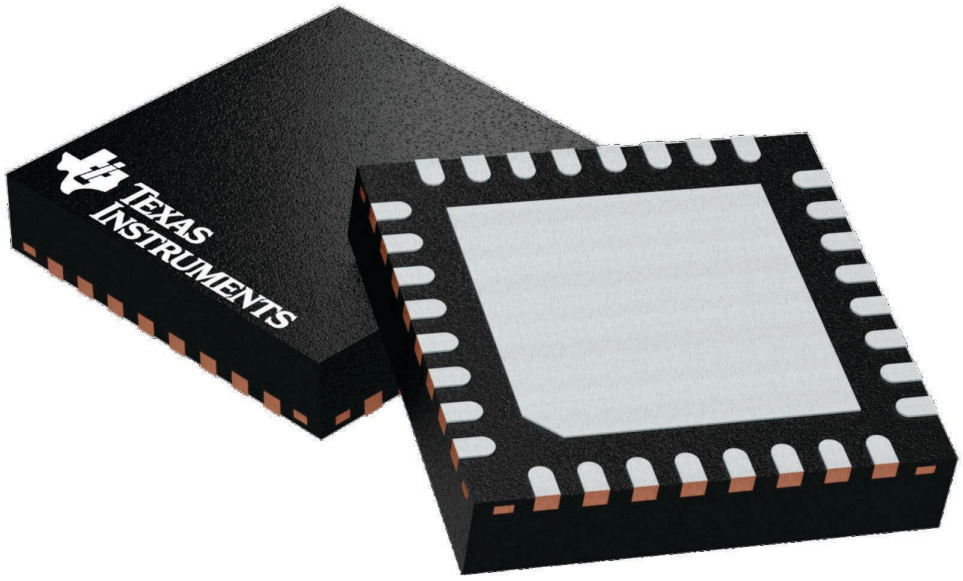
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

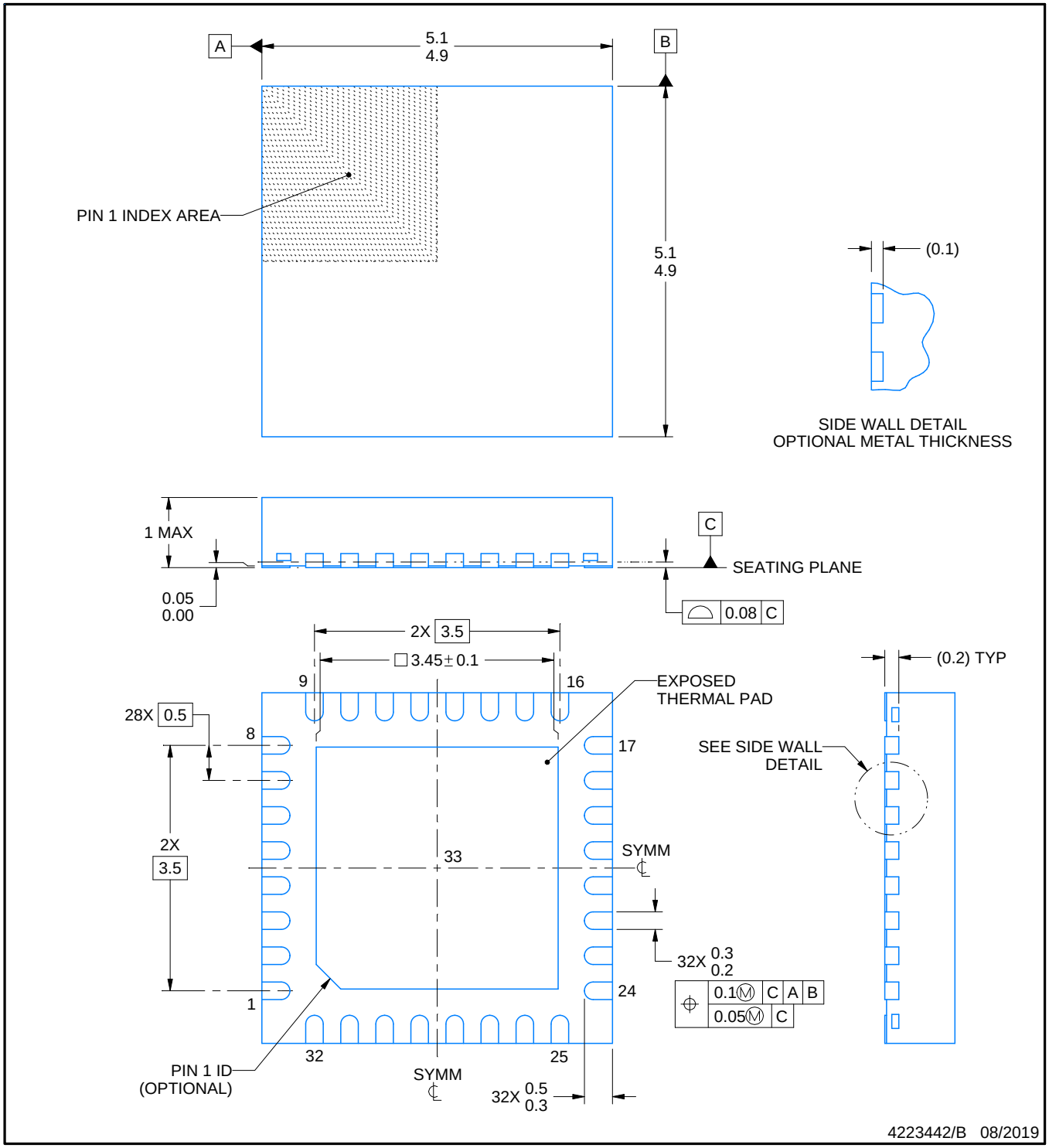
4224745/A

RHB0032E

PACKAGE OUTLINE

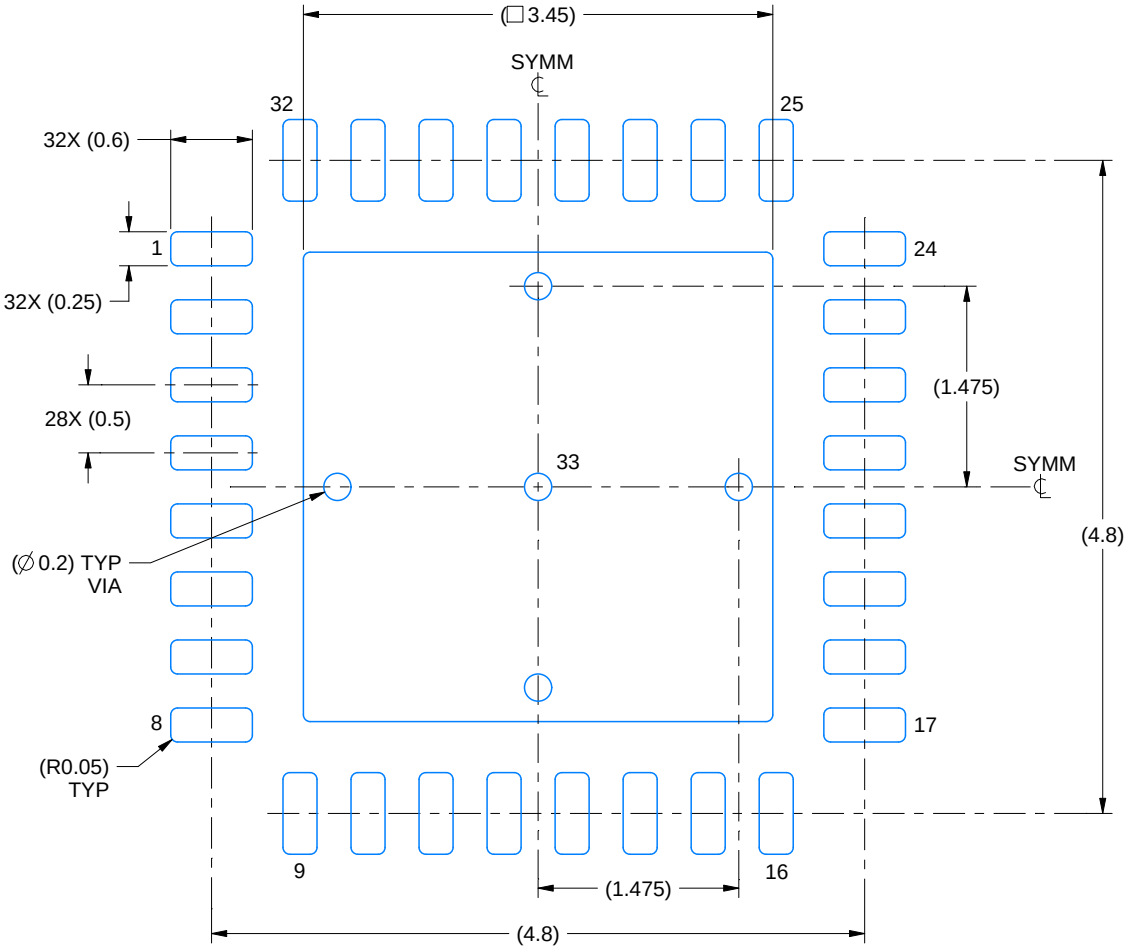
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

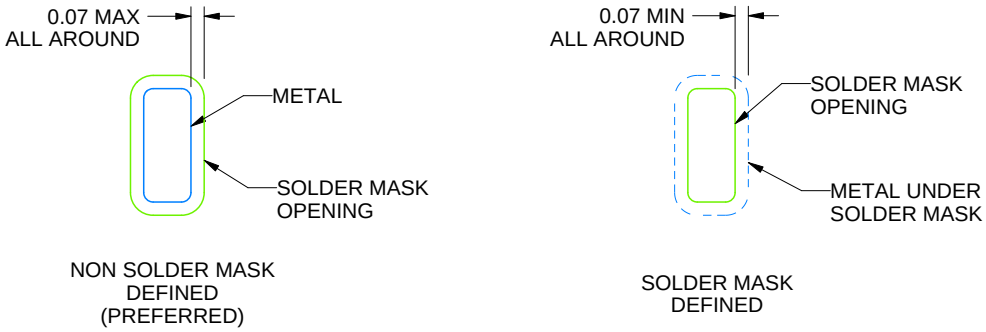


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

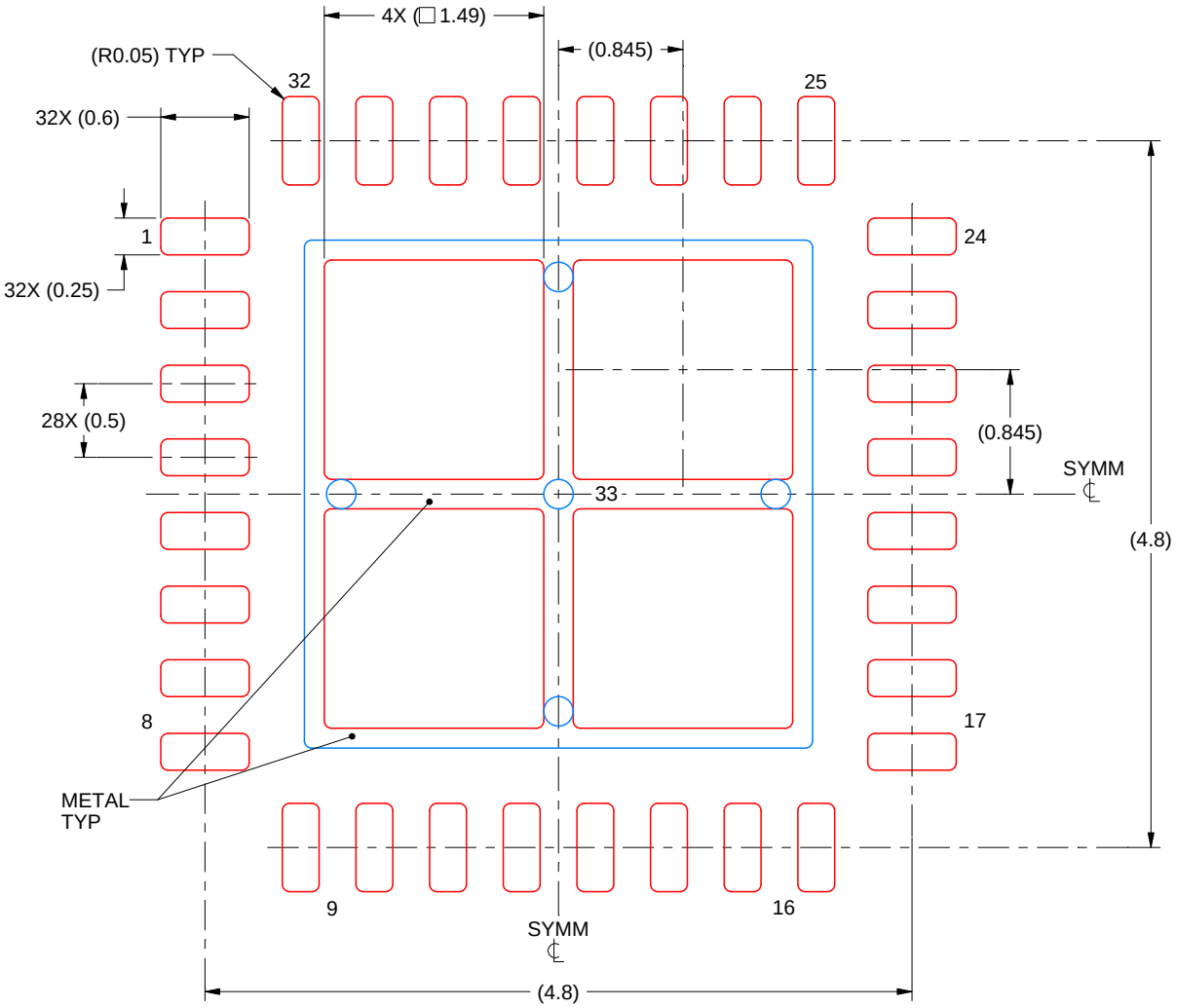


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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