TS3USB31 1:1 SPST High-Speed USB 2.0 (480-Mbps) Bus Isolation Switch With Single Enable

1 Features

- V_{CC} Operation at 3 V and 4.3 V
- 1.8-V Compatible Control-Pin Inputs
- I_{OFF} Supports Partial Power-Down Mode Operation
- r_{on} = 10 Ω Maximum
- Δr_{on} <0.35 Ω Typical
- $C_{io(ON)}$ = 6 pF Typical
- Low Power Consumption (1 µA Maximum)
- ESD Performance Tested Per JESD 22
  - 6000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
  - 250-V Machine Model (A115-A)
- Wide –3-dB Bandwidth = 1220 MHz Typical
- Packaged in 8-Pin TQFN (1.5 mm × 1.5 mm)

2 Applications

Bus Isolation for USB 1.0, 1.1, and 2.0

3 Description

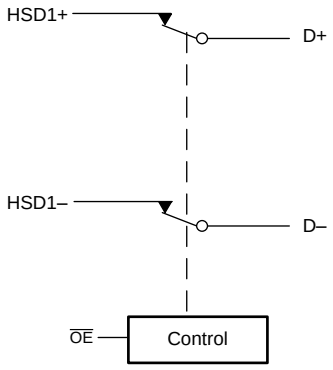
The TS3USB31 is a 1:1 SPST high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals. This device comes in a small UQFN package for use in a handset or consumer applications, such as cell phones, digital cameras, and notebooks with hubs. The wide bandwidth (750 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3USB31	UQFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

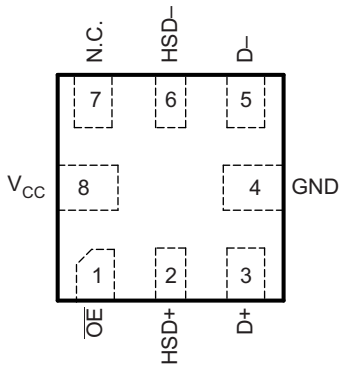
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2008) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

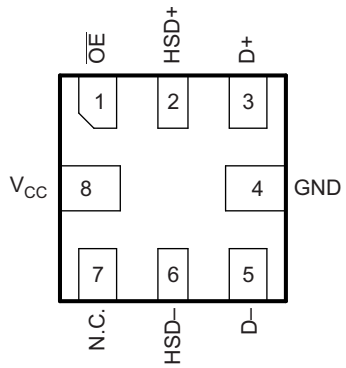
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5 Pin Configuration and Functions

RSE Package
8-Pin UQFN
Top View



RSE Package
8-Pin UQFN
Bottom View



N.C. – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Bus-switch enable, To isolate the D+/D- pins from the HSD+/HSD- pins set $\overline{OE}$ pin to valid high logic level, To connect D+/D- pins to HSD+/HSD- pins set $\overline{OE}$ pin to valid low logic level
D+	3	I/O	Data ports
D–	5	I/O	Data ports
HSD+	2	I/O	Data ports
HSD–	6	I/O	Data ports
N.C.	7	—	No connect, This pin should be left floating or connect to ground
GND	4	—	Ground
V_{CC}	8	I/O	Supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_{IN}	Control input voltage(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage (2)(3)(4)	HSD+, HSD–	–0.5	V_{CC} + 0.3	V
		D+, D– when V_{CC} > 0	–0.5	V_{CC} + 0.3	
		D+, D– when V_{CC} = 0		5.25	
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	4.3	V
V_{IH}	High-level control input voltage	V_{CC} = 3 V to 3.6 V	1.3		V
		V_{CC} = 4.3 V	1.7		
V_{IL}	Low-level control input voltage	V_{CC} = 3 V to 3.6 V		0.5	V
		V_{CC} = 4.3 V		0.7	
$V_{I/O}$	Data input/output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.4 Thermal Information

THERMAL METRIC[1]		TS3USB31 RSE (UQFN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IK}	Input Clamp Voltage	V_{CC} = 3 V, I_I = –18 mA			–1.2	V
I_{IN}	Control inputs	V_{CC} = 4.3 V or 0V, V_{IN} = 0 to 4.3 V,			±1	µA
I_{OZ}[3]		V_{CC} = 4.3 V, V_O = 0 to 3.6 V, V_I = 0, Switch OFF			±1	µA
I_{OFF}	D+ and D–	V_{CC} = 0 V, V_O = 0 V to 4.3 V, V_I = 0, V_{IN} = V_{CC} or GND			±2	µA
I_{CC}		V_{CC} = 4.3 V, $I_{I/O}$ = 0, Switch ON or OFF			1	µA
ΔI_{CC}[4]	Control inputs	V_{CC} = 4.3 V, V_{IN} = 2.6 V			10	µA
C_{in}	Control inputs	V_{CC} = 0 V, V_{IN} = V_{CC} or GND		1		pF
$C_{io(OFF)}$	Off-state Input/Output Capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, Switch OFF		2		pF
$C_{io(ON)}$	On-state Input/Output Capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, Switch ON		6		pF
r_{on}[5]	On-State Resistance	V_{CC} = 3 V, V_I = 0.4 V, I_O = –8 mA		6	10	Ω
Δr_{on}	Channel Match	V_{CC} = 3 V, V_I = 0.4 V, I_O = –8 mA		0.35		Ω
$r_{on(flat)}$	On-State Resistance Flatness	V_{CC} = 3 V, V_I = 0 V or 1 V, I_O = –8 mA		2		Ω

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Dynamic Electrical Characteristics

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP[1]	UNIT
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 240 MHz, See Figure 6	–53	dB
O_{IRR}	OFF isolation	R_L = 50 Ω, f = 240 MHz, See Figure 5	–30	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω, C_L = 5 pF, See Figure 7	1220	MHz

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

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6.7 Switching Characteristics

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2)(3)	R_L = 50 Ω, C_L = 5 pF, See Figure 8		0.25		ns
t_{ON}	Line enable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			30	ns
t_{OFF}	Line disable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			25	ns
$t_{SK(O)}$	Output skew between ports(2)	R_L = 50 Ω, C_L = 5 pF, See Figure 9		50		ps
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)	R_L = 50 Ω, C_L = 5 pF, See Figure 9		20		ps
t_J	Total jitter(2)	R_L = 50 Ω, C_L = 5 pF, t_R = t_F = 500 ps at 480 Mbps (PRBS = 2^{15} – 1)		200		ps

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

6.8 Typical Characteristics

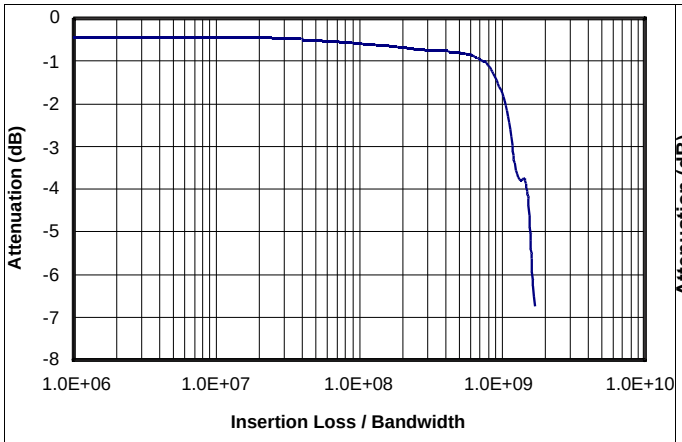


Figure 1. Insertion Loss / Bandwidth

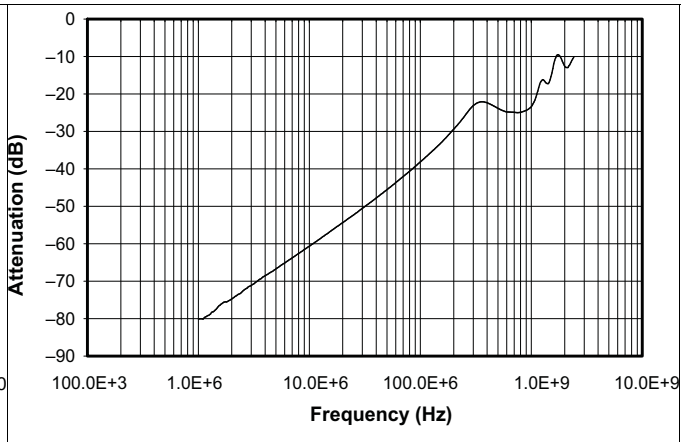


Figure 2. OFF Isolation

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Typical Characteristics (continued)

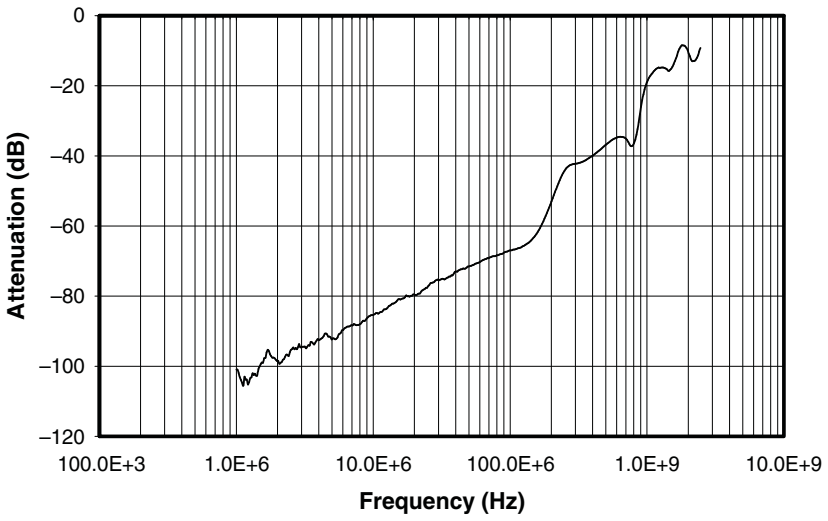
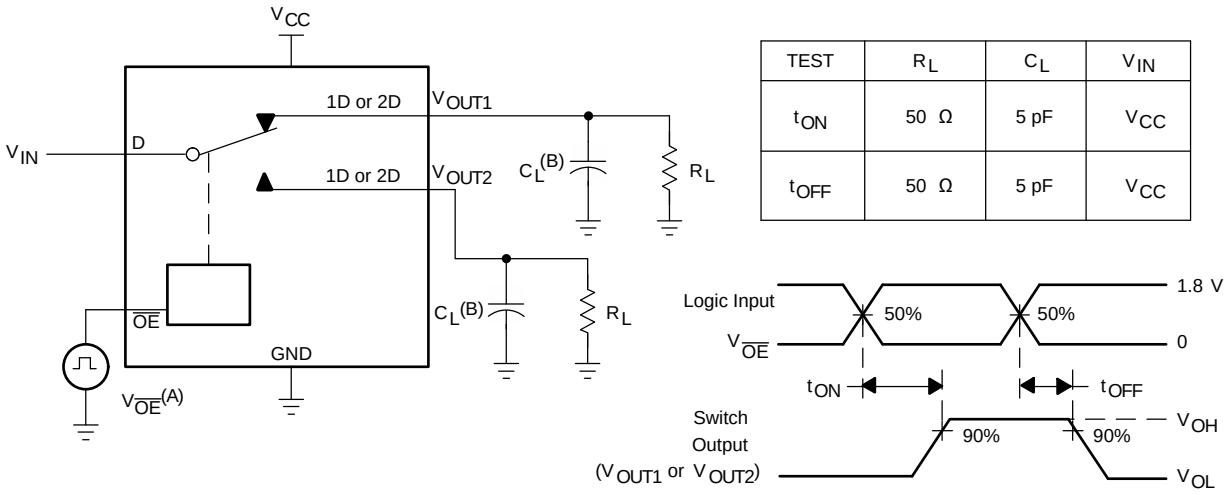


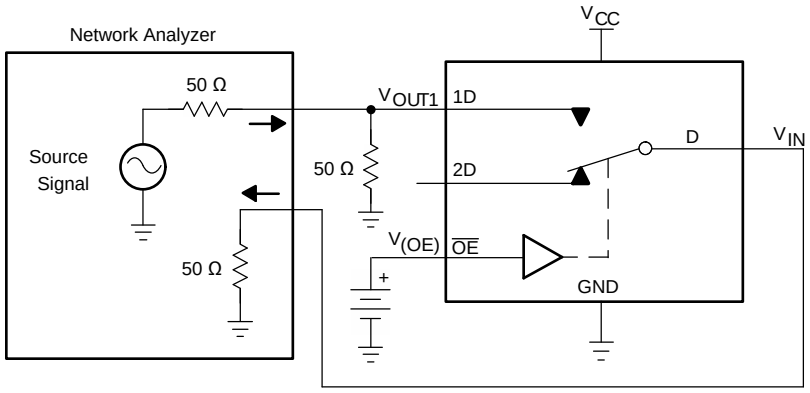
Figure 3. Crosstalk

7 Parameter Measurement Information



TEST	R_L	C_L	V_{IN}
t_{ON}	50 Ω	5 pF	V_{CC}
t_{OFF}	50 Ω	5 pF	V_{CC}

Figure 4. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



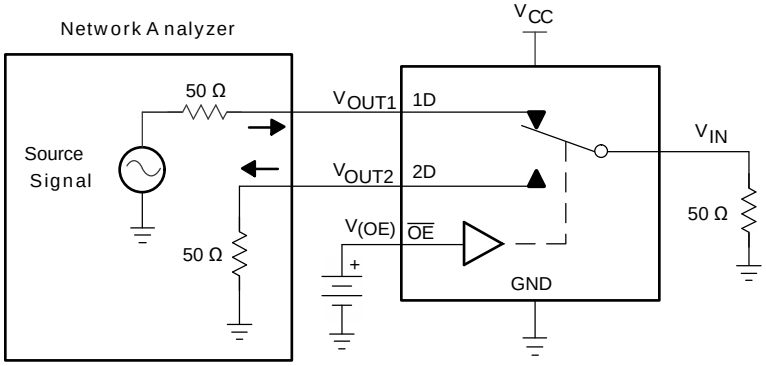
Channel OFF: 1D to D
$V_{(OE)} = V_{(CC)}$

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 5. OFF Isolation (O_{IRR})



Channel ON: 1D to D
Channel OFF: 2D to D
$V_{(OE)} = V_{(CC)}$

Network Analyzer Setup

Source Power= 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 6. Crosstalk (X_{TALK})

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Parameter Measurement Information (continued)

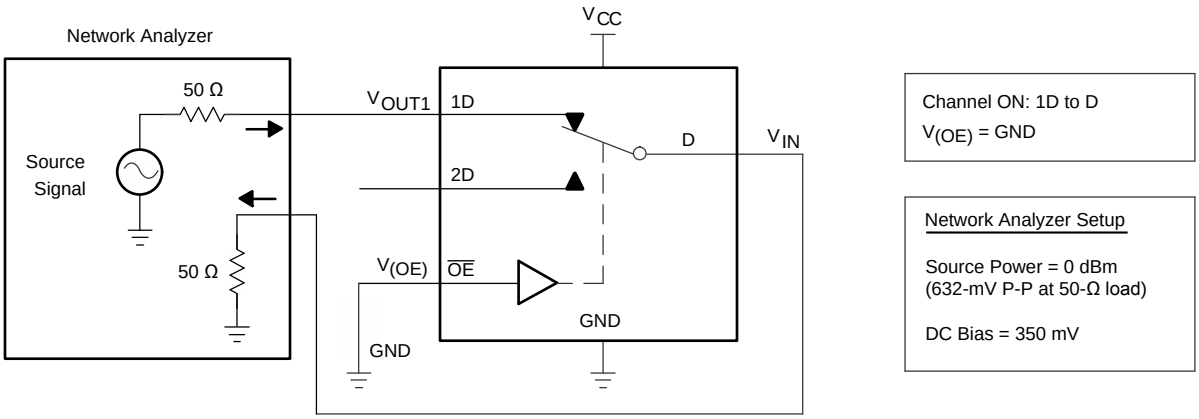


Figure 7. Bandwidth (BW)

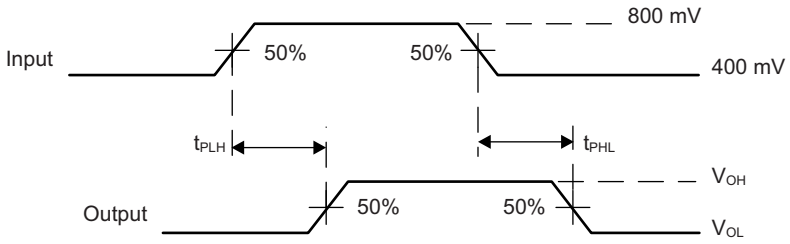


Figure 8. Propagation Delay

Parameter Measurement Information (continued)

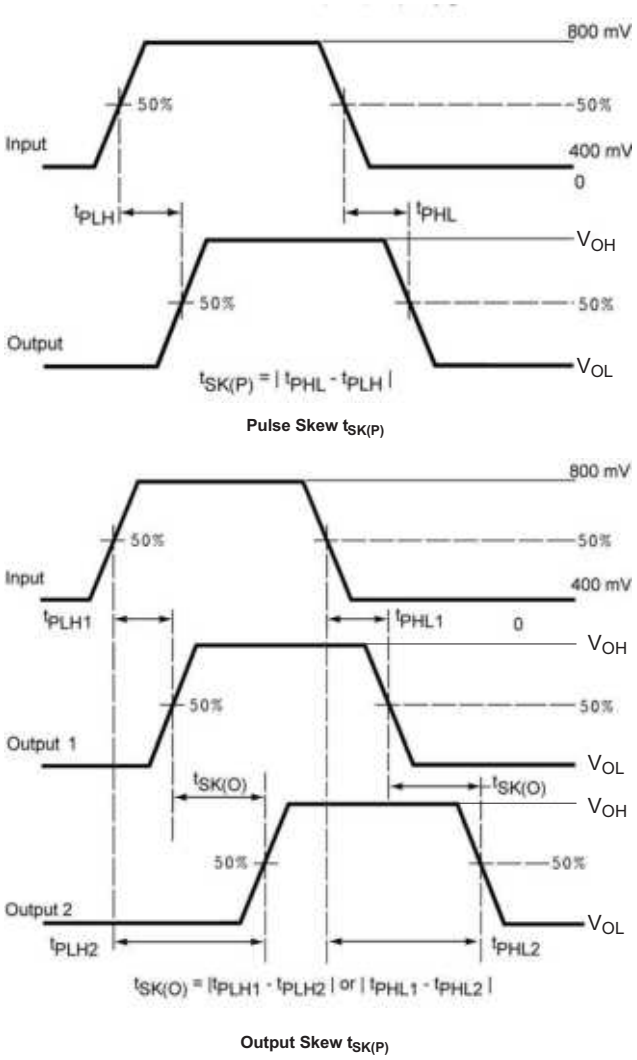


Figure 9. Skew Test

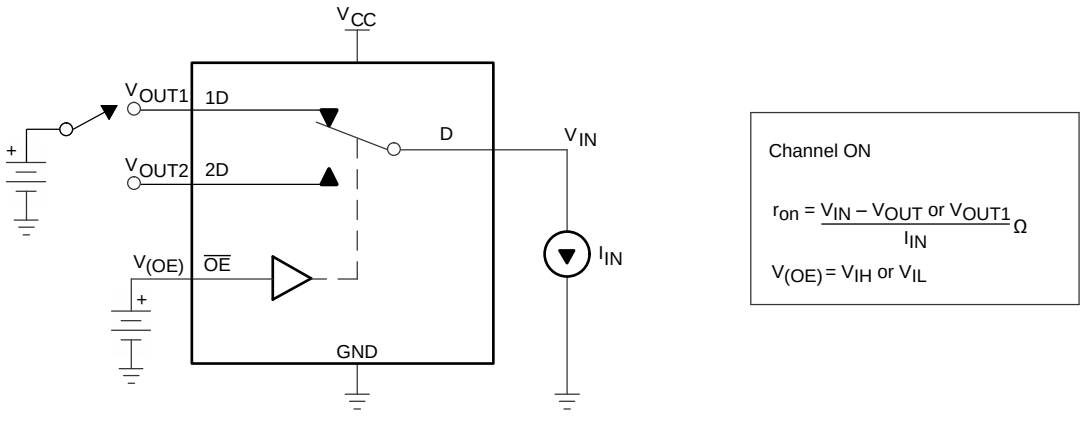


Figure 10. ON-State Resistance (r_{on})

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Parameter Measurement Information (continued)

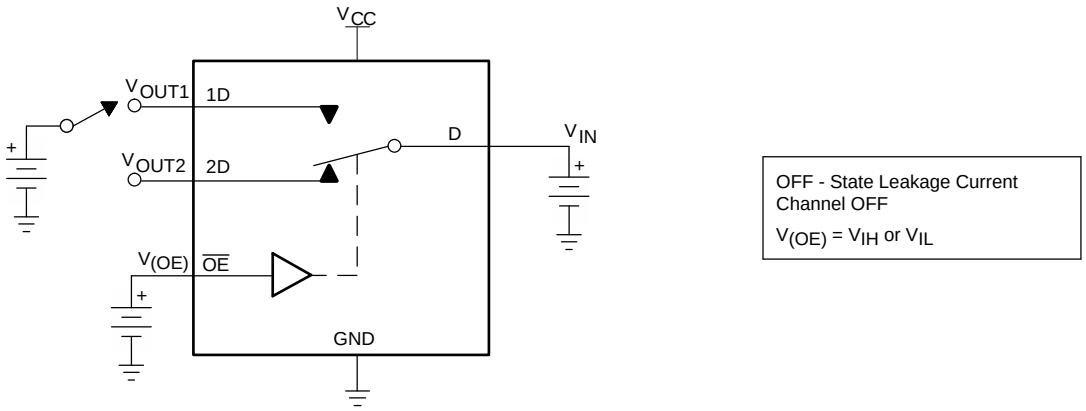


Figure 11. OFF-State Leakage Current

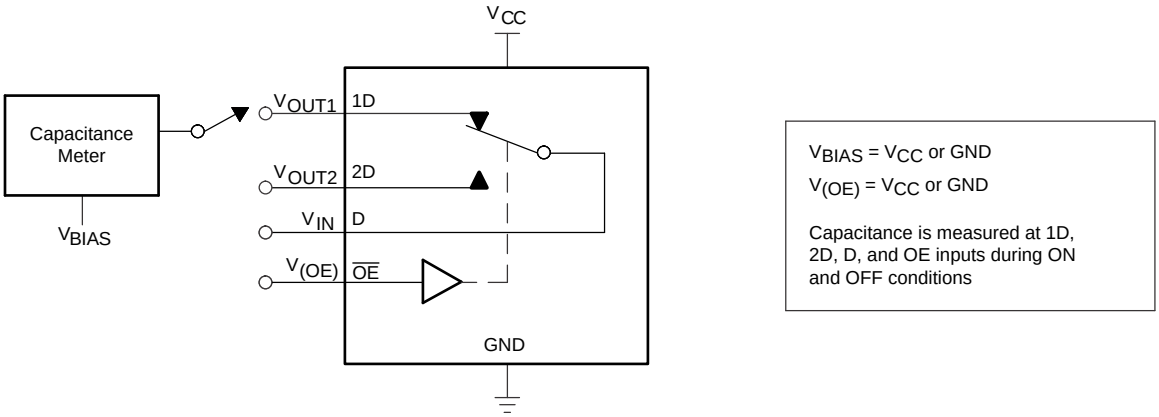


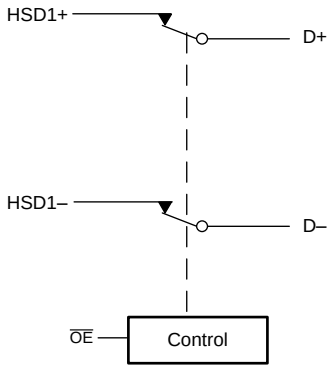
Figure 12. Capacitance

8 Detailed Description

8.1 Overview

The TS3USB31 is a 1:1 SPST high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals. The switch is bidirectional and offers little or no attenuation of the high-speed signals. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 I_{OFF} Supports Partial Power-Down Mode Operation

When V_{CC} = 0 V, the signal path is placed in a high impedance state which isolates the bus. This allows signals to be present on the D+/- and HSD+/- pins before the device is powered up without damaging the device.

8.4 Device Functional Modes

The TS3USB31 device has two modes that are digitally controlled by the OE pin. Setting the OE pin *High* isolates the signal path by a high impedance state.

Table 1. Truth Table

$\overline{OE}$	FUNCTION
H	Disconnect
L	D+, D– = HSD+, HSD–

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3USB31 device is used to isolate a USB bus when it is not in use to prevent two different USB devices from interfering with each other.

9.2 Typical Application

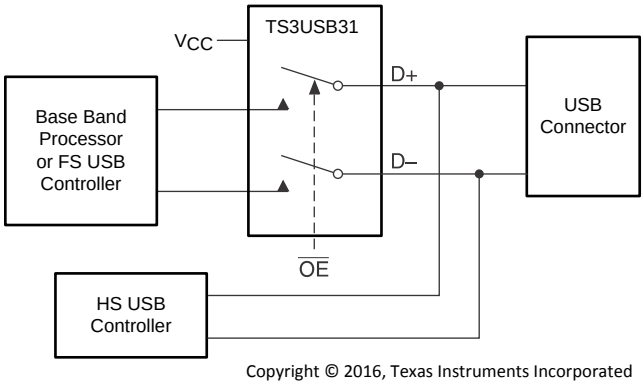


Figure 13. Application Diagram

9.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed. TI recommends that the digital control pin $\overline{OE}$ be pulled up to V_{CC} or down to ground to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure

The TS3USB31 can be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

The N.C pin should be left floating.

Typical Application (continued)

9.2.3 Application Curves

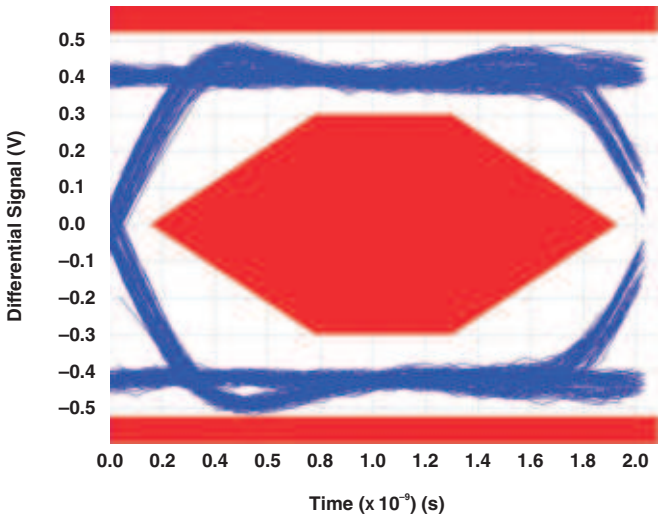


Figure 14. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

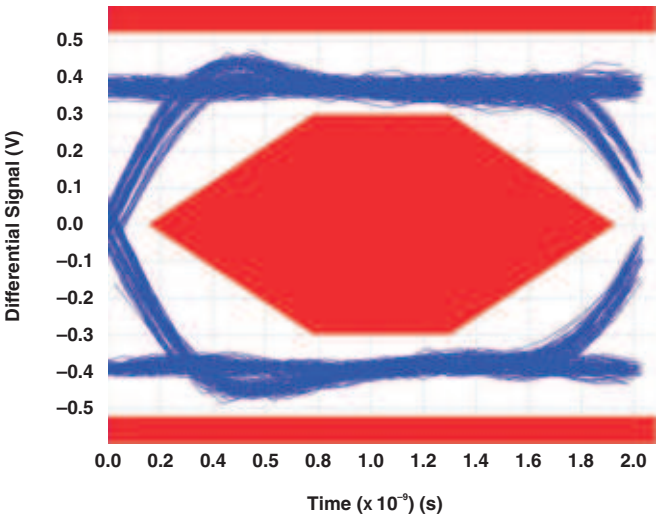


Figure 15. Eye Pattern: 480-Mbps USB Signal With Switch NO Path

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10 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

This device doesn't require any power sequencing with respect to other devices in the system due to its power off isolation feature which allows signals to be present on the D+/- and HSD+/- pins before the device is powered up without damaging the device.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the D+ and D– traces.

The high-speed D+ and D– traces should always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces should run on a single layer, preferably top layer. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082) and *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7).

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11.2 Layout Example

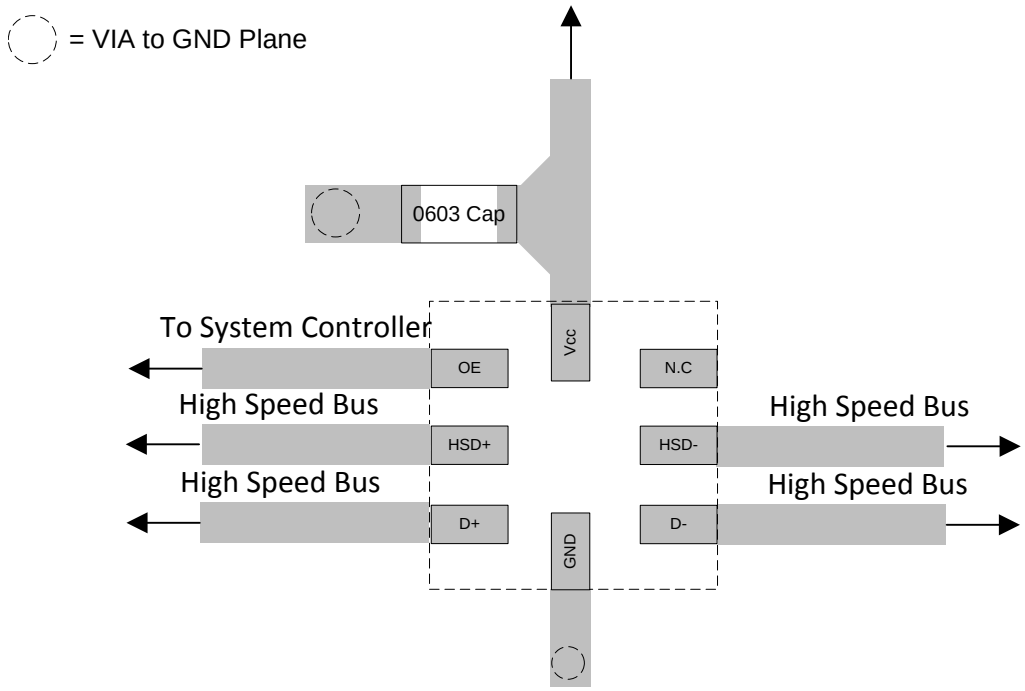


Figure 16. Layout Recommendation

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following

- *High Speed Layout Guidelines* (SCAA082)
- *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3USB31RSER	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	L9
TS3USB31RSER.B	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	L9
TS3USB31RSERG4	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	L9

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

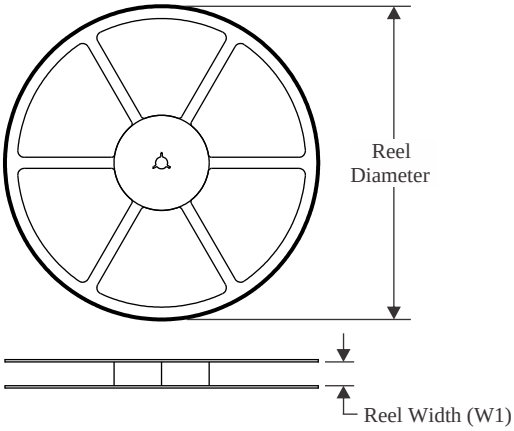
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

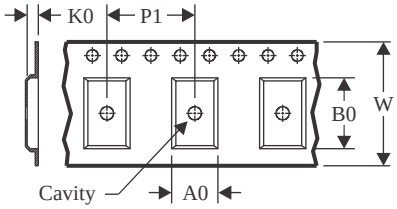
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

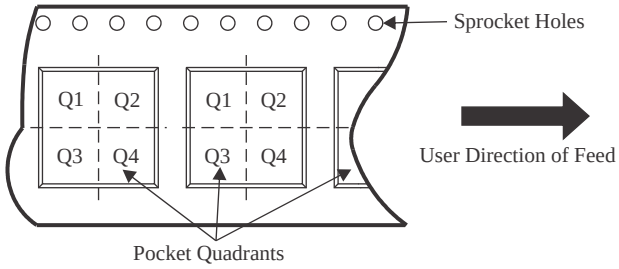


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

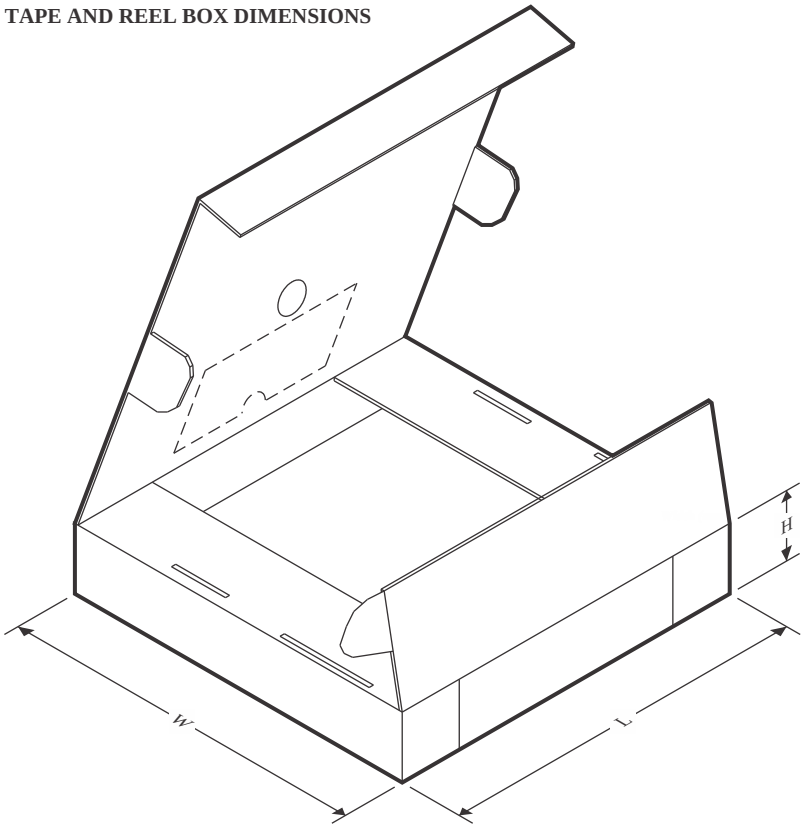
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB31RSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

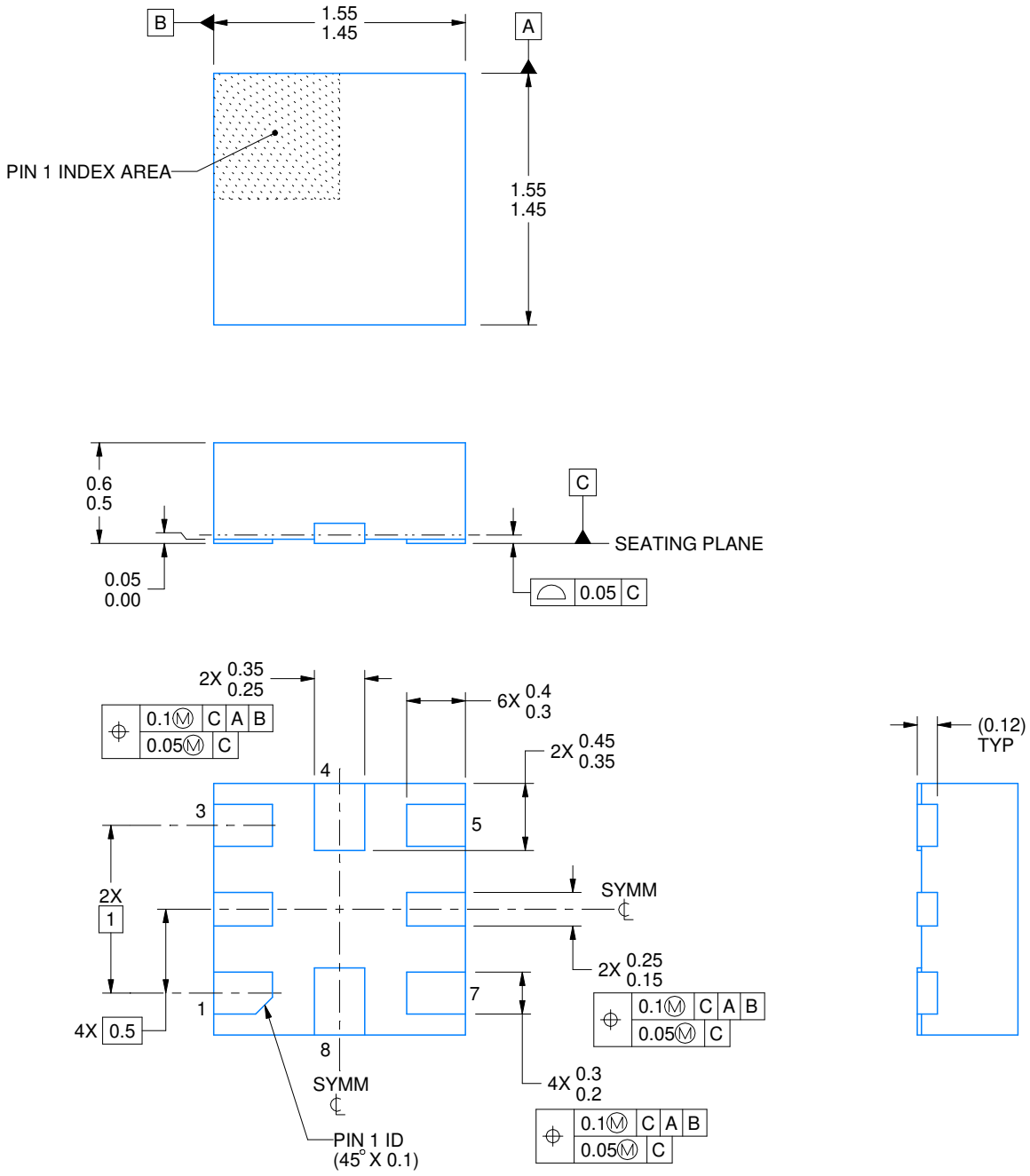
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB31RSER	UQFN	RSE	8	3000	202.0	201.0	28.0

RSE0008A

PACKAGE OUTLINE

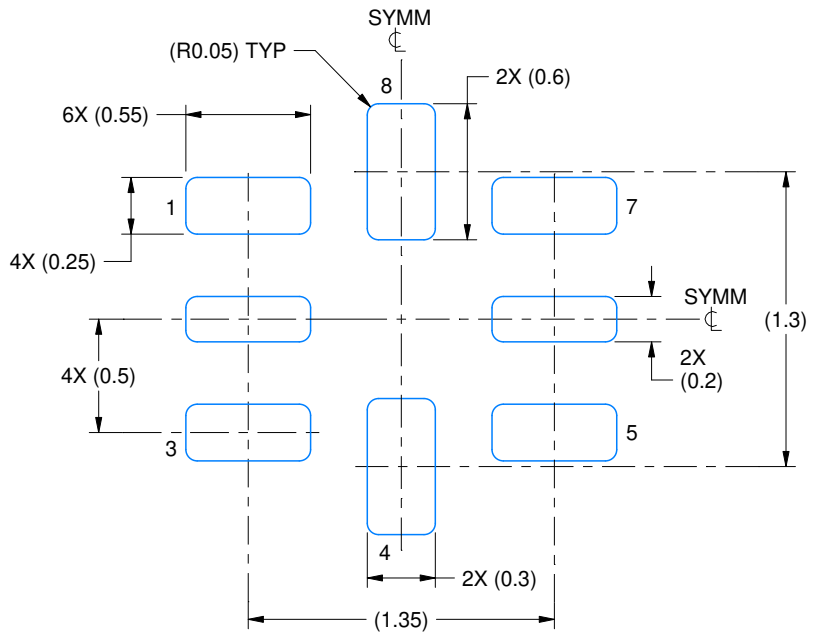
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

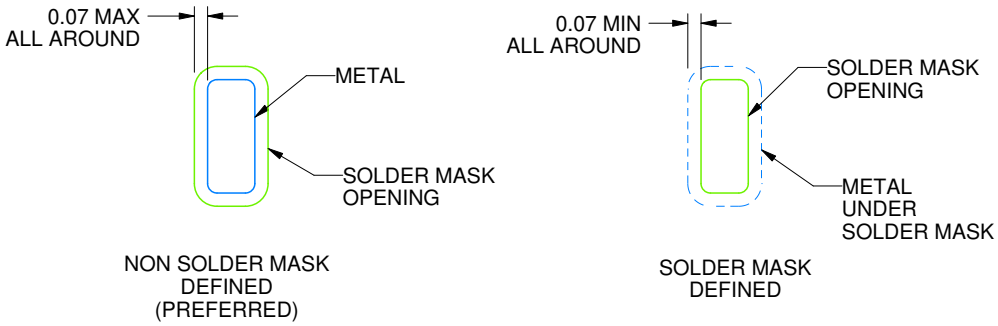


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

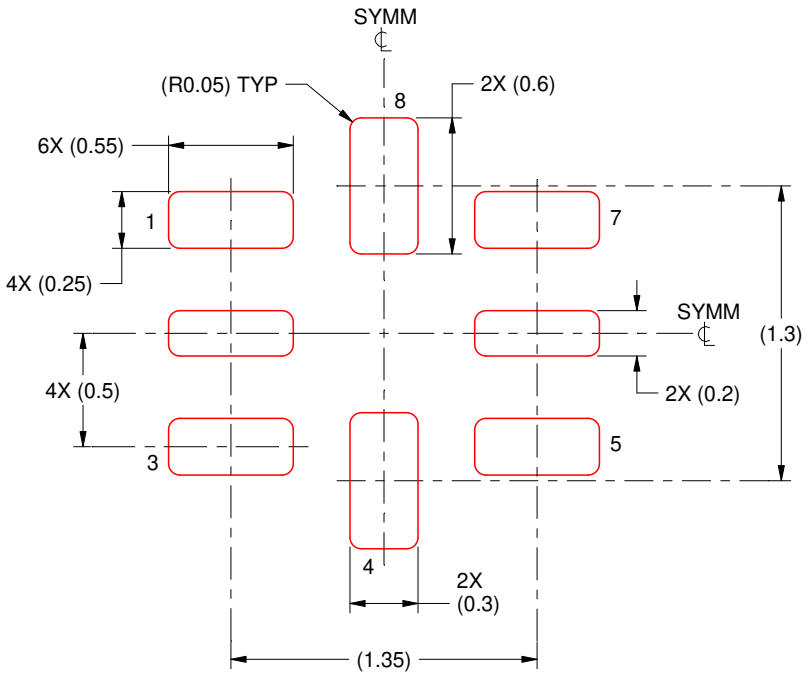


SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/B 03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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