FEATURES

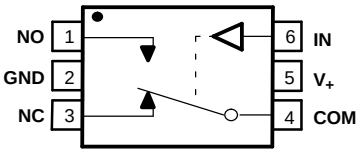
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Specified Break-Before-Make Switching**
- **Low ON-State Resistance (1 Ω)**
- **Control Inputs Are 5-V Tolerant**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **Low Total Harmonic Distortion**
- **1.65-V to 5.5-V Single-Supply Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not liited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this componenet beyond specified performance and environmental limits.

APPLICATIONS

- **Cell Phones**
- **PDAs**
- **Portable Instrumentation**

SOT-23 PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS5A3159-EP is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent ON-state resistance matching with the break-before-make feature to prevent signal distortion during the transferring of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Summary of Characteristics(1)

Configuration	2:1 Multiplexer/ Demultiplexer (1 × SPDT)
Number of channels	1
ON-state resistance (r_{on})	1.1 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	20 ns/15 ns
Break-before-make time (t_{BBM})	12 ns
Charge injection (Q_C)	36 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	–65 dB at 1 MHz
Crosstalk (X_{TALK})	–66 dB at 1 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{NO(OFF)}/(I_{NC(OFF)}$)	±20 nA
Package option	6-pin DBV

(1) V_+ = 5 V and T_A = 25°C

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2005–2006, Texas Instruments Incorporated

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT (SOT-23) – DBV	Tape and reel	TS5A3159MDBVREP	JA8R

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(2)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range(2)(3)(4)		–0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NO}, V_{COM} < 0 or V_{NO}, V_{COM} > V_+		±50	mA
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_+		±200	mA
	On-state peak switch current(5)			±400	mA
V_{IN}	Digital input voltage range(2)(3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0		–50	mA
	Continuous current through V_+ or GND			±100	mA
θ_{JA}	Package thermal impedance(6)			165	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Electrical Characteristics" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) Pulse at 1-ms duration < 10% duty cycle.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V (5 V nominal), T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –30 mA,	Switch ON, See Figure 11	25°C	4.5 V		1	1.5	Ω
				Full				1.5	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –30 mA,	Switch ON, See Figure 11	25°C	4.5 V		0.75	1.1	Ω
				Full				1.3	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –30 mA,	Switch ON, See Figure 11	25°C	4.5 V		0.1		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –30 mA	Switch ON, See Figure 11	25°C	4.5 V		0.233		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –30 mA					0.15		
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 4.5 V, V_{COM} = 0,	Switch OFF, See Figure 12	25°C	5.5 V	–6	0.2	4	nA
				Full		–20		60	
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 13	25°C	5.5 V	–6	2.8	4	nA
				Full		–40		70	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = 4.5 V or Open, V_{COM} = 4.5 V,	Switch ON, See Figure 13	25°C	5.5 V	–4	0.47	7	nA
				Full		–40		80	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		Full	5.5 V	–1		1	µA

(1) T_A = 25°C

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V (5 V nominal), T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	4.5 V to 5.5 V		20	35	ns
				Full				40	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	4.5 V to 5.5 V		15	20	ns
				Full				35	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	4.5 V to 5.5 V	1	12	14.5	ns
				Full		1			
Charge injection	Q_C	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 20	25°C	5 V		36		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	5 V		23		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	5 V		84		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	5 V		84		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 14	25°C	5 V		2.1		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	5 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	5 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	5 V		–65		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	5 V		0.01		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	5.5 V			0.1	µA

Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V (3.3 V nominal), T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –24 mA,	Switch ON, See Figure 11	25°C	3 V		1.35	2.15	Ω
				Full				2.15	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2 V, I_{COM} = –24 mA,	Switch ON, See Figure 11	25°C	3 V		1.15	1.7	Ω
				Full				1.7	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –24 mA,	Switch ON, See Figure 11	25°C	3 V		0.11		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –24 mA	Switch ON, See Figure 11	25°C	3 V		0.225		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –24 mA					0.25		
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 3 V, V_{COM} = 0,	Switch OFF, See Figure 12	25°C	3.6 V		0.2		nA
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 13	25°C	3.6 V		2.8		nA
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = 3 V or Open, V_{COM} = 3 V,	Switch ON, See Figure 13	25°C	3.6 V		0.47		nA
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0	0.6		V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		Full	3.6 V	–1		1	µA

(1) T_A = 25°C

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V (3.3 V nominal), T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	3 V to 3.6 V		30	40	ns
				Full				55	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	3 V to 3.6 V		20	25	ns
				Full				40	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	3 V to 3.6 V	1	21	29	ns
				Full		1			
Charge injection	Q_C	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 20	25°C	3.3 V		20		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	3.3 V		23		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	3.3 V		84		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	3.3 V		84		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 14	25°C	3.3 V		2.1		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	3.3 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	3.3 V		–65		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	3.3 V		–65		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	3.3 V		0.015		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	3.6 V			0.1	µA

Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V (2.5 V nominal), T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –8 mA,	Switch ON, See Figure 11	25°C	2.5 V		1.7	2.7	Ω
				Full				2.9	
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 11	25°C	2.5 V		1.45	2.3	Ω
				Full				2.5	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 11	25°C	2.5 V		0.7		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –8 mA	Switch ON, See Figure 11	25°C	2.5 V		0.5		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA					0.45		
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0,	Switch OFF, See Figure 12	25°C	2.7 V		0.2		nA
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 2.3 V, V_{COM} = Open,	Switch ON, See Figure 13	25°C	2.7 V		2.8		nA
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = 2.3 V or Open, V_{COM} = 2.3 V,	Switch ON, See Figure 13	25°C	2.7 V		0.47		nA
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0	0.6		V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		Full	2.7 V	–1		1	µA

(1) T_A = 25°C

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V (2.5 V nominal), T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	2.3 V to 2.7 V		40	55	ns
				Full				70	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	2.3 V to 2.7 V		30	40	ns
				Full				55	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	2.3 V to 2.7 V	1	33	39	ns
				Full		1			
Charge injection	Q_C	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 20	25°C	2.5 V		13		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	2.5 V		23		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		84		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		84		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 14	25°C	2.5 V		2.1		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	2.5 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	2.5 V		–64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	2.5 V		–64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 21	25°C	2.5 V		0.025		%
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	2.7 V			0.1	µA

Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V (1.8 V nominal), T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NC}, V_{NO}					0		V_+	V
Peak ON resistance	r_{peak}	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –2 mA,	Switch ON, See Figure 11	25°C	1.8 V		4	4.9	Ω
				Full			7		
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 11	25°C	1.8 V		1.7	3.2	Ω
				Full				4.2	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 11	25°C	1.8 V		0.7		Ω
				Full			0.7		
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –2 mA	Switch ON, See Figure 11	25°C	1.8 V		1.85		Ω
				Full			1.85		
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA		25°C			0.9		
				Full			0.9		
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0,	Switch OFF, See Figure 12	25°C	1.95 V		0.2		nA
NC, NO ON leakage current	$I_{NC(ON)}$, $I_{NO(ON)}$	V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 13	25°C	1.95 V		2.8		nA
COM ON leakage current	$I_{COM(ON)}$	V_{NC} or V_{NO} = 1.65 V or Open, V_{COM} = 1.65 V,	Switch ON, See Figure 13	25°C	1.95 V		0.47		nA
Digital Control Input (IN)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0	0.6		V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		Full	1.95 V	–1		1	µA

(1) T_A = 25°C

Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V (1.8 V nominal), T_A = –55°C to 125°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	1.65 V to 1.95 V		65	70	ns
				Full				95	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	1.65 V to 1.95 V		40	55	ns
				Full				70	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	1.65 V to 1.95 V	1	60	72	ns
				Full		0.5			
Charge injection	Q_C	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 20	25°C	1.8 V		13		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	1.8 V		23		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		84		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		84		pF
Digital input capacitance	C_{IN}	V_{IN} = V_+ or GND,	See Figure 14	25°C	1.8 V		2.1		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 17	25°C	1.8 V		100		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 18	25°C	1.8 V		–63		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 19	25°C	1.8 V		–63		dB
Supply									
Positive supply current	I_+	V_{IN} = V_+ or GND,	Switch ON or OFF	Full	1.95 V			0.1	µA

TYPICAL PERFORMANCE

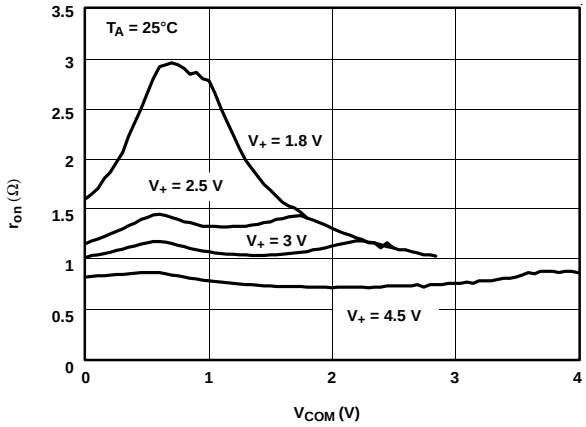


Figure 1. r_{on} vs V_{COM}

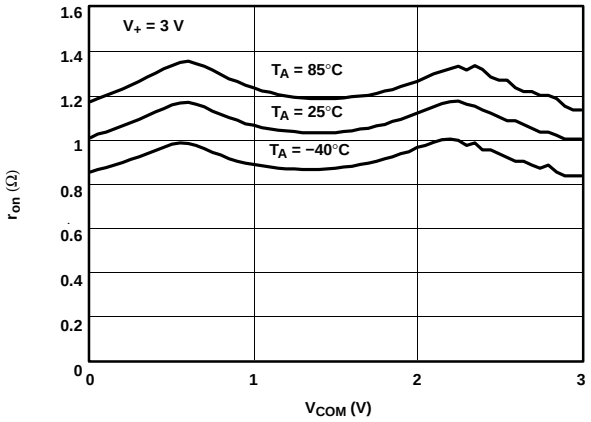


Figure 2. r_{on} vs V_{COM}

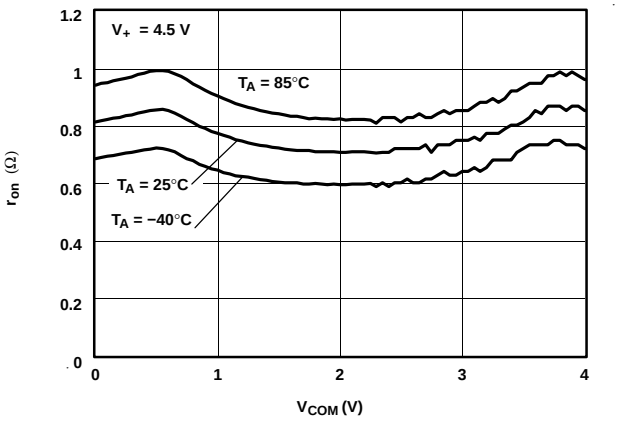


Figure 3. r_{on} vs V_{COM}

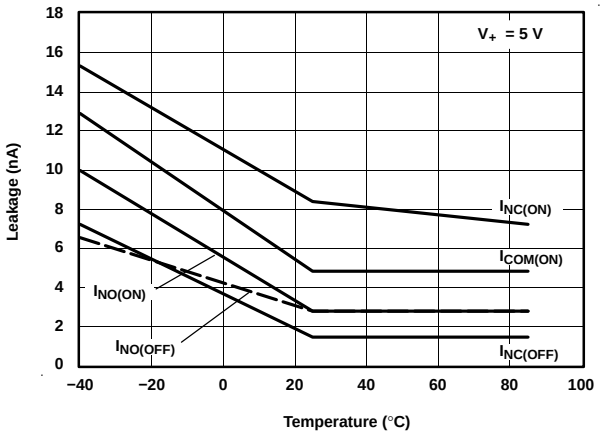


Figure 4. Leakage Current vs Temperature

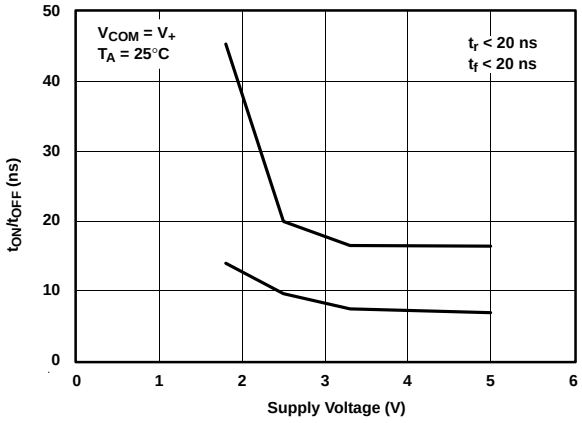


Figure 5. t_{ON}/t_{OFF} vs V_+

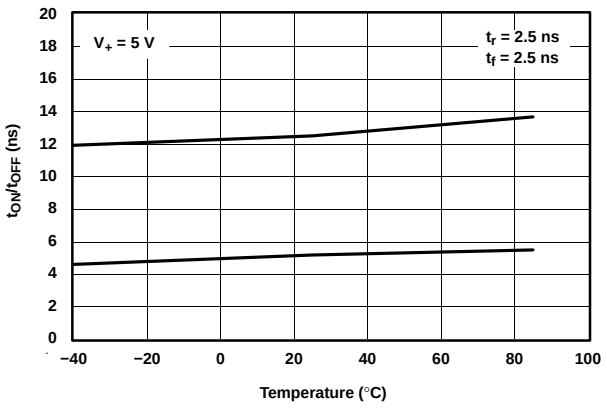


Figure 6. t_{ON}/t_{OFF} vs Temperature

TYPICAL PERFORMANCE (continued)

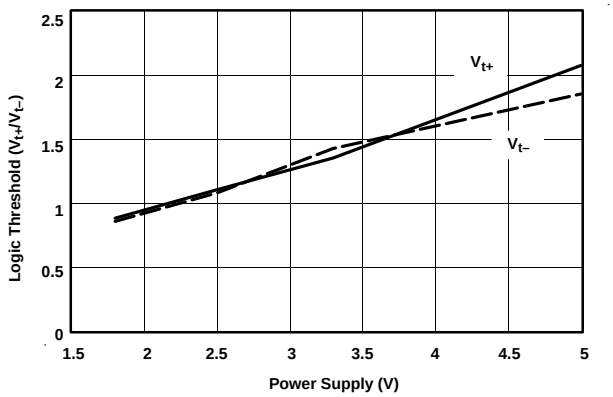


Figure 7. Logic Threshold vs Power Supply

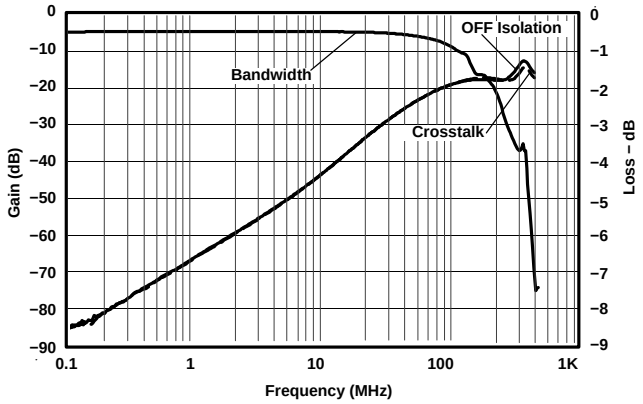


Figure 8. Frequency Response

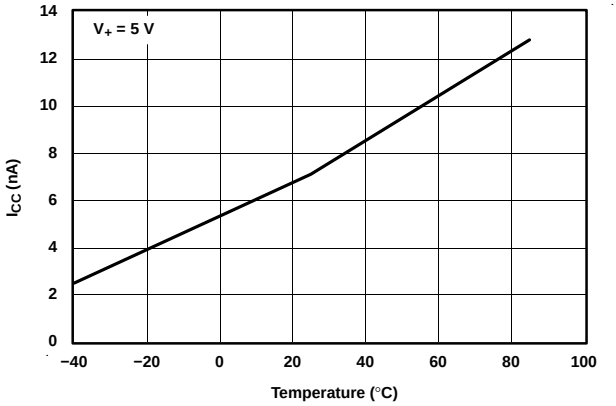


Figure 9. Power-Supply Current vs Temperature

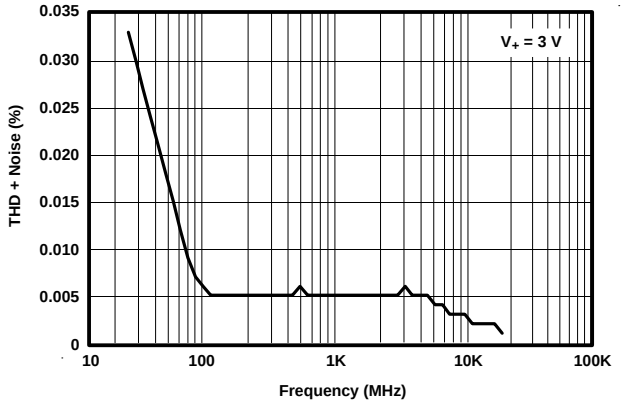


Figure 10. Total Harmonic Distortion (THD) vs Frequency

PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	NO	Normally open
2	GND	Digital ground
3	NC	Normally closed
4	COM	Common
5	V_+	Power supply
6	IN	Digital control to connect COM to NO or NC

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at IN
I_{IH}, I_{IL}	Leakage current measured at IN
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_{IN}	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.

PARAMETER DESCRIPTION (continued)

SYMBOL	DESCRIPTION
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

PARAMETER MEASUREMENT INFORMATION

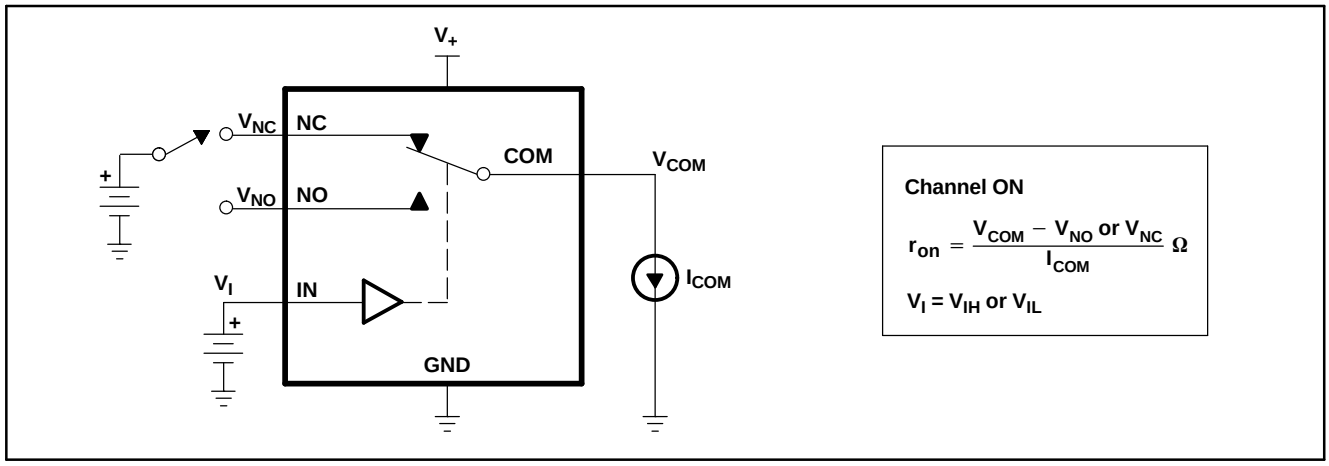


Figure 11. ON-State Resistance (r_{on})

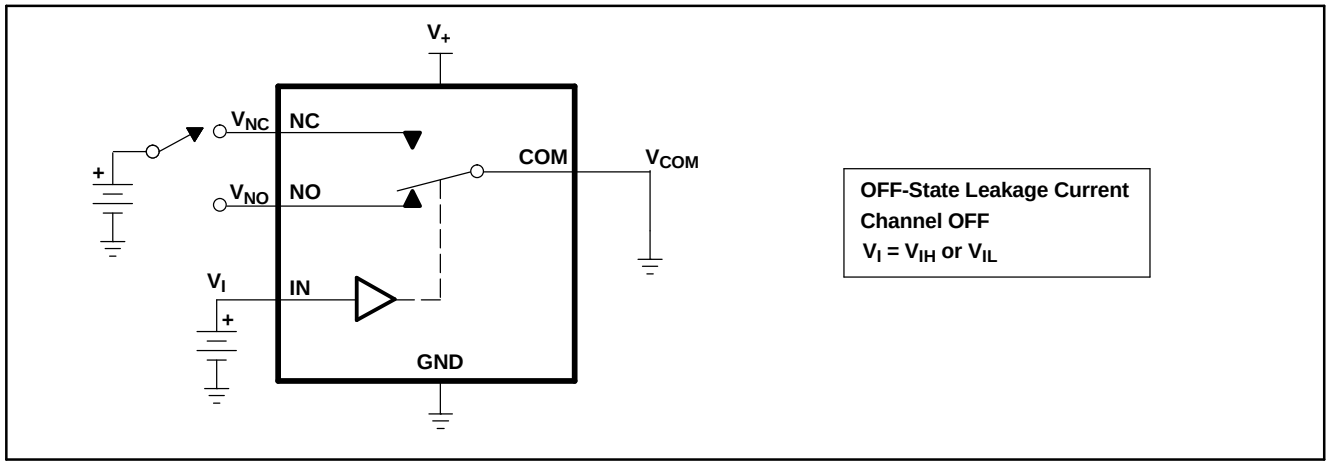


Figure 12. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$)

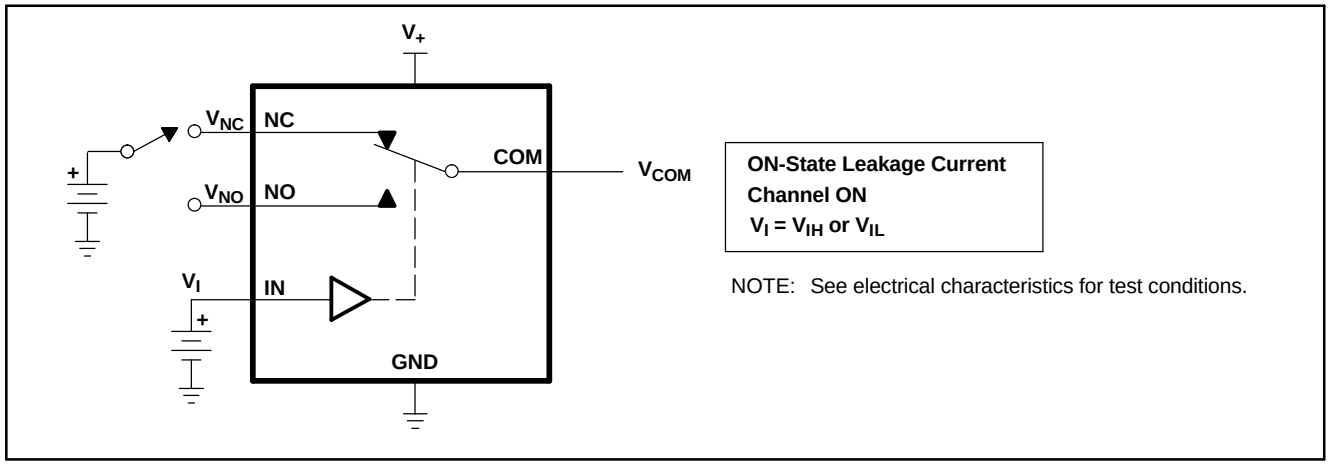


Figure 13. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

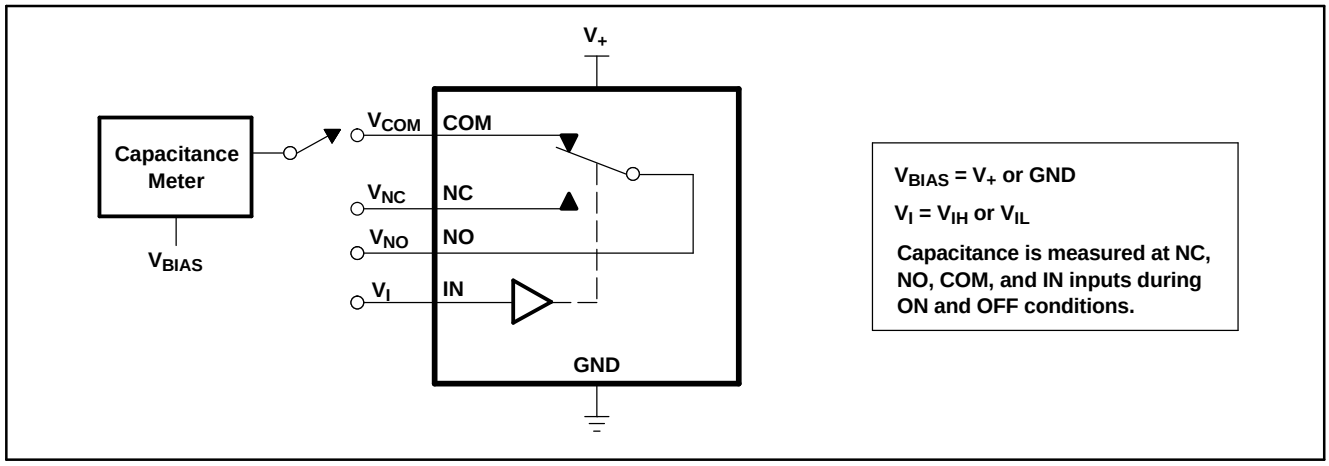
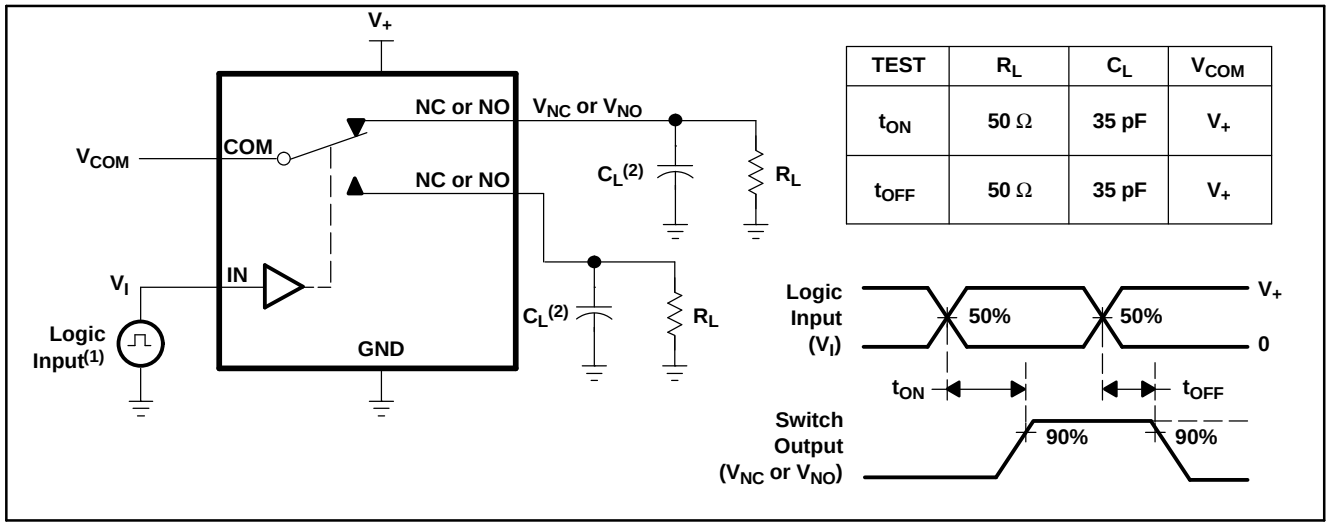


Figure 14. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



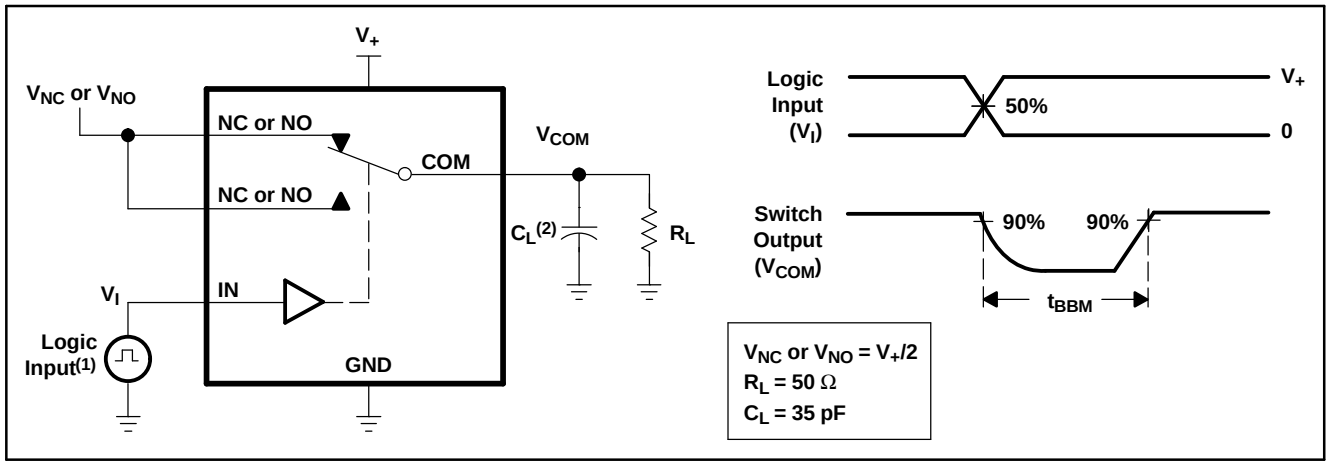
TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 15. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 16. Break-Before-Make Time (t_{BBM})

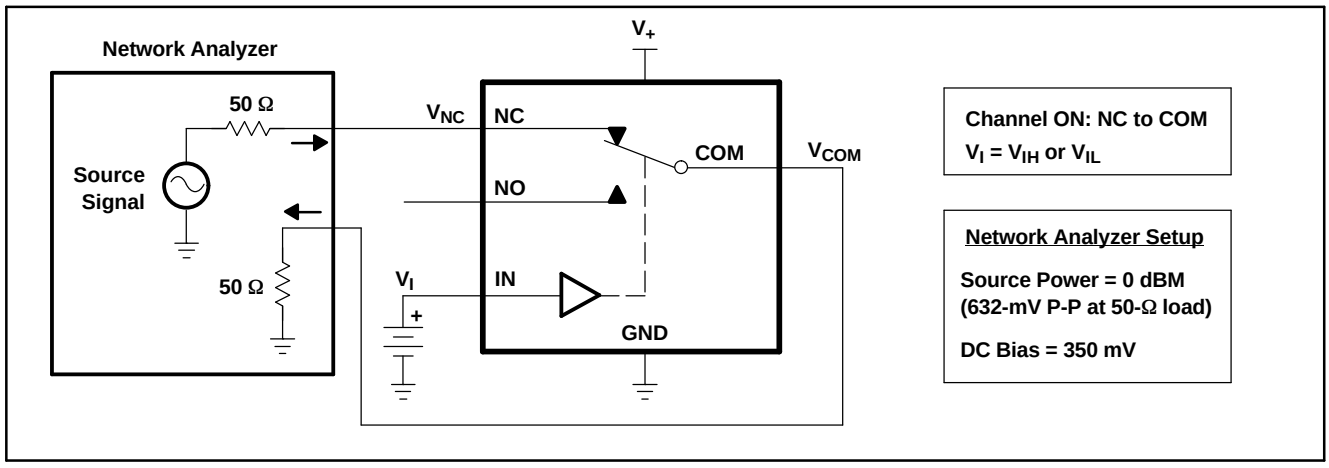


Figure 17. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

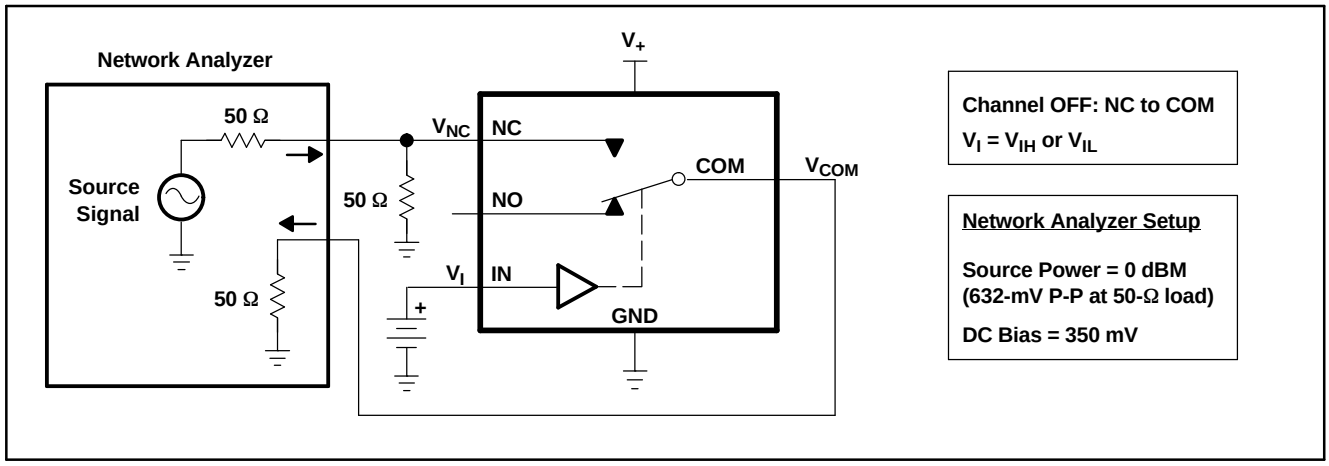


Figure 18. OFF Isolation (O_{ISO})

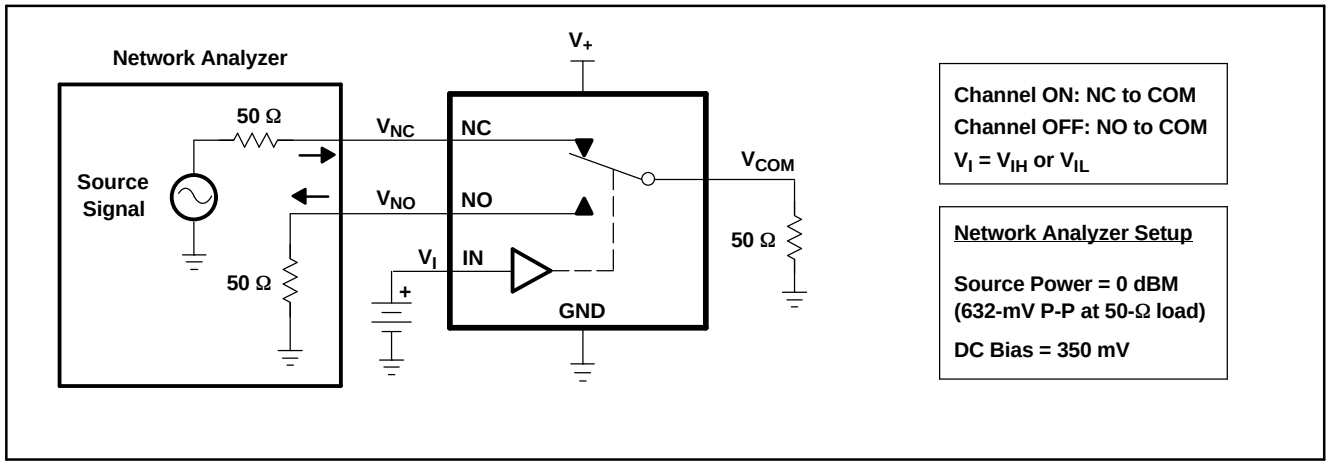
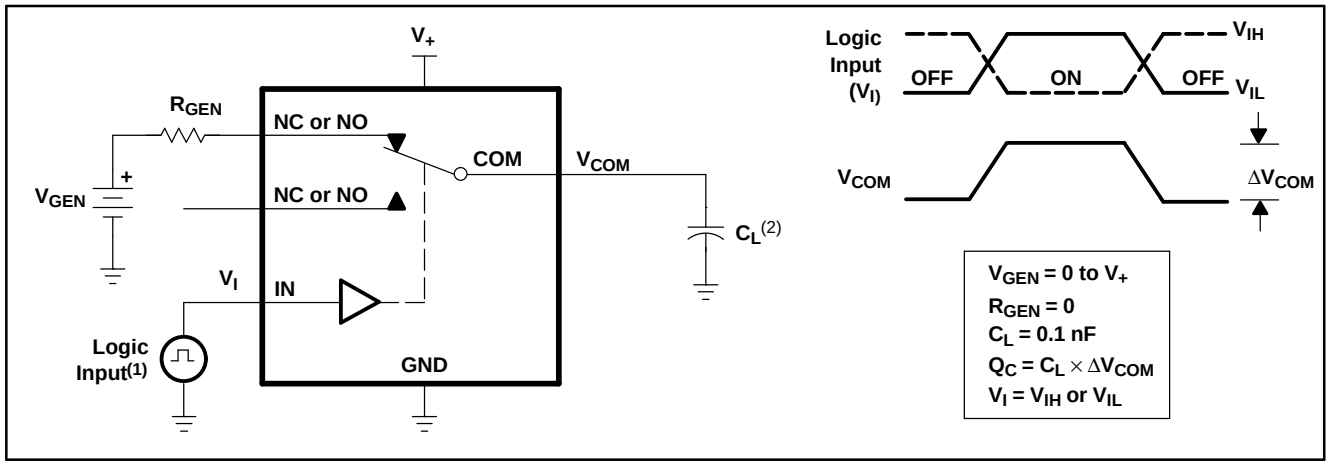


Figure 19. Crosstalk (X_{TALK})

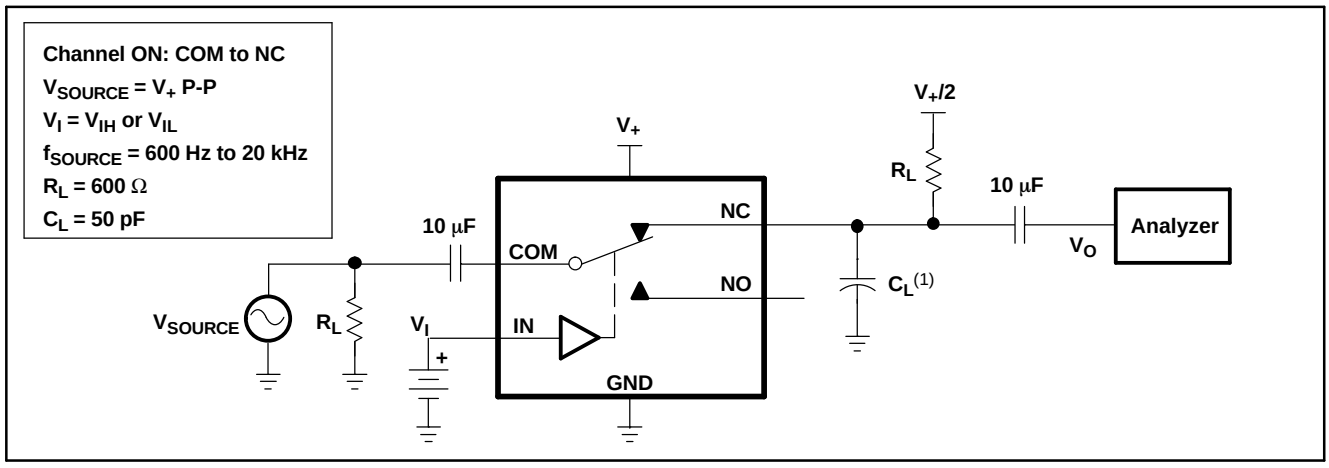
PARAMETER MEASUREMENT INFORMATION (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 20. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3159MDBVREP	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	JA8R
V62/06613-01XE	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	JA8R

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS5A3159-EP :

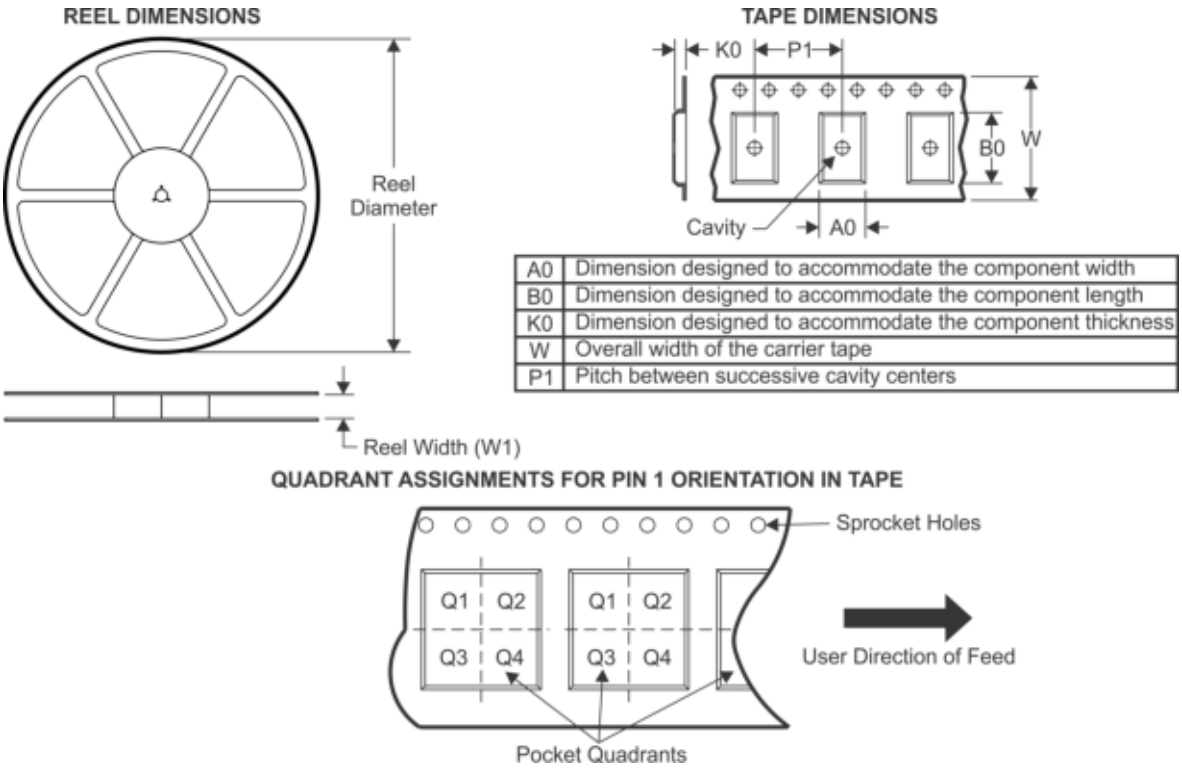
- Catalog : TS5A3159

- Automotive : TS5A3159-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

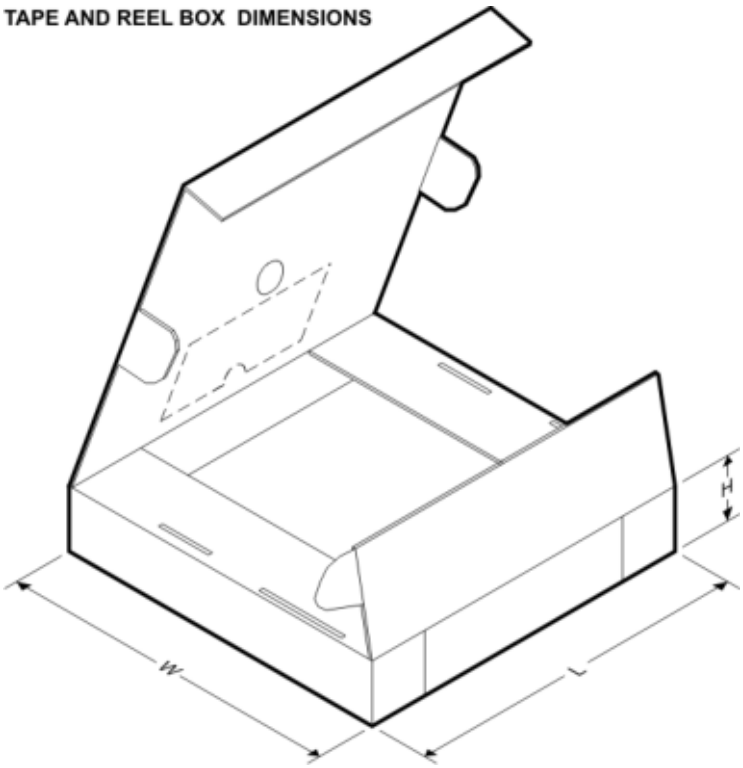


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159MDBVREP	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

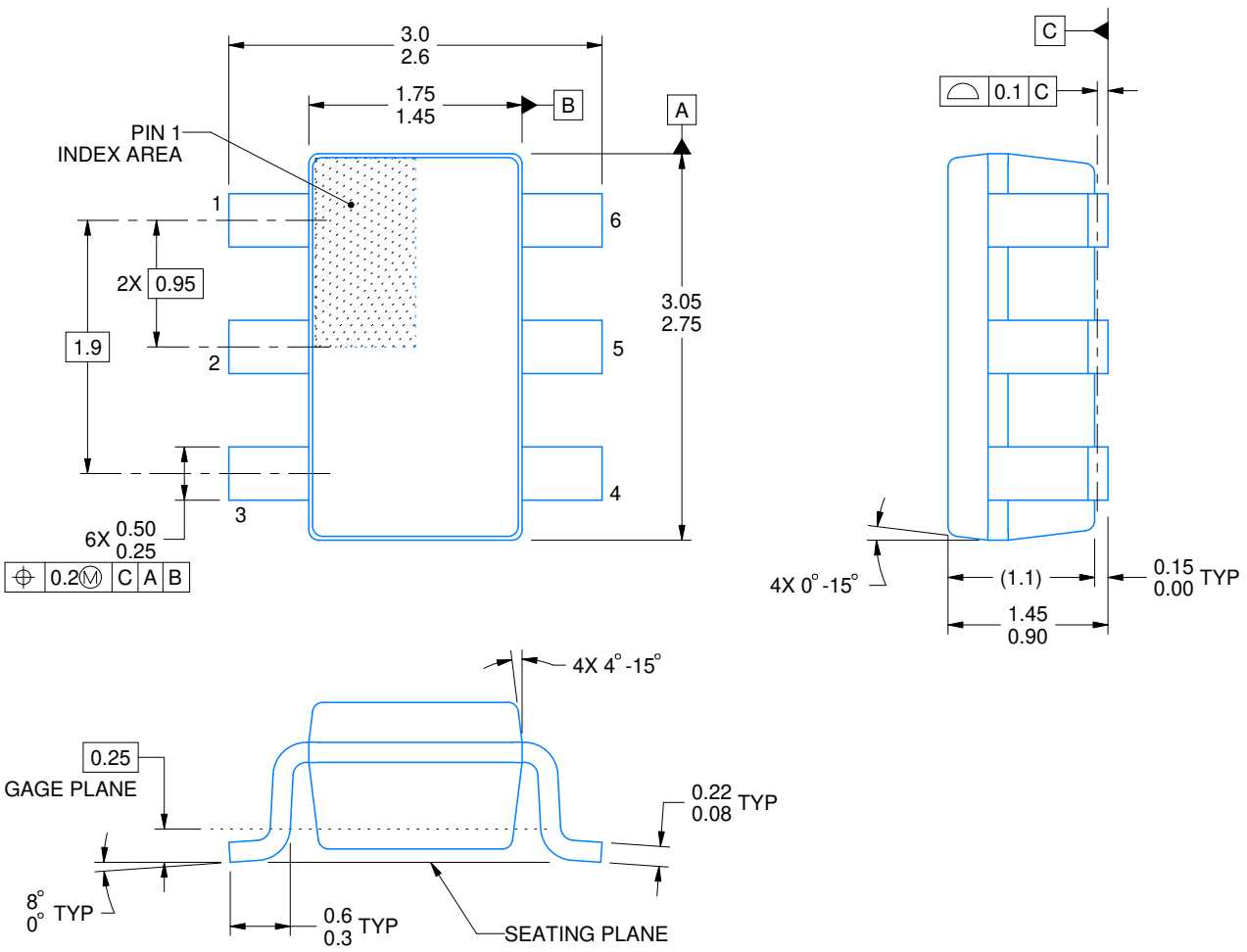
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3159MDBVREP	SOT-23	DBV	6	3000	202.0	201.0	28.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

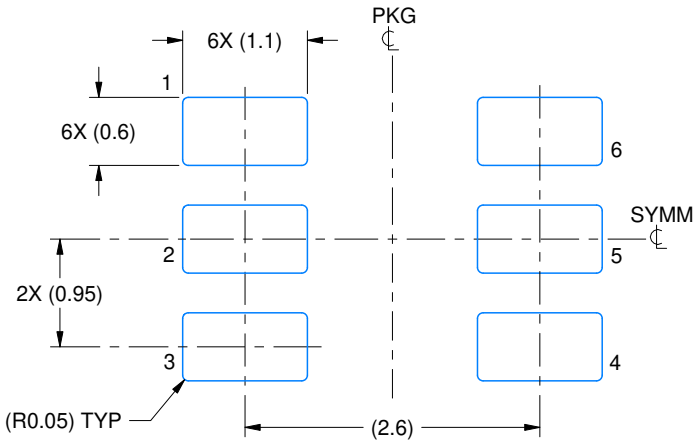
SMALL OUTLINE TRANSISTOR



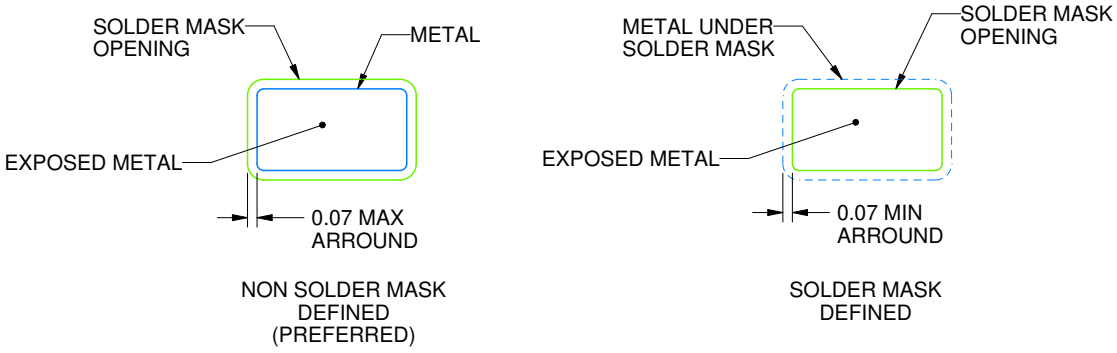
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

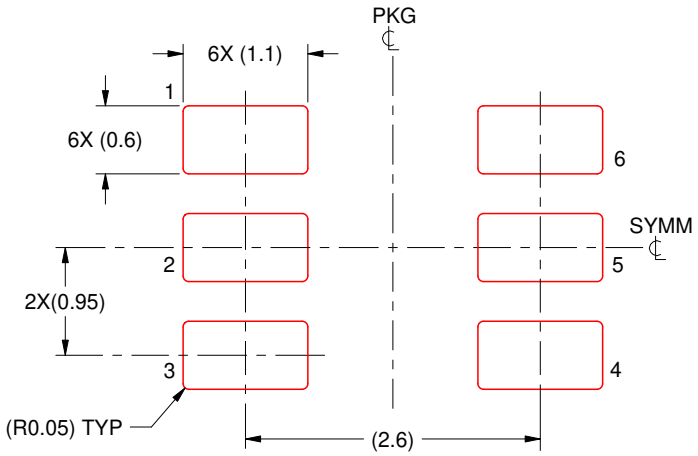


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025