TS5A3159A 1-Ω SPDT Analog Switch 5-V and 3.3-V Single-Channel 2:1 Multiplexer and Demultiplexer

1 Features

- Specified Break-Before-Make Switching
- Isolation in Power-Down Mode, $V_+ = 0$
- Terminal Compatible With TS5A3159 Device
- Low ON-State Resistance (1 Ω)
- Control Inputs are 5.5-V Tolerant
- Low Charge Injection
- Excellent On-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals

3 Description

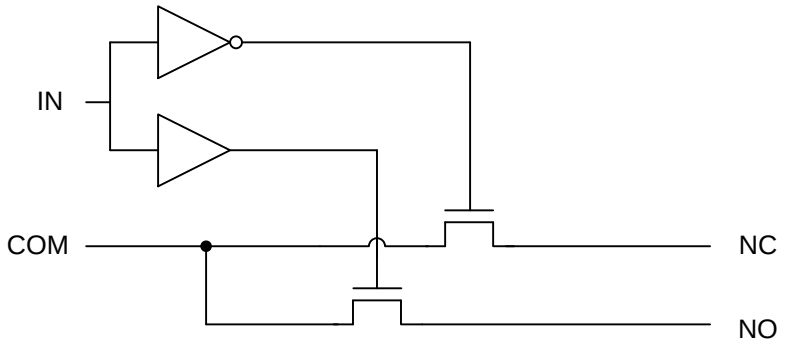
The TS5A3159A device is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers low on-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3159ADBVR	SOT-23 (6)	2.90 mm × 1.60 mm
TS5A3159ADCKR	SC70 (6)	2.00 mm × 1.25 mm
TS5A3159AYZPR	DSBGA (6)	1.41 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2015) to Revision F — **Page**

- Changed the YZP package From: 8 Pins To: 6 Pins in the *Thermal Information* table ... 4

Changes from Revision D (June 2015) to Revision E — **Page**

- Changed Pin Descriptions ... 3

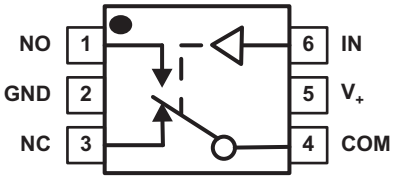
Changes from Revision C (May 2010) to Revision D — **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

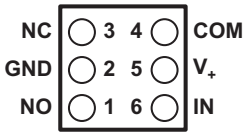
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5 Pin Configuration and Functions

DBV or DCK Packages
6-Pin SOT-23 or SC-70
Top View



YZP Packages
6-Pin DSBGA
Bottom View



NO – Normally open

NC – Normally closed

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23, SC-70	DSBGA		
COM	4	C2	I/O	Common switch port
GND	2	B1	—	Ground
IN	6	A2	I/O	Switch select. High = COM connected to NO; Low = COM connected to NC
NC	3	C1	I/O	Normally closed switched port
NO	1	A1	—	Normally open switch port
V+	5	B2	I	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	6.5	V
V_{NO}, V_{NC}, V_{COM}	Analog voltage(3)(4)(5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0	–50		mA
I_{NO}, I_{NC}, I_{COM}	ON-state switch current	V_{NO}, V_{NC}, V_{COM} = 0 to V_+	–200	200	mA
	ON-state peak switch current(6)		–400	400	mA
V_I	Digital input voltage(3)(4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_A	Absolute maximum operating temperature(7)	DBV or DCK package		150	°C
		YZP package		125	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle.
(7) The lifetime of the device will be reduced if the device operates continually at this temperature.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage	0	V_+	V
V+	Supply voltage	1.65	5.5	V
V_I	Control input voltage	0	5.5	V
T_A	Operating temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS5A3159A			UNIT
		DBV (SOT-23)	DCK (SC-70)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	259	123	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C	4.5 V		0.8	1.1	Ω
				Full				1.5	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C	4.5 V		0.7	0.9	Ω
				Full				1.1	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C	4.5 V		0.05	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C	4.5 V		0.15		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch on, see Figure 14	25°C			0.1	0.25	
				Full				0.25	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V to 4.5 V, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = 1 V to 4.5 V,	Switch off, see Figure 15	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch off, see Figure 15	25°C	0 V	–1	0.2	1	µA
				Full		–20		20	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 4.5 V, V_{COM} = Open,	Switch on, see Figure 16	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch off, see Figure 15	25°	0 V	–1	0.1	1	µA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 4.5 V,	Switch on, see Figure 16	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
DIGITAL INPUT (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	5.5 V	–2		2	nA
				Full		100		100	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 18	25°C	5 V	1	12	30	ns
				Full	4.5 V to 5.5 V	1		35	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 18	25°C	5 V	1	5	20	ns
				Full	4.5 V to 5.5 V	1		30	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,	C_L = 35 pF, see Figure 19	25°C	5 V		6		ns
				Full	4.5 V to 5.5 V	1		20	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see Figure 23	25°C	5 V		–20		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch off, see Figure 17	25°C	5 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch on, see Figure 17	25°C	5 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch on, see Figure 17	25°C	5 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 17	25°C	5 V		2		pF
BW	Bandwidth	R_L = 50 Ω,	Switch on, see Figure 20	25°C	5 V		100		MHz

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

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Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
O_{ISO}	Off isolation	R_L = 50 Ω, f = 1 MHz,	Switch off, see Figure 21	25°C	5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch on, see Figure 22	25°C	5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 200 Hz to 20 kHz, see Figure 24	25°C	5 V		0.004%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND,	Switch on or off	25°C	5.5 V		10	50	nA
				Full				500	

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C	3 V		1.3	1.6	Ω
				Full				2	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C	3 V		1.2	1.5	Ω
				Full				1.7	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C	3 V		0.1	0.15	Ω
				Full				0.15	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C	3 V		0.2		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch on, See Figure 14	25°C			0.15	0.3	
				Full				0.3	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO off leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = 1 V to 3 V, or V_{NC} or V_{NO} = 3 V, V_{COM} = 1 V to 3 V,	Switch off, See Figure 15	25°C	3.6 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch off, See Figure 15	25°C	0 V	–1	0.2	1	µA
				Full		–15		15	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO on leakage current	V_{NC} or V_{NO} = 1 V, V_{COM} = Open, or V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch on, See Figure 16	25°C	3.6 V	–10	2	10	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM off leakage current	V_{NC} or V_{NO} = 3.6 V to 0, V_{COM} = 0 to 3.6 V,	Switch off, See Figure 15	25°	0 V	–1	0.2	1	µA
				Full		–15		15	
$I_{COM(ON)}$	COM on leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 1 V, or V_{NC} or V_{NO} = Open, V_{COM} = 3 V,	Switch on, See Figure 16	25°C	3.6 V	–10	2	10	nA
				Full		–20		20	
DIGITAL INPUT (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	3.6 V	–2		2	nA
				Full		–100		100	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V	5	16	35	ns
				Full	3 V to 3.6 V	3		50	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V	1	9	20	ns
				Full	3 V to 3.6 V	1		30	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

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Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V		9		ns
				Full	3 V to 3.6 V	1		40	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	3.3 V		–11		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch off, See Figure 17	25°C	3.3 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch on, See Figure 17	25°C	3.3 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch on, See Figure 17	25°C	3.3 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 17	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω,	Switch on, See Figure 20	25°C	3.3 V		100		MHz
O_{ISO}	Off isolation	R_L = 50 Ω, f = 1 MHz,	Switch off, See Figure 21	25°C	3.3 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch on, See Figure 22	25°C	3.3 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V		0.01%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND,	Switch on or off	25°C	3.6 V		10	25	nA
				Full				100	

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	2.3 V		1.8	2.5	Ω
				Full				2.7	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	2.3 V		1.5	2	Ω
				Full				2.4	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	2.3 V		0.15	0.2	Ω
				Full				0.2	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	2.3 V		0.6		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C			0.6	1	
				Full				1	
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = 0.5 V to 2.3 V, or V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0.5 V to 2.3 V,	Switch off, See Figure 15	25°C	2.7 V	–20	2	20	nA
				Full		–50		50	
$I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch off, See Figure 15	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.5 V, V_{COM} = Open, or V_{NC} or V_{NO} = 2.2 V, V_{COM} = Open,	Switch on, See Figure 16	25°C	2.7 V	–10	2	10	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 2.7 V to 0, V_{COM} = 0 to 2.7 V,	Switch off, See Figure 15	25°	0 V	–1	0.1	10	µA
				Full		–10		20	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.5 V, or V_{NC} or V_{NO} = Open, V_{COM} = 2.2 V,	Switch on, See Figure 16	25°C	2.7 V	–10	2	10	nA
				Full		–20		20	
DIGITAL INPUT (IN)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	2.7 V	–2		2	nA
				Full		20		20	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V	5	22	40	ns
				Full	2.3 V to 2.7 V	5		50	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V	2	6	35	ns
				Full	2.3 V to 2.7 V	2		50	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V	2	13	35	ns
				Full	2.3 V to 2.7 V	2		45	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	2.5 V		–7		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch off, See Figure 17	25°C	2.5 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch on, See Figure 17	25°C	2.5 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch on, See Figure 17	25°C	2.5 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 17	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω,	Switch on, See Figure 20	25°C	2.5 V		100		MHz

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

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Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
O_{ISO}	Off isolation	R_L = 50 Ω, f = 1 MHz,	Switch off, See Figure 21	25°C	2.5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch on, See Figure 22	25°C	2.5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V		0.02%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND,	Switch on or off	25°C	2.7 V		10	20	nA
				Full				50	

6.8 Electrical Characteristics for 1.8-V Supply

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –2 mA,	Switch on, See Figure 14	25°C	1.65 V		5		Ω
				Full				15	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch on, See Figure 14	25°C	1.65 V		2	2.5	Ω
				Full				3.5	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 1.5 V, I_{COM} = –2 mA,	Switch on, See Figure 14	25°C	1.65 V		0.15	0.4	Ω
				Full				0.4	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –8 mA,	Switch on, See Figure 14	25°C	1.65 V		5		Ω
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch on, See Figure 14	25°C			4.5		
				Full					
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = 0.3 V to 1.65 V, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0.3 V to 1.65 V,	Switch off, See Figure 15	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
$I_{NC(PWROFF)}$ $I_{NO(PWROFF)}$		V_{NC} or V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch off, See Figure 15	25°C	0 V	–1	0.1	1	µA
				Full		–5		5	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 0.3 V, V_{COM} = Open, or V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open,	Switch on, See Figure 16	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
$I_{COM(PWROFF)}$	COM OFF leakage current	V_{NC} or V_{NO} = 1.95 V to 0, V_{COM} = 0 to 1.95 V,	Switch off, See Figure 15	25°	0 V	–1	0.1	7	µA
				Full		–5		5	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = Open, V_{COM} = 0.3 V, or V_{NC} or V_{NO} = Open, V_{COM} = 1.65 V,	Switch on, See Figure 16	25°C	1.95 V	–5	2	5	nA
				Full		–20		20	
DIGITAL INPUT (IN)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	1.95 V	–2		2	nA
				Full		20		20	
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	1.8 V	10	35	70	ns
				Full	1.65 V to 1.95 V	10		75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

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Electrical Characteristics for 1.8-V Supply (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	1.8 V	2	15	40	ns
				Full	1.65 V to 1.95 V	2		50	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	1.8 V		22		ns
				Full	1.65 V to 1.95 V	2		70	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	1.8 V		–4		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch off, See Figure 17	25°C	1.8 V		18		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND,	Switch on, See Figure 17	25°C	1.8 V		55		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND,	Switch on, See Figure 17	25°C	1.8 V		55		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See Figure 17	25°C	1.8 V		2		pF
BW	Bandwidth	R_L = 50 Ω,	Switch on, See Figure 20	25°C	1.8 V		105		MHz
O_{ISO}	Off isolation	R_L = 50 Ω, f = 1 MHz,	Switch off, See Figure 21	25°C	1.8 V		64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch on, See Figure 22	25°C	1.8 V		64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	1.8 V		0.06%		
SUPPLY									
I_+	Positive supply current	V_I = V_+ or GND,	Switch on or off	25°C	1.95 V		5	15	µA
				Full				50	

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6.9 Typical Characteristics

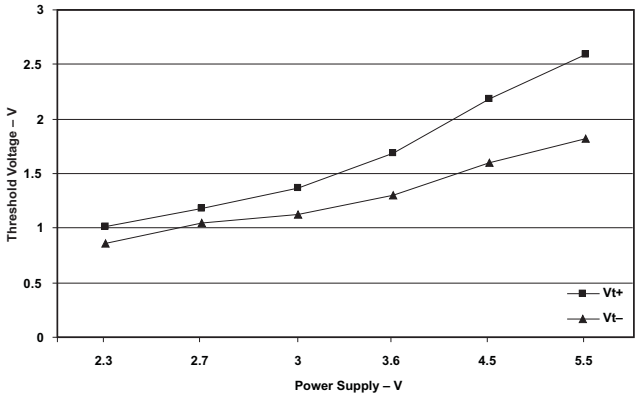


Figure 1. Logic Threshold vs Power Supply

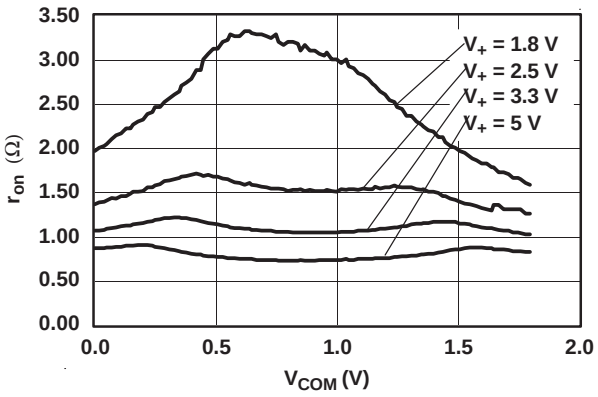


Figure 2. r_{on} vs V_{COM}

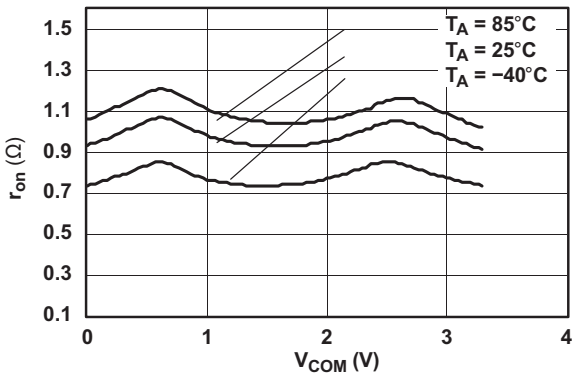


Figure 3. r_{on} vs V_{COM} (V_+ = 3.3 V)

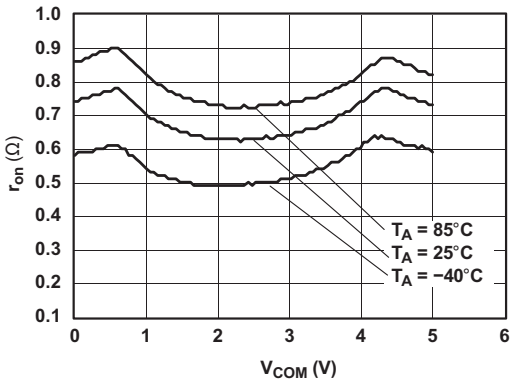


Figure 4. r_{on} vs V_{COM} (V_+ = 5 V)

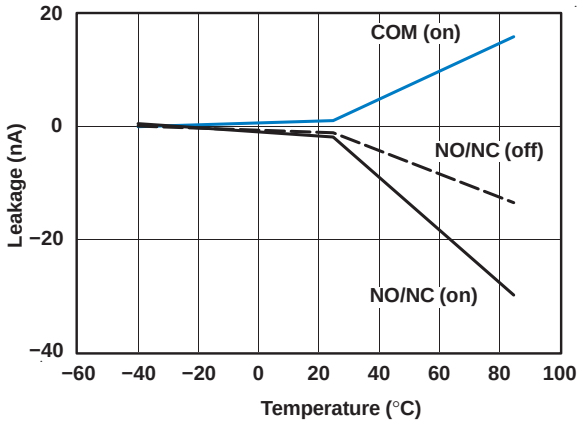


Figure 5. Leakage Current vs Temperature (V_+ = 3.3 V)

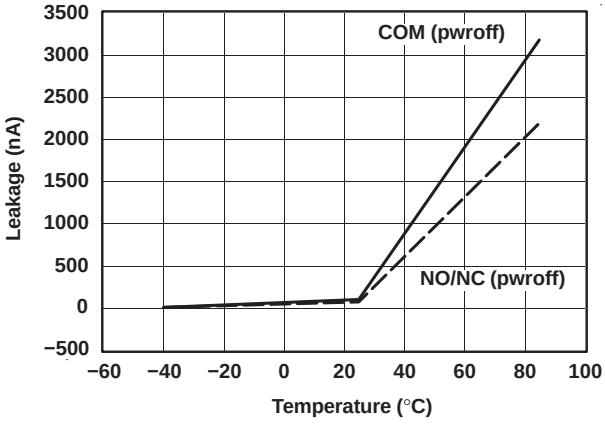


Figure 6. Leakage Current vs Temperature (V_+ = 5 V)

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Typical Characteristics (continued)

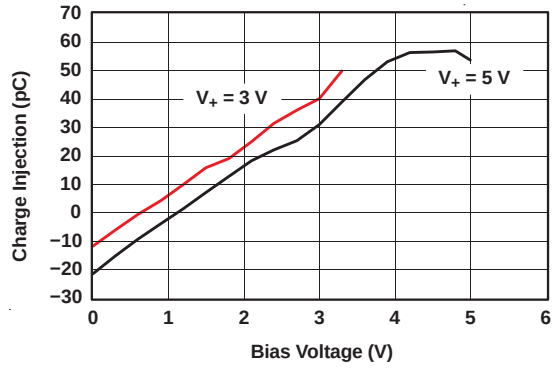


Figure 7. Charge Injection vs Bias Voltage

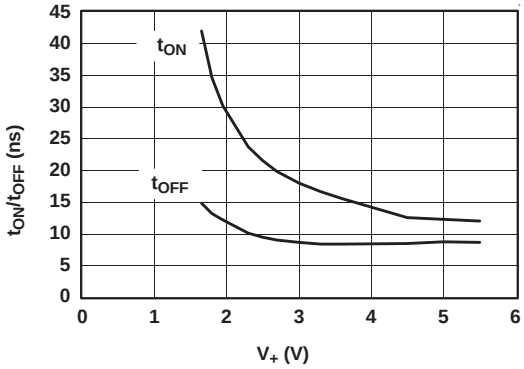


Figure 8. t_{ON} and t_{OFF} vs Supply Voltage

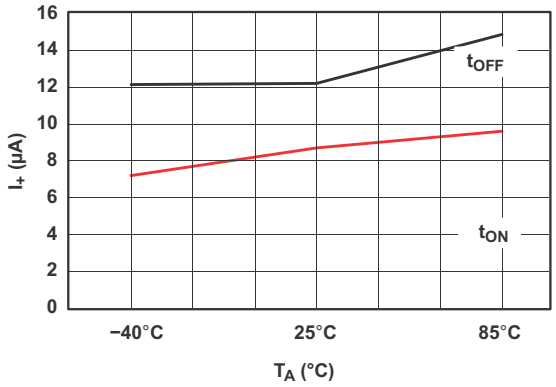


Figure 9. I_+ vs Temperature

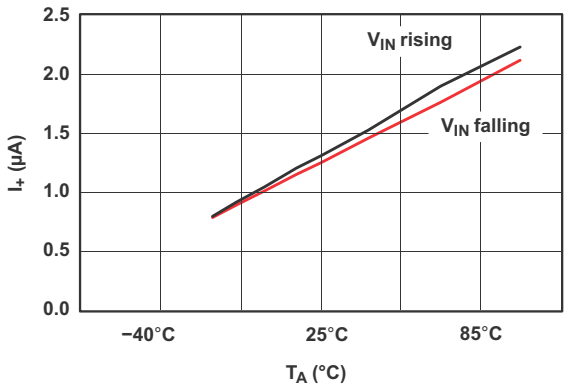


Figure 10. I_+ vs Temperature

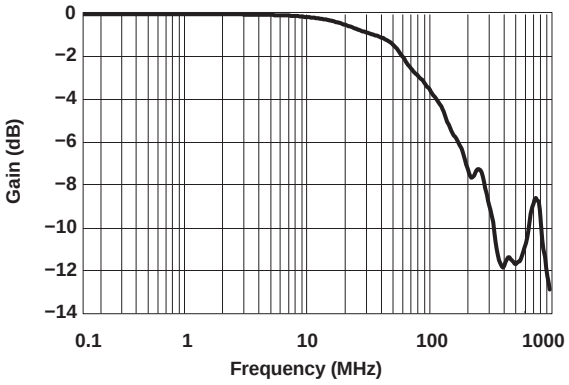


Figure 11. Bandwidth (V_+ = 5 V)

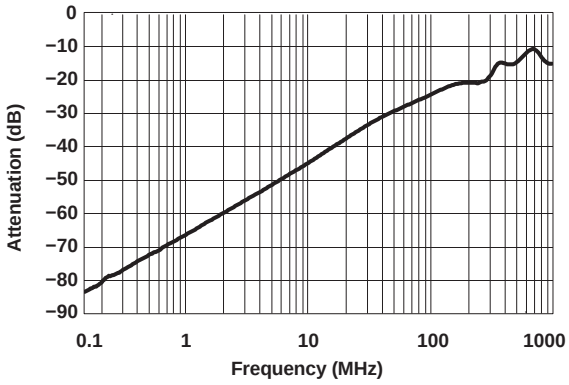


Figure 12. Attenuation vs Frequency

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Typical Characteristics (continued)

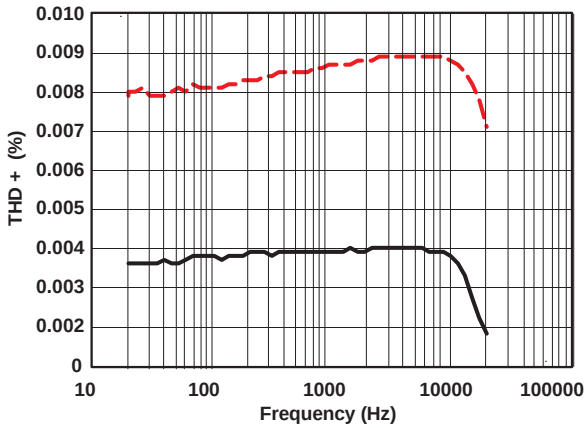


Figure 13. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

7 Parameter Measurement Information

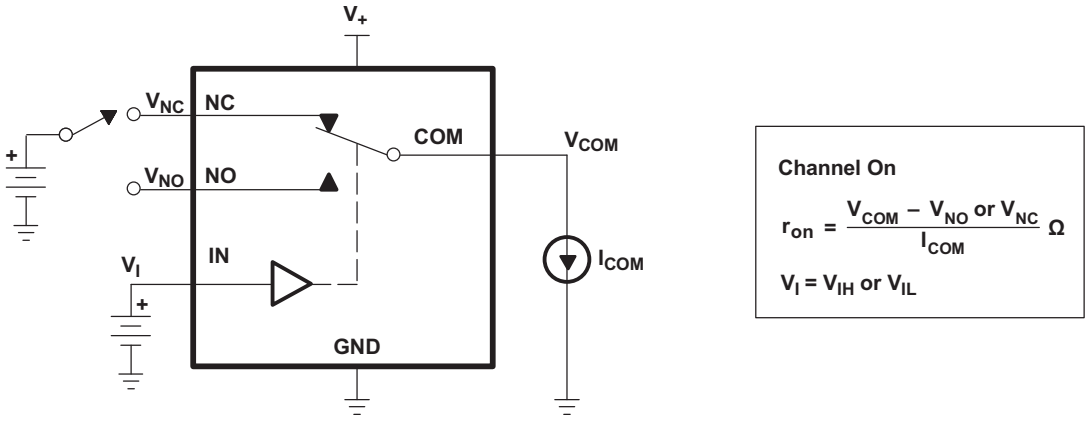


Figure 14. ON-State Resistance (r_{on})

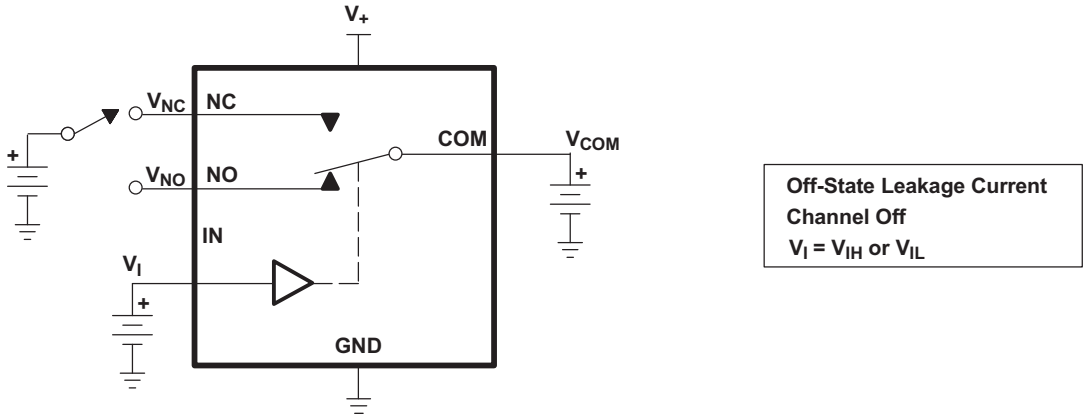


Figure 15. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

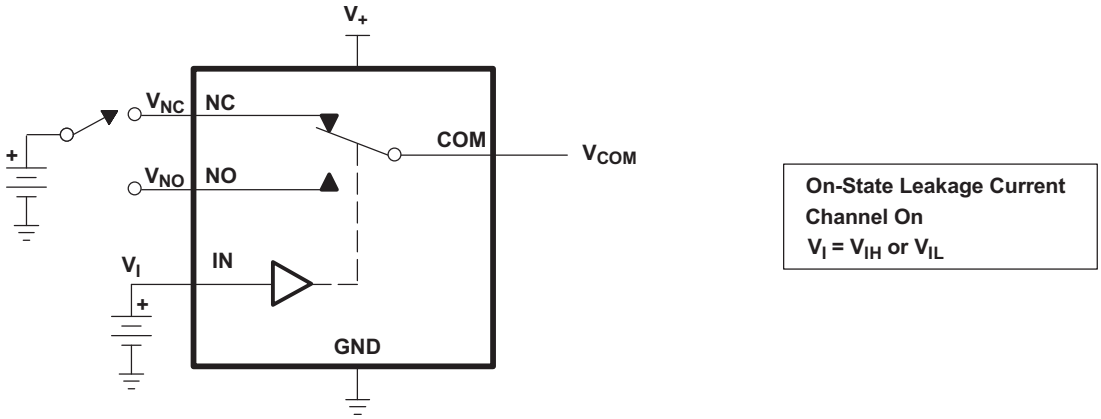


Figure 16. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

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Parameter Measurement Information (continued)

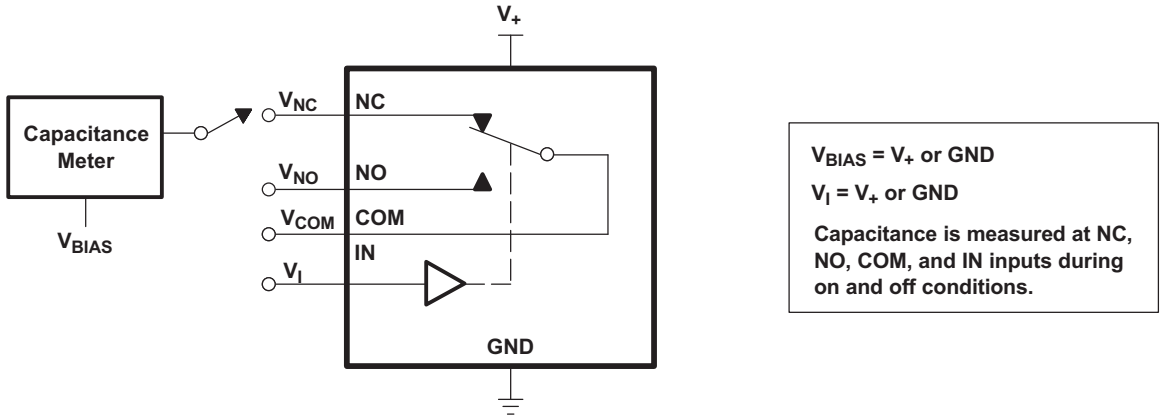
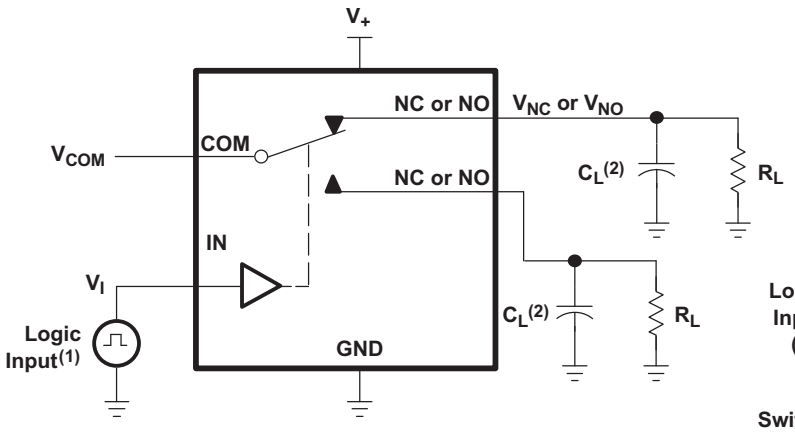
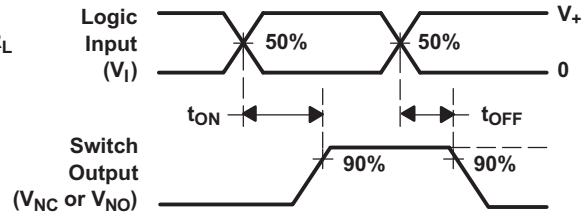


Figure 17. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

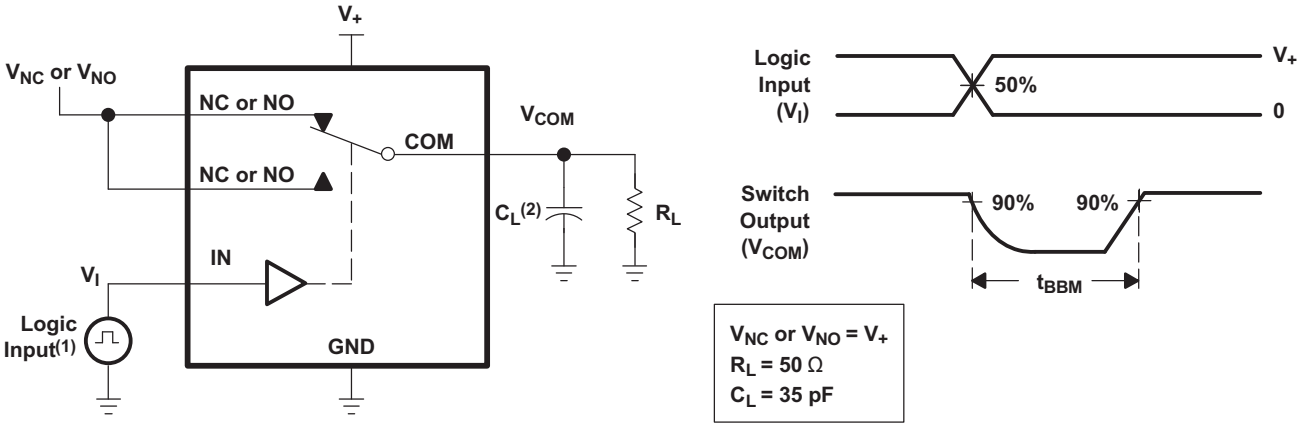


(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 18. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

Parameter Measurement Information (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 19. Break-Before-Make Time (t_{BBM})

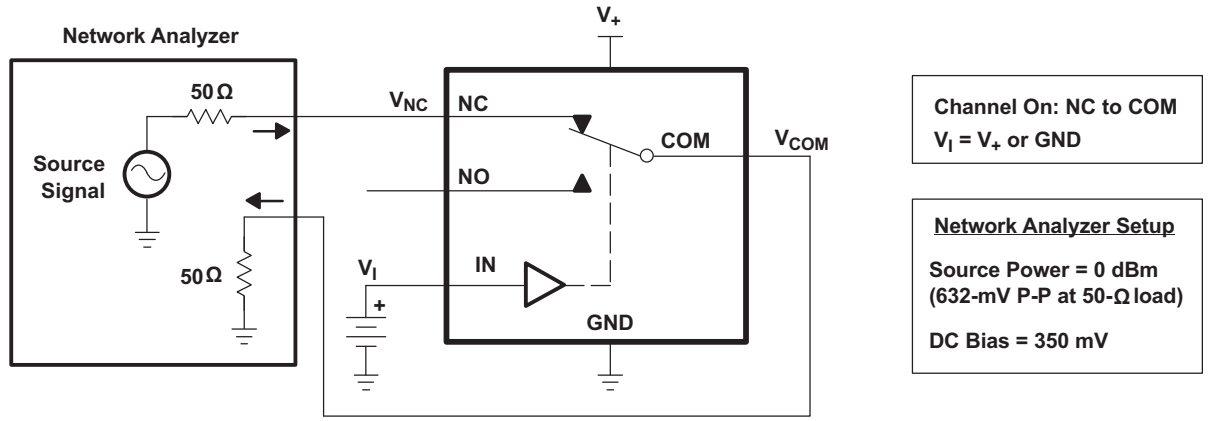


Figure 20. Bandwidth (BW)

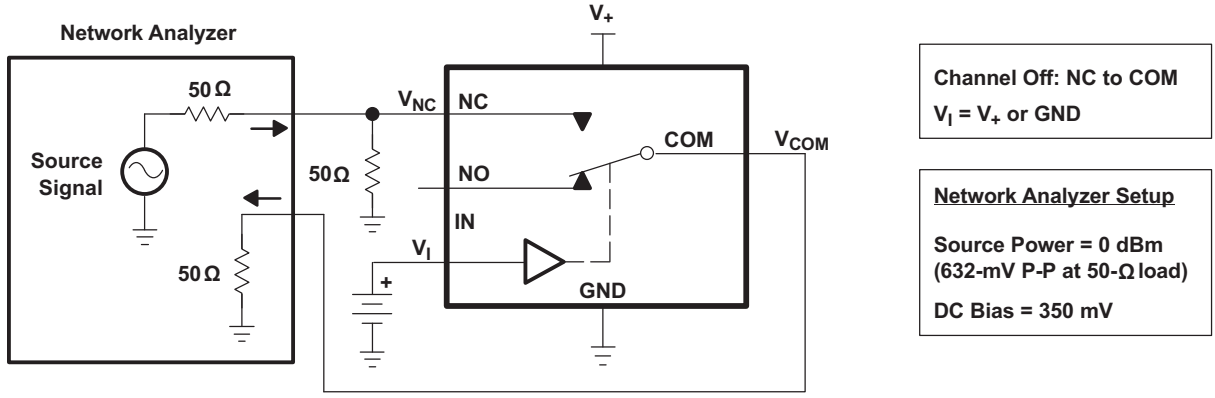


Figure 21. OFF Isolation (O_{ISO})

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Parameter Measurement Information (continued)

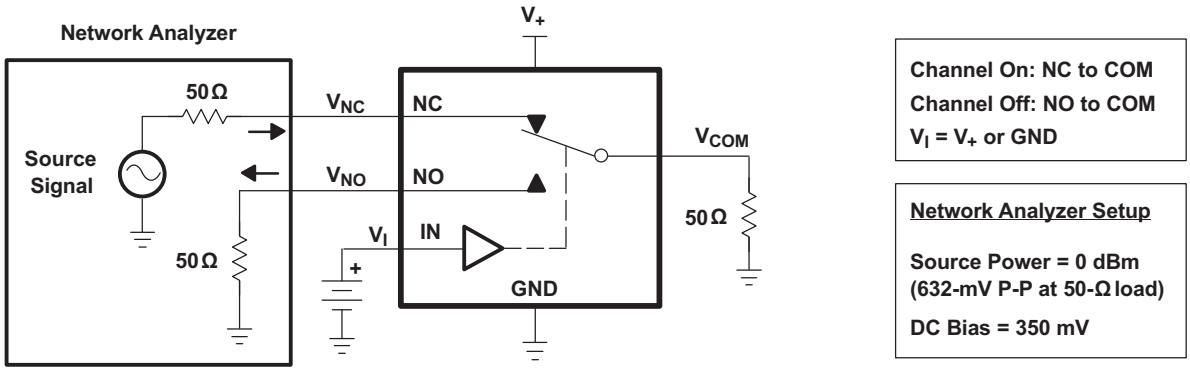
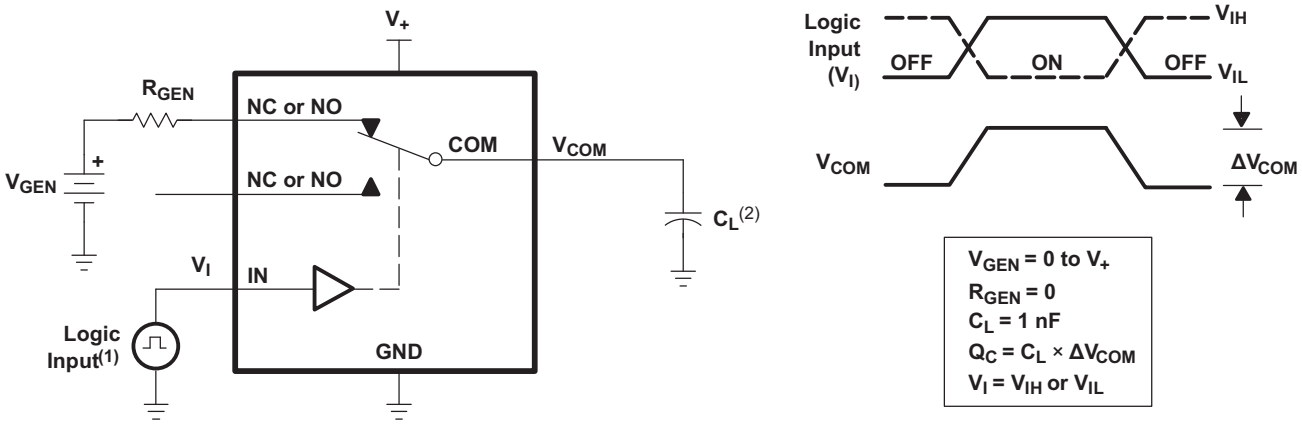


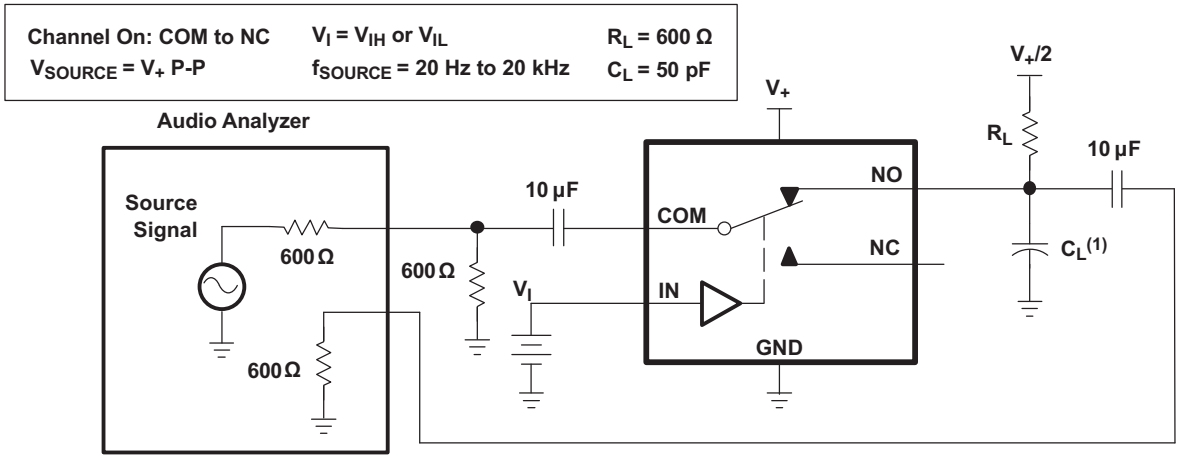
Figure 22. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 23. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)

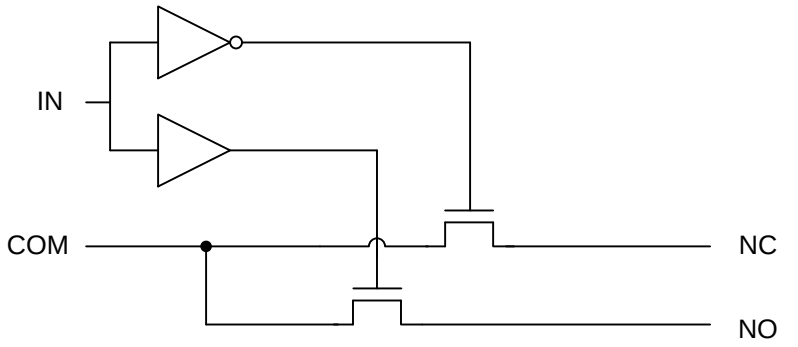
8 Detailed Description

8.1 Overview

The TS5A3159A is a single-pole-double-throw (SPDT) solid-state analog switch. The TS5A3159A, like all analog switches, is bidirectional. When powered on, each COM pin is connected to the NC pin. For this device, NC stands for *normally closed* and NO stands for *normally open*. If IN is low, COM is connected to NC. If IN is high, COM is connected to NO.

The TS5A3159A is a break-before-make switch. This means that during switching, a connection is broken before a new connection is established. The NC and NO pins are never connected to each other.

8.2 Functional Block Diagram



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8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3159A make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TS5A3159A.

Table 1. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3159A can be used in a variety of customer systems. The TS5A3159A can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

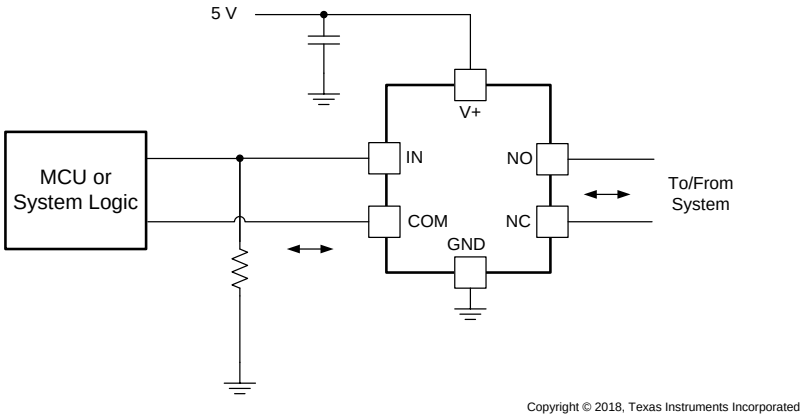


Figure 25. System Schematic for TS5A3159A

9.2.1 Design Requirements

In this particular application, V_+ was 5 V, although V_+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, IN is, by default, pulled low to GND. Choose the resistor size based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

9.2.3 Application Curve

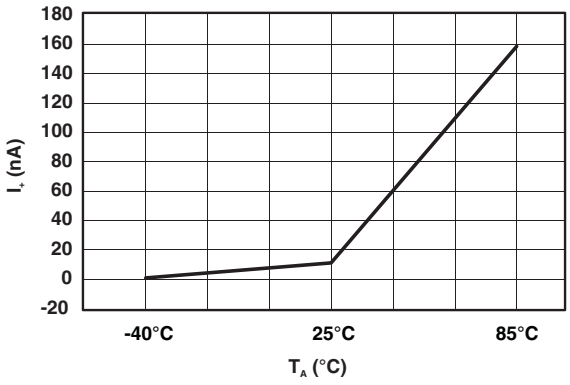


Figure 26. Power-Supply Current vs Temperature (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the VCC pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Figure 27 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN pin must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states.

11.2 Layout Example

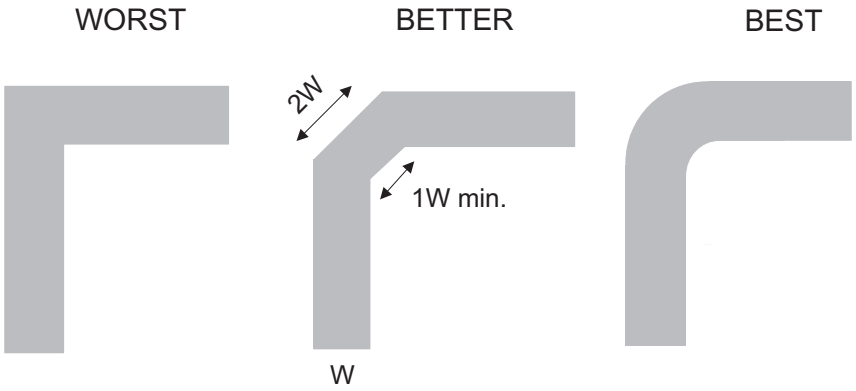


Figure 27. Trace Example

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 2. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is on
r_{peak}	Peak ON-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the off state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the off state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the on state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the on state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the on state and the output (NC or NO) being open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at (IN)
I_{IH}, I_{IL}	Leakage current measured at (IN)
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal when the switch is turning on.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal when the switch is turning off.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance and ΔV_O is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is off
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is off
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is on
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is on
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is on
C_{IN}	Capacitance of (IN)
O_{ISO}	OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the off state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an on channel to an off channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.

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Table 2. Parameter Description (continued)

SYMBOL	DESCRIPTION
BW	Bandwidth of the switch. This is the frequency in which the gain of an on channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio or root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power supply current with the control (IN) terminal at V_+ or GND

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3159ADBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAJR JAJH
TS5A3159ADBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JAJR JAJH
TS5A3159ADBVT	Obsolete	Production	SOT-23 (DBV) | 6	-	-	Call TI	Call TI	-40 to 85	(JAJK, JAJR) JAJH
TS5A3159ADCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JJK, JJR) JJH
TS5A3159ADCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JJK, JJR) JJH
TS5A3159ADCKT	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 85	(JJK, JJR) JJH
TS5A3159AYZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JJN
TS5A3159AYZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JJN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

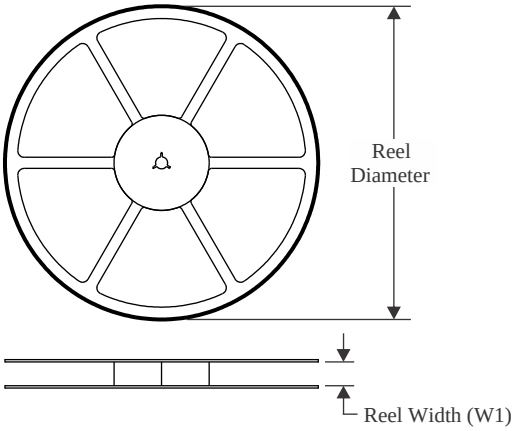
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

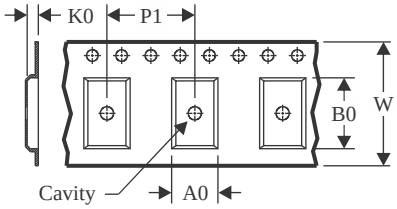
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

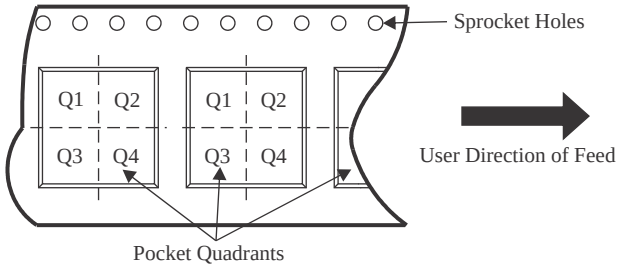


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

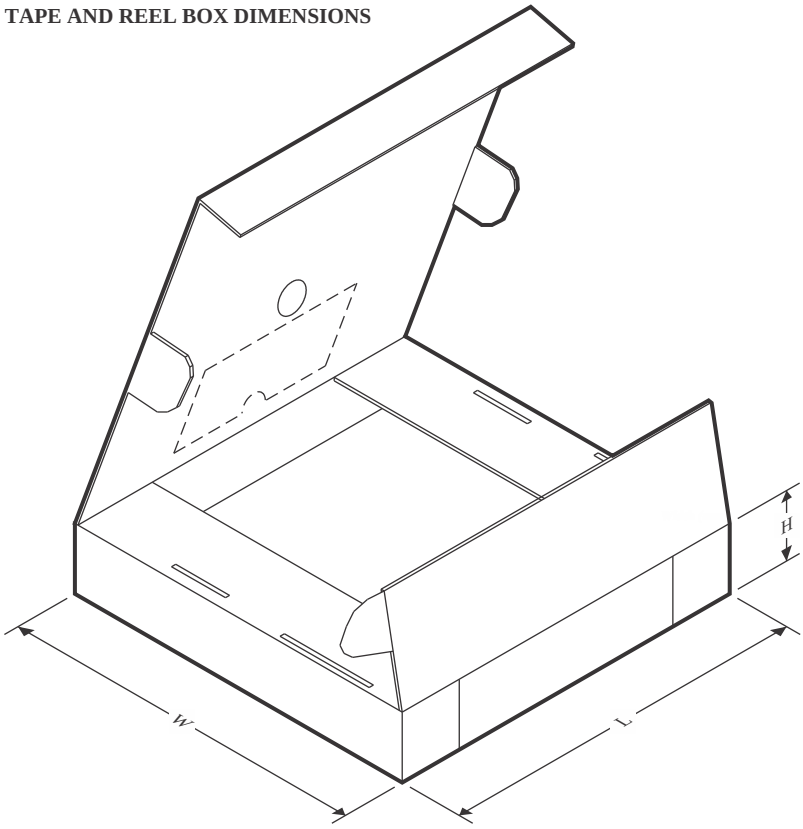
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159ADBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3159ADCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TS5A3159ADCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TS5A3159AYZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

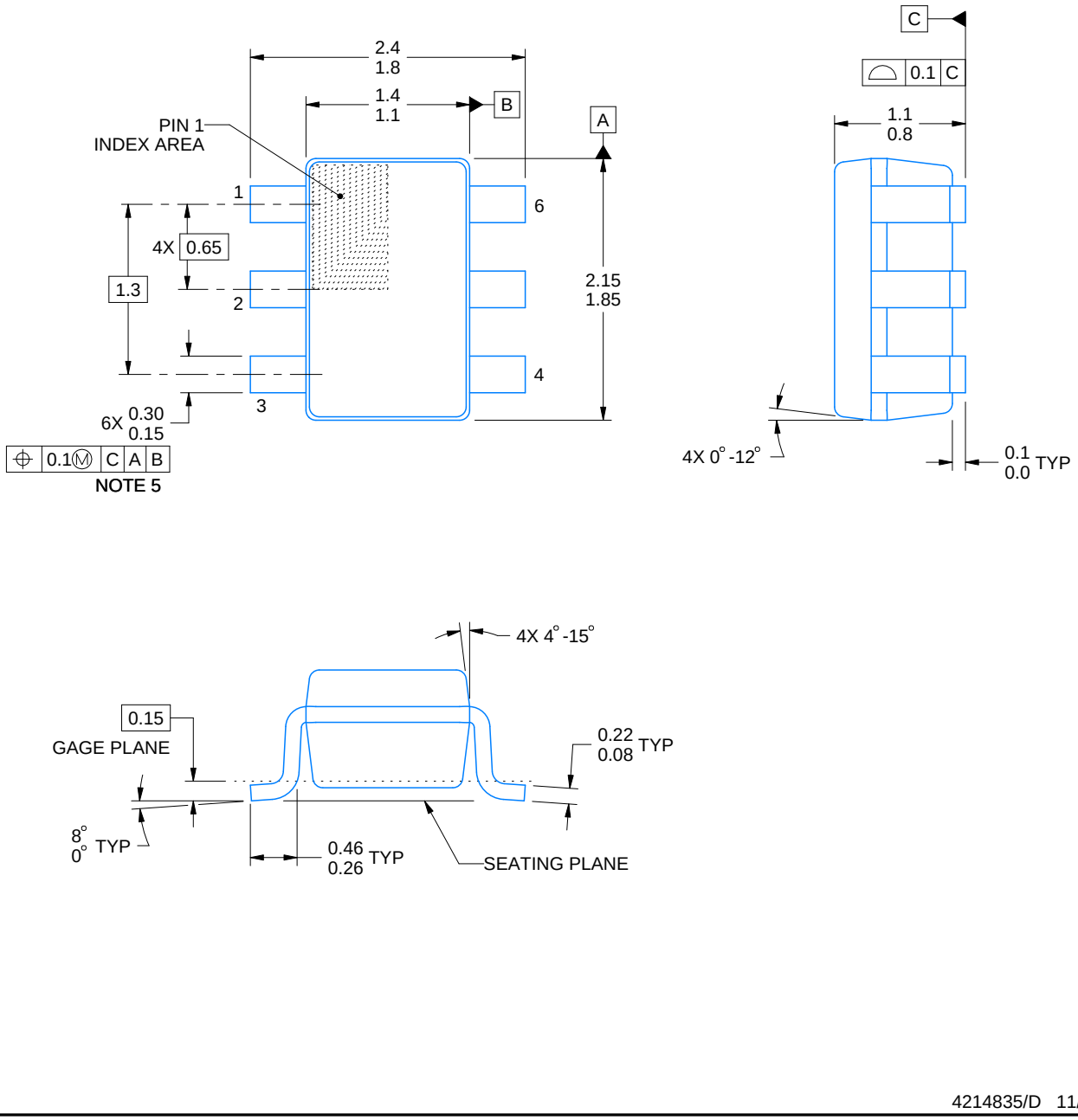
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3159ADBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TS5A3159ADCKR	SC70	DCK	6	3000	202.0	201.0	28.0
TS5A3159ADCKR	SC70	DCK	6	3000	205.0	200.0	33.0
TS5A3159AYZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

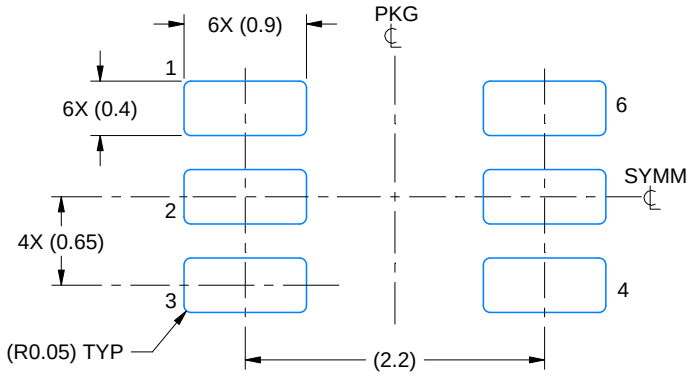
SMALL OUTLINE TRANSISTOR



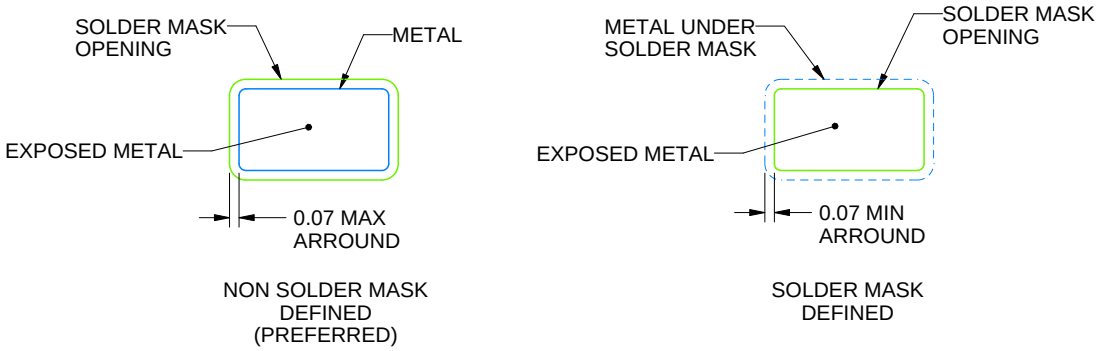
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

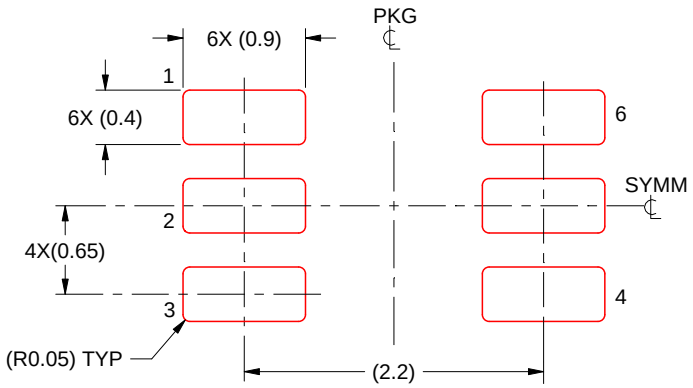


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

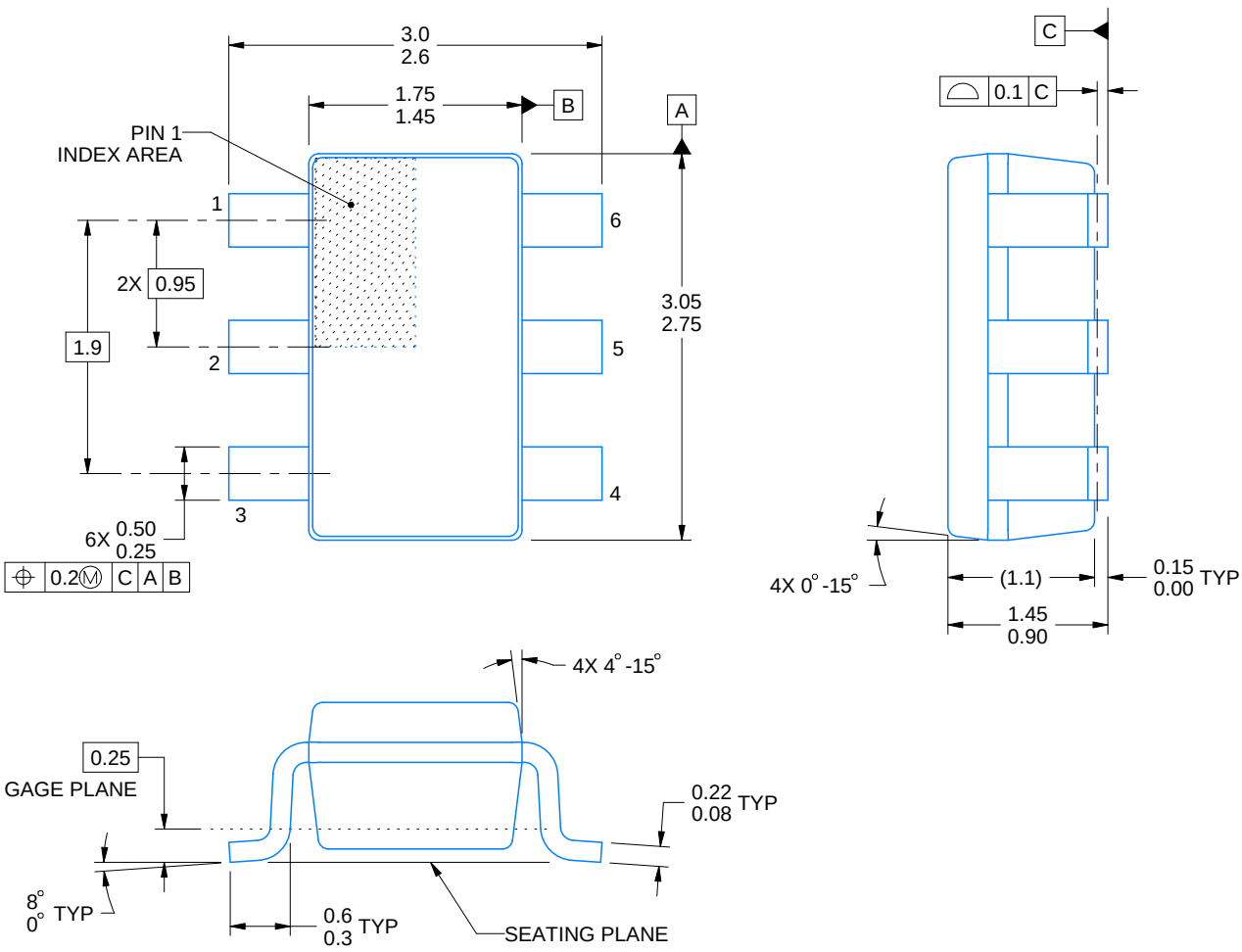
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

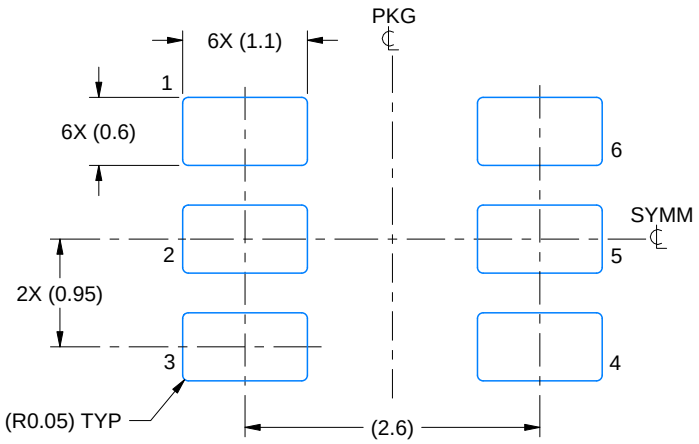
SMALL OUTLINE TRANSISTOR



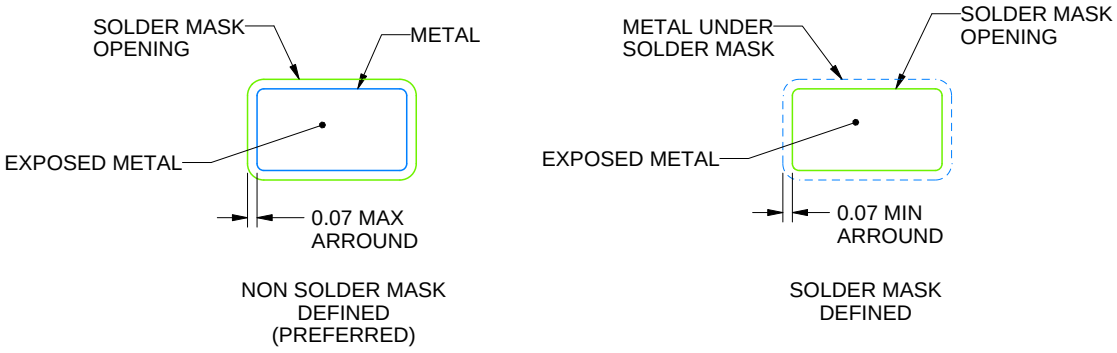
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

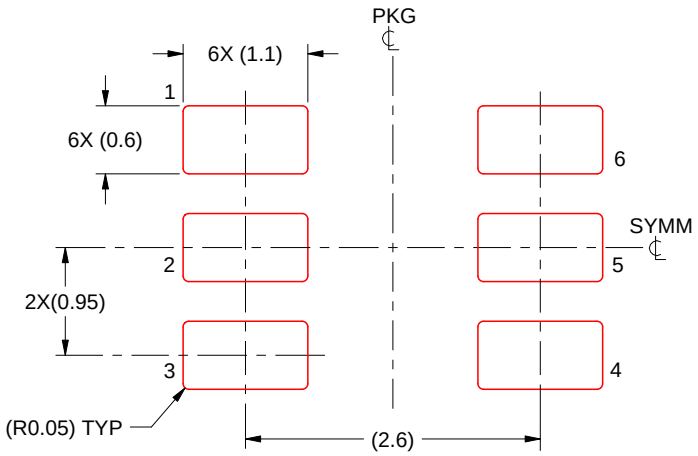


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

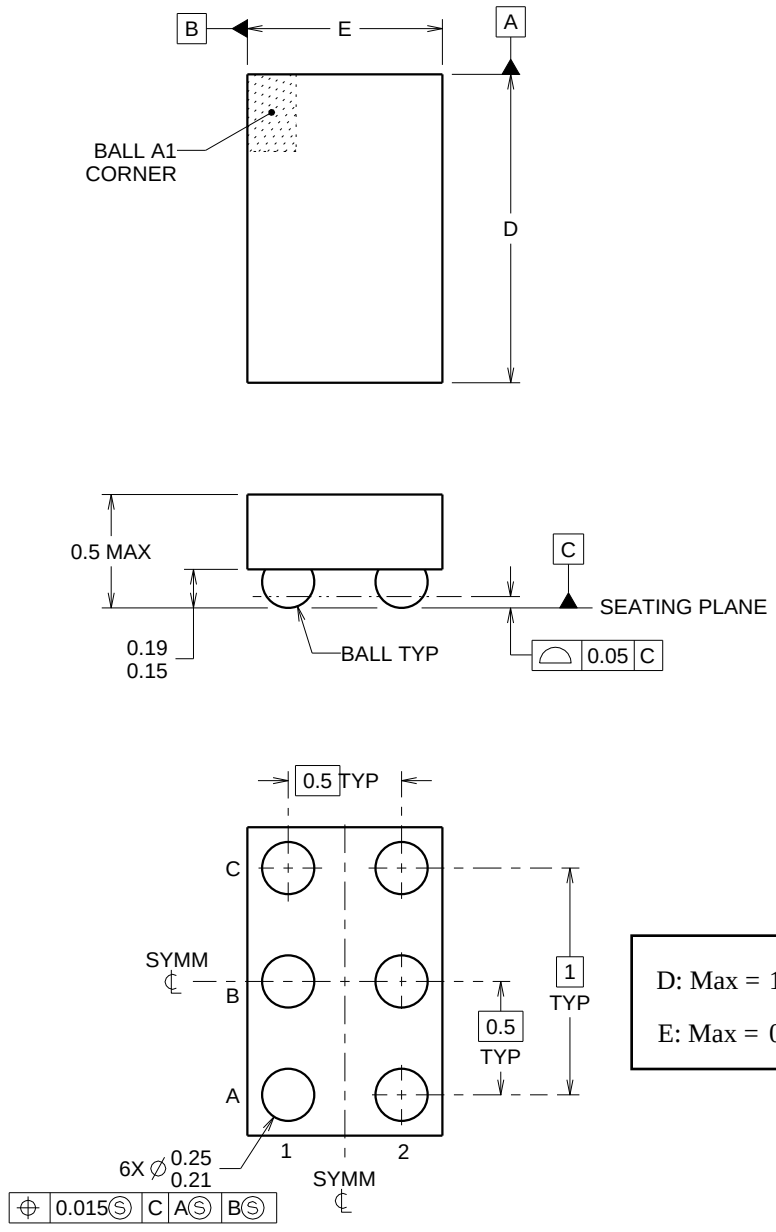
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.358 mm

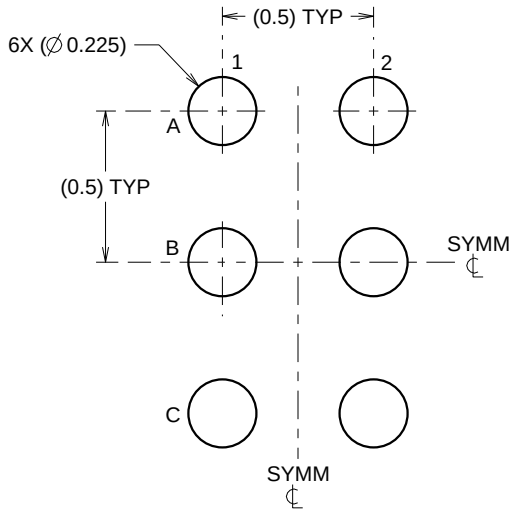
E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

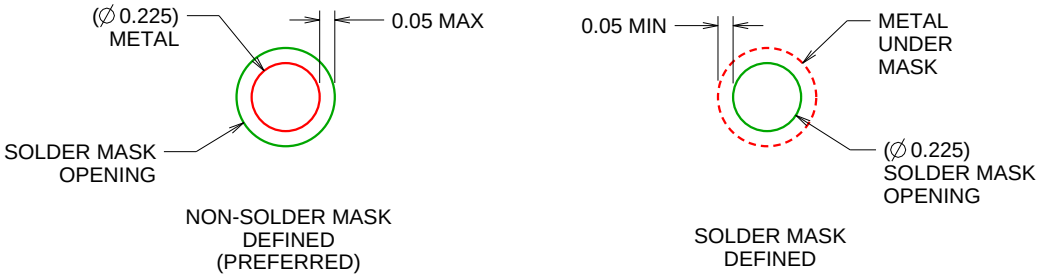
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X

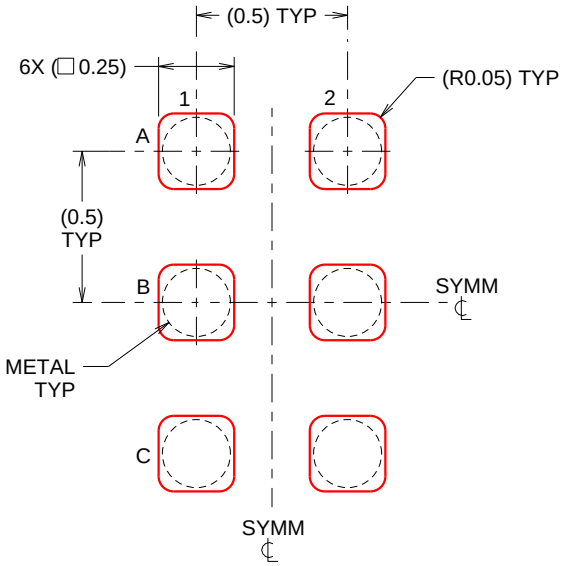


SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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