TS5A3359 1-Ω SP3T Bidirectional Analog Switch 5-V/3.3-V Single-Channel 3:1 Multiplexer and Demultiplexer

1 Features

- Isolation in power-down mode, V_{CC} = 0
- Specified break-before-make switching
- Low ON-state resistance (1 Ω)
- Control inputs are 5.5 V tolerant
- Low charge injection (5 pC V_{CC} = 1.8 V)
- Excellent ON-state resistance matching
- Low total harmonic distortion (THD)
- 1.65 V to 5.5 V single-supply operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22
  - 2000-V human-body model (A114-B, Class II)
  - 1000-V charged-device model (C101)

2 Applications

- Cell phones
- PDAs
- Portable instrumentation
- Audio and video signal routing
- Low-voltage data acquisition systems
- Communication circuits
- Modems
- Hard drives
- Computer peripherals
- Wireless terminals and peripherals

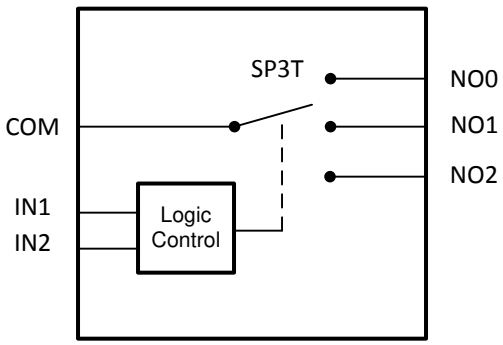
3 Description

The TS5A3359 device is a bidirectional, single channel, single-pole triple-throw (SP3T) analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3359 suitable for a wide range of applications in various markets including personal electronics, test and measurement equipment, and portable instrumentation. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS5A3359 device also has a specified break-before-make feature. The device consumes very low power and provides isolation when V_{CC} = 0.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3359	US8 (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.25 mm × 2.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2016) to Revision F (December 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the body size for the DSBGA (8) package in the *Device Information* table	1

Changes from Revision D (May 2015) to Revision E (January 2016)	Page
• Added T_J Junction Temperature to the *Absolute Maximum Ratings*	4
• Changed Input leakage current UNIT value From: µA To: nA in *Electrical Characteristics for 5-V Supply*	5

Changes from Revision C (June 2008) to Revision D (May 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed YZP pinout numbering	3

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5 Pin Configuration and Functions

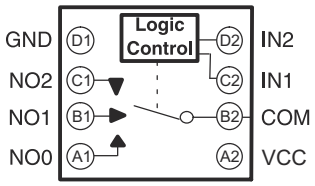


Figure 5-1. YZP Package 8-Pin DSBGA Bottom View

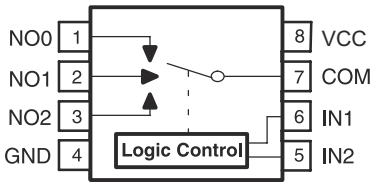


Figure 5-2. DCU Package 8-Pin US8 Top View

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	DCU	YZP		
NO0	1	A1	I/O	Normally open
NO1	2	B1	I/O	Normally open
NO2	3	C1	I/O	Normally open
GND	4	D1	—	Ground
IN2	5	D2	I	Digital control to connect COM to NO
IN1	6	C2	I	Digital control to connect COM to NO
COM	7	B2	I/O	Common
VCC	8	A2	—	Power supply

(1) I = input, O = output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage(3) (4) (5)		–0.5	V_{CC} + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0	–50		mA
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_{CC}	–200	200	mA
			–400	400	
V_I	Digital input voltage(3) (4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Analog voltage	1.65	5.5	V
V_{NO} V_{COM}		0	V_{CC}	V
V_I	Digital input voltage	0	V_{CC}	V

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6.4 Thermal Information

THERMAL METRIC[1]		TS5A3359		UNIT
		DCU (US8)	YZP (DSBGA)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.2	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.2	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.9	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.5	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C	4.5 V		0.8	1.1	Ω
				Full				1.5	
ON-state resistance	r_{on}	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C	4.5 V		0.7	0.9	Ω
				Full				1.1	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C	4.5 V		0.1	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C	4.5 V		0.15		Ω
		V_{NO} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C			0.1	0.25	
				Full				0.25	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V or 4.5 V, V_{COM} = 1 V to 4.5 V,	Switch OFF, See Figure 7-2	25°C	5.5 V	–20	5	20	nA
				Full		–150		150	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See Figure 7-2	25°C	0 V	–1	0.8	1	μA
				Full		–25		25	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V or 4.5 V, V_{COM} = Open,	Switch ON, See Figure 7-2	25°C	5.5 V	–30	5	30	nA
				Full		–220		220	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 4.5 V or 1 V, V_{COM} = 1 V or 4.5 V,	Switch OFF, See Figure 7-2	25°C	5.5 V	–25	8	25	nA
				Full		–250		250	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 5.5 V, V_{NO} = 5.5 V to 0,	Switch OFF, See Figure 7-2	25°C	0 V	–8	0.1	8	μA
				Full		–50		50	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 1 V or 4.5 V,	Switch ON, See Figure 7-2	25°C	5.5 V	–30	5	30	nA
				Full		–220		220	
DIGITAL CONTROL INPUTS (IN1, IN2)[2]									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	–2		2	nA
				Full		–20		20	

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6.5 Electrical Characteristics for 5-V Supply (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	5 V	1	2.5	21	ns
				Full	4.5 V to 5.5 V	1		23.5	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	5 V	1	6	10.5	ns
				Full	4.5 V to 5.5 V	1		12	
Break-before-make time	t_{BBM}	V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-6	25°C	5 V	0.5	8.5	18	ns
				Full	4.5 V to 5.5 V	0.5		23	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 7-10	25°C	5 V		20		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 7-4	25°C	5 V		18		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND, Switch OFF,	See Figure 7-4	25°C	2.5 V		54		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND, Switch ON,	See Figure 7-4	25°C	5 V		78		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC}or GND, Switch ON,	See Figure 7-4	25°C	5 V		78		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 7-4	25°C	5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 7-7	25°C	5 V		75		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz ,	Switch OFF, See Figure 7-8	25°C	5 V		–64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz ,	Switch ON, See Figure 7-9	25°C	5 V		–64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 7-11	25°C	5 V		0.005%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	5.5 V		16	50	nA
				Full				1200	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.6 Electrical Characteristics for 3.3-V Supply

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C	3 V		1.3	1.6	Ω
				Full				2	
ON-state resistance	r_{on}	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C	3 V		1.2	1.6	Ω
				Full				1.8	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C	3 V		0.1	0.15	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C	3 V		0.2		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 7-1	25°C			0.2	0.35	
				Full				0.35	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V or 3 V, V_{COM} = 1 V to 3 V,	Switch OFF, See Figure 7-2	25°C	3.6 V	–15	3	15	nA
				Full		–30		30	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See Figure 7-2	25°C	0 V	–1	0.2	1	µA
				Full		–10		10	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V or 3 V, V_{COM} = Open,	Switch ON, See Figure 7-2	25°C	3.6 V	–15	3	15	nA
				Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 0 V to 3.6 V, V_{COM} = 1 V or V_{NO} = 3.6 V to 0, V_{COM} = 3 V,	Switch OFF, See Figure 7-2	25°C	3.6 V	–15	3	15	nA
				Full		–75		75	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NO} = 3.6 V to 0,	Switch OFF, See Figure 7-2	25°C	0 V	–1	0.2	1	µA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 1 V or 3 V,	Switch ON, See Figure 7-2	25°C	3.6 V	–15	4	15	nA
				Full		–40		40	
DIGITAL CONTROL INPUTS (IN1, IN2)[2]									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–2		2	nA
				Full		–20		20	

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6.6 Electrical Characteristics for 3.3-V Supply (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	3.3 V	1	16	30.5	ns
				Full	3 V to 3.6 V	1		34	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	3.3 V	1	6	11.5	ns
				Full	3 V to 3.6 V	1		12.5	
Break-before-make time	t_{BBM}	V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-6	25°C	3.3 V	0.5	13	26	ns
				Full	3 V to 3.6 V	0.5		30	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 7-10	25°C	3.3 V		12		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 7-4	25°C	3.3 V		18		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND, Switch OFF,	See Figure 7-4	25°C	3.3 V		55		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND, Switch ON,	See Figure 7-4	25°C	3.3 V		78		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 7-4	25°C	3.3 V		78		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 7-4	25°C	3.3 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 7-7	25°C	3.3 V		73		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 7-8	25°C	3.3 V		–64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 7-9	25°C	3.3 V		–64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 7-11	25°C	3.3 V		0.01%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	3.6 V		2	20	nA
				Full				350	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.7 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See Figure 7-1	25°C	2.3 V		1.8	2.5	Ω
				Full				2.7	
ON-state resistance	r_{on}	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 7-1	25°C	2.3 V		1.5	2	Ω
				Full				2.4	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 7-1	25°C	2.3 V			0.2	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –8 mA,	Switch ON, See Figure 7-1	25°C	2.3 V		0.6		Ω
		V_{NO} = 0.8 V, 1.8 V I_{COM} = –8 mA,	Switch ON, See Figure 7-1	25°C			0.6	1	
				Full				1	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0.5 V or 2.3 V, V_{COM} = 0.5 V to 2.3 V,	Switch OFF, See Figure 7-2	25°C	2.7 V	–15	3	15	nA
				Full		–30		30	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,	Switch OFF, See Figure 7-2	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.5 V or 2.3 V, V_{COM} = Open,	Switch ON, See Figure 7-2	25°C	2.7 V	–15	3	15	nA
				Full		–35		35	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 0.3 V to 2.3 V, V_{COM} = 0.5 V or 2.3 V,	Switch OFF, See Figure 7-2	25°C	2.7 V	–15	3	15	nA
				Full		–60		60	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 2.7 V, V_{NO} = 2.7 V to 0,	Switch OFF, See Figure 7-2	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0.5 V or 2.2 V,	Switch ON, See Figure 7-2	25°C	2.7 V	–15	3.5	15	nA
				Full		–40		40	
DIGITAL CONTROL INPUTS (IN1, IN2)[2]									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	1		1	nA
				Full		10		10	

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6.7 Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	2.5 V	2	4.5	43	ns
				Full	2.3 V to 2.7 V	2		47.5	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	2.5 V	2	8.5	11	ns
				Full	2.3 V to 2.7 V	2		12.5	
Break-before-make time	t_{BBM}	V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-6	25°C	2.5 V	0.5	18.5	38.5	ns
				Full	2.3 V to 2.7 V	0.5		43	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 7-10	25°C	2.5 V		8		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 7-4	25°C	2.5 V		18.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND, Switch OFF,	See Figure 7-4	25°C	2.5 V		55		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND, Switch ON,	See Figure 7-4	25°C	2.5 V		78		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 7-4	25°C	2.5 V		78		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 7-4	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 7-7	25°C	2.5 V		73		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 7-8	25°C	2.5 V		–64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 7-9	25°C	2.5 V		–64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 7-11	25°C	2.5 V		0.03%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	2.7 V		1	10	nA
				Full				250	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.8 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –2 mA,	Switch ON, See Figure 7-1	25°C	1.65 V		5		Ω
				Full				30	
ON-state resistance	r_{on}	V_{NO} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 7-1	25°C	1.65 V		2	2.5	Ω
				Full				3.5	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 7-1	25°C	1.65 V		0.15	0.4	Ω
				Full				0.4	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –2 mA,	Switch ON, See Figure 7-1	25°C	1.65 V		5		Ω
		V_{NO} = 0.6 V, 1.5 V I_{COM} = –2 mA,	Switch ON, See Figure 7-1	25°C			4.5		
				Full			5		
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} =0.3 V or 1.65 V, V_{COM} = 0.3 V to 1.65 V,	Switch OFF, See Figure 7-2	25°C	1.95 V	–15	3	15	nA
				Full		–30		30	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch OFF, See Figure 7-2	25°C	0 V	–1	0.1	1	µA
				Full		–15		15	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} =0.3 V or 1.65 V, V_{COM} = Open,	Switch ON, See Figure 7-2	25°C	1.95 V	–15	3	15	nA
				Full		–30		30	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 0.3 V to 1.65 V, V_{COM} =0.3 V or 1.65 V,	Switch OFF, See Figure 7-2	25°C	1.95 V	–15	3	15	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 1.95 V, V_{NO} = 1.95 V to 0,	Switch OFF, See Figure 7-2	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0.3 V or 1.65 V,	Switch ON, See Figure 7-2	25°C	1.95 V	–15	3	15	nA
				Full		–30		30	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	–2		2	nA
				Full		–20		20	

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6.8 Electrical Characteristics for 1.8-V Supply (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	1.8 V	3	38.5	85	ns
				Full	1.65 V to 1.95 V	3		90	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-5	25°C	1.8 V	2	8.5	16	ns
				Full	1.65 V to 1.95 V	2		18	
Break-before-make time	t_{BBM}	V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 7-6	25°C	1.8 V	1	33	75	ns
				Full	1.65 V to 1.95 V	1		80	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 7-10	25°C	1.8 V		5		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 7-4	25°C	1.8 V		18.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND, Switch OFF,	See Figure 7-4	25°C	1.8 V		55		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND, Switch ON,	See Figure 7-4	25°C	1.8 V		78		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 7-4	25°C	1.8 V		78		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 7-4	25°C	1.8 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 7-7	25°C	1.8 V		73		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 M Hz ,	Switch OFF, See Figure 7-8	25°C	1.8 V		–64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 7-9	25°C	1.8 V		–64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 7-11	25°C	1.8 V		0.08%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	1.95 V		1		nA
				Full				200	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

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6.9 Typical Characteristics

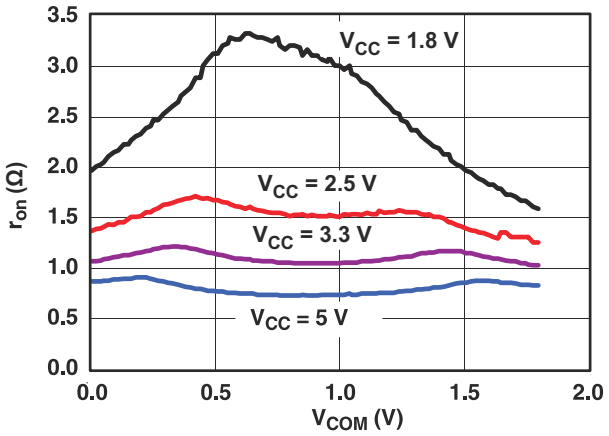


Figure 6-1. R_{on} vs V_{COM}

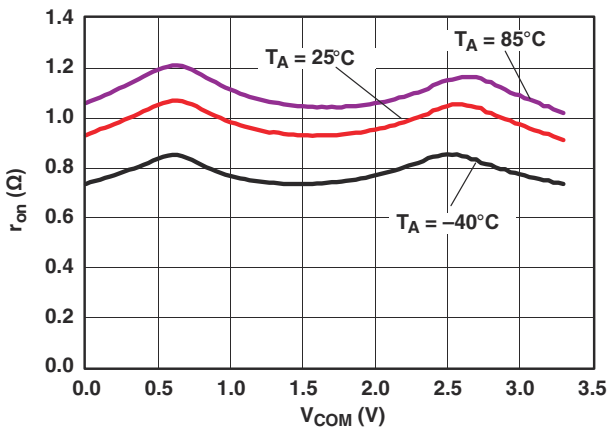


Figure 6-2. R_{on} vs V_{COM} Over Temperature (V_{CC} = 3.3 V)

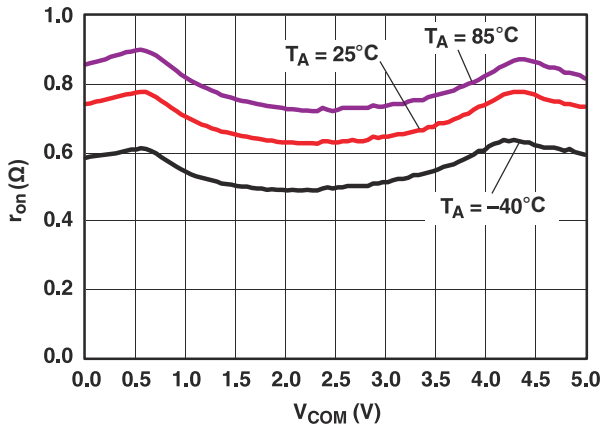


Figure 6-3. R_{on} vs V_{COM} Over Temperature(V_{CC} = 5 V)

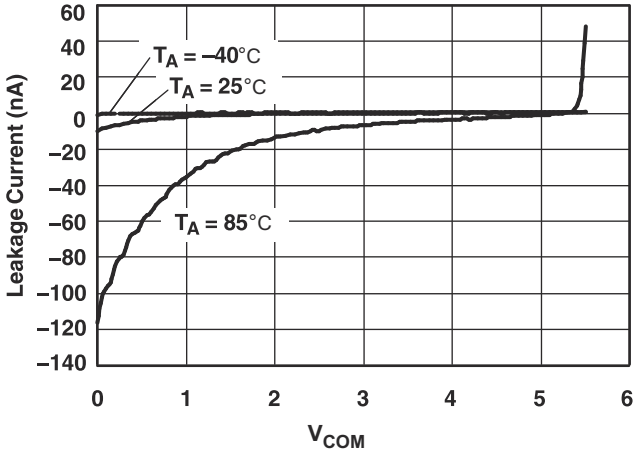


Figure 6-4. $I_{COM(OFF)}$Leakage Current vs V_{COM} Over Temperature (V_{CC} = 5 V)

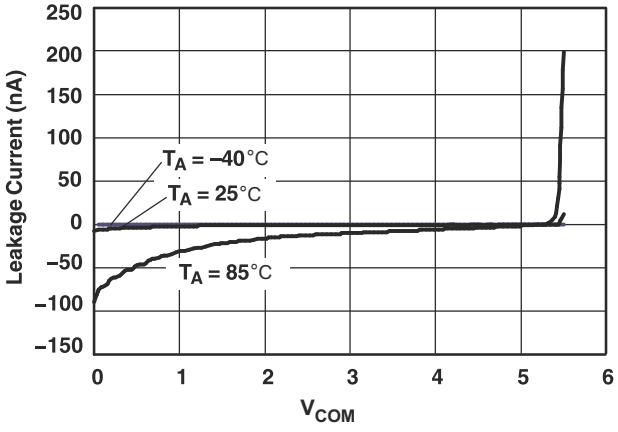


Figure 6-5. $I_{NO(OFF)}$Leakage Current vs V_{COM} Over Temperature (V_{CC} = 5 V)

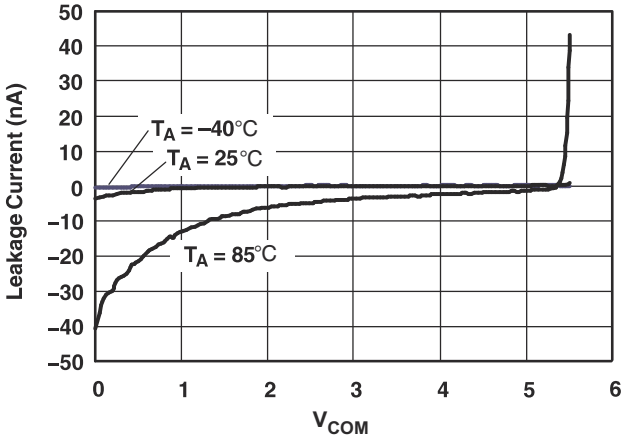


Figure 6-6. $I_{COM(ON)}$Leakage Current vs V_{COM} Over Temperature (V_{CC} = 5 V)

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6.9 Typical Characteristics (continued)

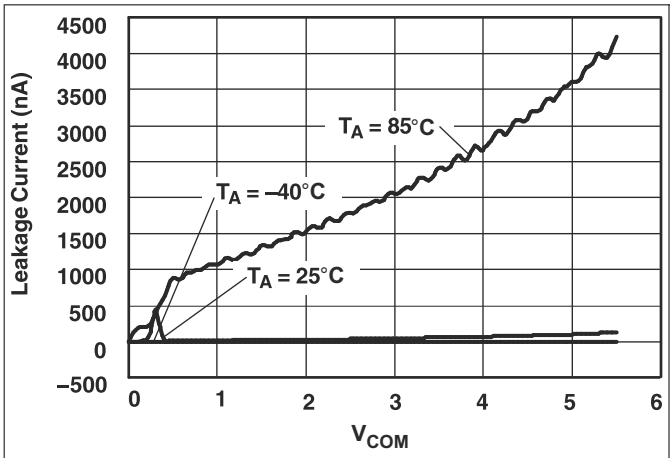


Figure 6-7. $I_{COM(PWROFF)}$ Leakage Current vs V_{COM} Over Temperature (V_{CC} = 0 V)

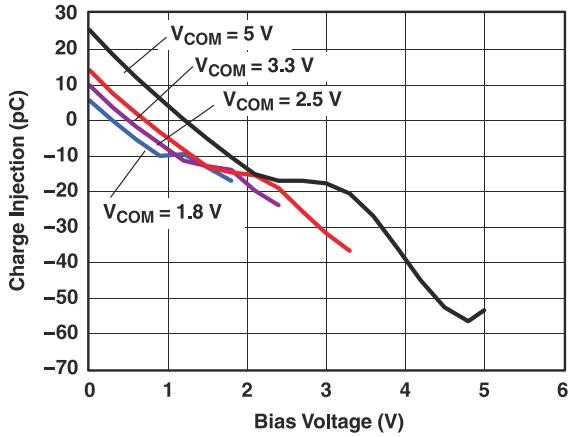


Figure 6-8. Charge Injection (Q_C) vs V_{COM}

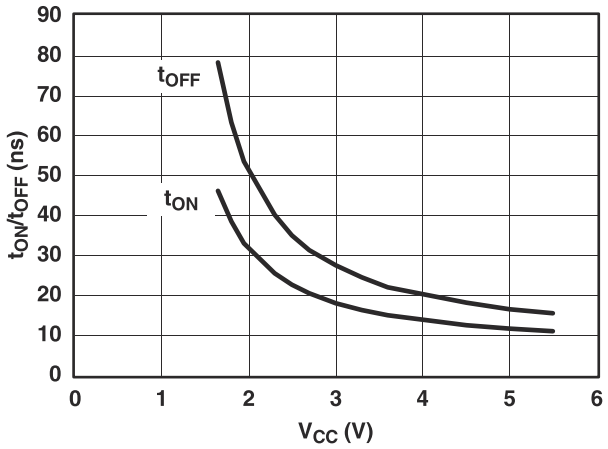


Figure 6-9. t_{ON} and t_{OFF} vs Supply Voltage

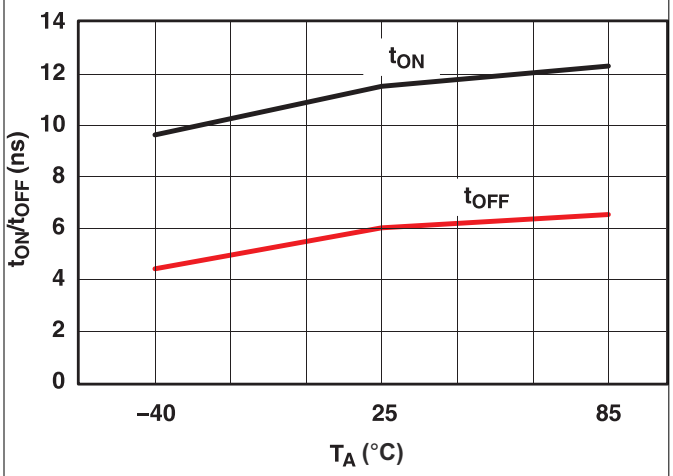


Figure 6-10. T_{ON} and T_{OFF} vs Temperature

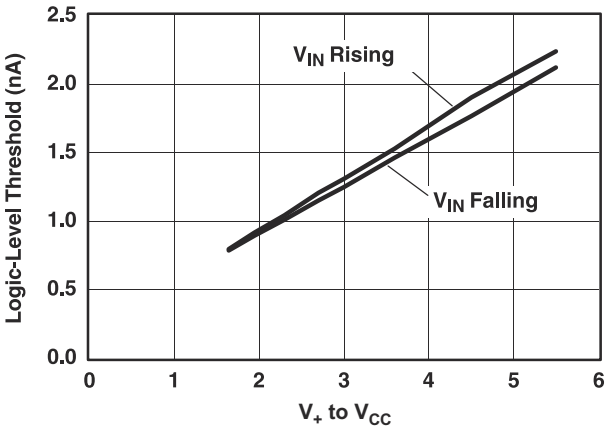


Figure 6-11. Logic-Level Threshold vs V_{CC}

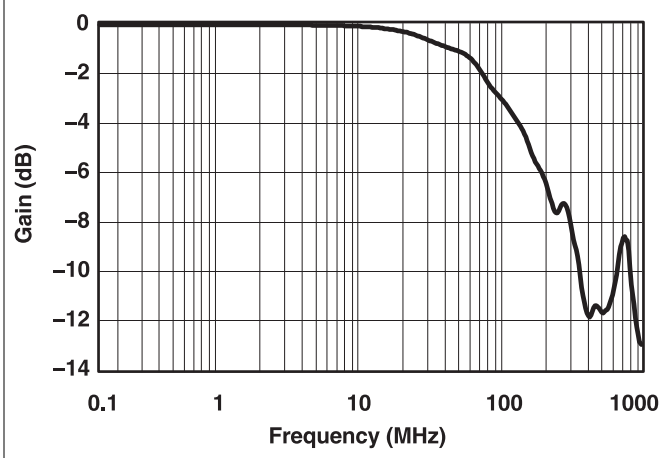


Figure 6-12. Bandwidth (V_{CC} = 5 V)

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6.9 Typical Characteristics (continued)

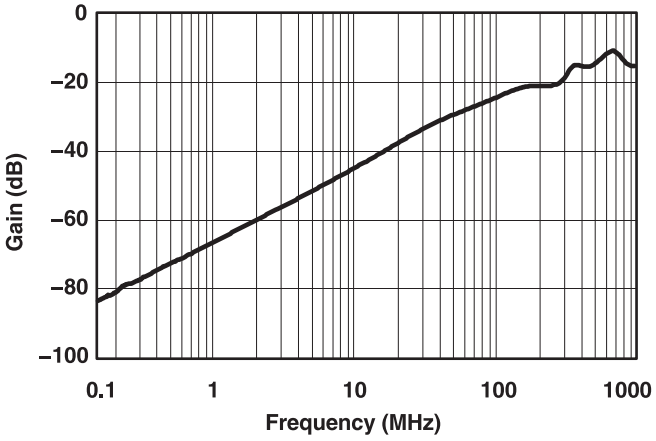


Figure 6-13. Off Isolation (V_{CC} = 5 V)

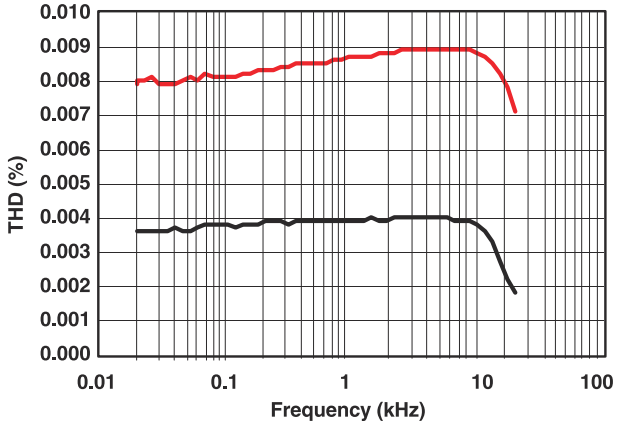


Figure 6-14. Total Harmonic Distortion vs Frequency (V_{CC} = 5 V)

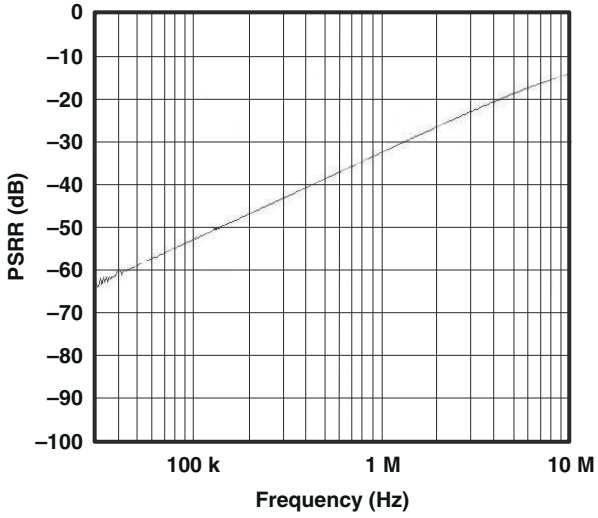


Figure 6-15. Com Port to No2 PSRR, In1 = V_{CC}, In2 = V_{CC} (V_{CC} = 5 V)

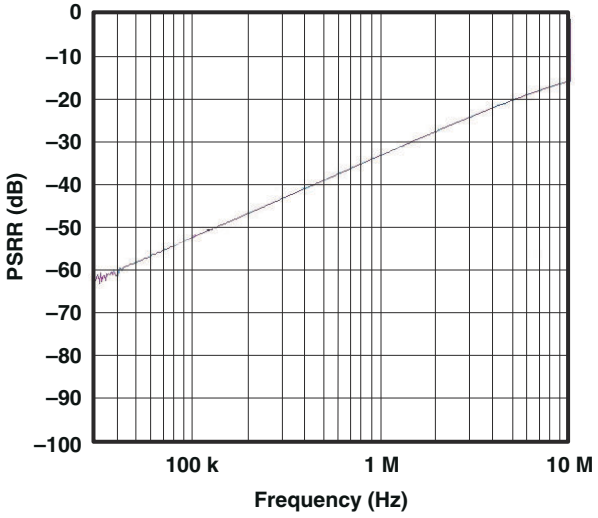


Figure 6-16. Com Port to No0 PSRR, In1 = V_{CC}, In2 = V_{CC} (V_{CC} = 5 V)

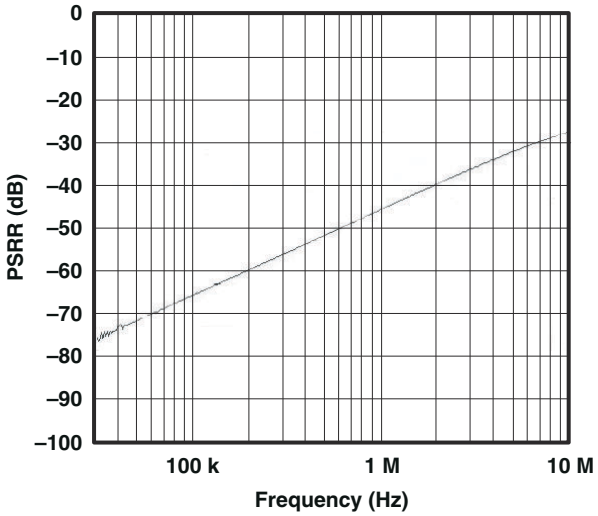


Figure 6-17. Com Port Hi-Z PSRR, In1 = 0 V, In2 = 0 V (V_{CC} = 5 V)

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7 Parameter Measurement Information

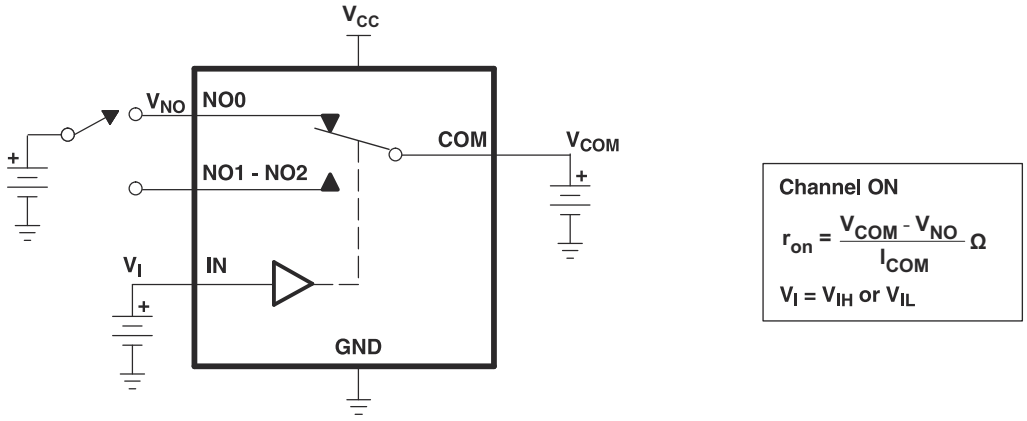


Figure 7-1. ON-State Resistance (R_{on})

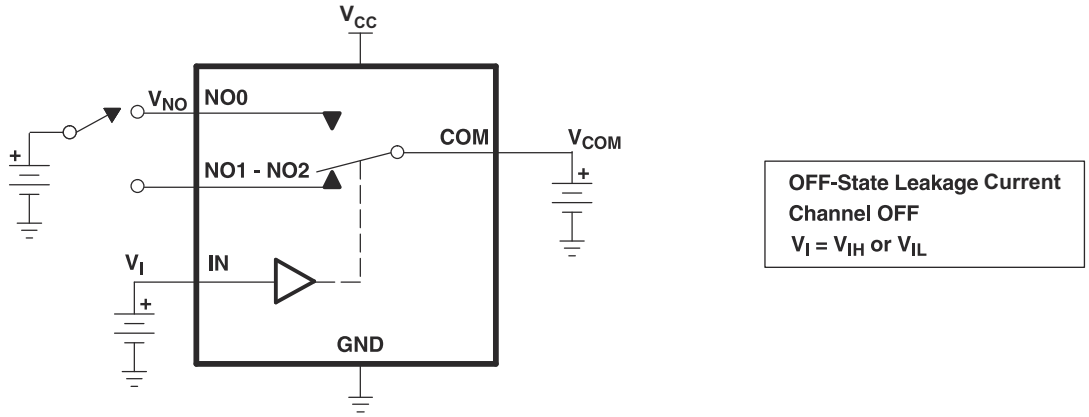


Figure 7-2. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

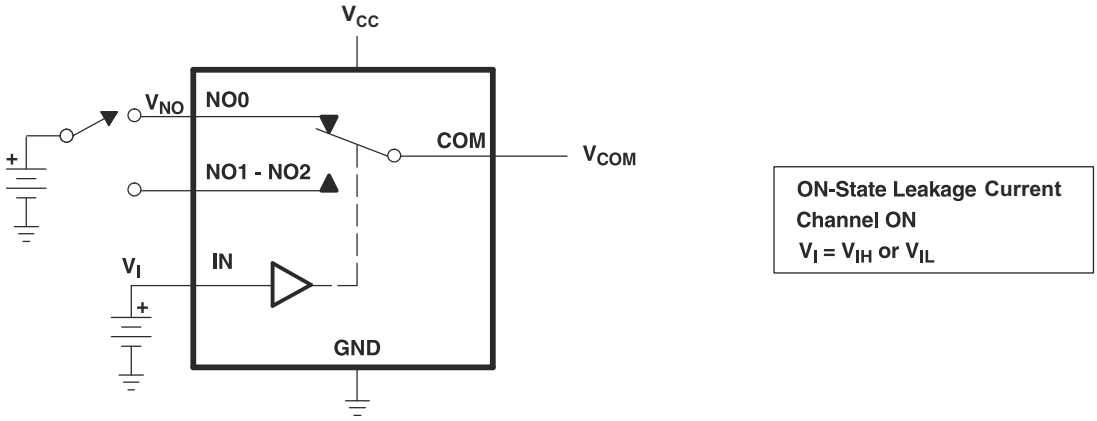


Figure 7-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

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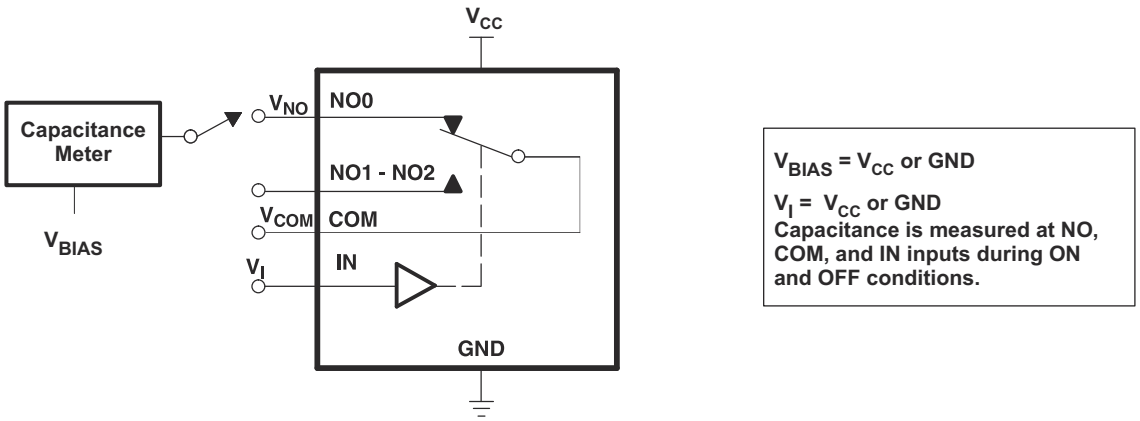
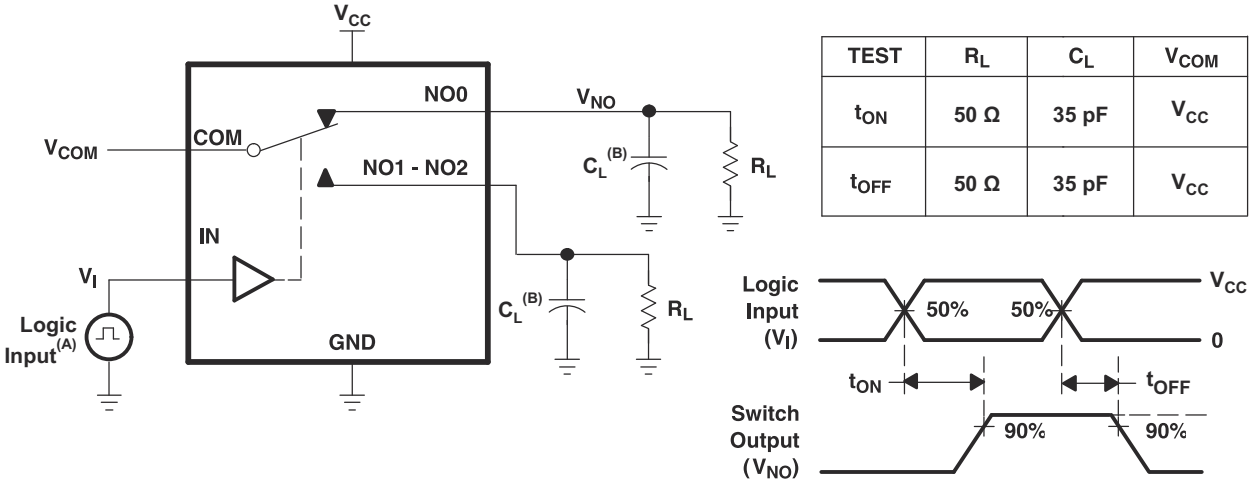


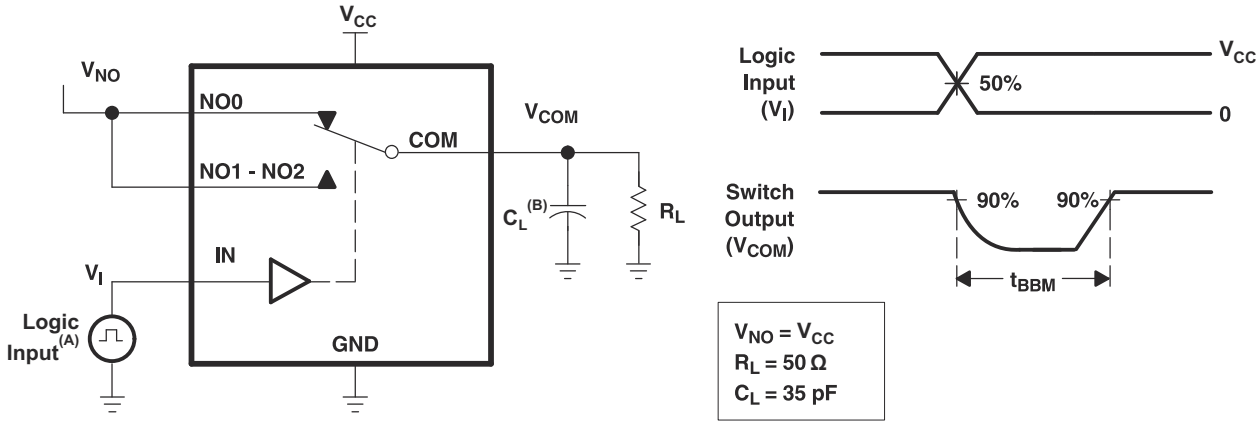
Figure 7-4. Capacitance (C_I, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{COM(OFF)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{CC}
t_{OFF}	50 Ω	35 pF	V_{CC}

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, t_r < 5 ns, t_f < 5 ns.
B. C_L includes probe and jig capacitance.

Figure 7-5. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, t_r < 5 ns, t_f < 5 ns.
B. C_L includes probe and jig capacitance.

Figure 7-6. Break-Before-Make Time (t_{BBM})

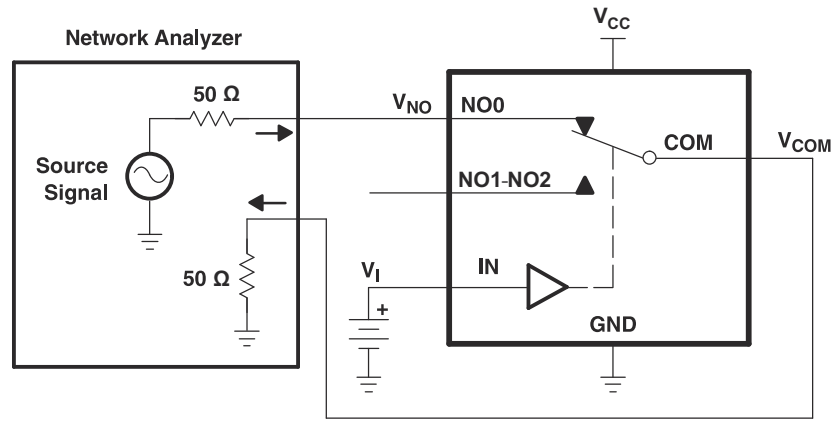


Figure 7-7. Bandwidth (BW)

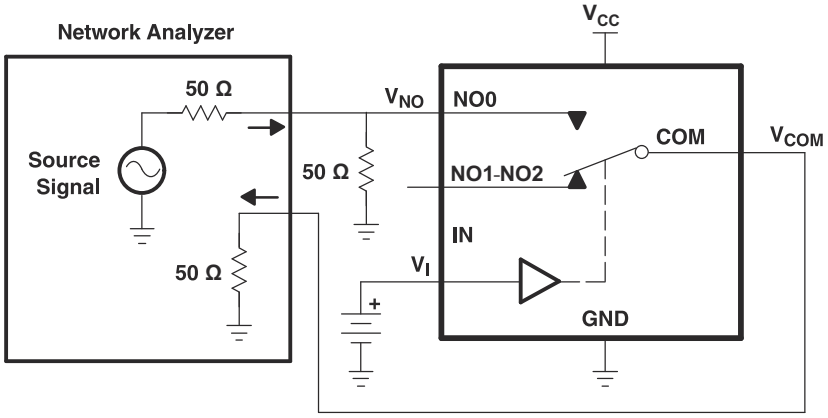


Figure 7-8. Off Isolation (O_{ISO})

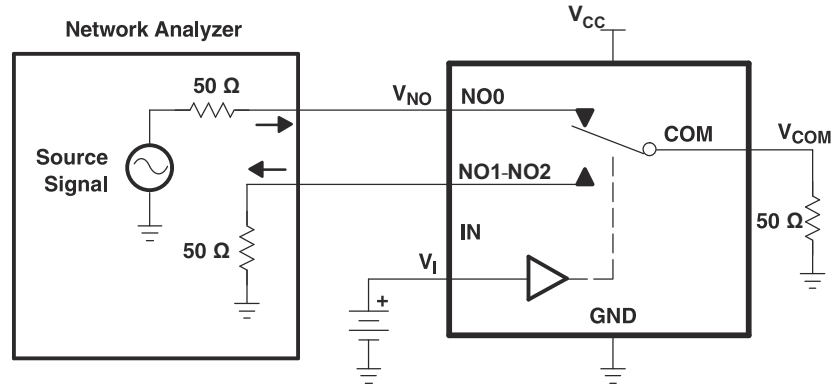
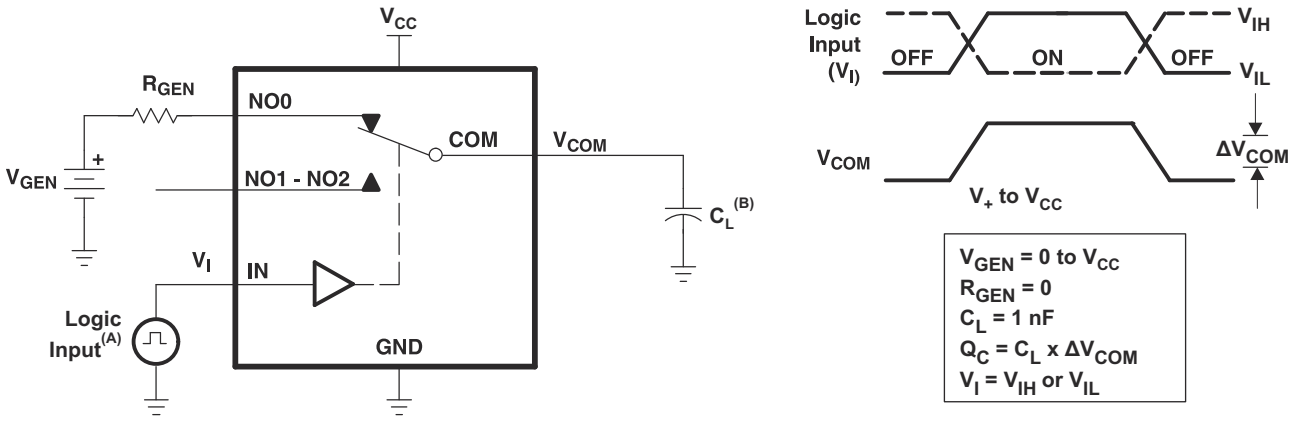


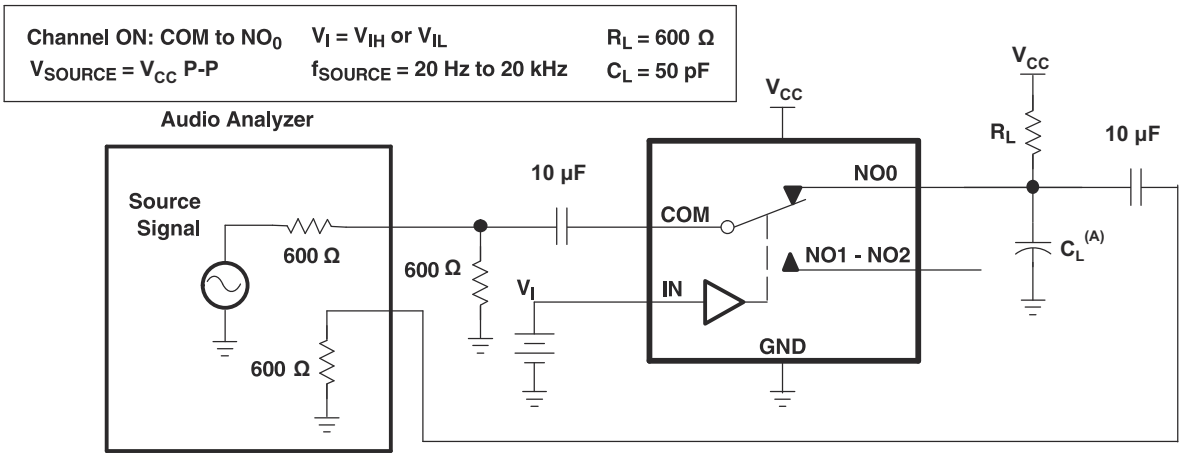
Figure 7-9. Crosstalk (X_{TALK})

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A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, t_r < 5 ns, t_f < 5 ns.
B. C_L includes probe and jig capacitance.

Figure 7-10. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 7-11. Total Harmonic Distortion (THD)

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Table 7-1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r_{peak}	Peak ON-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, V_{CC} = 0.
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(OFF)}$	Leakage current measured at the COM port during the power-down condition, V_{CC} = 0
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, V_{CC} = 0.
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB less than the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_{CC}	Static power-supply current with the control (IN) pin at V_{CC} or GND

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Table 7-2. Summary of Characteristics(1)

PARAMETER	CHARACTERISTIC
Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance (r_{on})	1.1 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turnon/turnoff time (t_{ON}/t_{OFF})	40 ns/35 ns
Break-before-make time (t_{BBM})	1 ns
Charge injection (Q_C)	40 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	–65 dB at 10 MHz
Crosstalk (X_{TALK})	–66 dB at 10 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{COM(OFF)}/I_{NO(OFF)}$)	±20 µA
Power supply current (I_{CC})	0.1 µA
Package options	8-pin DCU or YZP

(1) V_{CC} = 5 V, T_A = 25°C

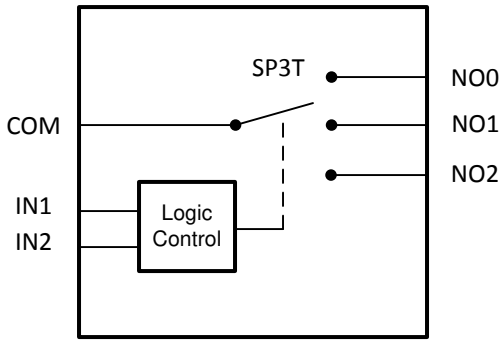
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8 Detailed Description

8.1 Overview

The TS5A3359 is a bidirectional, single-channel, single-pole triple-throw (SP3T) analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3359 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS5A3359 device also has a specified break-before-make feature. The device consumes very low power and provides isolation when V_{CC} = 0.

8.2 Functional Block Diagram



8.3 Feature Description

Isolation in Power-Down Mode, V_{CC} = 0

When power is not supplied to the VCC pin, V_{CC} = 0 , the signal paths NO and COM are high impedance. This is specificed in the electrical characterisitics table under the COM and NO OFF leakage current when V_{CC} = 0. Because the device is high impedance when it is not powered, you may connect other signals to the signal chain without interference of the TS5A3359.

8.4 Device Functional Modes

Table 8-1. Function Table

IN2	IN1	COM TO NO, NO TO COM
L	L	OFF
L	H	COM = NO0
H	L	COM = NO1
H	H	COM = NO2

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3359 switch is bidirectional, so the NO and COM pins can be used as either inputs or outputs. This switch is typically used when there is only one signal path that needs to be able to communicate to 3 different signal paths.

9.2 Typical Application

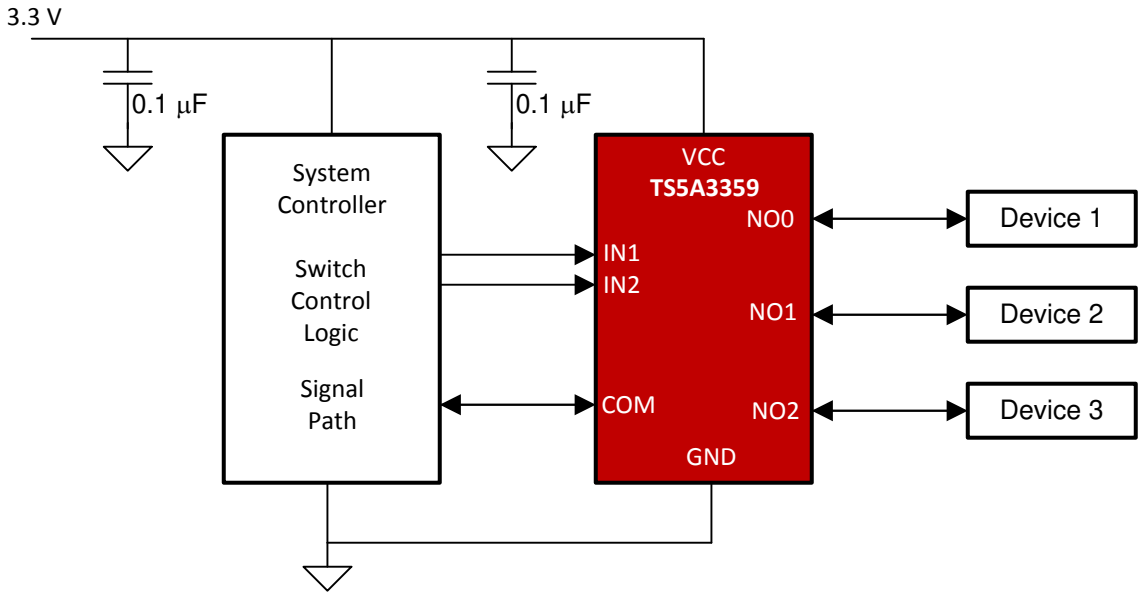


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

The TS5A3359 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3359 input and output signal swing through NO and COM are dependent on the supply voltage V_{CC}. For example, if the desired signal level to pass through the switch is 5 V, V_{CC} must be greater than or equal to 5 V. V_{CC} = 3.3 V would not be valid for passing a 5-V signal since the Analog signal voltage cannot exceed the supply.

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9.2.2 Detailed Design Procedure

The TS5A3359 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3359 input/output signal swing through NO and COM are dependant of the supply voltage V_{CC}.

9.2.3 Application Curve

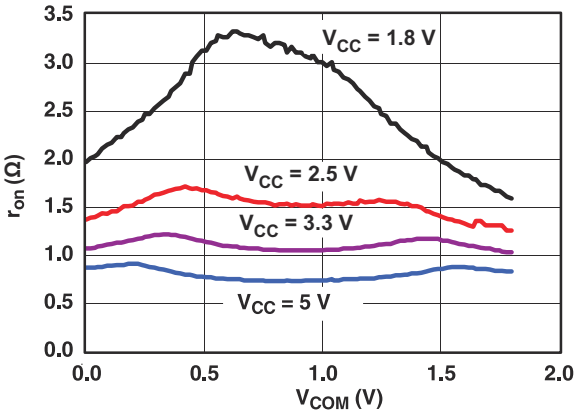


Figure 9-2. R_{on} vs V_{COM}

10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-µF capacitor, connected from VCC to GND, is adequate for most applications.

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11 Layout

11.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

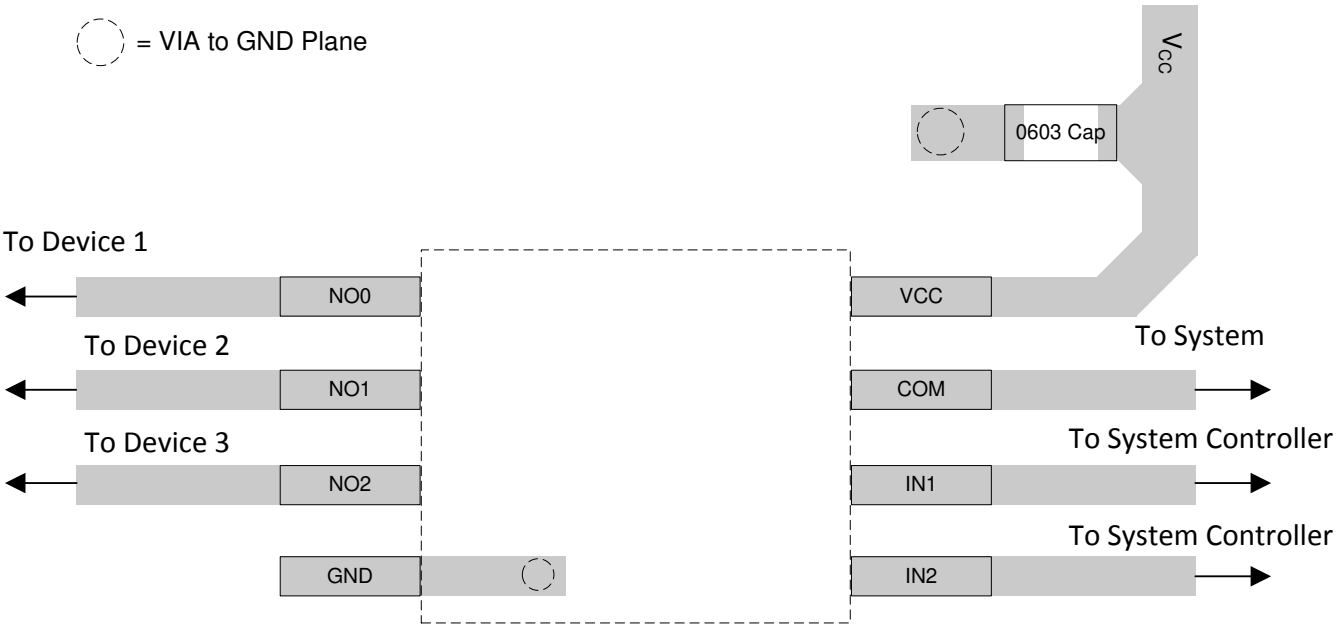


Figure 11-1. Recommended Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3359DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL, JALR) JZ
TS5A3359DCUR.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL, JALR) JZ
TS5A3359DCUR1G4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JALR
TS5A3359DCUR1G4.B	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JALR
TS5A3359DCUT	Obsolete	Production	VSSOP (DCU) | 8	-	-	Call TI	Call TI	-40 to 85	(AL, JALR) JZ
TS5A3359YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J9
TS5A3359YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J9

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

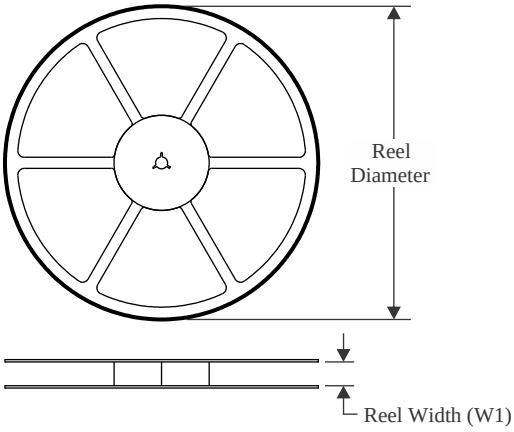
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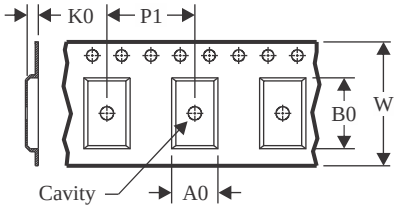
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

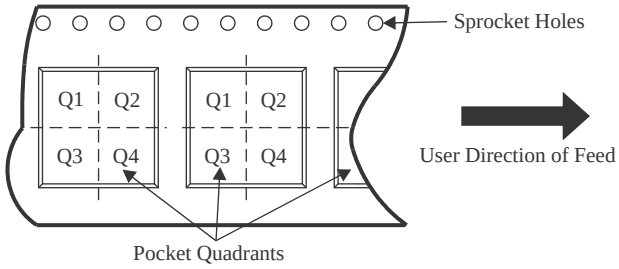


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

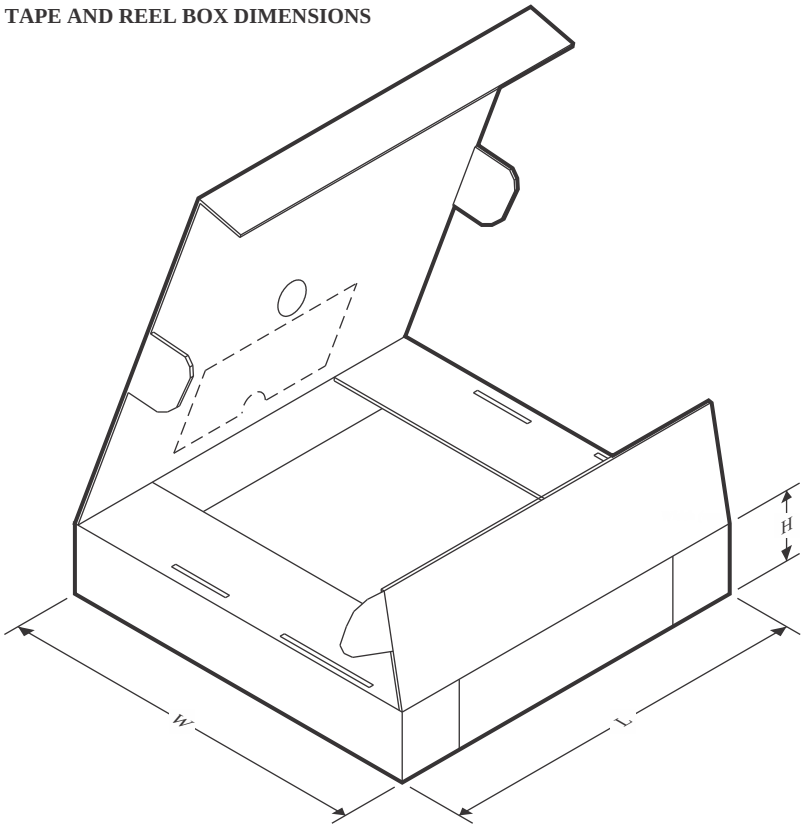
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3359DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3359DCUR1G4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3359YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3359DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3359DCUR1G4	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3359YZPR	DSBGA	YZP	8	3000	210.0	185.0	35.0

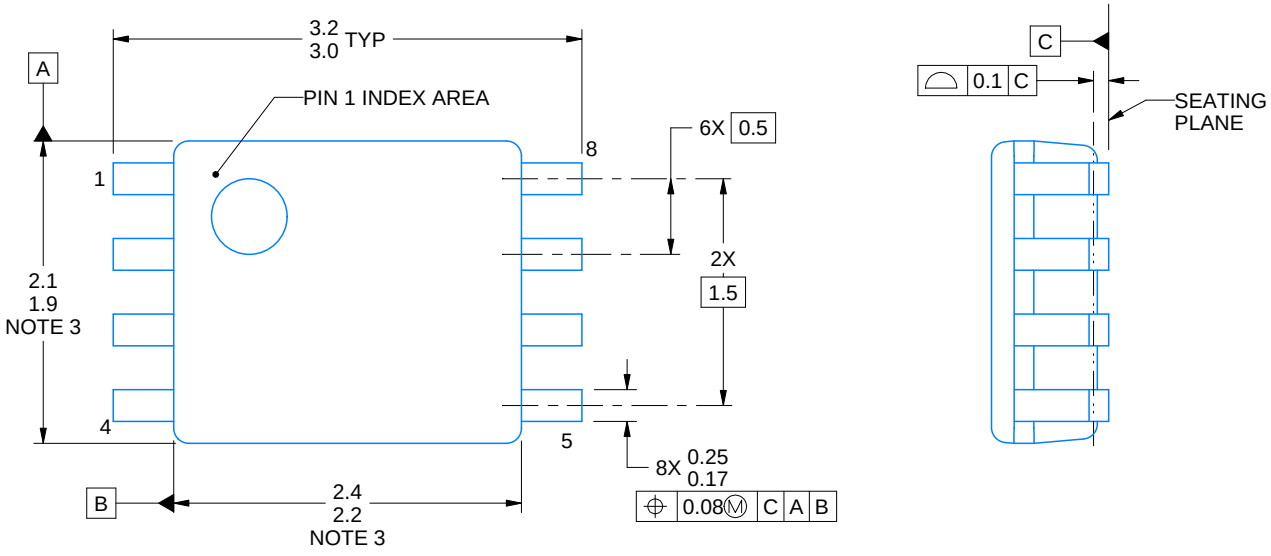
DCU0008A

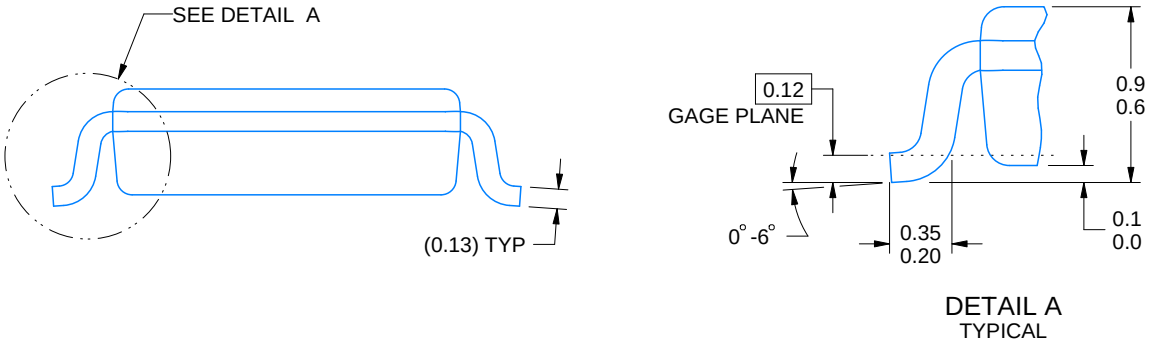


PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

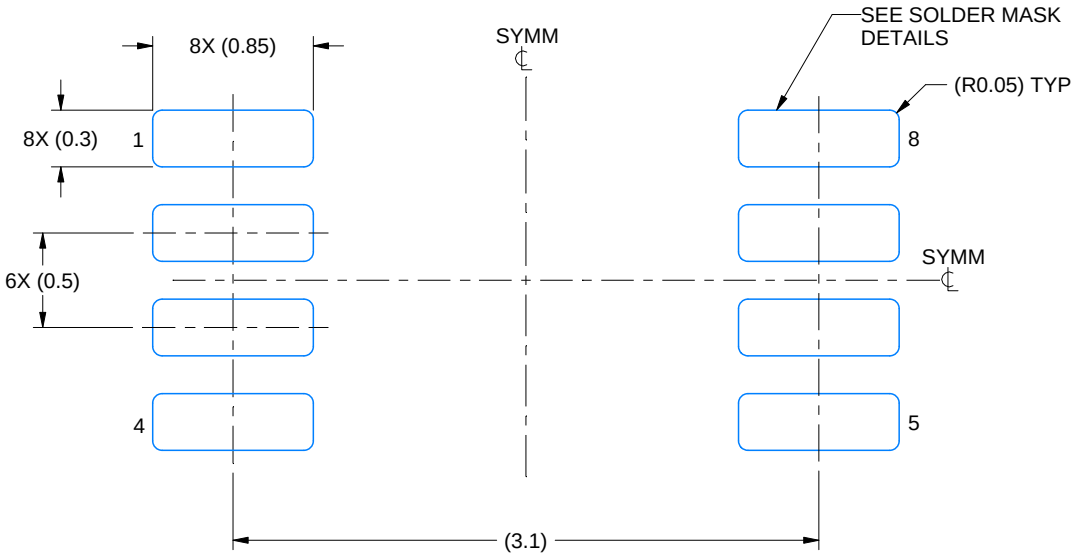




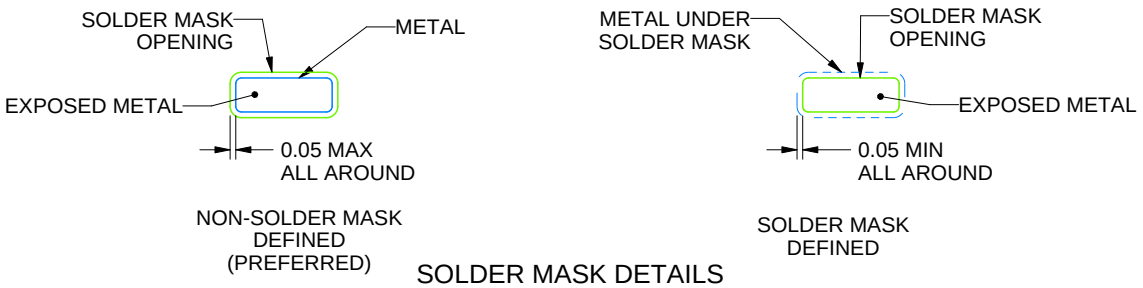
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

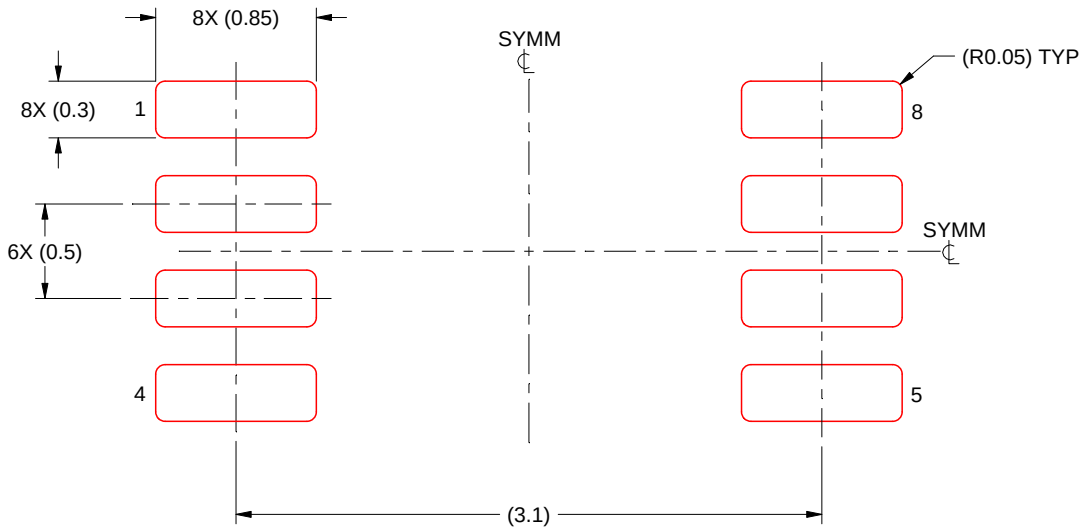


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

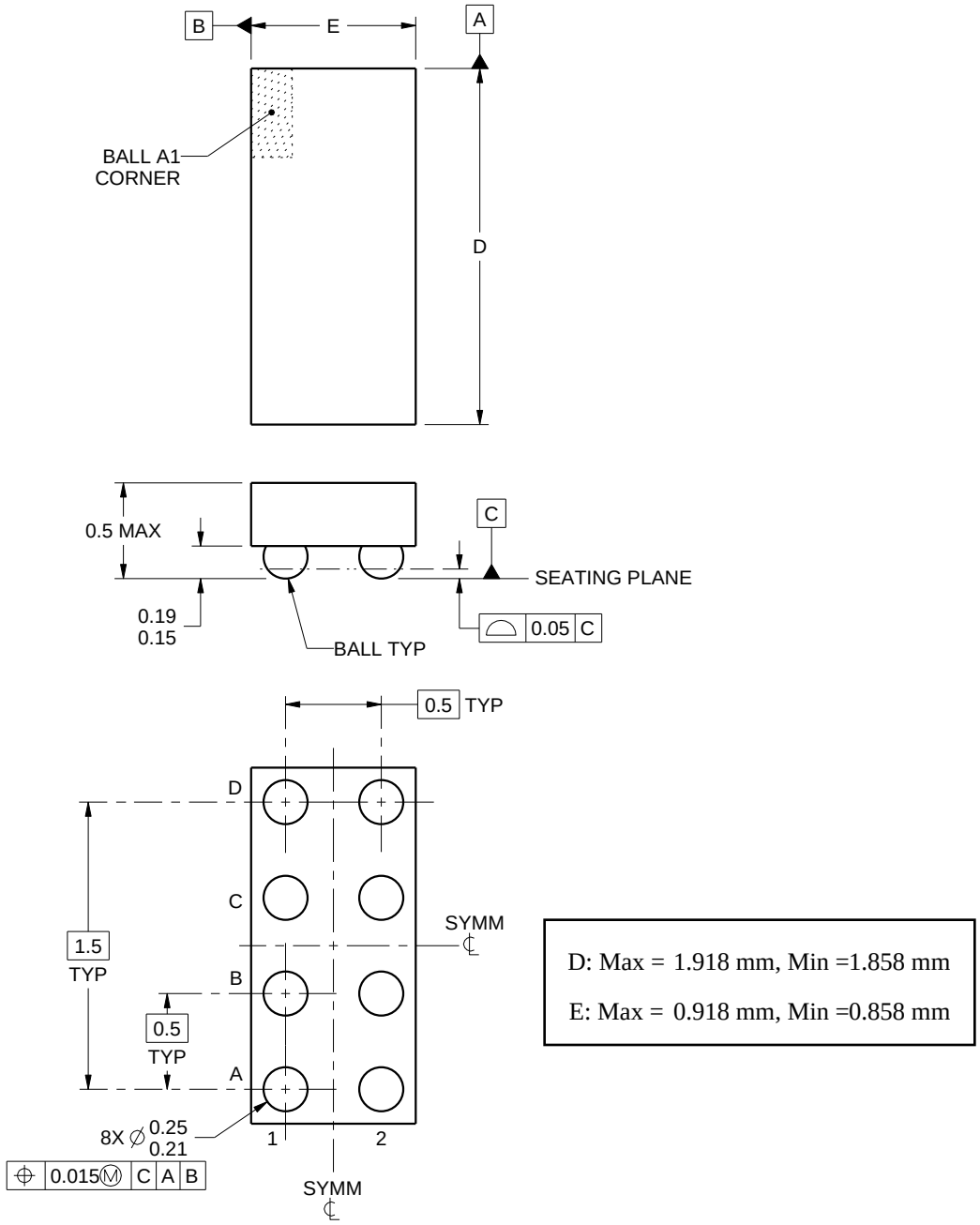
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

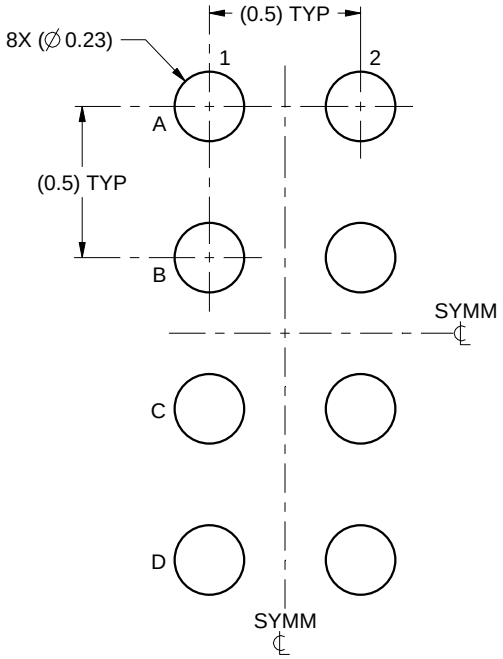
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

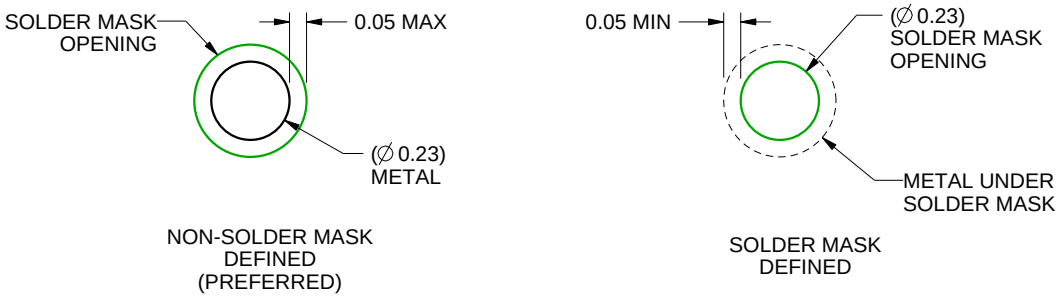


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

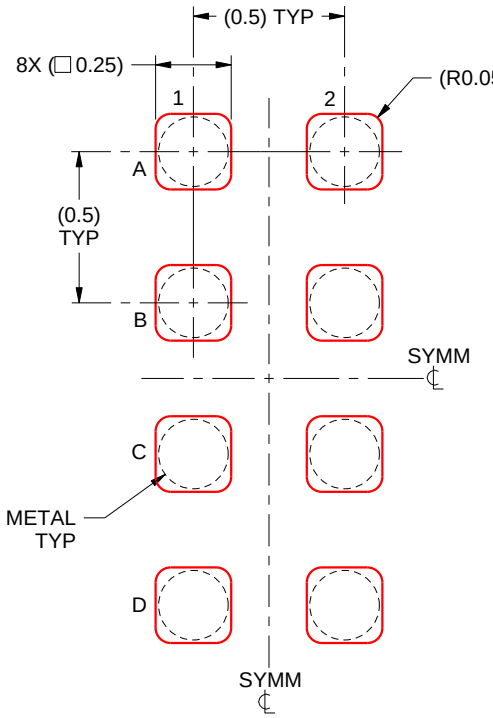


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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