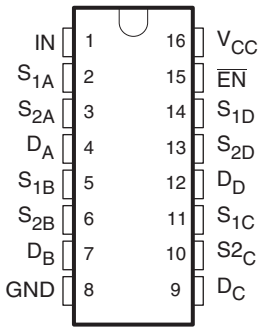
QUAD SPDT WIDE BANDWIDTH VIDEO SWITCH WITH LOW ON-STATE RESISTANCE

Check for Samples: TS5V330C

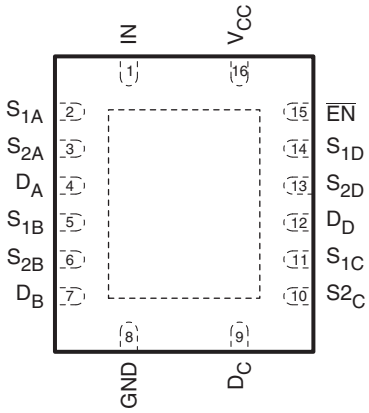
FEATURES

- **Low Differential Gain and Phase (Typical D_G = 0.24%, Typical D_P = 0.039°)**
- **Wide Bandwidth (Typical BW > 288 MHz)**
- **Low Cross-Talk (Typical X_{TALK} = –87 dB)**
- **Low Power Consumption (Maximum I_{CC} = 3 µA)**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (Typical r_{ON} = 3 Ω)**
- **V_{CC} Operating Range From 4.5 V to 5.5 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Data and Control Inputs Provide Undershoot Clamp Diode**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Suitable for Both RGB and Composite Video Switching**

D, DB, DBQ, OR PW PACKAGE (TOP VIEW)



RGY PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TS5V330C is a 4-bit 1-of-2 multiplexer/demultiplexer video switch with a single switch-enable ($\overline{EN}$) input. The select (IN) input controls the data path of the multiplexer/demultiplexer. When EN is low, the switch is enabled and the D port is connected to the S port. When $\overline{EN}$ is high, the switch is disabled and a high impedance state exists between the D and S ports.

Low differential gain and phase makes this switch ideal for video applications. The device has a wide bandwidth and low cross talk which makes it suitable for high frequency video applications. The device can be used for RGB and composite video switching applications.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{EN}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	TS5V330CRGYR	TE330C
	SOIC – D	Tube	TS5V330CD	TS5V330C
		Tape and reel	TS5V330CDR	
	SSOP – DB	Tape and reel	TS5V330CDBR	TE330C
	SSOP (QSOP) – DBQ	Tape and reel	TS5V330CDBQR	TE330C
	TSSOP – PW	Tube	TS5V330CPW	TE330C
		Tape and reel	TS5V330CPWR	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. FUNCTION TABLE

INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{EN}$	IN		
L	L	S1	D port = S1 port
L	H	S2	D port = S2 port
H	X	Z	Disconnect

Table 2. PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
S1, S2	Analog video I/Os
D	Analog video I/Os
IN	Select input
$\overline{EN}$	Switch-enable input

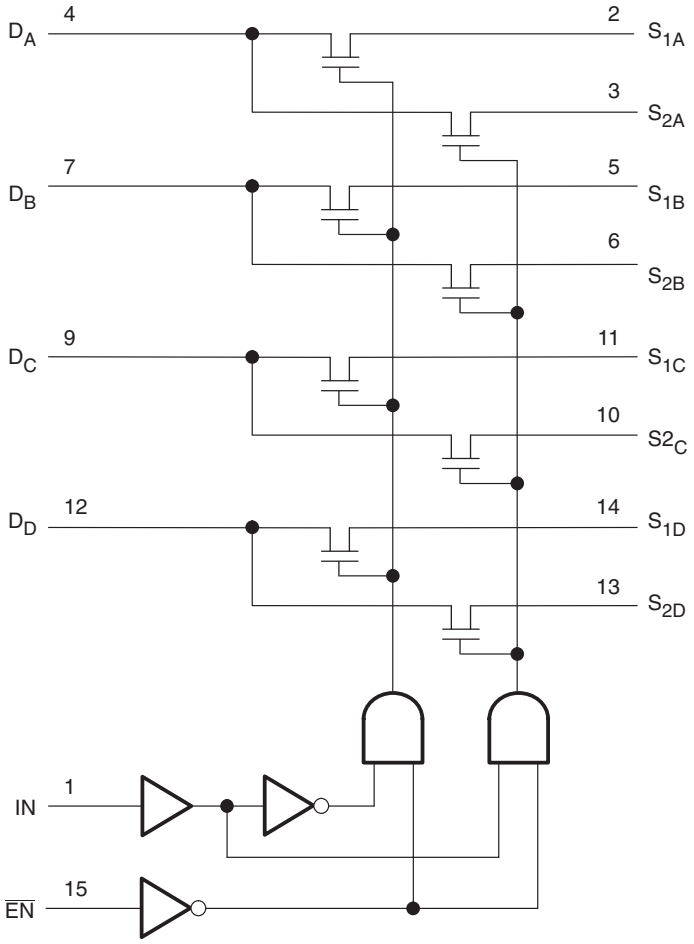
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PARAMETER DEFINITIONS

PARAMETER	DESCRIPTION
r_{ON}	Resistance between the D and S ports with the switch in the ON-state
I_{OZ}	Output leakage current measured at the D and S ports with the switch in the OFF-state
I_{OS}	Short circuit current measured at the I/O pins.
V_{IN}	Voltage at the IN pin
V_{EN}	Voltage at the $\overline{EN}$ pin
C_{IN}	Capacitance at the control inputs ($\overline{EN}$, IN)
C_{OFF}	Capacitance at the analog I/O port when the switch is OFF
C_{ON}	Capacitance at the analog I/O port when the switch is ON
V_{IH}	Minimum input voltage for logic high for the control inputs ($\overline{EN}$, IN)
V_{IL}	Minimum input voltage for logic low for the control inputs ($\overline{EN}$, IN)
V_H	Hysteresis voltage at the control inputs ($\overline{EN}$, IN)
V_{IK}	I/O and control inputs diode clamp voltage ($\overline{EN}$, IN)
V_I	Voltage applied to the D or S pins when D or S is the switch input.
V_O	Voltage applied to the D or S pins when D or S is the switch output.
I_{IH}	Input high leakage current of the control inputs ($\overline{EN}$, IN)
I_{IL}	Input low leakage current of the control inputs ($\overline{EN}$, IN)
I_I	Current into the D or S pins when D or S is the switch input.
I_O	Current into the D or S pins when D or S is the switch output.
I_{off}	Output leakage current measured at the D and S ports with V_{CC} = 0
t_{ON}	Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned ON.
t_{OFF}	Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned OFF.
BW	Frequency response of the switch in the ON-state measured at –3 dB
X_{TALK}	Unwanted signal coupled from channel to channel. Measured in –dB. X_{TALK} = 20 LOG V_{OUT}/V_{IN}. This is a non-adjacent crosstalk.
O_{IRR}	Off-isolation is the resistance (measured in –dB) between the input and output with the switch OFF.
D_G	Magnitude variation between analog input and output pins when the switch is ON and the DC offset of composite video signal varies at the analog input pin. In NTSC standard the frequency of the video signal is 3.58 MHz and DC offset is from 0 to 0.714 V.
D_P	Phase variation between analog input and output pins when the switch is ON and the DC offset of composite video signal varies at the analog input pin. In NTSC standard the frequency of the video signal is 3.58 MHz and DC offset is from 0 to 0.714 V.
I_{CC}	Static power supply current
I_{CCD}	Variation of I_{CC} for a change in frequency in the control inputs ($\overline{EN}$, IN)
ΔI_{CC}	This is the increase in supply current for each control input that is at the specified voltage level, rather than V_{CC} or GND.

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LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_{IN}	Control input voltage range(2) (3)		–0.5	7	V
$V_{I/O}$	Output voltage range(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

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PACKAGE THERMAL IMPEDANCE

over operating free-air temperature range (unless otherwise noted)

				UNIT
θ_{JA}	Package thermal impedance	D package(1)	73	°C/W
		DB package(1)	82	
		DBQ package(1)	90	
		PW package(1)	108	
		RGY package(2)	39	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.
(2) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage ($\overline{EN}$, IN)	2	5.5	V
V_{IL}	Low-level control input voltage ($\overline{EN}$, IN)	0	0.8	V
V_{ANALOG}	Analog input/output voltage	0	Vcc	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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ELECTRICAL CHARACTERISTICS(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}	$\overline{EN}$, IN	V_{CC} = 4.5 V,	I_{IN} = –18 mA				–1.8	V
V_H	$\overline{EN}$, IN						400	mV
I_{IH}	$\overline{EN}$, IN	V_{CC} = 5.5 V,	V_{IN} and V_{EN} = V_{CC}				±1	µA
I_{IL}	$\overline{EN}$, IN	V_{CC} = 5.5 V,	V_{IN} and V_{EN} = GND				±1	µA
I_{OZ} (3)		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF			±10	µA
I_{OS}		V_{CC} = 5.5 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch ON			±110	mA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			±1	µA
I_{CC}		V_{CC} = 5.5 V,	$I_{I/O}$ = 0,	Switch ON or OFF			3	µA
ΔI_{CC}	$\overline{EN}$, IN	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
I_{CCD}		V_{CC} = 5.5 V, V_{EN} = GND,	D and S ports are open,	V_{IN} switching 50% duty cycle			0.25	mA/ MHz
C_{in}	$\overline{EN}$, IN	V_{IN} or V_{EN} = 0	f = 1 MHz			3.5		pF
C_{OFF}	D port	$V_{I/O}$ = 3 V or 0,	Switch OFF,	V_{IN} = V_{CC} or GND		8.5		pF
	S port		Switch ON,			5.5		
C_{ON}		V_I = 0,	f = 1 MHz, outputs open,	Switch ON		16.5		pF
r_{ON} (4)		V_{CC} = 4.5 V	V_I = 1 V,	I_O = 13 mA, R_L = 75 Ω		3	7	Ω
			V_I = 2 V,	I_O = 26 mA, R_L = 75 Ω		3	10	

(1) V_I , V_O, I_I, and I_O refer to the I/O pins.
(2) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) Measured by the voltage drop between the D and S terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (S or D) terminals.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ±10%, R_L = 75 Ω, C_L = 20 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{ON}	S	D	1.5		6.0	ns
t_{OFF}	S	D	1.5		5.9	ns

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
D_G	R_L = 150 Ω, f = 3.58 MHz, see Figure 6		0.24		%
D_P	R_L = 150 Ω, f = 3.58 MHz, see Figure 6		0.039		°
BW	R_L = 150 Ω, see Figure 7		250		MHz
X_{TALK}	R_{IN} = 10 Ω, R_L = 150 Ω, f = 10 MHz, see Figure 7		–87		dB
O_{IRR}	R_L = 150 Ω, f = 10 MHz, see Figure 7		–54		dB

(1) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

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TYPICAL PERFORMANCE

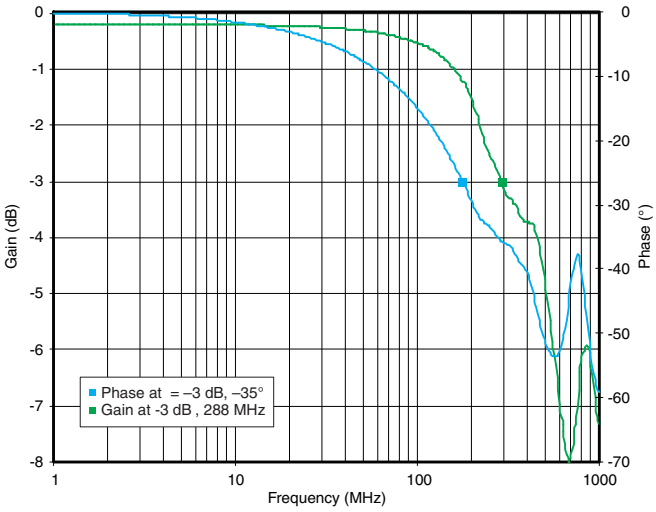


Figure 1. Frequency Response

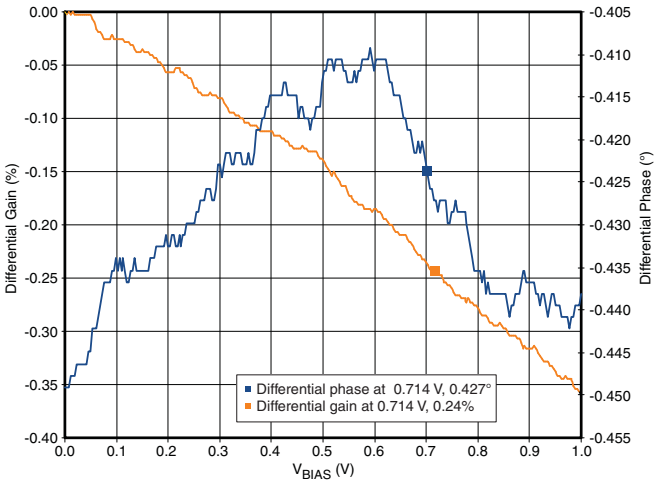


Figure 2. Differential Gain/Phase vs V_{BIAS}

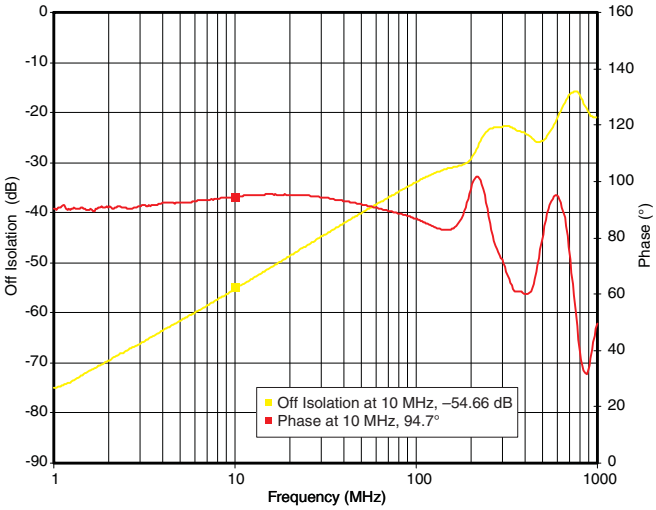


Figure 3. OFF-Isolation vs Frequency

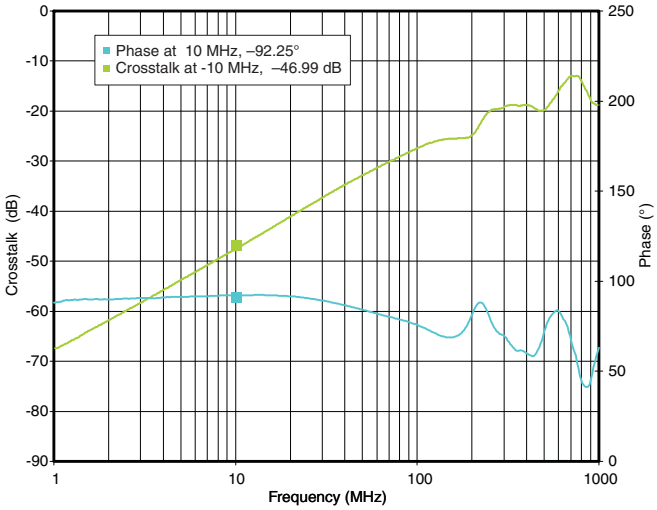
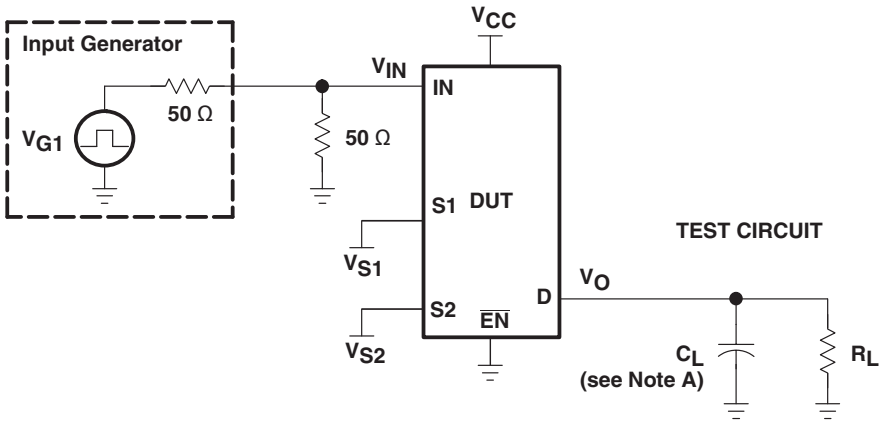


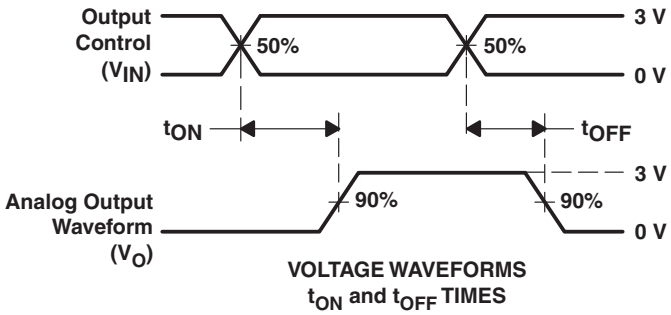
Figure 4. Crosstalk vs Frequency

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PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	R_L	C_L	V_{S1}	V_{S2}
t_{ON}	5 V ± 0.5 V 5 V ± 0.5 V	75 Ω 75 Ω	20 pF 20 pF	GND 3 V	3 V GND
t_{OFF}	5 V ± 0.5 V 5 V ± 0.5 V	75 Ω 75 Ω	20 pF 20 pF	GND 3 V	3 V GND



A. C_L includes probe and jig capacitance.

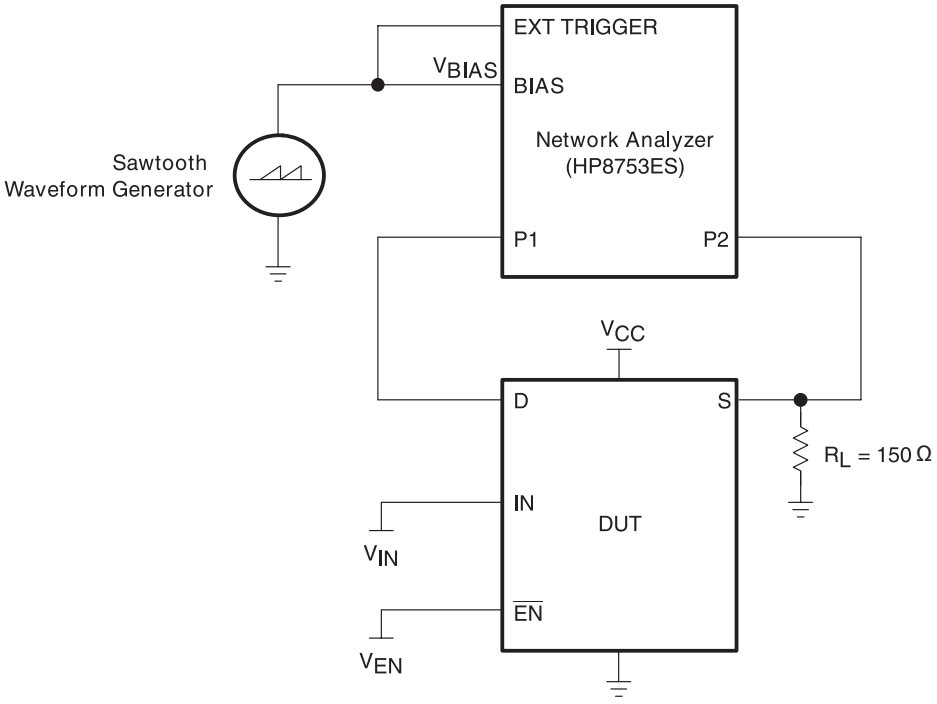
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤2.5 ns.

C. The outputs are measured one at a time with one transition per measurement.

Figure 5. Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION (continued)



For additional information, refer to the TI application report, *Measuring Differential Gain and Phase*, literature number SLOA040.

Figure 6. Test Circuit for Differential Gain/Phase Measurement

The differential gain and phase is measured at the output of the ON channel. For example, when V_{IN} = 0, V_{EN} = 0, and D_A is the input, the output is measured at S_{1A}.

HP8753ES Setup

Average = 20

RBW = 300 Hz

Smoothing = 2%

V_{BIAS} = 0 to 1 V

ST = 1.381 s.

P1 = –7 dBM

CW frequency = 3.58 MHz

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PARAMETER MEASUREMENT INFORMATION (continued)

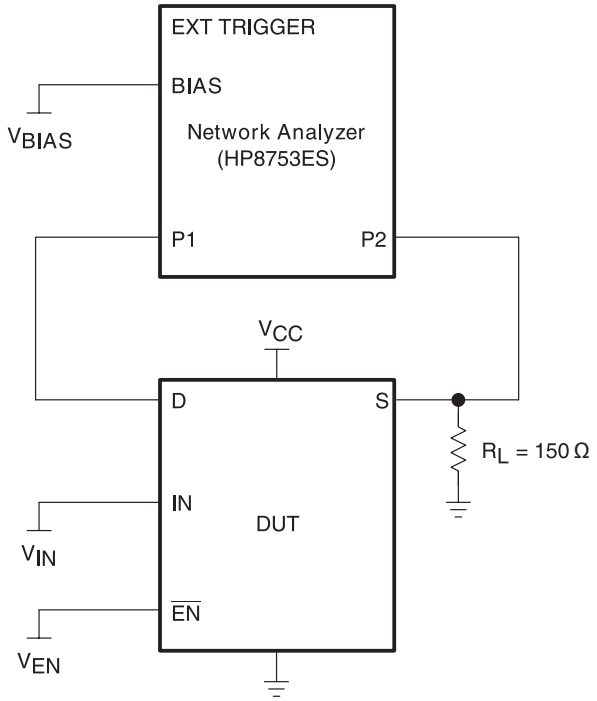


Figure 7. Test Circuit for Frequency Response, Crosstalk, and OFF-Isolation

The frequency response is measured at the output of the ON channel. For example, when V_{IN} = 0, V_{EN} = 0, and D_A is the input, the output is measured at S_{1A}. All unused analog I/O ports are held at V_{CC} or GND.

The crosstalk is measured at the output of the non-adjacent ON channel. For example, when V_{IN} = 0, V_{EN} = 0, and D_A is the input, the output is measured at S_{1B}. All unused analog I/O ports are held at V_{CC} or GND.

The off-isolation is measured at the output of the OFF channel. For example, when V_{IN} = 0, V_{EN} = V_{CC}, and D_A is the input, the output is measured at S_{1A}. All unused analog I/O ports are held at V_{CC} or GND.

HP8753ES Setup

Average = 4

RBW = 3 kHz

Smoothing = 0%

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5V330CDBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TE330C
TS5V330CDBQR.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TE330C
TS5V330CDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS5V330C
TS5V330CDR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS5V330C
TS5V330CPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	TE330C
TS5V330CPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TE330C
TS5V330CPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TE330C
TS5V330CPWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TE330C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

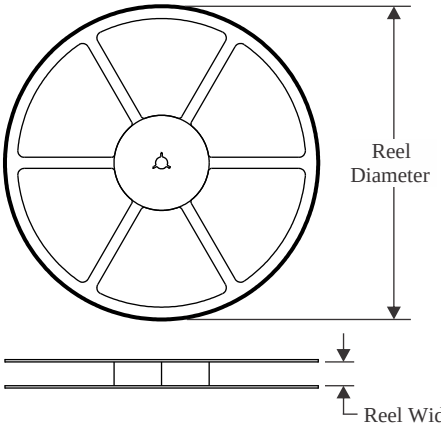
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

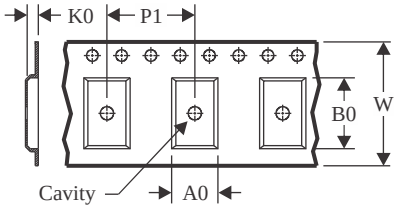
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

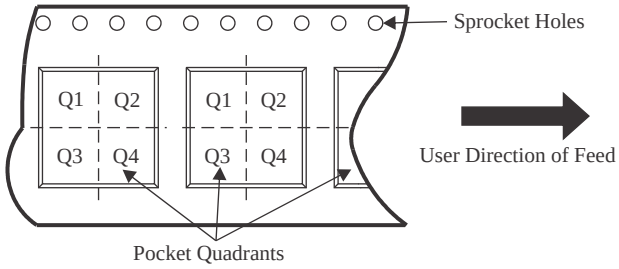


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

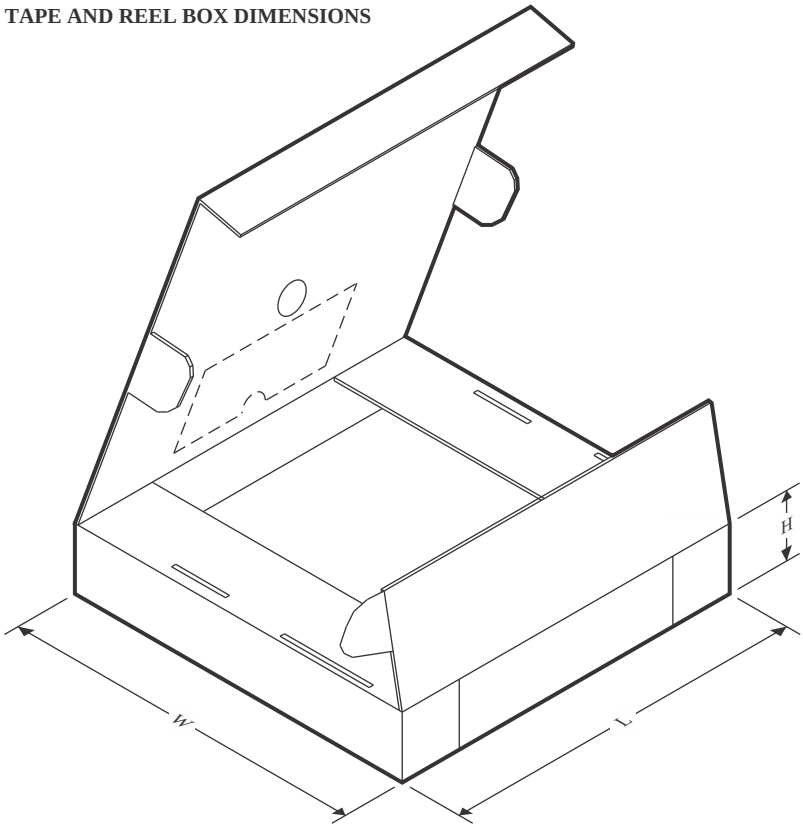
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5V330CDBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS5V330CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS5V330CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS5V330CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS5V330CPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

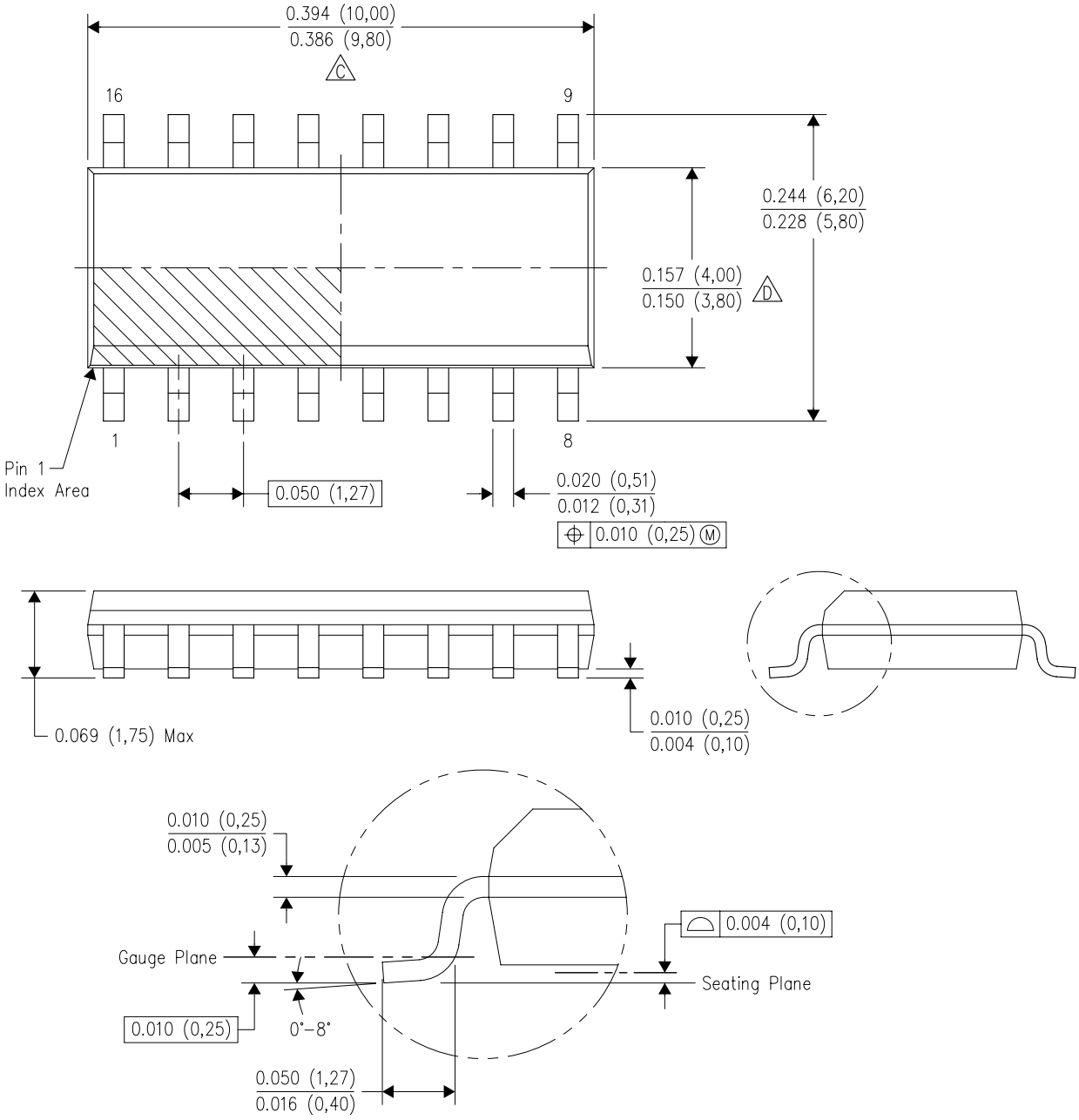
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5V330CDBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
TS5V330CDR	SOIC	D	16	2500	353.0	353.0	32.0
TS5V330CPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TS5V330CPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TS5V330CPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



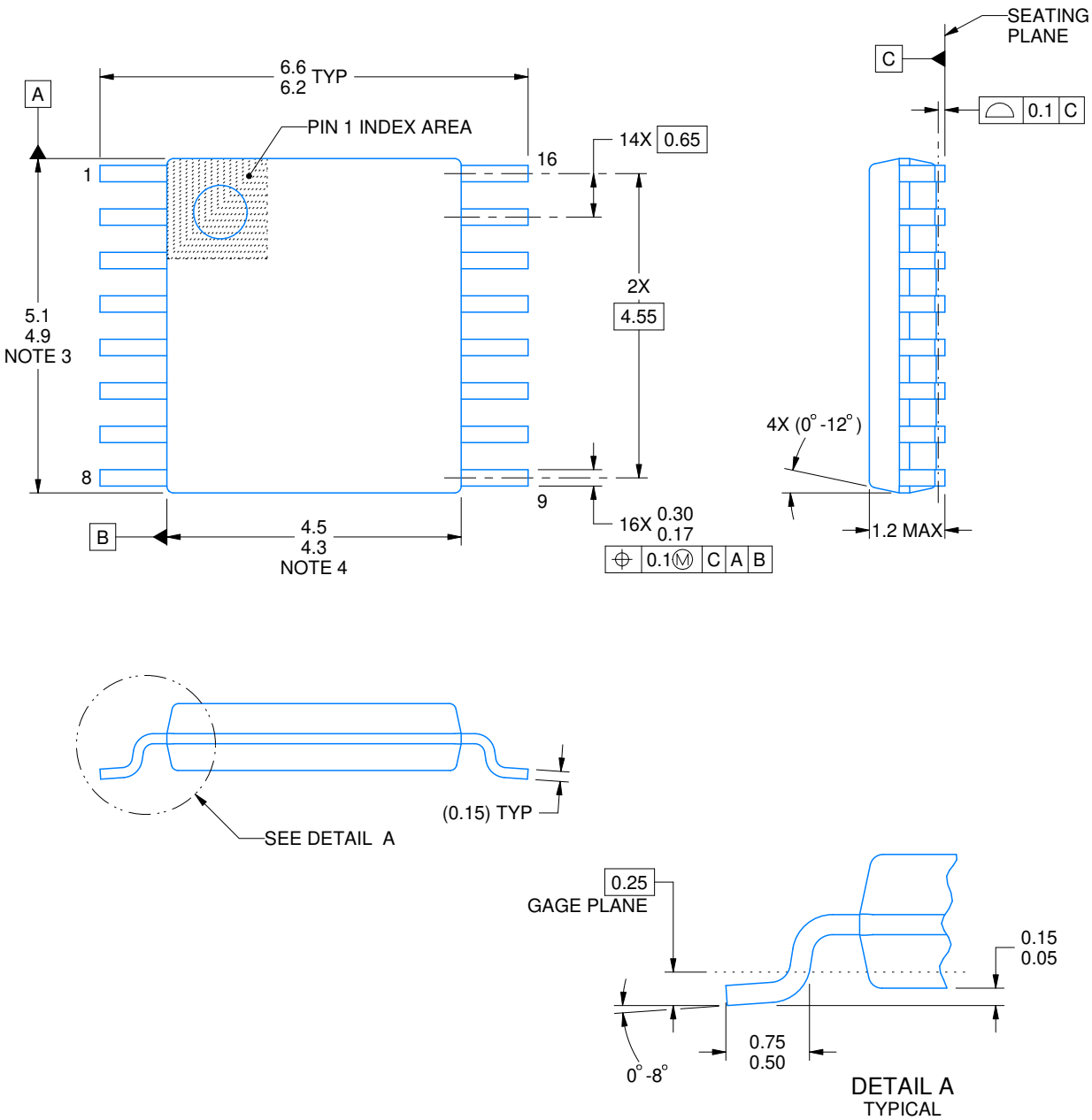
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

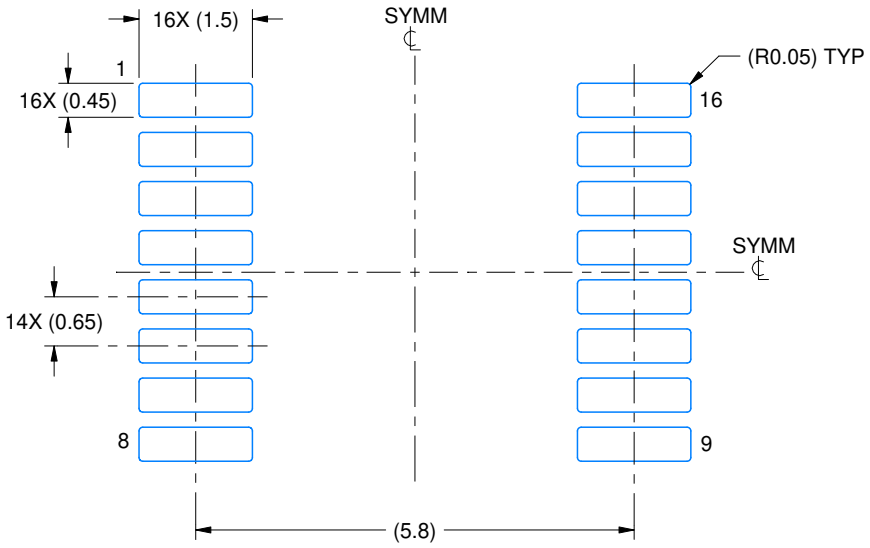
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

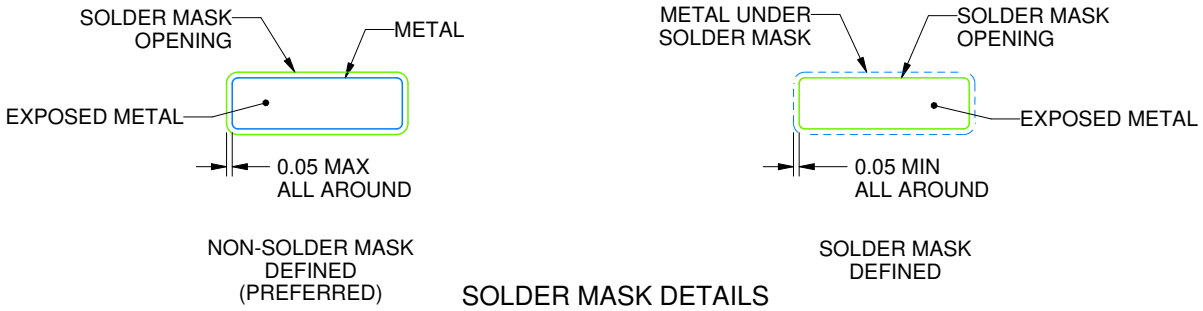


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

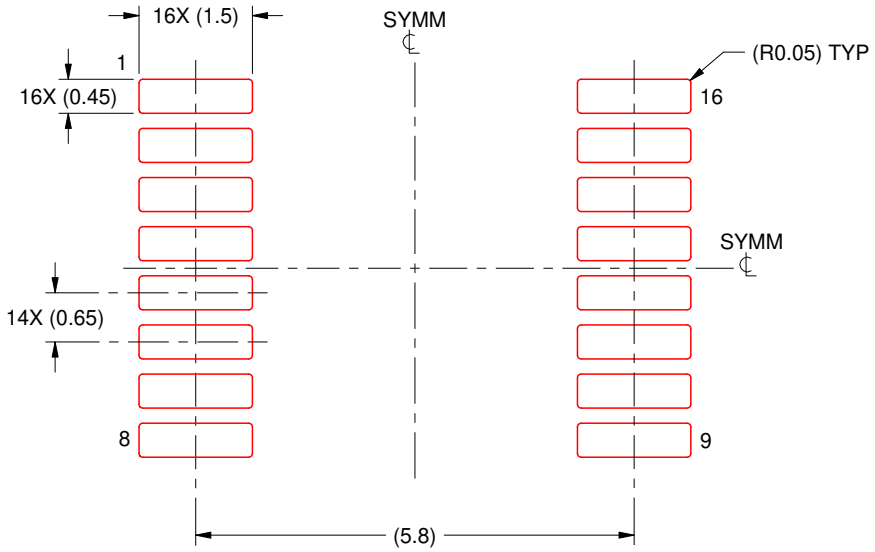


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

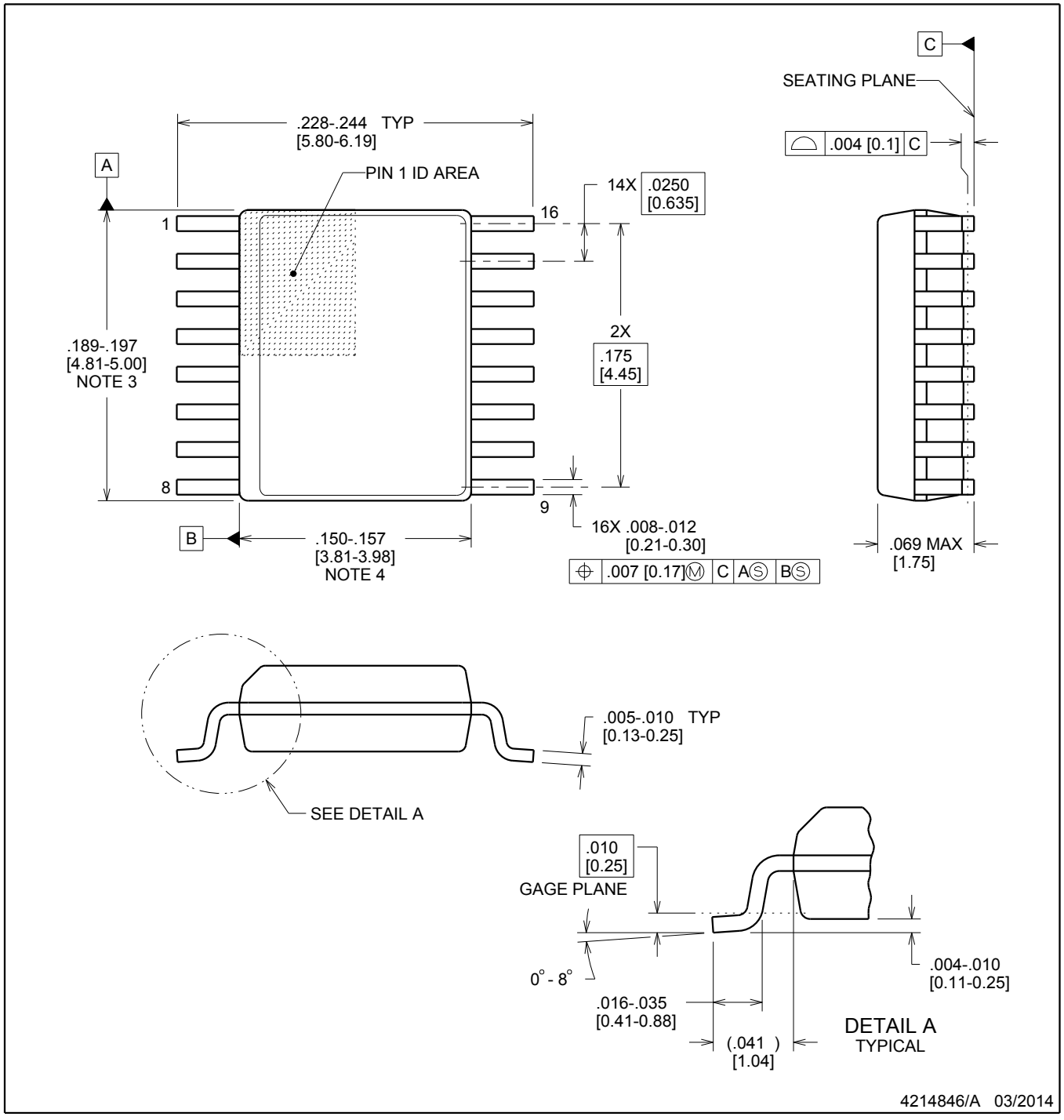


PACKAGE OUTLINE

DBQ0016A

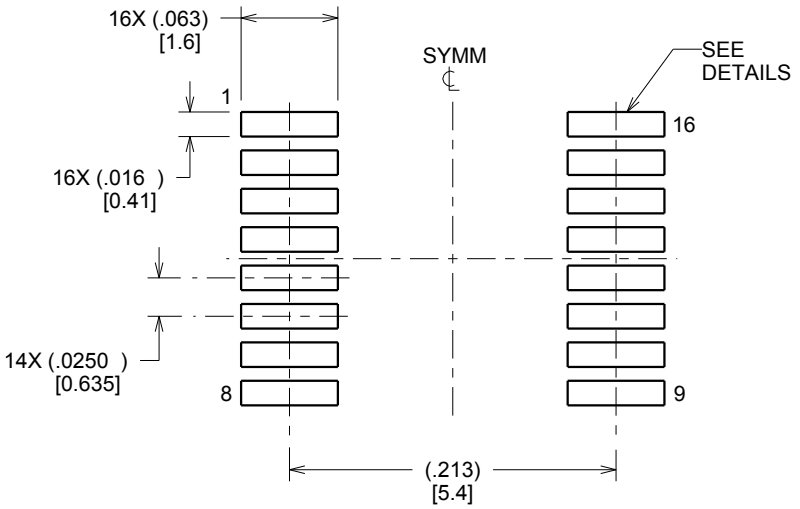
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

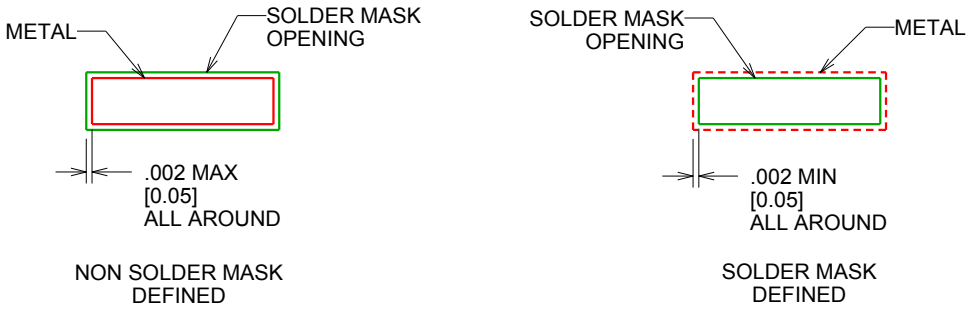


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

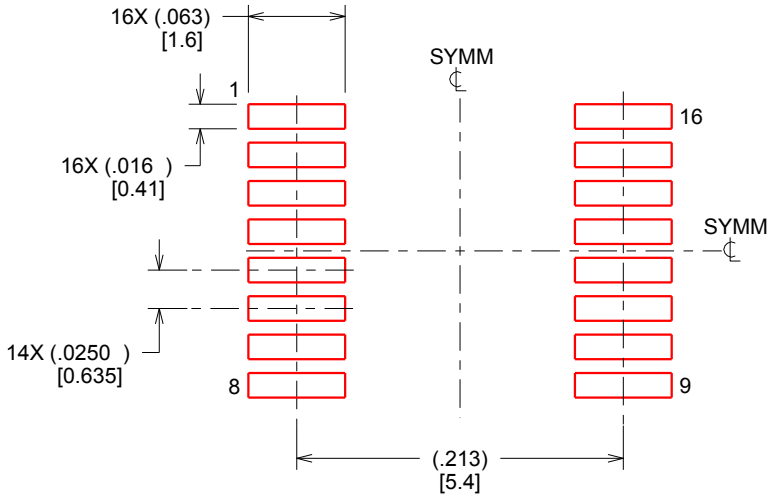


SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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