TSM102, TSM102A
DUAL OPERATIONAL AMPLIFIER, DUAL COMPARATOR, AND VOLTAGE REFERENCE

SLVS602 – MARCH 2006

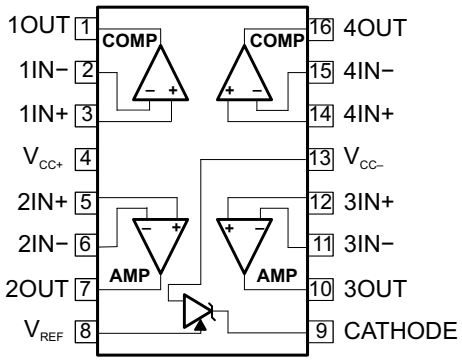
FEATURES

- **OPERATIONAL AMPLIFIERS**
  - **Low Supply Current…200 μA/A**
  - **Medium Speed…2.1 MHz**
  - **Low-Level Output Voltage Close to V_{CC-}…0.1 V Typ (R_L = 10 kΩ)**
  - **Input Common-Mode Voltage Range Includes Ground**
- **COMPARATORS**
  - **Low Supply Current…200 μA/A (V_{CC} = 5 V)**
  - **Input Common-Mode Voltage Range Includes Ground**
  - **Low Output Saturation Voltage… Typically 250 mV (I_{sink} = 4 mA)**
- **VOLTAGE REFERENCE**
  - **Adjustable Output Voltage…V_{REF} to 36 V**
  - **Sink Current Capability…1 mA to 100 mA**
  - **0.4% (A Grade) and 1% (Standard Grade) Precision**
  - **Latch-Up Immunity**

APPLICATIONS

- **Switch-Mode Power Supplies**
- **Battery Chargers**
- **Voltage and Current Sensing**
- **Power-Good, Overvoltage, Undervoltage, Overcurrent Detection**
- **Window Comparators**
- **Alarms, Detectors, and Sensors**

D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TSM102 and TMS102A combine the building blocks of a dual operational amplifier, a dual comparator, and a precision voltage reference, all of which often are used to implement a wide variety of power-management functions, including overcurrent detection, undervoltage/overvoltage detection, power-good detection, window comparators, error amplifiers, etc. Additional applications include alarm and detector/sensor applications.

The TSM102A offers a tight V_{REF} tolerance of 0.4% at 25°C. The TSM102 and TSM102A are characterized for operation from –40°C to 85°C.

ORDERING INFORMATION

T_A	MAX V_{REF} TOLERANCE (25°C)	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	A grade: 0.4% precision	SOIC – D	Tube of 75	TSM102AID	TSM102AI
			Reel of 2500	TSM102AIDR	
		TSSOP – PW	Tube of 90	TSM102AIPW	SN102AI
			Reel of 2000	TSM102AIPWR	
	Standard grade: 1% precision	SOIC – D	Tube of 75	TSM102ID	TSM102I
			Reel of 2500	TSM102IDR	
		TSSOP – PW	Tube of 90	TSM102IPW	SN102I
			Reel of 2000	TSM102IPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2006, Texas Instruments Incorporated

Absolute Maximum Ratings(1)

over free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage			36	V
V_{ID}	Input differential voltage			36	V
V_I	Input voltage range		–0.3	36	V
I_{KA}	Voltage reference cathode current			100	mA
θ_{JA}	Package thermal impedance(2)(3)	D package		73	°C/W
		PW package		108	
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC+} – V_{CC–}$	Supply voltage	3	30	V
V_{ID}	Comparator differential input voltage		$V_{CC+} – V_{CC–}$	V
V_{KA}	Cathode-to-anode voltage	V_{REF}	36	V
I_K	Reference cathode current	1	100	mA
T_A	Operating free-air temperature	–40	85	°C

Total Device Electrical Characteristics

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{CC}	Total supply current, excluding reference cathode current	V_{CC+} = 5 V, $V_{CC–}$ = 0 V, No load	25°C		0.8	1.5	mA
			Full range			2	

Operational Amplifier Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = GND, R1 connected to V_{CC}/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			25°C		1	4.5	mV
				Full range			6.5	
αV_{IO}	Input offset voltage drift			25°C		10		µV/°C
I_{IO}	Input offset current			25°C		5	20	nA
				Full range			40	
I_{IB}	Input bias current			25°C		20	100	nA
				Full range			200	
A_{VD}	Large-signal voltage gain	V_{CC+} = 30 V, R1 = 10 kΩ, V_O = 5 V to 25 V		25°C	50	100		V/mV
				Full range	25			
k_{SVR}	Supply-voltage rejection ratio	V_{CC+} = 5 V to 30 V		25°C	80	100		dB
V_{ICM}	Input common-mode voltage			25°C	V_{CC-}		V_{CC+} – 1.8	V
				Full range	V_{CC-}		V_{CC+} – 2.2	
CMRR	Common-mode rejection ratio	V_{CC+} = 30 V, V_{ICM} = 0 V to V_{CC+} – 1.8 V		25°C	70	90		dB
I_{SC}	Short-circuit current	V_{ID} = ±1 V, V_O = 2.5 V	Source	25°C	3	6		mA
			Sink		3	6		
V_{OH}	High-level output voltage	V_{CC+} = 30 V, R_L = 10 kΩ		25°C	27	28		V
				Full range	26			
V_{OL}	Low-level output voltage	R_L = 10 kΩ		25°C		130	170	mV
				Full range			200	
SR	Slew rate	V_{CC} = ±15 V, C_L = 100 pF, V_I = ±10 V, R_L = 10 kΩ		25°C	1.3	2		V/µs
GBW	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF, f = 100 kHz		25°C	1.4	2.1		MHz
Φm	Phase margin	R_L = 10 kΩ, C_L = 100 pF		25°C		45		°
THD	Total harmonic distortion			25°C		0.01		%
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		19		nV/√Hz

Comparator Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C			5	mV
			Full range			9	
V_{ID}	Comparator differential input voltage		Full range			V_{CC+}	V
I_{IO}	Input offset current		25°C			50	nA
			Full range			150	
I_{IB}	Input bias current		25°C			250	nA
			Full range			400	
I_{OH}	High-level output current	V_{ID} = 1 V, V_{CC} = V_O = 30 V	25°C		0.1		nA
			Full range			1	µA
V_{OL}	Low-level output voltage	V_{ID} = –1 V, I_{sink} = 4 mA	25°C		250	400	mV
			Full range			700	
A_{VD}	Large-signal voltage gain	V_{CC+} = 15 V, R1 = 15 kΩ, V_O = 1 V to 11 V	25°C		200		V/mV
I_{sink}	Output sink current	V_O = 1.5 V, V_{ID} = –1 V	25°C	6	16		mA
V_{ICM}	Input common-mode voltage range		25°C	0		V_{CC+} – 1.5	V
			Full range	0		V_{CC+} – 2	
t_{RESP}	Response time (1)	R1 = 5.1 kΩ to V_{CC+}, V_{REF} = 1.4 V	25°C		1.3		µs
$t_{RESP,large}$	Large-signal response time	R1 = 5.1 kΩ to V_{CC+}, V_{REF} = 1.4 V, V_I = TTL	25°C		300		ns

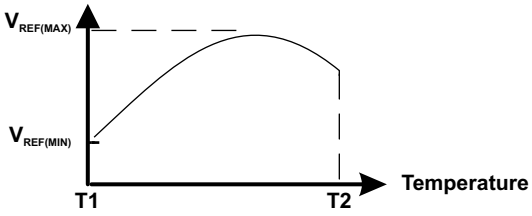
(1) The response-time specification is for 100-mV input step with 5-mV overdrive. For larger overdrive signals, 300 ns can be obtained.

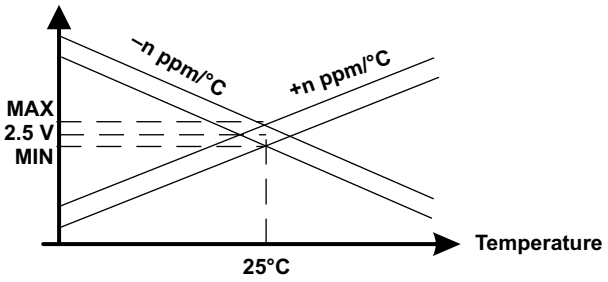
Voltage-Reference Electrical Characteristics

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage(1)	TSM102	$V_{KA} = V_{REF}$, I_K = 10 mA, See Figure 1	25°C	2.475	2.5	2.525	V
		TSM102A		25°C	2.49	2.5	2.51	
ΔV_{REF}	Reference input voltage deviation over temperature range(1)		$V_{KA} = V_{REF}$, I_K = 10 mA, See Figure 1	Full range		7	30	mV
$\frac{\Delta V_{REF}}{\Delta T}$	Average temperature coefficient of reference input voltage(2)		$V_{KA} = V_{REF}$, I_K = 10 mA	Full range		±22	±100	ppm/°C
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Ratio of change in reference voltage to change in cathode voltage		V_{KA} = 3 V to 36 V, I_K = 10 mA, See Figure 2	25°C		–1.1	–2	mV/V
I_{REF}	Reference input current		I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, See Figure 2	25°C		1.5	2.5	µA
				Full range			3	
ΔI_{REF}	Reference input current deviation over temperature range		I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, See Figure 2	Full range		0.5	1	µA
I_{min}	Minimum cathode current for regulation		$V_{KA} = V_{REF}$, See Figure 1	25°C		0.5	1	mA
$I_{K,OFF}$	Off-state cathode current		See Figure 3	25°C		180	500	nA

(1) ΔV_{REF} is defined as the difference between the maximum and minimum values obtained over the full temperature range.
$\Delta V_{REF} = V_{REF(MAX)} - V_{REF(MIN)}$

(2) The temperature coefficient is defined as the slopes (positive and negative) of the voltage vs temperature limits within which the reference voltage is specified.





PARAMETER MEASUREMENT INFORMATION

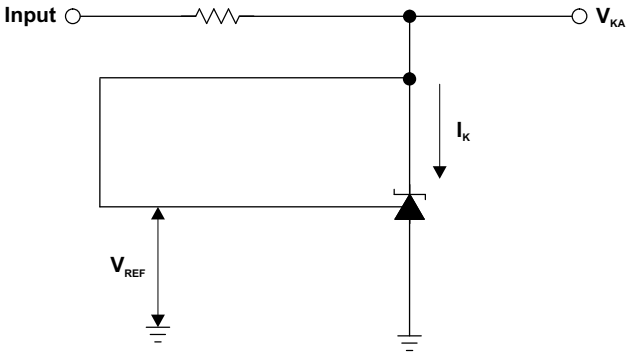


Figure 1. Test Circuit for $V_{KA} = V_{REF}$

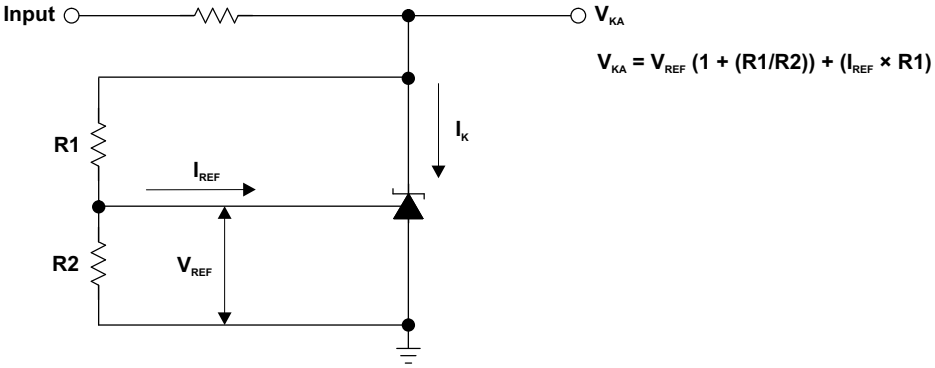


Figure 2. Test Circuit for $V_{KA} > V_{REF}$

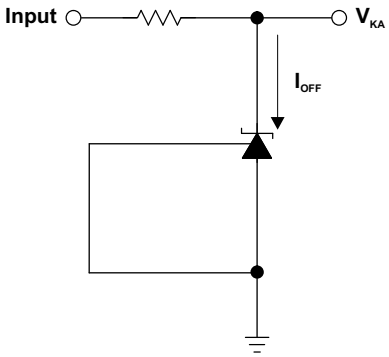


Figure 3. Test Circuit for I_{OFF}

TYPICAL CHARACTERISTICS

AMPLIFIER TOTAL HARMONIC DISTORTION vs FREQUENCY

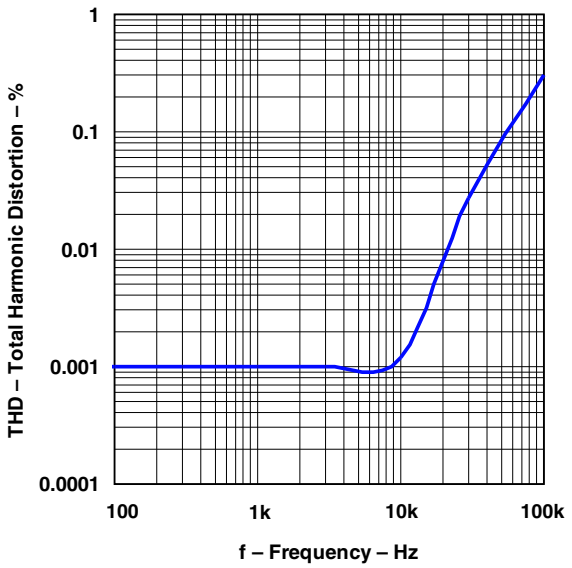


Figure 4.

AMPLIFIER NOISE VOLTAGE vs FREQUENCY

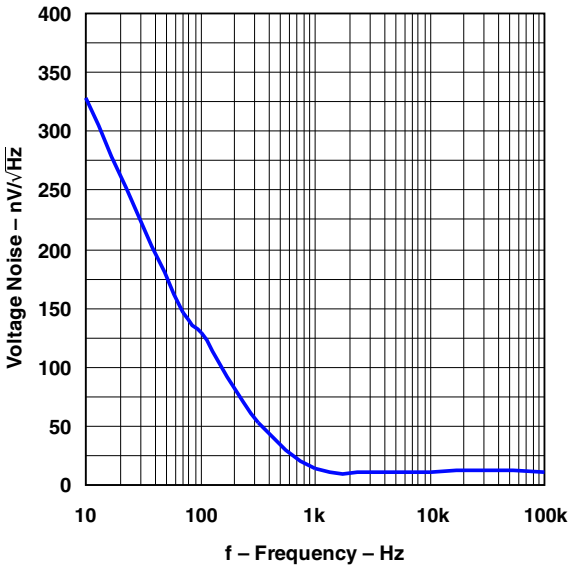


Figure 5.

GAIN AND PHASE vs FREQUENCY

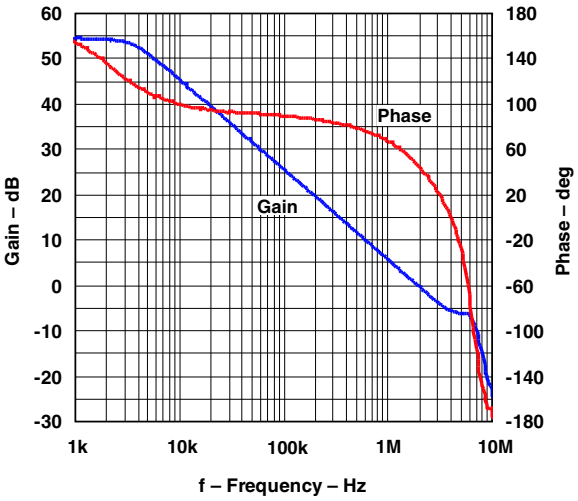


Figure 6.

V_{REF} STABILITY vs CAPACITANCE

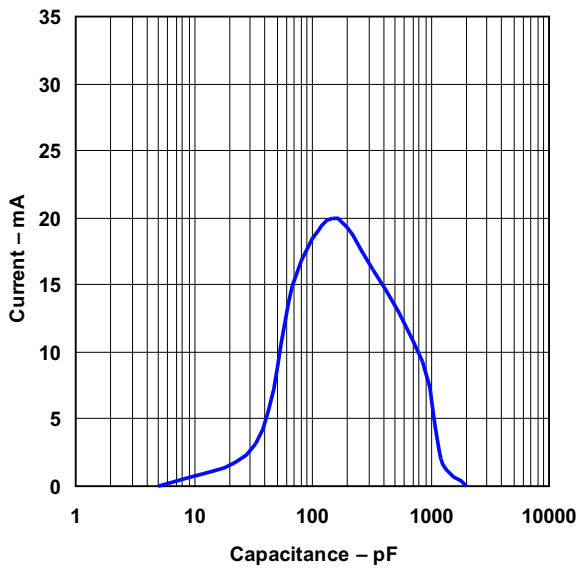


Figure 7.

TYPICAL CHARACTERISTICS (continued)

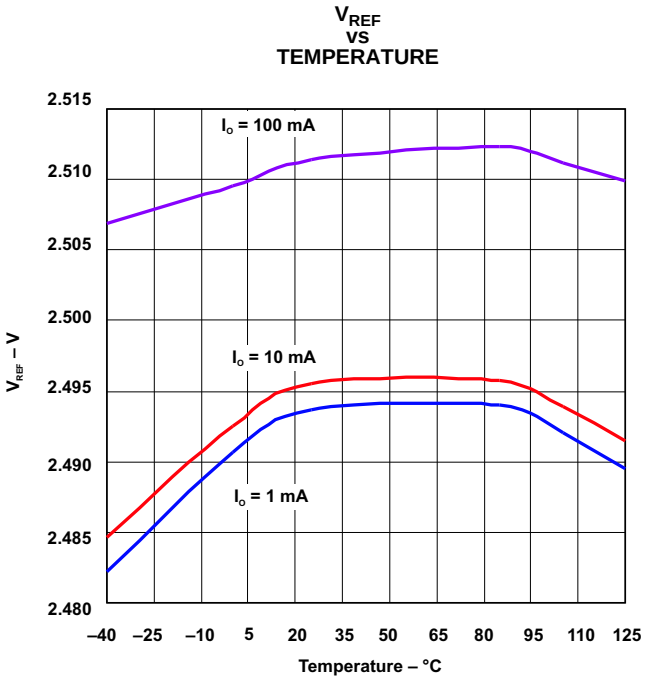


Figure 8.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSM102AIDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102AI
TSM102AIDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102AI
TSM102AIPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI
TSM102AIPW.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI
TSM102AIPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI
TSM102AIPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102AI
TSM102ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I
TSM102ID.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I
TSM102IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I
TSM102IDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TSM102I
TSM102IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102I
TSM102IPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN102I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

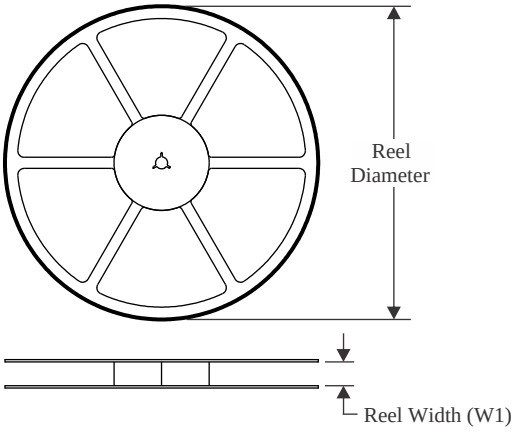
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

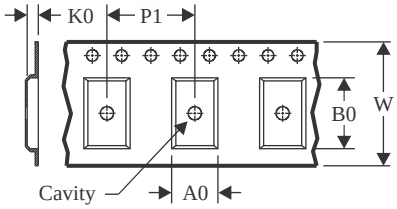
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

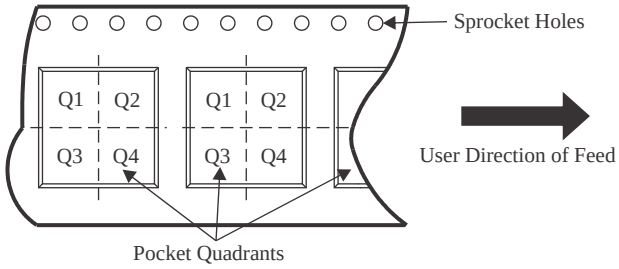


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

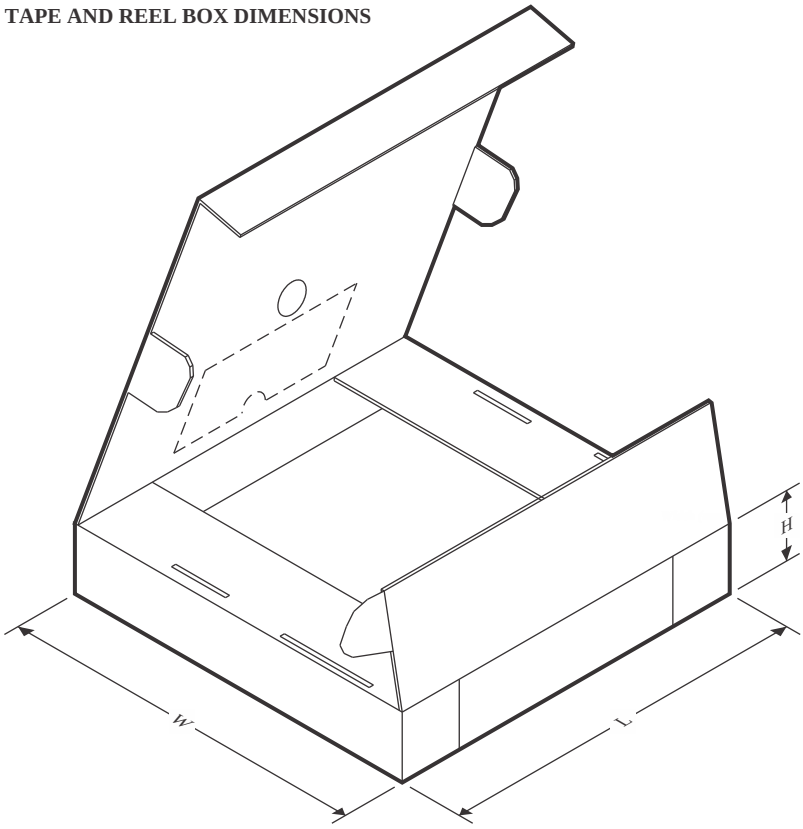
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM102AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TSM102AIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSM102IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TSM102IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

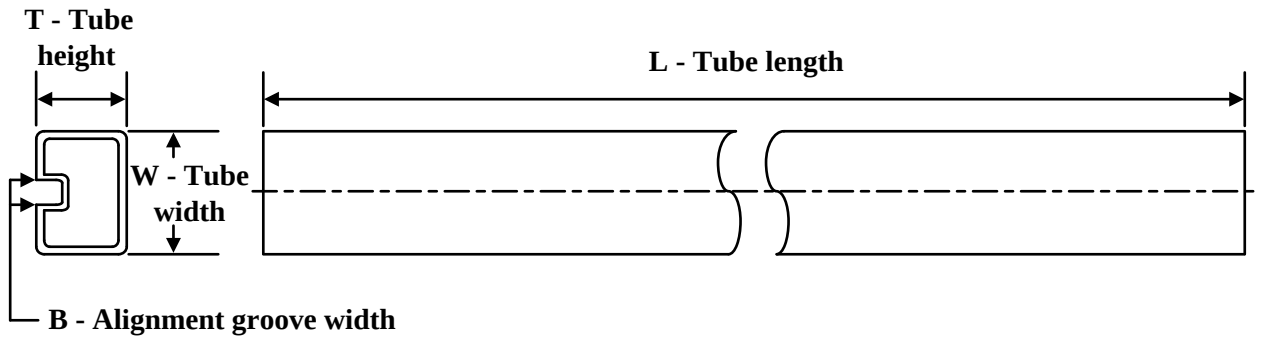
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSM102AIDR	SOIC	D	16	2500	353.0	353.0	32.0
TSM102AIPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TSM102IDR	SOIC	D	16	2500	353.0	353.0	32.0
TSM102IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

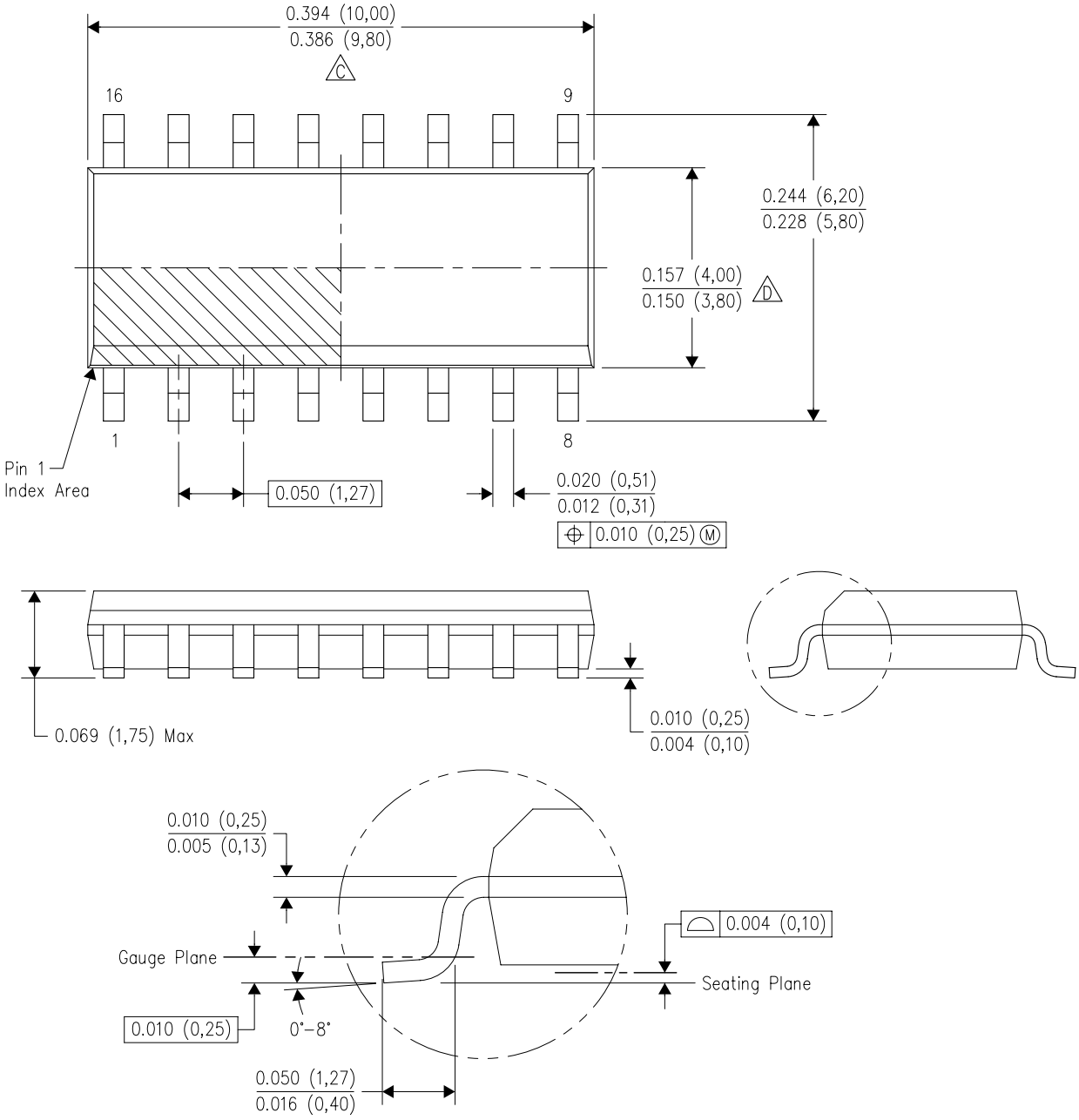
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TSM102AIPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TSM102AIPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5
TSM102ID	D	SOIC	16	40	506.6	8	3940	4.32
TSM102ID.A	D	SOIC	16	40	506.6	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



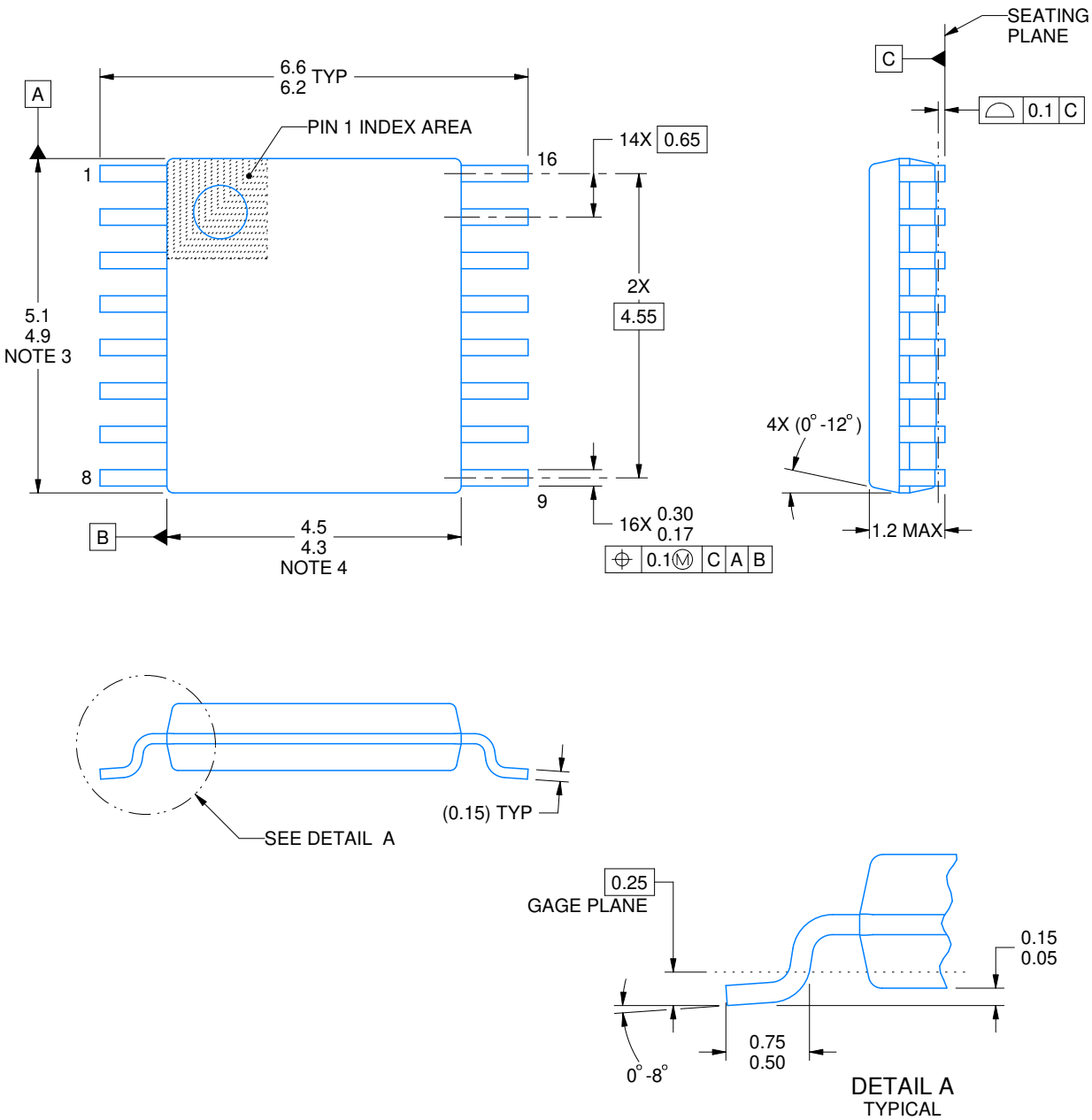
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

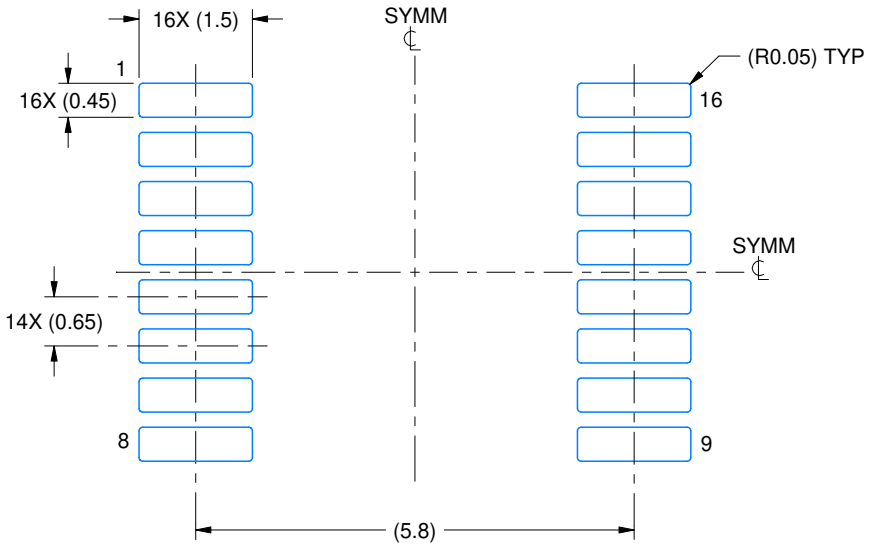
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

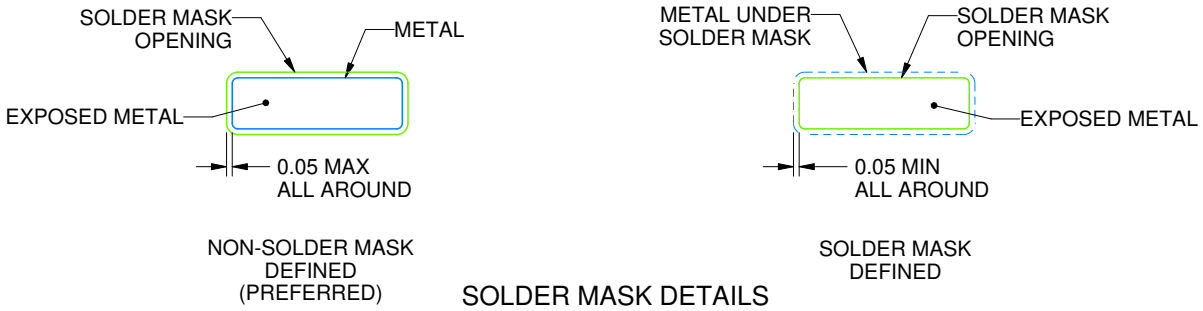


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

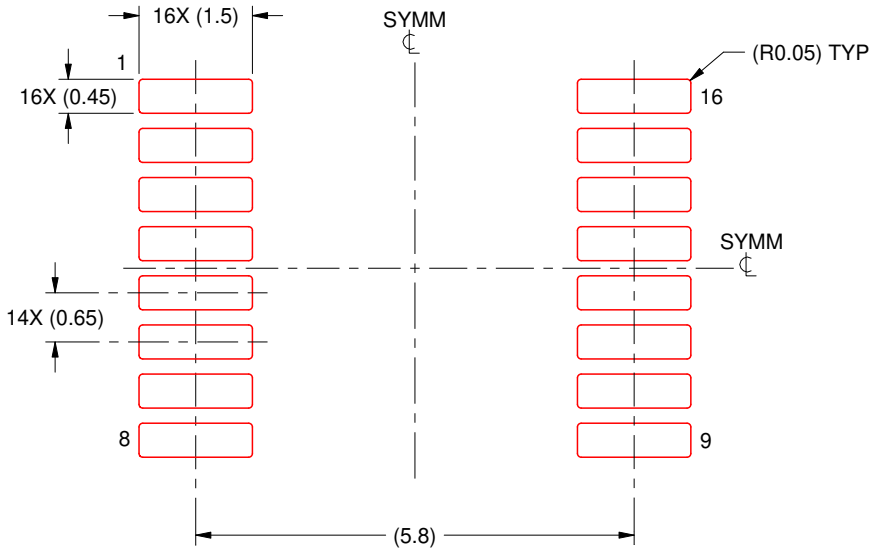


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025