TUSB8040A
Four-Port USB 3.0 Hub

Data Manual

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Four-Port USB 3.0 Hub

Check for Samples: TUSB8040A

1 PRODUCT OVERVIEW

1.1 Features

- USB 3.0 Compliant Hub, TID# 330000037
  - Upstream Port Supports SuperSpeed USB, High-Speed and Full-Speed Connections
  - Supports Four Downstream Ports
  - Each of the Four Downstream Ports Support SuperSpeed USB, High-Speed, Full-Speed or Low-Speed Connections
- USB 2.0 Hub Features
  - Multi Transaction Translator (MTT) Hub: Four Transaction Translators, One Per Port
  - Four Asynchronous Endpoint Buffers Per Transaction Translator (TT) for Better Throughput Than the USB Required Minimum of Two Buffers Per TT
- Supports Battery Charging Applications
  - Battery Charging 1.2 Compliant Charging Downstream Port (CDP) when Upstream Port is Connected
  - Battery Charging 1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009 Compliant Dedicated Charging Port (DCP) when Upstream Port is Disconnected
- Supports Operation as a USB 3.0 or USB 2.0 Compound Device
- Supports Per Port or Ganged Power Switching and Over-Current Notification Inputs
- Provides the following status outputs:
  - High-Speed Upstream Connection
  - High-Speed Upstream Port Suspended
  - SuperSpeed USB Upstream Connection
  - SuperSpeed USB Upstream Port Suspended
- Optional Serial EEPROM or SMBus Slave Interface for Custom Configurations:
  - VID or PID
  - Manufacturer and Product Strings
  - Serial Number
- Using Pin Selection or EEPROM and SMBus Slave Interface, Each Downstream Port Can Be Independently:
  - Enabled or Disabled
  - Marked as Removable or Permanently Attached (for Compound Applications)
  - Have Battery Charging Enabled or Disabled
- Provides 128-Bit Universally Unique Identifier (UUID)
- Optionally Supports USB 2.0 Compliant Port Indicator LEDs
- Configurable SMBus Address to Support Multiple Devices on the Same SMBus Segment
- Supports On-Board and In-System EEPROM Programming Via the USB 2.0 Upstream Port
- Single Clock Input, 24-MHz Crystal or Oscillator
- No Special Driver Requirements; Works Seamlessly With Any Operating System With USB Stack Support

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1.2 Applications

- **Computer Systems**
- **Docking Stations**
- **Monitors**
- **Set-top Boxes**

1.3 Introduction

The TUSB8040A is a four-port USB 3.0 compliant hub and is available in a 100-pin QFN package. The device is designed for operation over the commercial temperature range of 0°C to 70°C.

The TUSB8040A provides simultaneous SuperSpeed USB and high-speed or full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, full-speed, or low-speed connections on the downstream ports. When the upstream port is connected to an electrical environment that only supports high-speed, full-speed or low-speed connections, SuperSpeed USB connectivity is disabled on the downstream ports. When the upstream port is connected to an electrical environment that only supports full-speed or low-speed connections, SuperSpeed USB and high-speed connectivity are disabled on the downstream ports.

The TUSB8040A supports up to four downstream ports. It may be configured to report one to four downstream ports by pin selection or by an attached EEPROM or SMBus controller. The configuration options provide the ability to scale the device by application.

A typical system view of the TUSB8040A is shown in Figure 1-1.

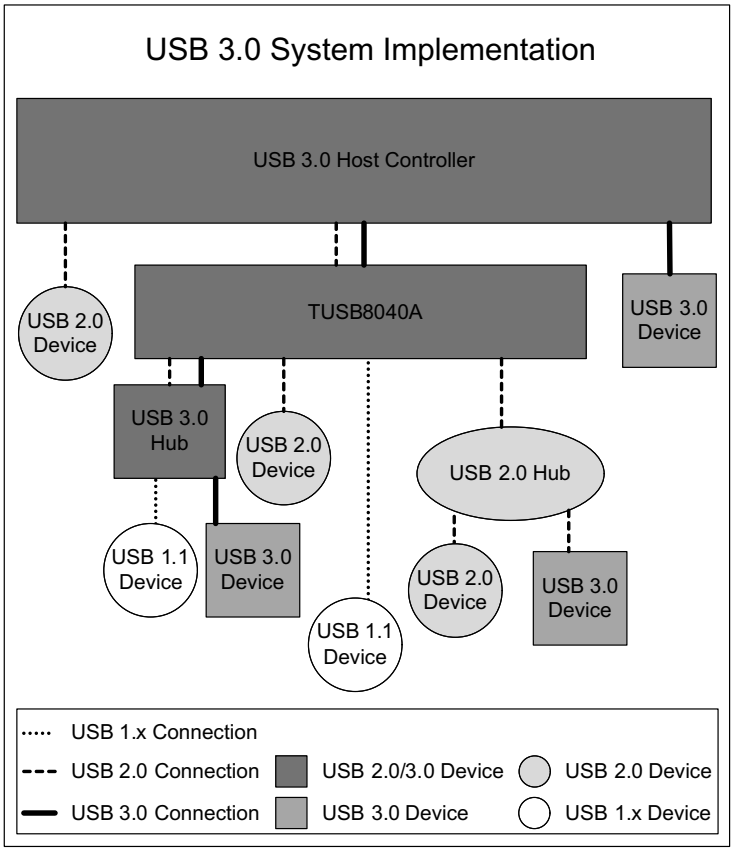


Figure 1-1. Typical Application

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1.4 Functional Description

The TUSB8040A supports per port or ganged power switching and over-current protection.

An individually port power controlled hub switches power on or off to each downstream port as requested by the USB host. Also when an individually port power controlled hub senses an over-current event, only power to the affected downstream port will be switched off.

A ganged hub switches on power to all its downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also when a ganged hub senses an over-current event, power to all downstream ports will be switched off.

The TUSB8040A also provides customization using an I^2C EEPROM or configuration via an SMBus host for vendor specific PID, VID, and strings. For the TUSB8040A ports can also be marked as disabled or permanently attached using pin selection, I^2C EEPROM or an SMBus host. The Device Status and Command Register at F8h cannot be modified by the contents of the I^2C EEPROM.

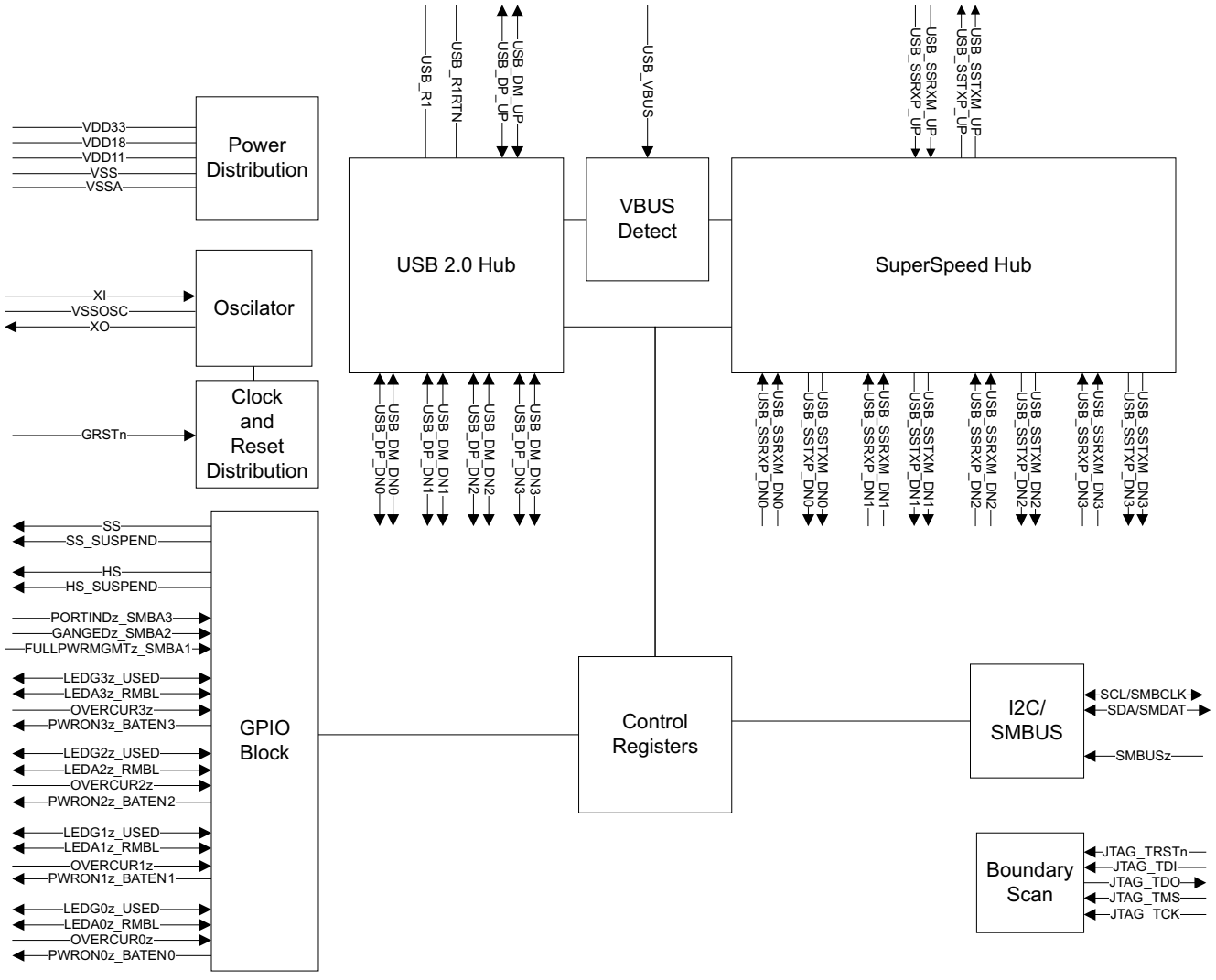
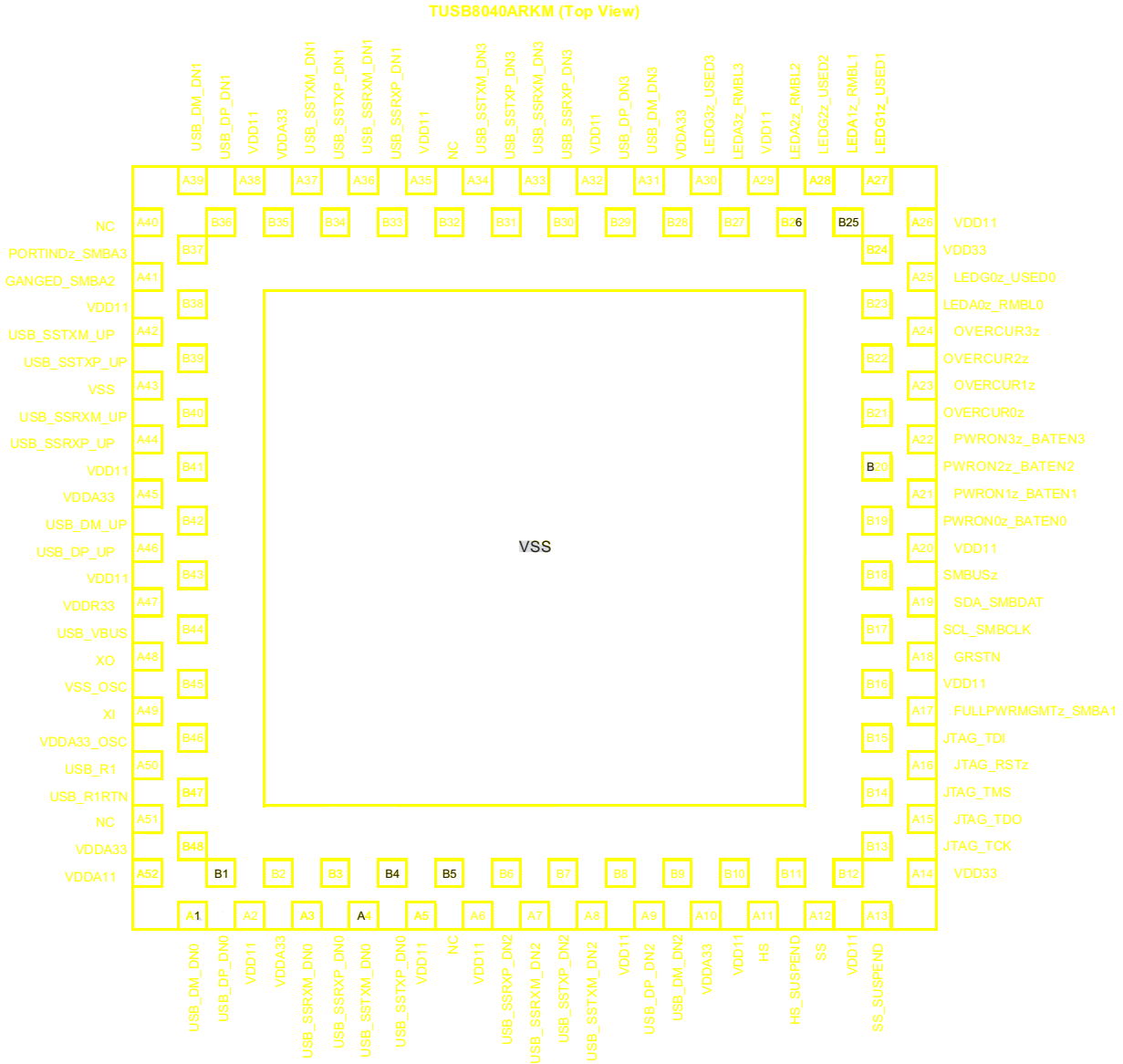


Figure 1-2. TUSB8040A Functional Block Diagram

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2 PIN DESCRIPTIONS



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2.1 Signal Descriptions

Table 2-1. Signal Descriptions

TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input/output
PD, PU	Internal pull-down/pull-up
PT	Passive pass through
P	Power Supply
G	Ground

2.2 Clock and Reset Signals

Table 2-2. Clock and Reset Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
GRSTz	I, PU	A18	Global power reset. This reset brings all of the TUSB8040A internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional. GRSTz should be asserted a minimum of 3 ms after all power rails are valid at the device.
XI	I	A49	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
XO	O	A48	Crystal output. This terminal is crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between XI and XO.
VSSOSC	I	B45	Oscillator return. If using a crystal, the load capacitors should use this signal as the return path and it should not be connected to the PCB ground. If using an oscillator, this terminal should be connected to PCB Ground.

2.3 USB Upstream Signals

Table 2-3. USB Upstream Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
USB_SSTXP_UP	O	B39	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_UP	O	A42	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_UP	I	A44	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_UP	I	B40	USB SuperSpeed receiver differential pair (negative)
USB_DP_UP	I/O	A46	USB high-speed differential transceiver (positive)
USB_DM_UP	I/O	B42	USB high-speed differential transceiver (negative)
USB_R1	PT	A50	Precision resistor reference. A 9.09-kΩ ±1% resistor should be connected between USB_R1 and USB_R1RTN.
USB_R1RTN	PT	B47	Precision resistor reference return
USB_VBUS	I	B44	USB Upstream port power monitor. The USB_VBUS input is a 1.2-V I/O cell and requires a voltage divider to prevent damage to the input. The signal USB_VBUS must be connected to VBUS through a 90.9-kΩ ±1% resistor, and to signal ground through a 10-kΩ ±1% resistor. This allows the input to detect VBUS present from a minimum of 4 V and sustain a maximum VBUS voltage up to 10 V (applied to the voltage divider).

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2.4 USB Downstream Signals

Table 2-4. USB Downstream Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
USB_SSTXP_DN0	O	B4	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN0	O	A4	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN0	I	B3	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN0	I	A3	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN0	I/O	B1	USB high-speed differential transceiver (positive)
USB_DM_DN0	I/O	A1	USB high-speed differential transceiver (negative)
PWRON0z_BATEN0	I/O, PD	B19	USB Port 0 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch; in addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charger support for the port as indicated in the Battery Charger Support register: 0 = Battery charging not supported 1 = Battery charging supported This terminal provides the port power control for all downstream ports if GANGED_SMBA2 = 1. This terminal also determines the battery charging support of all downstream ports if GANGED_SMBA2 = 1.
OVERCUR0z	I, PU	B21	USB Port 0 over-current detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This terminal should be pulled high using a 10-kΩ resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power switch.
USB_SSTXP_DN1	O	B34	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN1	O	A37	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN1	I	B33	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN1	I	A36	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN1	I/O	B36	USB High-speed differential transceiver (positive)
USB_DM_DN1	I/O	A39	USB High-speed differential transceiver (negative)
PWRON1z_BATEN1	I/O, PD	A21	USB Port 1 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch for Port 1. In addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 1 as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR1z	I, PU	A23	USB Downstream Port 1 Over-Current Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This terminal should be pulled high using a 10-kΩ resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power management device.
USB_SSTXP_DN2	O	B7	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN2	O	A8	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN2	I	B6	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN2	I	A7	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN2	I/O	A9	USB High-speed differential transceiver (positive)
USB_DM_DN2	I/O	B9	USB High-speed differential transceiver (negative)

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Table 2-4. USB Downstream Signals (continued)

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
PWRON2z_BATEN2	I/O, PD	B20	USB Port 2 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch for Port 2. In addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 2 as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR2z	I, PU	B22	USB Downstream Port 2 Over-Current Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This terminal should be pulled high using a 10-kΩ resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power management device.
USB_SSTXP_DN3	O	B31	USB SuperSpeed transmitter differential pair (positive)
USB_SSTXM_DN3	O	A34	USB SuperSpeed transmitter differential pair (negative)
USB_SSRXP_DN3	I	B30	USB SuperSpeed receiver differential pair (positive)
USB_SSRXM_DN3	I	A33	USB SuperSpeed receiver differential pair (negative)
USB_DP_DN3	I/O	B29	USB High-speed differential transceiver (positive)
USB_DM_DN3	I/O	A31	USB High-speed differential transceiver (negative)
PWRON3z_BATEN3	I/O, PD	A22	USB Port 3 Power On Control for Downstream Power/Battery Charging Enable. The terminal is used for control of the downstream power switch for Port 3. In addition, the value of the terminal is sampled at the de-assertion of reset to determine the value of the battery charger support for Port 3 as indicated in the Battery Charger Support register: 0 = Battery Charging Not Supported 1 = Battery Charging Supported
OVERCUR3z	I, PU	A24	USB Downstream Port 3 Over-Current Detection. 0 = An overcurrent event has occurred 1 = An overcurrent event has not occurred This terminal should be pulled high using a 10K resistor if power management is not implemented. If power management is enabled, the external circuitry needed should be determined by the power management device.
LEDA0z_RMBL0	I, PU	B23	USB Port 0 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable
LEDA1z_RMBL1	I/O, PU	B25	USB Port 1 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable
LEDA2z_RMBL2	I/O, PU	B26	USB Port 2 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable
LEDA3z_RMBL3	I/O, PU	B27	USB Port 3 Amber LED Indicator & Device Removable Configuration Bit 1 = Device is Removable 0 = Device is NOT Removable
LEDG0z_USED0	I/O, PU	A25	USB Port 0 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used
LEDG1z_USED1	I/O, PU	A27	USB Port 1 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used

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Table 2-4. USB Downstream Signals (continued)

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
LEDG2z_USED2	I/O, PU	A28	USB Port 2 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used
LEDG3z_USED3	I/O, PU	A30	USB Port 3 Green LED Indictor & Port Used Configuration Bit 1 = Port Used 0 = Port is NOT Used

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2.5 I²C/SMBUS Signals

Table 2-5. I²C/SMBUS Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
SCL/SMBCLK	I/O, PD	B17	I²C clock/SMBus clock. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial clock interface for an I²C EEPROM. When SMBUSz = 0, this terminal acts as the serial clock interface for an SMBus host. The SCL_SMBCLK terminal is sampled at the deassertion of reset to determine if SuperSpeed USB low power states U1 and U2 are initiated. If SCL_SMBCLK is low, (default), U1 / U2 power states are enabled. If SCL_SMBCLK is high, entry to U1 / U2 power states is not initiated by the hub downstream ports, but is accepted. This input is over-ridden if SDA_SMBDAT is sampled as a '1'. If an EEPROM is installed, U1/U2 power state support is controlled by the Device Configuration Register. Can be left unconnected if external interface not implemented.
SDA/SMBDAT	I/O, PD	A19	I²C data/SMBus data. Function of terminal depends on the setting of the SMBUSz input. When SMBUSz = 1, this terminal acts as the serial data interface for an I²C EEPROM. When SMBUSz = 0, this terminal acts as the serial data interface for an SMBus host. The SDA_SMBDAT terminal is sampled at the deassertion of reset to determine if SuperSpeed USB low power states U1 and U2 are disabled. If SDA_SMBDAT is high, U1 and U2 low power states are disabled. If SDA_SMBDAT is low, U1 and U2 low power states are enabled. If the optional EEPROM or SMBUS is implemented, the value of the u1u2Disable bit of the Device Configuration Register determines if the low power states U1 and U2 are enabled. Can be left unconnected if external interface not implemented and U1 and U2 are to be enabled.
SMBUSz	I, PU	B18	I²C/SMBus mode select. 1 = I²C Mode Selected 0 = SMBus Mode Selected Can be left unconnected if external interface not implemented.

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2.6 Test and Miscellaneous Signals

Table 2-6. Test and Miscellaneous Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
JTAG_TCK	I/O, PD	B13	JTAG test clock. Can be left unconnected.
JTAG_TDI	I/O, PU	B15	JTAG test data in. Can be left unconnected.
JTAG_TDO	I/O, PD	A15	JTAG test data out. Can be left unconnected.
JTAG_TMS	I/O, PU	B14	JTAG test mode select. Can be left unconnected.
JTAG_RSTz	I/O, PD	A16	JTAG reset. Pull down using an external 1-kΩ resistor for normal operation.
HS_SUSPEND	I/O, PD	B11	High-speed suspend status output. 0 = High-speed upstream port not suspended 1= High-speed upstream port suspended The value of the terminal is sampled at the deassertion of reset to determine the polarity of the PWRONxz_BATENx pins. If it is sampled as a '0' (default), the polarity is active low. If it is sampled as a '1', the polarity is active high. Can be left unconnected.
SS_SUSPEND	I/O, PD	A13	SuperSpeed USB suspend status output. 0 = SuperSpeed USB upstream port not suspended 1= SuperSpeed USB upstream port suspended The value of the terminal is sampled at the deassertion of reset to determine if spread spectrum clocking is enabled or disabled. If it is sampled as a '0' (default), SSC is enabled. If it is sampled as a '1', SSC is disabled. Can be left unconnected.
HS	O	A11	High-speed status. The terminal is to indicate the connection status of the upstream port as documented below: 0 = Hub in low/full speed mode 1 = Hub in high-speed mode Can be left unconnected.
SS	O	A12	SuperSpeed USB status. The terminal is to indicate the connection status of the upstream port as documented below: 0 = Hub not in SuperSpeed USB mode 1 = Hub in SuperSpeed USB mode Can be left unconnected.
FULLPWRMGMTz_SMBA1	I, PU	A17	Full power management enable/SMBus address bit 1. The value of the terminal is sampled at the de-assertion of reset to set the power switch control follows: 0 = Full power management supported 1 = Full Power management not supported Full power management is the ability to control power to the downstream ports of the TUSB8040 using the PWRON0z_BATEN0 terminal. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 1. SMBus slave address bits 2 and 3 are always 1 for the TUSB8040. When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 1. Can be left unconnected if full power management and SMBus are not implemented.
GANGED_SMBA2	I, PU	A41	Ganged operation enable/SMBus Address bit 2. The value of the terminal is sampled at the deassertion of reset to set the power switch and over current detection mode as follows: 0 = Power indicator LEDs are enabled 1 = Power indicator LEDs are NOT enabled When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 3.

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Table 2-6. Test and Miscellaneous Signals (continued)

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
PORTINDz_SMBA3	I, PU	B37	Port Indicator LED Status/SMBus Address bit 3. The value of the terminal is sampled at the deassertion of reset to determine the port indicator support for the hub as follows: 0 = Port Indicator LEDs are enabled 1 = Port Indicator LEDs are not enabled When SMBus mode is enabled using SMBUSz, this terminal sets the value of the SMBus slave address bit 3.

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2.7 Power Signals

Table 2-7. Power Signals

SIGNAL NAME	TYPE	PIN NO.	DESCRIPTION
VDD33	P	B2, A10, A14, B24, B28, B35, A45, A47, B46, B48	3.3-V power rail
VDD11	P	A2, A5, A6, B8, B10, B12, B16, A20, A26, A29, A32, A35, A38, B38, B41, B43, A52	1.1-V power rail
GND	G	A43, A53	Ground, Power Pad
GND_NC	G	C1, C2, C3, C4	The corner pins, which are for mechanical stability of the package, are connected to ground internally. These pins may be connected to GND or left unconnected.
NC	NC	A40, A51, B5, B32,	No connect

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3 FUNCTIONAL DESCRIPTION

3.1 TUSB8040A Register Map

Table 3-1. TUSB8040A Register Map

BYTE ADDRESS	CONTENTS
00h	ROM Signature (55h)
01h	Vendor ID LSB
02h	Vendor ID MSB
03h	Product ID LSB
04h	Product ID MSB
05h	Device Configuration Register
06h	Battery Charging Support Register
07h	Device Removable Configuration Register
08h	Port Used Configuration Register
09h-0Fh	Reserved
10h-1Fh	Reserved
20h-21h	LangID Byte [1:0]
22h	Serial Number String Length
23h	Manufacturer String Length
24h	Product String Length
25h-2Fh	Reserved
30h-4Fh	Serial Number String Byte [31:0]
50h-8Fh	Manufacturer String Byte [63:0]
90h-CFh	Product String Byte [63:0]
D0-F7h	Reserved
F8h	Device Status and Command Register
F9-FFh	Reserved

3.2 I_2C EEPROM Operation

The TUSB8040A supports a single-master, standard mode (100 kbit/s) connection to a dedicated I^2C EEPROM when the I^2C interface mode is enabled. In I^2C mode, the TUSB8040A reads the contents of the EEPROM at bus address 1010000b using 7-bit addressing starting at address 0. If the value of the EEPROM contents at byte 00h equals 55h, the TUSB8040A loads the configuration registers according to the EEPROM map. If the first byte is not 55h, the TUSB8040A exits the I^2C mode and continues execution with the default values in the configuration registers. The hub will not connect on the upstream port until the configuration is completed.

Note, the bytes located below offset 9h are optional. The requirement for data in those addresses is dependent on the options configured in the Device Configuration and Phy Custom Configuration registers.

For details on I^2C operation refer to the UM10204 I^2C-bus Specification and User Manual.

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3.3 SMBus Slave Operation

When the SMBus interface mode is enabled, the TUSB8040A supports read block and write block protocols as a slave-only SMBus device.

The TUSB8040ARKM slave address is 1000 pgxy, where:

- p is the state of PORTINDz_SMBA3 at reset,
- g is the state of GANGED_SMBA2 at reset,
- x is the state of FULLPWRMGMTz_SMBA1 at reset, and
- y indicates read (logic 1) or write (logic 0) access.

If the TUSB8040A is addressed by a host using an unsupported protocol it will not respond. The TUSB8040A will wait indefinitely for configuration by the SMBus host and will not connect on the upstream port until the SMBus host indicates configuration is complete by clearing the CFG_ACTIVE bit.

For details on SMBus requirements refer to the System Management Bus Specification.

3.4 Configuration Registers

The internal configuration registers are accessed on byte boundaries. The configuration register values are loaded with defaults but can be over-written when the TUSB8040A is in I^2C or SMBus mode.

3.4.1 ROM Signature Register

Table 3-2. Register Offset 0h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 3-3. Bit Descriptions – ROM Signature Register

Bit	Field Name	Access	Description
7:0	romSignature	RW	ROM Signature Register. This register is used by the TUSB8040A in I^2C mode to validate the attached EEPROM has been programmed. The first byte of the EEPROM is compared to the mask 55h and if not a match, the TUSB8040A aborts the EEPROM load and executes with the register defaults.

3.4.2 Vendor ID LSB Register

Table 3-4. Register Offset 1h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	1	0	1	0	0	0	1

Table 3-5. Bit Descriptions – Vendor ID LSB Register

Bit	Field Name	Access	Description
7:0	vendorIdLsb	RW	Vendor ID LSB. Least significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 51h representing the LSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID.

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3.4.3 Vendor ID MSB Register

Table 3-6. Register Offset 2h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0

Table 3-7. Bit Descriptions – Vendor ID MSB Register

Bit	Field Name	Access	Description
7:0	vendorIdMsb	RW	Vendor ID MSB. Most significant byte of the unique vendor ID assigned by the USB-IF; the default value of this register is 04h representing the MSB of the TI Vendor ID 0451h. The value may be over-written to indicate a customer Vendor ID.

3.4.4 Product ID LSB Register

Table 3-8. Register Offset 3h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	X	X	0	0	0	0	1

Table 3-9. Bit Descriptions – Vendor ID LSB Register

Bit	Field Name	Access	Description
7:0	productIdLsb	RW	Product ID LSB. Least significant byte of the product ID assigned by Texas Instruments; the default value of this register is 41h representing the LSB of the product ID assigned by Texas Instruments. The value of this register will be reported as configured for the SuperSpeed USB Device descriptor. The USB 2.0 Device descriptor will report the value in this register with bit [1] toggled. This ensures that the USB drivers load properly for both hubs. The value may be over-written to indicate a customer product ID.

3.4.5 Product ID MSB Register

Table 3-10. Register Offset 4h

Bit No.	7	6	5	4	3	2	1	0
Reset State	1	0	0	0	0	0	0	0

Table 3-11. Bit Descriptions – Vendor ID MSB Register

Bit	Field Name	Access	Description
7:0	productIdMsb	RW	Product ID MSB. Most significant byte of the product ID assigned by Texas Instruments; the default value of this register is 80h representing the MSB of the product ID assigned by Texas Instruments. The value may be over-written to indicate a customer product ID.

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3.4.6 Device Configuration Register

Table 3-12. Register Offset 5h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	X	X	X	X	0

Table 3-13. Bit Descriptions – Device Configuration Register

Bit	Field Name	Access	Description
6	customSernum	RW	Custom Serial Number Enable. When the TUSB8040A is in I^2C mode, the TUSB8040A loads the serial number register from the contents of the EEPROM. When the TUSB8040A is in SMBUS mode, the Serial Number registers may written by an SMBus host. This bit defaults to 0.
5	u1u2Disable	RW	U1 U2 Disable. When this bit is set the TUSB8040A will not initiate or accept any U1 or U2 requests on any port, upstream or downstream, unless it receives or sends a Force_LinkPM_Accept LMP. After receiving or sending an FLPMA LMP, it will continue to enable U1 and U2 according to USB 3.0 protocol until it gets a power-on reset or is disconnected on its upstream port. This bit is loaded at the de-assertion of reset with the value of the SDA_SMBDAT terminal. When the TUSB8040A is in I^2C mode, the TUSB8040A loads this bit from the contents of the EEPROM. When the TUSB8040A is in SMBUS mode, the value may be over-written by an SMBus host.
4	portIndz	RW	Port Indicator Status. This bit shall be loaded at the de-assertion of reset with the value of PORTINDz_SMBA3 terminal. When the TUSB8040A is in I^2C mode, the TUSB8040A loads this bit from the contents of the EEPROM. When the TUSB8040A is in SMBUS mode, the value may be overwritten by an SMBus host.
3	ganged	RW	Ganged. This bit shall be loaded at the de-assertion of reset with the value of GANGEd_SMBA2 terminal. When the TUSB8040A is in I^2C mode, the TUSB8040A loads this bit from the contents of the EEPROM. When the TUSB8040A is in SMBUS mode, the value may be overwritten by an SMBus host.
2	fullPwrMgmtz	RW	Full Power Management. This bit is loaded at the de-assertion of reset with the value of the FULLPWRMGMTz_SMBA1 terminal. When this bit is 0, power switching and over-current detection is supported whether bus- or self-powered. When the bit is 1 and the device is bus powered, power switching is supported but over-current detection is not supported. When the bit is 1 and the device is self-powered over-current detection is supported but power switching is not supported. When the TUSB8040A is in I^2C mode, the TUSB8040A loads this bit from the contents of the EEPROM. When the TUSB8040A is in SMBUS mode, the value may be over-written by an SMBus host.
1	u1u2TimerOvr	RW	U1 U2 Timer Override. When this bit is set the TUSB8040A will override the downstream ports u1/u2 timeout values set by software. If software sets a value in the range of 1-FF, the TUSB8040A will use the value FF. If software sets a value of 0, the TUSB8040A will use the value 0.This bit is loaded at the de-assertion of reset with the value of the SCL_SMBCLK terminal. When the TUSB8040A is in I^2C mode, the TUSB8040A loads this bit from the contents of the EEPROM. When the TUSB8040A is in SMBUS mode, the value may be over-written by an SMBus host.
0	RSVD	RO	Reserved. Read only, returns 0 when read.

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3.4.7 Battery Charging Support Register

Table 3-14. Register Offset 6h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	X	X	X	X

Table 3-15. Bit Descriptions – Battery Charging Support Register

Bit	Field Name	Access	Description
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	batEn[3:0]	RW	Battery Charger Support. The bits in this field indicate whether the downstream port implements the charging port features. A value of 0 indicates the port does not implement the charging port features. A value of 1 indicates the port does support the charging port features. Each bit corresponds directly to a downstream port, i.e. batEn0 corresponds to downstream port 0. When in I^2C/SMBus mode the bits in this field corresponding to the enabled ports per used[3:0] may be over-written by EEPROM contents or by an SMBus host. The default value for these bits are loaded at the de-assertion of reset with the value of the PWRON[3:0]z_BATEN[3:0] as follows: bateEn[3:0] defaults to wxyzb, where w is PWRON3z_BATEN3, x is PWRON2z_BATEN2, y is PWRON1z_BATEN1 and z is PWRON0z_BATEN0.

3.4.8 Device Removable Configuration Register

Table 3-16. Register Offset 7h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	X	X	X	X

Table 3-17. Bit Descriptions – Device Removable Configuration Register

Bit	Field Name	Access	Description
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	rmbl[3:0]	RW	Removable. The bits in this field indicate whether a device attached to downstream ports 3 through 0 are removable or permanently attached. A value of 0 indicates the device attached to the port is not removable. A value of 1 indicates the device attached to the port is removable. The default value for these bits are loaded at the de-assertion of reset with the value of LEDA[3:0]z_RMBL[3:0] as follows: rmbl[3:0] defaults to wxyzb, where w is LEDA3z_RMBL3, x is LEDA2z_RMBL2, y is LEDA1z_RMBL1 and z is LEDA0z_RMBL0.

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3.4.9 Port Used Configuration Register

Table 3-18. Register Offset 8h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	X	X	X	X

Table 3-19. Bit Descriptions – Port Used Configuration Register

Bit	Field Name	Access	Description
7:4	RSVD	RO	Reserved. Read only, returns 0 when read.
3:0	used[3:0]	RW	Used. The bits in this field indicate whether downstream ports 3 through 0 are enabled or disabled for use. A value of 0 indicates the port is not used. A value of 1 indicates the port is used. The default value for these bits are loaded at the de-assertion of reset with the value of LEDG[3:0]z_USED[3:0] as follows: used[3:0] defaults to wxyzb, where w is LEDG3z_USED3, x is LEDG2z_USED2, y is LEDG1z_USED1 and z is LEDG0z_USED0.

3.4.10 Language ID LSB Register

Table 3-20. Register Offset 20h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	1	0	0	1

Table 3-21. Bit Descriptions – Language ID LSB Register

Bit	Field Name	Access	Description
7:0	langIdLsb	RW	Language ID least significant byte. This register contains the value returned in the LSB of the LANGID code in string index 0. The TUSB8040A only supports one language ID. The default value of this register is 09h representing the LSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

3.4.11 Language ID MSB Register

Table 3-22. Register Offset 21h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	1	0	0

Table 3-23. Bit Descriptions – Language ID MSB Register

Bit	Field Name	Access	Description
7:0	langIdMsb	RW	Language ID most significant byte. This register contains the value returned in the MSB of the LANGID code in string index 0. The TUSB8040A only supports one language ID. The default value of this register is 04h representing the MSB of the LangID 0409h indicating English United States. When customStrings is 1, this field may be over-written by the contents of an attached EEPROM or by an SMBus host.

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3.4.12 Serial Number String Length Register

Table 3-24. Register Offset 22h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 3-25. Bit Descriptions – Serial Number String Length Register

Bit	Field Name	Access	Description
7:6	RSVD	RO	Reserved. Read only, returns 0 when read.
5:0	serNumStringLen	RW	Serial number string length. The string length in bytes for the serial number string. The default value is 0, indicating that a serial number string is not supported. The maximum string length is 32 bytes. This field may be over-written by the contents of an attached EEPROM or by an SMBus host. When the field is non-zero, a serial number string of serNumbStringLen bytes is returned at string index 1 from the data contained in the Serial Number String registers.

3.4.13 Manufacturer String Length Register

Table 3-26. Register Offset 23h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 3-27. Bit Descriptions – Manufacturer String Length Register

Bit	Field Name	Access	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	mfgStringLen	RW	Manufacturer string length. The string length in bytes for the manufacturer string. The default value is 0, indicating that a manufacturer string is not provided. The maximum string length is 64 bytes. When the field is non-zero, a manufacturer string of mfgStringLen bytes is returned at string index 3 from the data contained in the Manufacturer String registers.

3.4.14 Product String Length Register

Table 3-28. Register Offset 24h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 3-29. Bit Descriptions – Product String Length Register

Bit	Field Name	Access	Description
7	RSVD	RO	Reserved. Read only, returns 0 when read.
6:0	prodStringLen	RW	Product string length. The string length in bytes for the product string. The default value is 0, indicating that a product string is not provided. The maximum string length is 64 bytes. When the field is non-zero, a product string of prodStringLen bytes is returned at string index 2 from the data contained in the Product String registers.

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3.4.15 Serial Number Registers

Table 3-30. Register Offset 30h-4Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	X	X	x	x	x	x	x	x

Table 3-31. Bit Descriptions – Serial Number Registers

Bit	Field Name	Access	Description
7:0	serialNumber[n]	RW	Serial Number byte N. The serial number returned in the Serial Number string descriptor at string index 1. The default value of these registers is calculated from the Die ID fields in the fuseRom. When customSernum is 1, these registers may be over-written by EEPROM contents or by an SMBus host. The serial number will be returned in USB 2.0 descriptor of the TUSB8040A.

3.4.16 Manufacturer String Registers

Table 3-32. Register Offset 50h-8Fh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 3-33. Bit Descriptions – Manufacturer String Registers

Bit	Field Name	Access	Description
7:0	mfgStringByte[n]	RW	Manufacturer string byte N. These registers provide the string values returned for string index 3 when mfgStringLen is greater than 0. The number of bytes returned in the string is equal to mfgStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

3.4.17 Product String Registers

Table 3-34. Register Offset 90h-CFh

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 3-35. Bit Descriptions – Product String Registers

Bit	Field Name	Access	Description
7:0	prodStringByte[n]	RW	Product string byte N. These registers provide the string values returned for string index 2 when prodStringLen is greater than 0. The number of bytes returned in the string is equal to prodStringLen. The programmed data should be in UNICODE UTF-16LE encodings as defined by The Unicode Standard, Worldwide Character Encoding, Version 5.0.

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3.4.18 Device Status and Command Register

Table 3-36. Register Offset F8h

Bit No.	7	6	5	4	3	2	1	0
Reset State	0	0	0	0	0	0	0	0

Table 3-37. Bit Descriptions – Device Status and Command Register

Bit	Field Name	Access	Description
7:2	RSVD	RO	Reserved. Read only, returns 0 when read.
1	smbusRst	RSU	SMBus interface reset. This bit resets the SMBus slave interface to its default state and loads the registers back to their GRSTz values. This bit is set by writing a 1 and is cleared by hardware on completion of the reset. A write of 0 has no effect. (Not used with I^2C)
0	cfgActive	RCU	Configuration active. This bit indicates that configuration of the TUSB8040A is currently active. The bit is set by hardware when the device enters the I^2C or SMBus mode. The TUSB8040A does not connect on the upstream port while this bit is 1.When in I^2C mode, the bit is cleared by hardware when the TUSB8040A exits the I^2C mode. When in the SMBus mode, this bit must be cleared by the SMBus host in order to exit the configuration mode and allow the upstream port to connect. The bit is cleared by a writing 1. A write of 0 has no effect.

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4 CLOCK GENERATION

The TUSB8040A accepts a crystal input to drive an internal oscillator or an external clock source. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below. Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

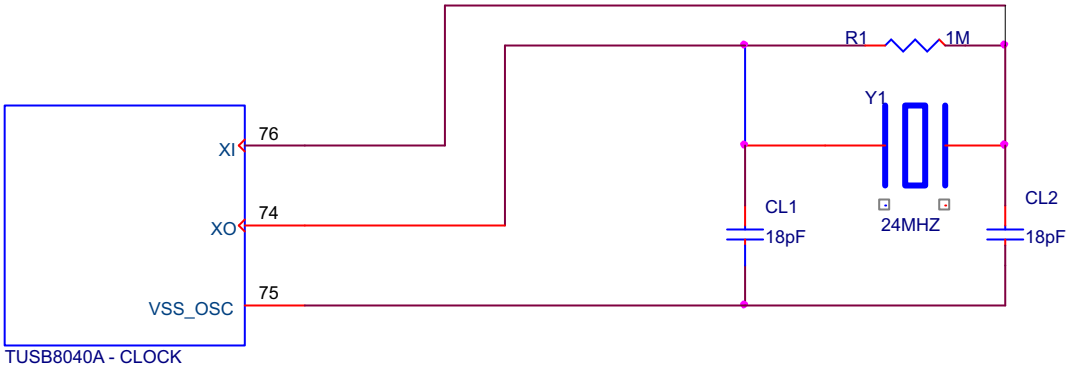


Figure 4-1. TUSB8040A Clock

4.1 Crystal Requirements

The crystal must be fundamental mode with load capacitance of 12 pF to 24 pF and frequency stability rating of ±100 PPM or better. To ensure proper startup oscillation condition, a maximum crystal equivalent series resistance (ESR) of 50 Ω is recommended. A parallel, 18-pF load capacitor should be used if a crystal source is used. VSSOSC should not be connected to the PCB ground plane.

4.2 Input Clock Requirements

When using an external clock source such as an oscillator, the reference clock should have a ±100 PPM or better frequency stability and have less than 50-ps absolute peak to peak jitter or less than 25-ps peak to peak jitter after applying the USB 3.0 jitter transfer function. XI should be tied to the 1.8-V clock source and XO should be left floating. VSSOSC should be connected to the PCB ground plane.

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5 POWER UP AND RESET

The TUSB8040A does not have specific power sequencing requirements with respect to the core power (VDD11) or I/O and analog power (VDD33). The core power (VDD11) or I/O power (VDD33) may be powered up for an indefinite period of time while the other is not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 3 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. This can be generated using programmable-delay supervisory device or using an RC circuit.

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6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{DD33}	Steady-state supply voltage	-0.3 to 3.8	V
V_{DD11}		-0.3 to 1.4	
V_{IO}	USB 2.0 DP/DM	-0.3 to VDD33 + 0.3 ≤ 3.8	V
	SuperSpeed USB TXP/M and RXP/M	-0.3 to VDD33 + 0.3 ≤ 3.8	
	XI/XO	-0.3 to 1.98	
	3.3-V Tolerant I/O	-0.3 to VDD33 + 0.3 ≤ 3.8	
V_{USB_VBUS}		-0.3 to 1.2	V
T_{stg}	Storage temperature range	-65 to 150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Expose to absolute-maximum-rated conditions for extended periods may affect device reliability

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD33}	Steady-state supply voltage	3	3.3	3.6	V
V_{DD11} (1)		0.99	1.1	1.26	
V_{IO}	USB 2.0 DP/DM	0		VDD33	V
	SuperSpeed USB TXP/M and RXP/M	0		VDD33	
	XI/XO	0		1.8	
	3.3-V Tolerant I/O	0		VDD33	
V_{USB_VBUS}		0		1.155	V
T_A	Operating free-air temperature range	0	25	70	°C
T_J	Operating junction temperature range	0	25	105	°C

(1) A 1.05-V supply may be used as long as minimum supply conditions are met.

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6.3 Thermal Information

THERMAL METRIC		TUSB8040A RKM 100 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance (1)	25.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (2)	9.5	
θ_{JB}	Junction-to-board thermal resistance (3)	15.2	
ψ_{JT}	Junction-to-top characterization parameter (4)	0.1	
ψ_{JB}	Junction-to-board characterization parameter (5)	7.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (6)	0.4	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.4 3.3-V I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage (1)	VDD33		2	VDD33	V
V_{IL}	Low-level input voltage (1)	VDD33		0	0.8	V
			JTAG pins only	0	0.55	
V_I	Input voltage			0	VDD33	V
V_O	Output voltage (2)			0	VDD33	V
t_t	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis (3)				0.13 x VDD33	V
V_{OH}	High-level output voltage	VDD33	I_{OH} = -4 mA	2.4		V
V_{OL}	Low-level output voltage	VDD33	I_{OL} = 4 mA		0.4	V
I_{OZ}	High-impedance, output current (2)	VDD33	V_I = 0 to VDD33		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor (4)	VDD33	V_I = 0 to VDD33		±225	µA
I_I	Input current (5)	VDD33	V_I = 0 to VDD33		±15	µA

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) Applies to GRSTz.
(4) Applies to pins with internal pullups/pulldowns.
(5) Applies to external input buffers.

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6.5 Hub Input Supply Current

Typical values measured at T_A = 25°C

PARAMETER	VDD33	VDD11	UNIT
	3.3 V	1.1 V	
LOW POWER MODES			
Power On (after Reset)	4	68	mA
Upstream Disconnect	4	68	mA
Suspend	4	68	mA
ACTIVE MODES (US state / DS State)			
3.0 host / 1 SS Device and Hub in U1	46	260	mA
3.0 host / 1 SS Device and Hub in U0	46	400	mA
3.0 host / 2 SS Devices and Hub in U1	46	330	mA
3.0 host / 2 SS Devices and Hub in U0	46	540	mA
3.0 host / 3 SS Devices and Hub in U1	46	420	mA
3.0 host / 3 SS Devices and Hub in U0	46	650	mA
3.0 host / 4 SS Devices and Hub in U1	46	560	mA
3.0 host / 4 SS Devices and Hub in U0	46	770	mA
3.0 host / 1 SS and 1 HS Devices in U0 and active	90	430	mA
3.0 host / 2 SS and 2 HS Devices in U0 and active	105	570	mA
2.0 host / HS Device active	46	90	mA
2.0 host / 4 HS Device active	90	115	mA

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TUSB8040ARKMR	NRND	Production	WQFN-MR (RKM) | 100	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8040A RKM
TUSB8040ARKMR.A	NRND	Production	WQFN-MR (RKM) | 100	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8040A RKM
TUSB8040ARKMT	NRND	Production	WQFN-MR (RKM) | 100	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8040A RKM
TUSB8040ARKMT.A	NRND	Production	WQFN-MR (RKM) | 100	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB8040A RKM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

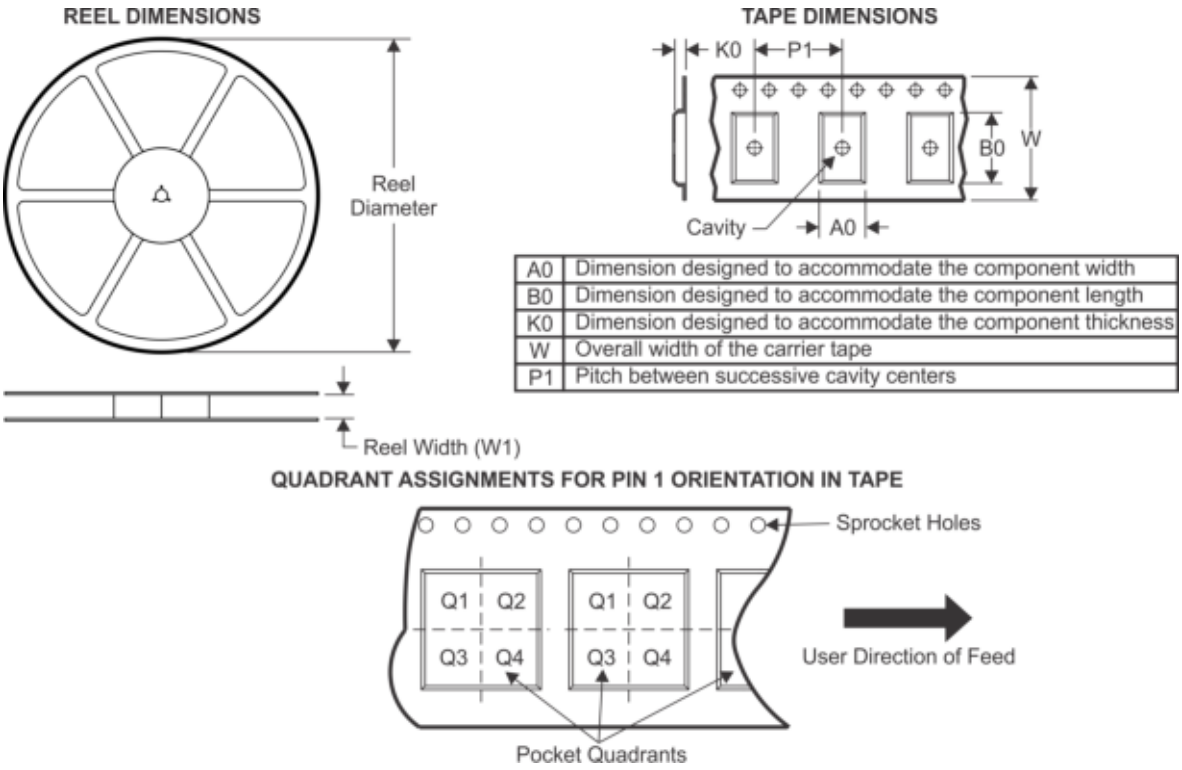
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

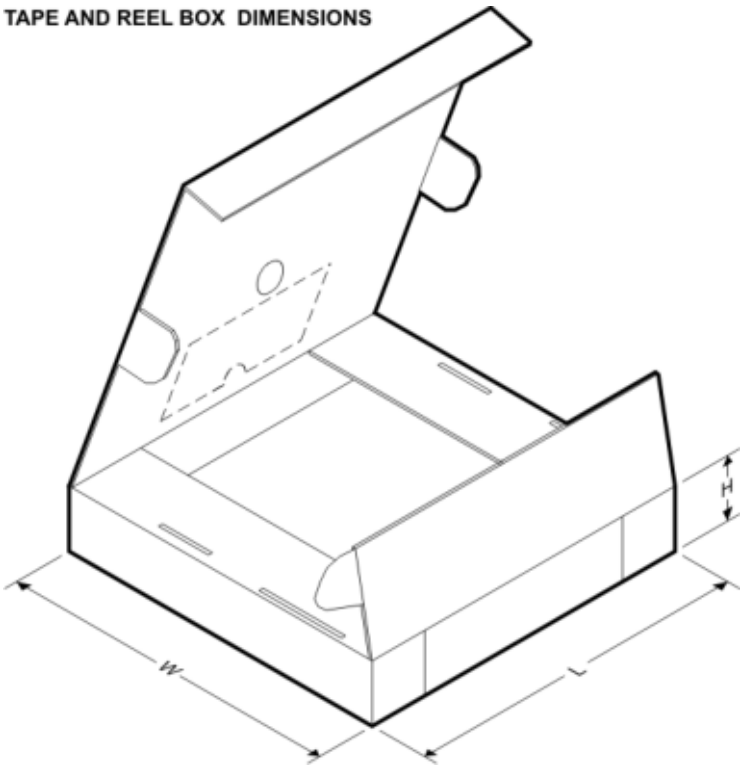


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB8040ARKMR	WQFN-MR	RKM	100	3000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
TUSB8040ARKMT	WQFN-MR	RKM	100	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

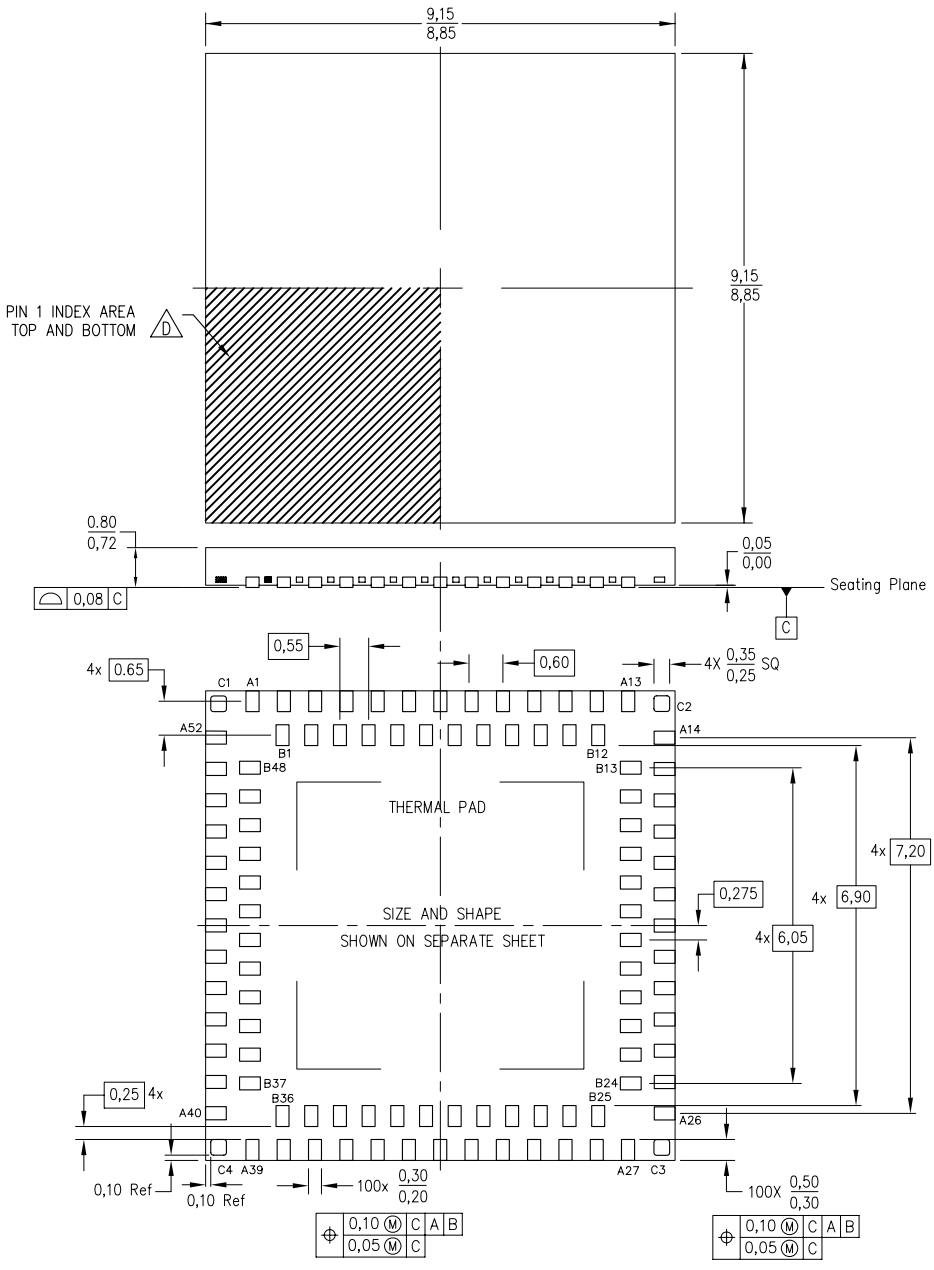
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB8040ARKMR	WQFN-MR	RKM	100	3000	367.0	367.0	38.0
TUSB8040ARKMT	WQFN-MR	RKM	100	250	210.0	185.0	35.0

RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD



4211055/C 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) staggered multi–row package configuration.
D. Pin A1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin A1 identifiers are either a molded, marked, or metal feature.
E. The package thermal pad must be soldered to the board for thermal and mechanical performance.
F. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

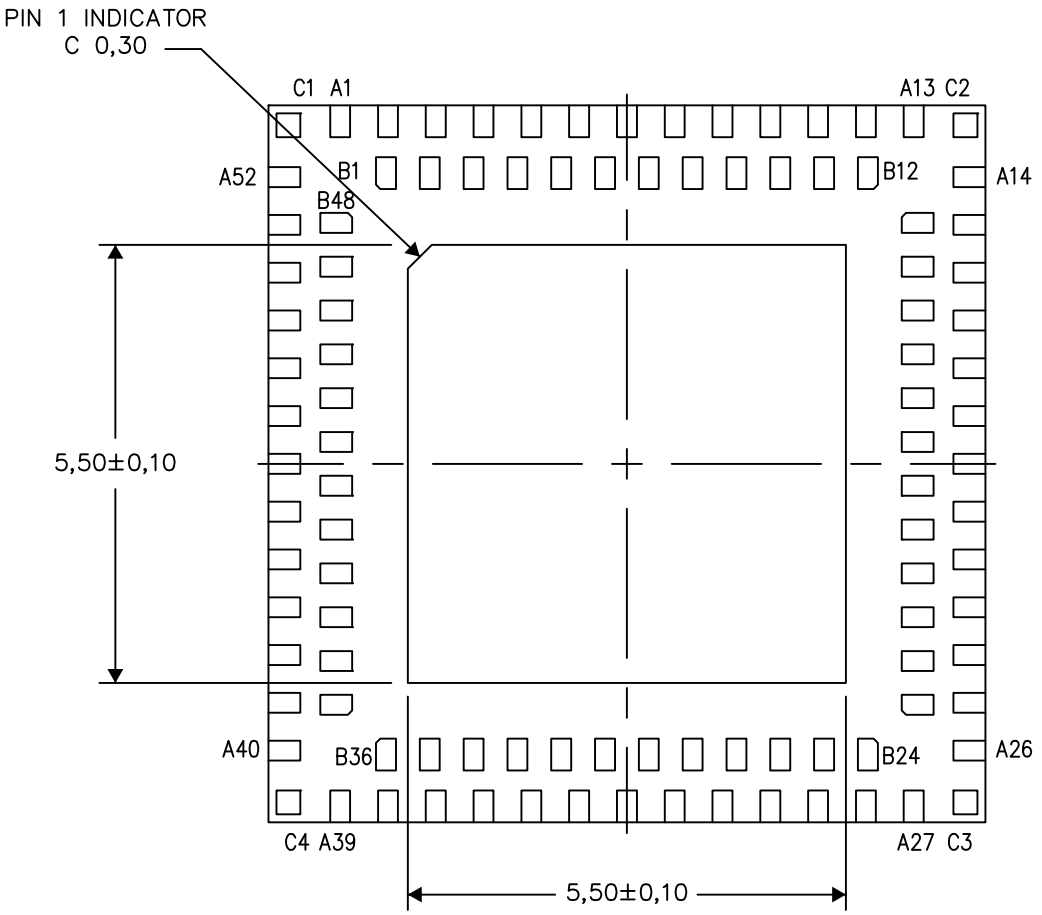
RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

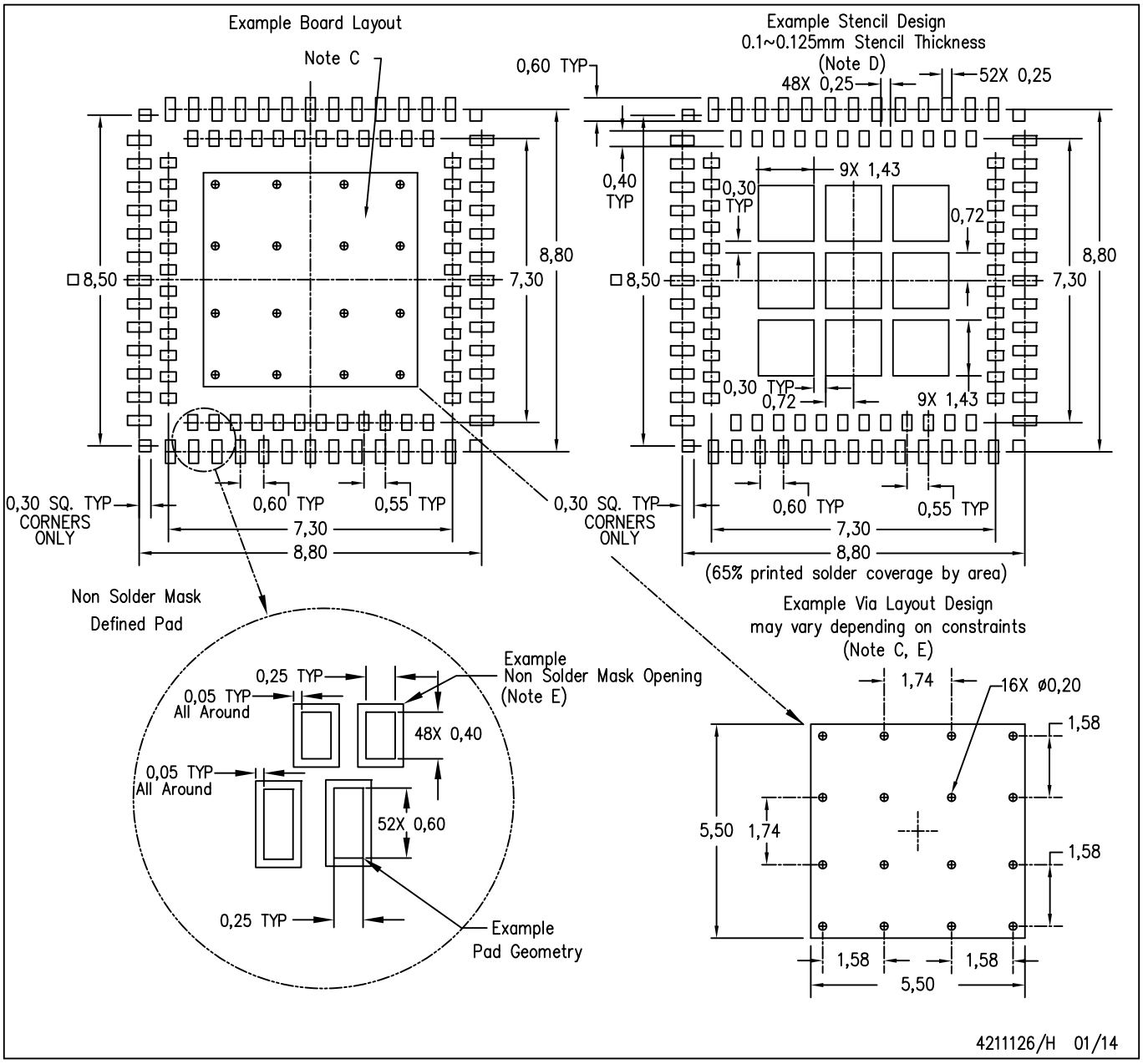


Bottom View

Exposed Thermal Pad Dimensions 4211101/D 01/14

NOTE: All linear dimensions are in millimeters

RKM (S–PWQFN–N100) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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