# uP1966E

## Dual-Channel Gate Driver for Enhanced Mode GaN Transistors

## General Description

The uP1966E is designed to drive both high-side and low-side GaN FETs in half bridge topologies. It integrates an internal bootstrap supply and UVLO. The uP1966E has split gate outputs that can operate to several MHz on both high and low side drive channels, providing the ability to adjust both turn-on and turn-off transition times independently. A clamping circuit is used on the high side drive to keep unwanted transients from damaging GaN device gates. The uP1966E has two PWM inputs that independently control high side and low side drive signals. The uP1966E is available in a 12-pin WLCSP package that minimizes package inductance for improved high-speed operation. The uP1966E comes in a 1.6mm WLCSP1.6x1.6-12B package.

## Features

- **0.4Ω/0.7Ω Pull-Down/Pull-Up Resistance**
- **Fast Propagation Delays (20ns,Typical)**
- **Fast Rise and Fall Times (8ns/4ns,Typical)**
- **Adjustable Output for Turn-On/Turn-Off Ability**
- **CMOS Compatible Input Logic Threshold**
- **WLCSP 1.6x1.6-12B Package**
- **RoHS Compliant and Halogen Free**

## Ordering Information

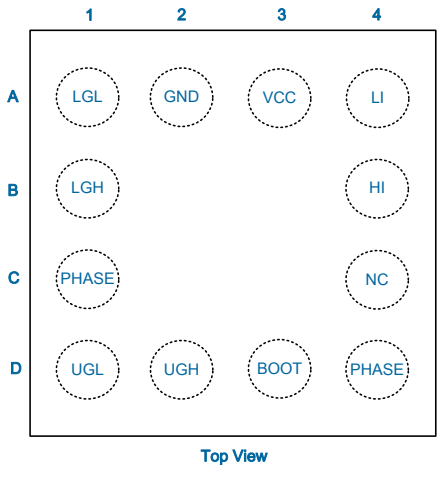
| Order Number | Package Type | Top Marking |
|---|---|---|
| uP1966EFBB | WLCSP1.6x1.6-12B | WY |

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

## Applications

- **Half-Bridge and Full-Bridge Converters**
- **High Input Voltage Converters**

## Pin Configuration

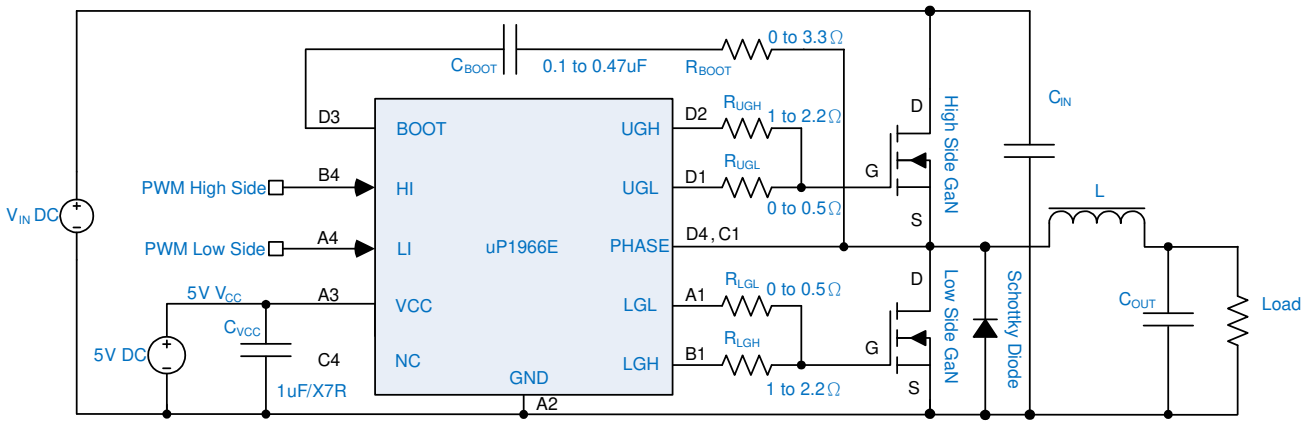



Top View


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# uP1966E

## Typical Application Circuit




Note:

1. The external damp resistor of the driver makes the most appropriate selection based on different GaN FET.
2. The Schottky Diode is recommended and the reverse voltage of Schottky Diode is selected based on the GaN FET.



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## Functional Pin Description

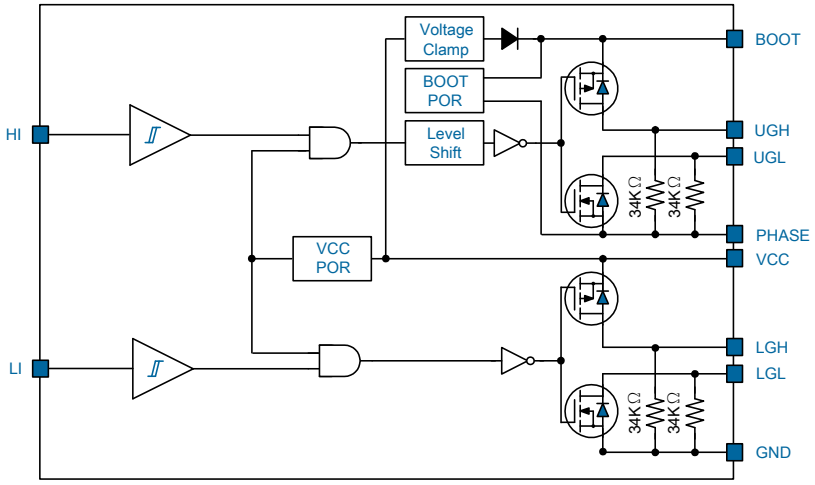
| Pin No. | Name | Pin Function |
|---|---|---|
| B4 | HI | **High Side Driver PWM Input.** Connect this pin to the high side driver control PWM input. |
| A4 | LI | **Low Side Driver PWM Input.** Connect this pin to the low side driver control PWM input. |
| A3 | VCC | **Supply Voltage for the IC.** This pin provides bias voltage for the IC. Connect this pin to 5V voltage source with at least 1uF MLCC bypass capacitor. |
| C1,D4 | PHASE | **PHASE Switch Node.** Connect this pin to the source of the upper GaN FET and the drain of the lower GaN FET. This pin is used as the return path for the UGATE driver. |
| D3 | BOOT | **Bootstrap Supply.** For the floating upper gate driver. Connect the bootstrap capacitor $C_{BOOT}$ between BOOT pin and PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper GaN FET. Make sure that $C_{BOOT}$ is placed near the IC. |
| D2 | UGH | **Upper Gate Driver Turn-On Output.** Connect this pin to the gate of upper GaN FET. Use a resistor to set the turn-on speed. |
| D1 | UGL | **Upper Gate Driver Turn-Off Output.** Connect this pin to the gate of upper GaN FET. Use a resistor to set the turn-off speed. |
| B1 | LGH | **Lower Gate Driver Turn-On Output.** Connect this pin to the gate of lower GaN FET. Use a resistor to set the turn-on speed. |
| A1 | LGL | **Lower Gate Driver Turn-Off Output.** Connect this pin to the gate of lower GaN FET. Use a resistor to set the turn-off speed. |
| A2 | GND | **Ground for the IC.** All voltage levels are measured with respect to this pin. |
| C4 | NC | **Not Internally Connected.** |



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# uP1966E

## Functional Block Diagram





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## Functional Description

**Under Voltage Protection (UVLO)**

When the uP1966E detects a starting threshold voltage level of 4.0V (typical) on a rising edge, the device will go from its 120uA quiescent current state to normal operation. The uP1966E will turn off after the input falls 0.35V below the starting threshold. A POR signal is initiated from the UVLO circuit that is used internally to assure that the output(s) will only function if the drive voltage levels are valid (~5V).

**PWM Inputs**

There are two non-inverting inputs, HI and LI, that control the two output channels of the uP1966E. Provided that a POR is granted, the HI PWM input at a logic high turns on the high-side gate driver output, UGH, turns off UGL. When the HI PWM input goes low the high-side gate driver output, UGL, and turns on, UGH turns off.

The LI PWM input at a logic high turns on the low-side gate driver output, LGH, turns off LGL. When the LI PWM input goes low the low-side gate driver output, LGL, and turns on, LGH turns off.

***There is no lockout between HI and LI inputs: both GaN devices can be driven on at the same time.***

If these inputs are not used they should be tied to ground. Although there is a 200kΩ resistor to ground on each PWM input under no circumstances should either of these inputs be allowed to float. Figure 1 shows the typical operation of the PWM Input in a synchronous regulator application. LI turns off, add delay time (a “dead time”) determined by external control then HI turns on. In reverse, HI turns off, add a delay time, and then LI turns on. The minimum delay time of 30ns is recommended for operation application.

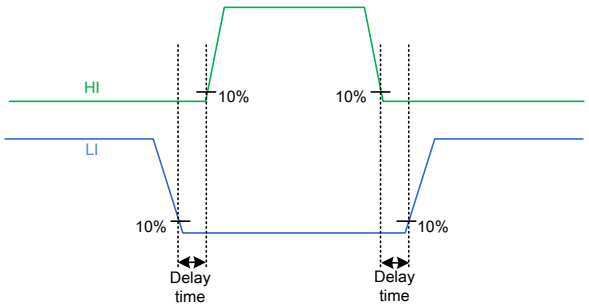



Figure 1. PWM Input Timing Diagram

**High-Side Driver**

The high-side driver is designed to “float” meaning that its reference (ground) floats with the PHASE pin of the uP1966E which is normally tied to the source of an N channel GaN FET. The bias voltage to the high-side driver is supplied to the BOOT pin through a bootstrap switch (diode) see Figure 2, so that a capacitor, $C_{BOOT}$, can be charged up each time the low side GaN device is turned on. As the high-side GaN FETs turns on PHASE rises to $V_{IN}$, forcing the BOOT pin voltage to $V_{IN}+V_{CC}$ that provides a voltage to hold the high-side GaN FET on.

When the boot voltage on $C_{BOOT}$ detects a starting threshold voltage level of 3.2V (typical) on a rising edge, the output will become active. The output will become inactive after the input falls 0.2V below the starting threshold.

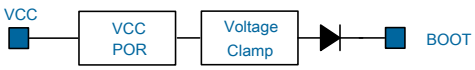



Figure 2. Bootstrap Switch Circuit



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## Functional Description

**Low-Side Driver**

The low-side driver is designed to drive a ground referenced GaN FET. The bias to the low-side driver is internally connected to VCC supply and GND.

**Switching Timing Diagram**

Figure 3 shows the definitions of the turn-on and turn-off propagation delay times. The interval between input signal and output signal is defined as match delay time.

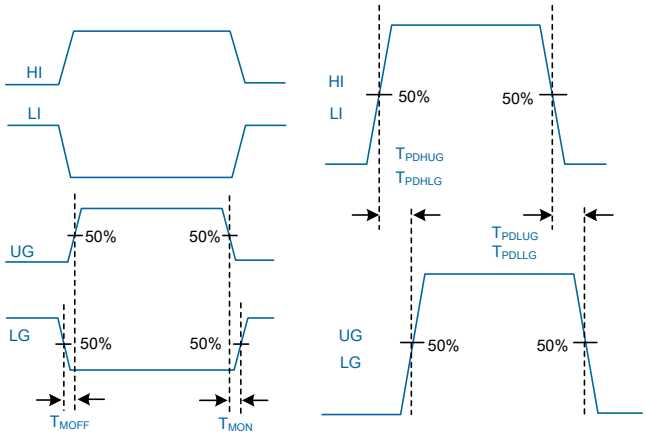



Figure 3. I/O Delay Time



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## Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +7V
BOOT to PHASE ---------- -0.3V to +7V
UGH, UGL ---------- (PHASE-0.3V) to (BOOT+0.3V)
LGH,LGL ---------- -0.3V to (VCC+0.3V)
HI, LI ---------- -0.3V to +7V
PHASE to GND ---------- -5V to +85V
BOOT to GND ---------- 0V to +85V
Storage Temperature Range ---------- -55°C to +150°C
Junction Temperature ---------- 150°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- ±1kV
CDM (Charged Device Mode) ---------- ±1kV

## Thermal Information

Package Thermal Resistance (Note 3)
WLCSP1.6x1.6-12B $\theta_{JA}$ ---------- 79.3°C/W
WLCSP1.6x1.6-12B $\theta_{JB}$ ---------- 12°C/W
WLCSP1.6x1.6-12B $\theta_{JC}$ ---------- 0.65W

## Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40 °C to +125 °C
Supply Input Voltage, VCC ---------- +4.5V to +5.5V

**Note 1.** Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on an area array surface mount package test boards of *JEDEC 51-9* thermal measurement standard.

**Note 4.** The device is not guaranteed to function outside its operating conditions.



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## Electrical Characteristics

($V_{CC}$ = 5V, $T_J$ = 25℃, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Input** | | | | | | |
| Supply Current | $I_{CC}$ | PWM = 0V, $V_{CC}$ = 5V | -- | 120 | -- | uA |
| | | $F_{SW}$ = 500kHz, not output $C_{LOAD}$ | -- | 4000 | -- | |
| VCC POR Rising Threshold | $V_{CCRTH}$ | $V_{CC}$ rising | 3.8 | 4 | 4.2 | V |
| VCC Threshold Hysteresis | $V_{CCHYS}$ | | -- | 0.35 | -- | V |
| **PWM Input** | | | | | | |
| Input High Threshold | $PWM_{RTH}$ | | 2.3 | -- | -- | V |
| Input Low Threshold | $PWM_{FTH}$ | | -- | -- | 0.5 | V |
| Input Pull Down Resistance | $R_I$ | | -- | 200 | -- | kΩ |
| Input Voltage Hysteresis | $V_{IHYS}$ | | -- | 400 | -- | mV |
| Minimum Input Pulse Width That Changes the Output | $T_{PW}$ | (*1) | -- | 5 | -- | ns |
| **Bootstrap Switch** | | | | | | |
| Low-Current Forward Voltage | $V_{DL}$ | $I_{VCC-BOOT}$ = 100uA | -- | 0.2 | -- | V |
| High-Current Forward Voltage | $V_{DH}$ | $I_{VCC-BOOT}$ = 100mA | -- | 0.9 | -- | V |
| Boot POR Rising Threshold | $V_{BOOTPOR}$ | | 2.5 | 3.2 | 3.94 | V |
| Boot POR Threshold Hysteresis | $V_{BOOTHYS}$ | | -- | 0.2 | -- | V |
| **High Side Driver** | | | | | | |
| Output Resistance, Sourcing | $R_{H_SRC}$ | $V_{BOOT}$ - $V_{PHASE}$ = 5V, $I_{UGATE}$ = 500mA | -- | 0.7 | 1.4 | Ω |
| Output Resistance, Sinking | $R_{H_SNK}$ | $V_{BOOT}$ - $V_{PHASE}$ = 5V, $I_{UGATE}$ = -500mA | -- | 0.4 | 0.8 | Ω |
| Output Rising Time | $T_{RUGATE}$ | $V_{BOOT}$ - $V_{PHASE}$ = 5V, $C_{LOAD}$ = 3000pF | -- | 8 | 10 | ns |
| Output Falling Time | $T_{FUGATE}$ | $V_{BOOT}$ - $V_{PHASE}$ = 5V, $C_{LOAD}$ = 3000pF | -- | 4 | 6 | ns |
| Rising Propagation Delay Time | $T_{PDHUG}$ | $V_{BOOT}$ - $V_{PHASE}$ = 5V | -- | 20 | 25 | ns |
| Falling Propagation Delay Time | $T_{PDLUG}$ | $V_{BOOT}$ - $V_{PHASE}$ = 5V | -- | 20 | 25 | ns |
| **Low Side Driver** | | | | | | |
| Output Resistance, Sourcing | $R_{L_SRC}$ | $V_{CC}$ = 5V, $I_{LGATE}$= 500mA | -- | 0.7 | 1.4 | Ω |
| Output Resistance, Sinking | $R_{L_SNK}$ | $V_{CC}$ = 5V, $I_{LGATE}$= -500mA | -- | 0.4 | 0.8 | Ω |
| Output Rising Time | $T_{RLGATE}$ | $V_{CC}$ = 5V, $C_{LOAD}$ = 3000pF | -- | 8 | 10 | ns |
| Output Falling Time | $T_{FLGATE}$ | $V_{CC}$ = 5V, $C_{LOAD}$ = 3000pF | -- | 4 | 6 | ns |
| Rising Propagation Delay Time | $T_{PDHLG}$ | $V_{CC}$ = 5V | -- | 20 | 25 | ns |
| Falling Propagation Delay Time | $T_{PDLLG}$ | $V_{CC}$ = 5V | -- | 20 | 25 | ns |
| **Match Delay Time** | | | | | | |
| Delay Matching LG On & UG Off | $T_{MON}$ | | -- | 1.5 | 6 | ns |
| Delay Matching LG Off & UG On | $T_{MOFF}$ | | -- | 1.5 | 6 | ns |

Note 1: Guaranteed by design but not tested in production.

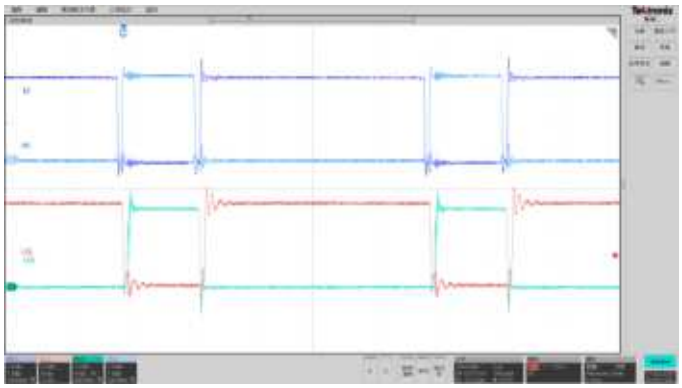


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# uP1966E

## Typical Operation Characteristics

### Driver Input and Output

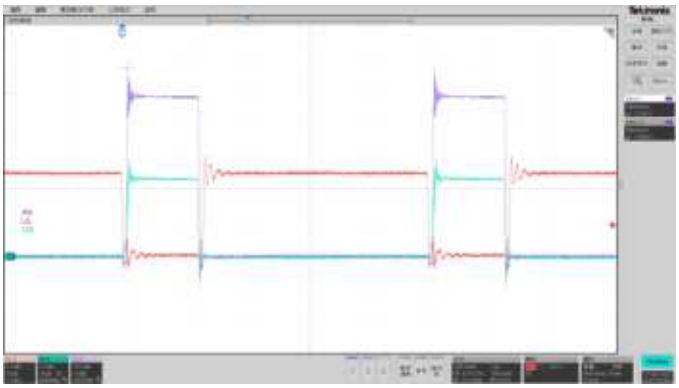


Time: 200ns/Div

CH1:LI (2V/Div),CH2:LG(2V/Div),CH3:UG(2V/Div),CH5:HI(2V/Div)

Input Voltage=48V, 1-MHz, Load Current=10A, CLoad=600pF

### Driver Output and PHASE-Node

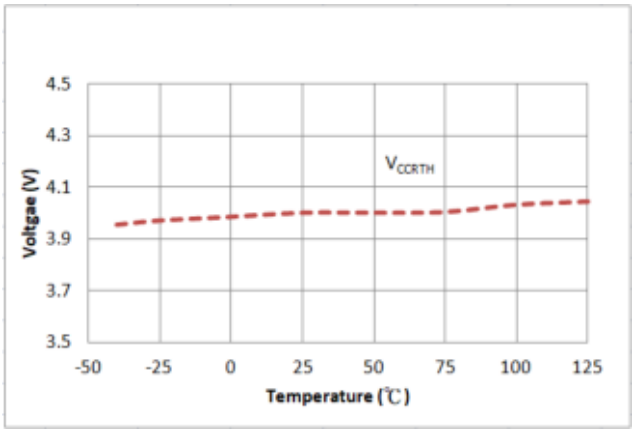


Time:200ns/Div

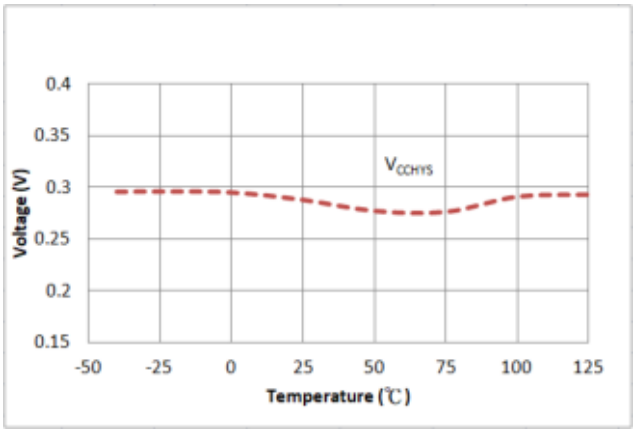
CH2:LG(2V/Div),CH3:UG(2V/Div),CH4:PHASE(10V/Div)

Input Voltage=48V, 1-MHz, Load Current=10A, CLoad=600pF

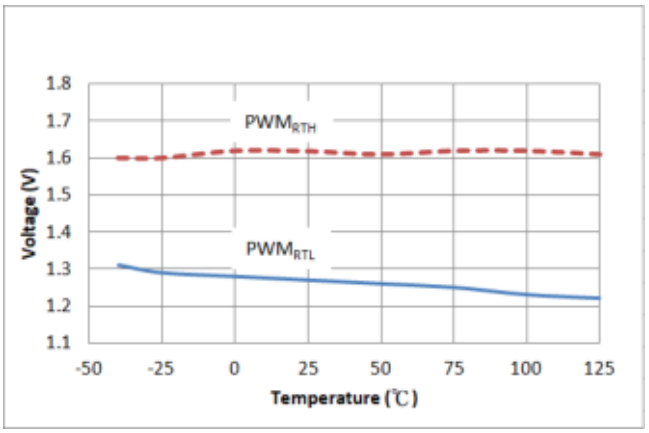
### VCC POR Rising Thresholds vs Temperature



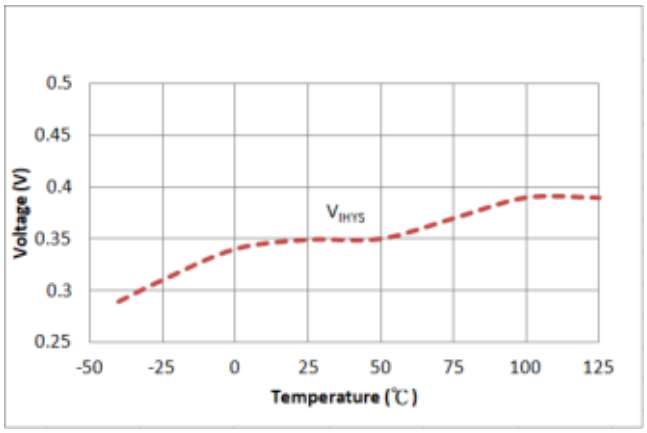

### VCC POR HYS Thresholds vs Temperature




### Input Thresholds vs Temperature




### Input Threshold Hysteresis vs Temperature

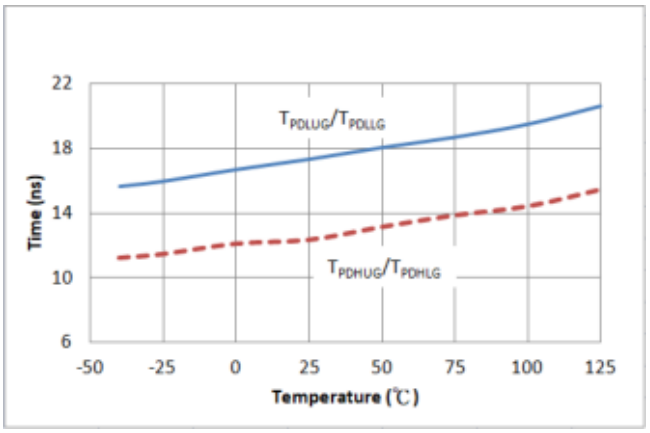





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## Typical Operation Characteristics

**Propagation Delay vs. Temperature**

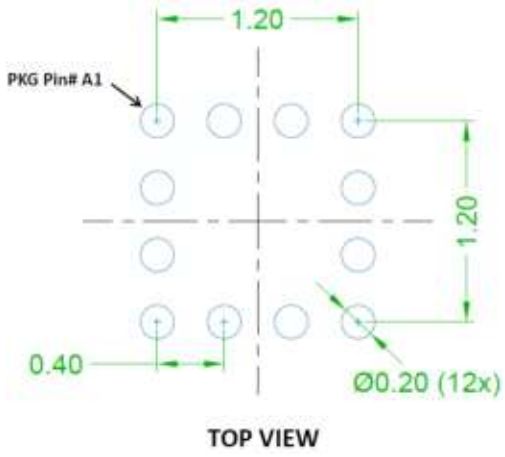





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## Application Information

**Recommended Land Pattern**




**Layout Recommendation**

The GaN FETs feature a small gate capacitance and a small miller capacitance to operate with fast-speed switching and high dv/dt and high di/dt. Care must be taken with a gate threshold voltage to avoid over voltage condition. Therefore, the circuit layout is crucial to the optimal performance. Figure 4 and Figure 5 show the reference PCB layout for uP1966E.

The layout guidelines are as follows:

1. The driver controls charging and discharging of the gate of GaN FET. It may produce high peak charge and discharge current. The driver must be placed close to the GaN FETs. This design layout minimizes the loops of parasitic inductance and reduces the noise on the gate loop of the driver to GaN FETs.
2. The bootstrap capacitor is recharged from VCC voltage through bootstrap diode to the reference ground of VCC capacitor. The high peak current may occur during recharging time; therefore, minimizing the distance between $C_{BOOT}$ and $C_{VCC}$ to the driver is recommended and $C_{BOOT}$ and $C_{VCC}$ should be placed on the same side as the driver.
3. The driver turns off the layout path to GaN FETs and causes parasitic inductance, driver pull-down goes along the control loop the gate capacitor, and it produced an RLC resonant tank, resulting in gate voltage oscillations. The gate loop of driver selects a suitable resistor to damp the ringing.
4. In order to avoid the parasitic inductance between high-side GaN FET and low-side GaN FET in series, which induces excessive negative voltage to the driver, it is recommended to minimize the distance between high-side GaN FET and low-side GaN FET.

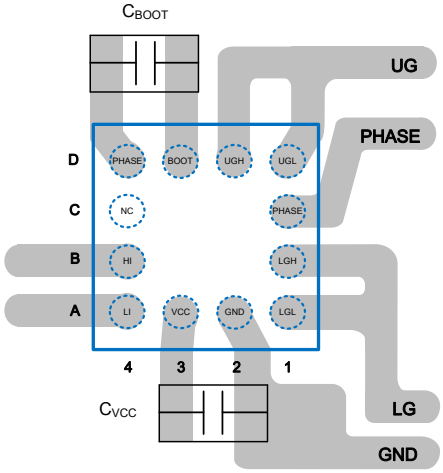



Figure 4. Layout Example without Damp Resistors

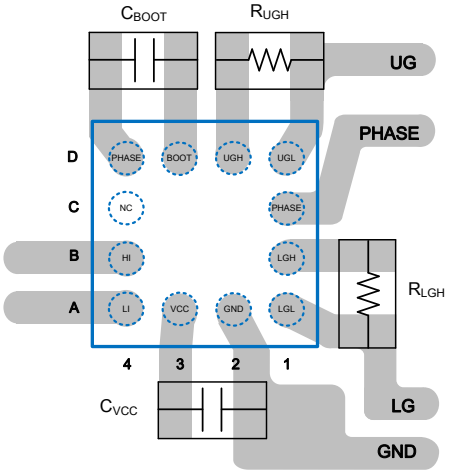


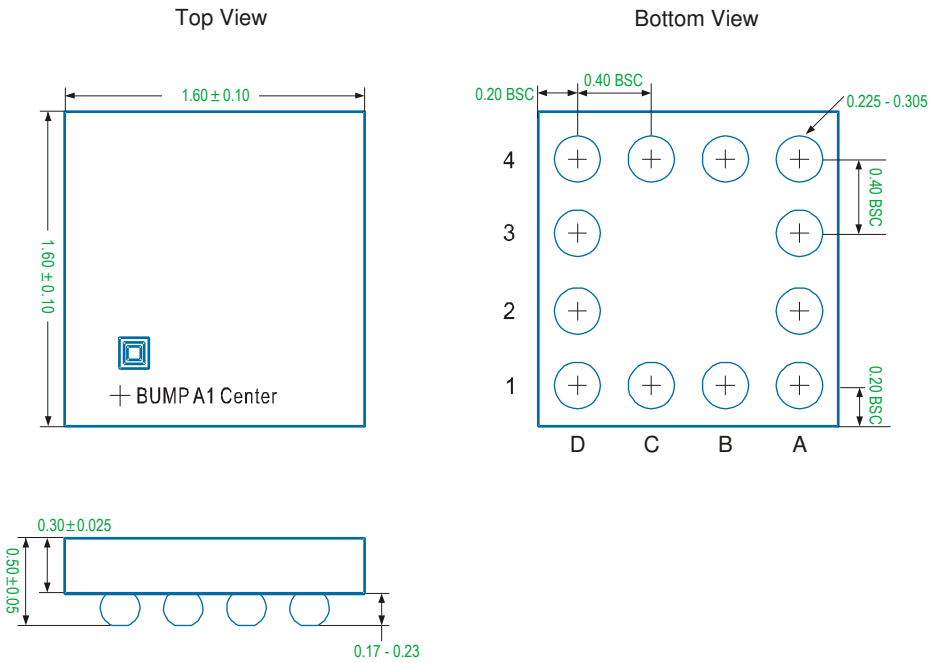

Figure 5. Layout Example with Source Damp Resistors



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## Package Information

WLCSP1.6x1.6-12B




Note

1. Package Outline Unit Description:
   MIN: Minimum dimension specified.
   NOM: Nominal. Provided as a general value.
   MAX: Maximum dimension specified.
   BSC: Basic. Represents theoretical exact dimension or dimension target.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.



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