UCC2751x Single-Channel, High-Speed, Low-Side Gate Driver (With 4-A Peak Source and 8-A Peak Sink)

1 Features

- Low-Cost Gate-Driver Device Offering Superior Replacement of NPN and PNP Discrete Solutions
- 4-A Peak Source and 8-A Peak Sink Asymmetrical Drive
- Strong Sink Current Offers Enhanced Immunity Against Miller Turnon
- Split Output Configuration (Allows Easy and Independent Adjustment of Turnon and Turnoff Speeds) in the UCC27511 Saves 1 Diode
- Fast Propagation Delays (13-ns Typical)
- Fast Rise and Fall Times (9-ns and 7-ns Typical)
- 4.5-V to 18-V Single Supply Range
- Outputs Held Low During VDD UVLO (Ensures Glitch-Free Operation at Power Up and Power Down)
- TTL and CMOS Compatible Input-Logic Threshold (Independent of Supply Voltage)
- Hysteretic-Logic Thresholds for High-Noise Immunity
- Dual-Input Design (Choice of an Inverting (IN– Pin) or Noninverting (IN+ Pin) Driver Configuration)
  - Unused Input Pin can be Used for Enable or Disable Function
- Output Held Low When Input Pins Are Floating
- Input Pin Absolute Maximum Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage
- Operating Temperature Range of –40°C to 140°C
- 6-Pin DBV (SOT-23) and 6-Pin DRS (3-mm × 3-mm WSON With Exposed Thermal Pad) Package Options

2 Applications

- Switched-Mode Power Supplies
- DC-to-DC Converters
- Companion Gate-Driver Devices for Digital Power Controllers
- Solar Power, Motor Control, UPS
- Gate Driver for Emerging Wide Band-Gap Power Devices (such as GaN)

3 Description

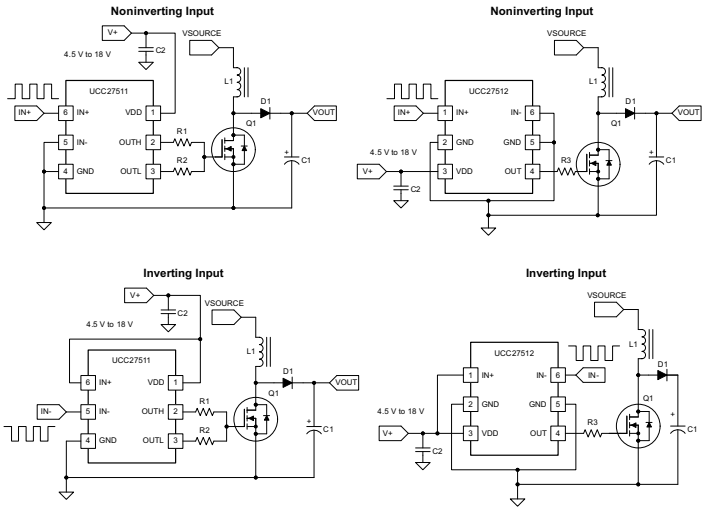
The UCC27511 and UCC27512 single-channel, high-speed, low-side gate-driver device can effectively drive MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, UCC27511 and UCC27512 are capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay, typically 13 ns.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27511	SOT-23 (6)	2.90 mm x 1.60 mm
UCC27512	WSON (6)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Diagrams



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2013) to Revision F — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision D (May 2013) to Revision E — **Page**

- Changed OUTL in the ABS Max Ratings table to show DC and Repetitive pulse values ... 7

Changes from Revision C (June 2012) to Revision D — **Page**

- Added 0.05 to P_{SW} equation in the *Power Dissipation* section. ... 26

Changes from Revision B (March, 2012) to Revision C — **Page**

- Added UCC27512 device throughout. ... 1
- Added 6-Pin DRS package feature. ... 1
- Added DRS pinout for the UCC27512. ... 5
- Added UCC27512 TERMINAL FUNCTIONS table. ... 6
- Added OUT voltage ab max ratings for the UCC27512. ... 7
- Added (1) ... 7
- Changed ESD ratings of Human Body Model, HBM from 2000 V to 4000 V. ... 7
- Changed ESD ratings of Charged Device Model, CDM SOT-23 from 500 V to 1000 V. ... 7
- Added UCC27512 Thermal Information. ... 8
- Added power dissipation conditions note to Thermal Information section. ... 8
- Added UCC27512 Functional Block Diagram. ... 16

(1) Values are verified by characterization on bench.

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- Added UCC27512 application diagrams. 22
- Added Typical Application Diagram note..... 23
- Added PCB layout bullet..... 28

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5 Description (Continued)

UCC27511 features a dual-input design which offers flexibility of implementing both inverting (IN– pin) and noninverting (IN+ pin) configuration with the same device. Either IN+ or IN– pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For safety purpose, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when input pins are in floating condition. Hence the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation.

The input pin threshold of the UCC27511 device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

The UCC27511 and UCC27512 provides 4-A source, 8-A sink (asymmetrical drive) peak-drive current capability. Strong sink capability in asymmetrical drive boosts immunity against parasitic, Miller turnon effect. The UCC27511 device also features a unique split output configuration where the gate-drive current is sourced through OUTH pin and sunk through OUTL pin. This unique pin arrangement allows the user to apply independent turnon and turnoff resistors to the OUTH and OUTL pins respectively and easily control the switching slew rates.

UCC27511 and UCC27512 are designed to operate over a wide V_{DD} range of 4.5 to 18 V and wide temperature range of –40°C to 140°C. Internal Undervoltage Lockout (UVLO) circuitry on V_{DD} pin holds output low outside V_{DD} operating range. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

6 UCC2751x Product Family

The UCC2751x family of gate-driver products (Table 1) represent Texas Instruments' latest generation of single-channel low-side high-speed gate-driver devices featuring high-source/sink current capability, industry best-in-class switching characteristics and a host of other features (Table 2) all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 1. UCC2751x Product Family Summary

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV	SOT-23, 6 pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27512DRS	3-mm x 3-mm WSON, 6 pin		
UCC27516DRS (1)	3-mm x 3-mm WSON, 6 pin	4-A/4-A (Symmetrical Drive)	
UCC27517DBV (1)	SOT-23, 5 pin		
UCC27518DBV (1)	SOT-23, 5 pin		CMOS (follows VDD bias voltage)
UCC27519DBV (1)	SOT-23, 5 pin		

(1) Visit www.ti.com for the latest product datasheet.

Table 2. UCC2751x Features and Benefits

FEATURE	BENEFIT
High Source and Sink Current Capability 4 A and 8 A (Asymmetrical) – UCC2751/6/7/8/9 4 A and 4 A (Symmetrical) – UCC27511 and UCC27512	High current capability offers flexibility in employing UCC2751x family of devices to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low pulse-transmission distortion
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design Low VDD operation ensures compatibility with emerging wide band-gap power devices such as GaN
Expanded Operating Temperature range of –40°C to 140°C (See *Electrical Characteristics* table)	
VDD UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable glitch-free operation at power up and power down
Outputs held low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification

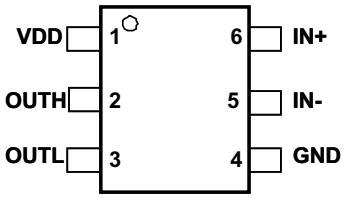
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Table 2. UCC2751x Features and Benefits (continued)

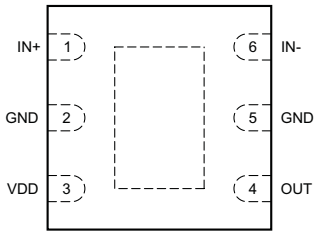
FEATURE	BENEFIT
Ability of input pins (and enable pin in UCC27518/9) to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Split output structure in UCC27511 (OUTH, OUTL)	Allows independent optimization of turnon and turnoff speeds
Strong sink current (8 A) and low pulldown impedance (0.375 Ω) in UCC27511 and UCC27512	High immunity to C x dV/dt Miller turnon events
CMOS/TTL compatible input-threshold logic with wide hysteresis in UCC27511, UCC27512, UCC27516 and UCC27517	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
CMOS input threshold logic in UCC27518/9 (VIN_H – 70% VDD, VIN_L – 30% VDD)	Well suited for slow input-voltage signals, with flexibility to program delay circuits (RCD)

7 Pin Configuration and Functions

6-Pins
DBV Package
(Top View)



6-Pins
DRS Package
(Top View)



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Pin Functions - UCC27511

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VDD	I	**Bias supply input.**
2	OUTH	O	**Sourcing current output of driver**. Connect resistor between OUTH and Gate of power-switching device to adjust turnon speed.
3	OUTL	O	**Sinking current output of driver.** Connect resistor between OUTL and Gate of power-switching device to adjust turnoff speed.
4	GND	-	**Ground:** All signals referenced to this pin.
5	IN-	I	**Inverting input:** When the driver is used in noninverting configuration, connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating
6	IN+	I	**Noninverting input:** When the driver is used in inverting configuration, connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating

Pin Functions - UCC27512

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN+	I	**Noninverting input:** When the driver is used in inverting configuration, connect IN+ to VDD in order to enable output, OUT held LOW if IN+ is unbiased or floating.
2, 5	GND	-	**Ground:** All signals referenced to this pin. TI recommends to connect pin 2 and pin 5 on PCB as close to the device as possible.
3	VDD	I	**Bias supply input.**
4	OUT	O	**Sourcing/sinking current output of driver.**
6	IN-	I	**Inverting input:** When the driver is used in noninverting configuration, connect IN- to GND in order to enable output, OUT held LOW if IN- is unbiased or floating.

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8 Specifications

8.1 Absolute Maximum Ratings(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	20	V
OUTH voltage, (UCC27511)		–0.3	VDD + 0.3	
OUTL voltage, (UCC27511)	DC	–0.3	20	
	Repetitive pulse less than 200 ns(4)	–2	20	
OUT voltage, (UCC27512)	DC	–0.3	VDD + 0.3	
	Repetitive pulse less than 200 ns(4)	–2	VDD + 0.3	
Output continuous current (OUTH source current and OUTL sink current)	I_{OUT_DC} (source)		0.3	A
	I_{OUT_DC} (sink)		0.6	
Output pulsed current (0.5 µs) (OUTH source current and OUTL sink current)	I_{OUT_pulsed}(source)		4	
	I_{OUT_pulsed}(sink)		8	
IN+, IN–(5)		–0.3	20	V
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into and negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(4) Values are verified by characterization on bench.
(5) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–4000	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	–40		140	°C
Input voltage, IN+ and IN-	0		18	V

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8.4 Thermal Information

THERMAL METRIC		UCC27511	UCC27512	UNIT
		DBV	WSON(1)	
		6 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	217.8	85.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	97.6	100.1	
θ_{JB}	Junction-to-board thermal resistance(4)	72.2	58.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	8.6	7.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	71.6	58.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	23.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

NOTE

Under identical power dissipation conditions, the DRS package will allow to maintain a lower die temperature than the DBV. θ_{JA} metric should be used for comparison of power dissipation capability between different packages (Refer to the *Power Dissipation* Section).

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8.5 Electrical Characteristics

V_{DD} = 12 V, T_A = T_J = –40°C to 140°C, 1-µF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
BIAS CURRENTS							
$I_{DD(off)}$	Startup current	VDD = 3.4 V	IN+ = VDD, IN– = GND	40	100	160	µA
			IN+ = IN– = GND or IN+ = IN– = VDD	25	75	145	
			IN+ = GND, IN– = VDD	20	60	115	
UNDERVOLTAGE LOCKOUT (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C		3.91	4.20	4.5	V
		T_A = –40°C to 140°C		3.70	4.20	4.65	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	
V_{DD_H}	Supply voltage hysteresis			0.2	0.3	0.5	
INPUTS (IN+, IN-)							
V_{IN_H}	Input signal high threshold	Output high for IN+ pin, Output low for IN– pin			2.2	2.4	V
V_{IN_L}	Input signal low threshold	Output low for IN+ pin, Output high for IN– pin		1.0	1.2		
V_{IN_HYS}	Input signal hysteresis				1.0		
SOURCE/SINK CURRENT							
$I_{SRC/SNK}$	Source/sink peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz			-4/+8		A
OUTPUTS (OUTH, OUTL, OUT)							
V_{DD}- V_{OH}	High output voltage	VDD = 12 V I_{OUTH} = -10 mA			50	90	mV
		VDD = 4.5 V I_{OUTH} = -10 mA			60	130	
V_{OL}	Low output voltage	VDD = 12 I_{OUTL} = 10 mA			5	6.5	
		VDD = 4.5 V I_{OUTL} = 10 mA			5.5	10	
R_{OH}	Output pull-up resistance(2)	VDD = 12 V I_{OUTH} = -10 mA			5.0	7.5	Ω
		VDD = 4.5 V I_{OUTH} = -10 mA			5.0	11.0	
R_{OL}	Output pull-down resistance	VDD = 12 V I_{OUTL} = 10 mA			0.375	0.650	
		VDD = 4.5 V I_{OUTL} = 10 mA			0.45	0.750	

(1) Ensured by Design.
(2) R_{OH} represents on-resistance of P-Channel MOSFET in pullup structure of the output stage of the UCC27511 and UCC27512.

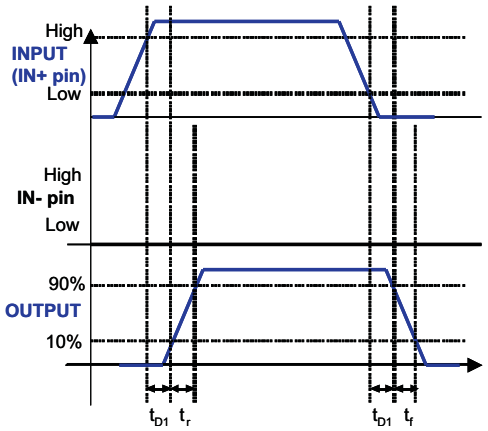
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8.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time(1)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together		8	12	ns
		VDD = 4.5 V C_{LOAD} = 1.8 nF		16	22	
t_F	Fall time(1)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together		7	11	
		VDD=4.5V C_{LOAD} = 1.8 nF		7	11	
t_{D1}	IN+ to output propagation delay(1)	VDD = 12 V 5-V input pulse C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	13	23	
		VDD = 4.5 V 5-V input pulse C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	15	26	
t_{D2}	IN- to output propagation delay(1)	VDD = 12 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	13	23	
		VDD = 4.5 V C_{LOAD} = 1.8 nF, connected to OUTH and OUTL pins tied together	4	19	30	

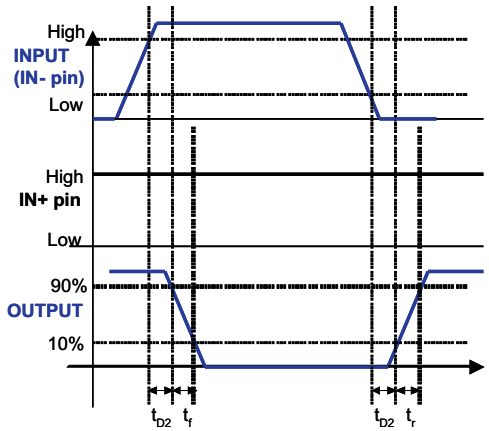
(1) See timing diagrams in Figure 1, Figure 2, Figure 3 and Figure 4.



(PWM Input to IN+ Pin (IN– Pin Tied to GND), Output Represents OUTH And OUTL Pins Tied Together in the UCC27511)

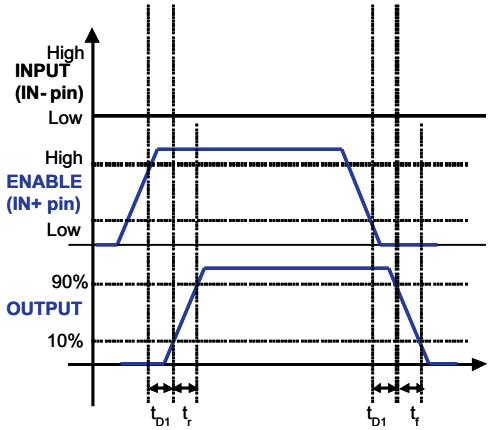
Figure 1. Noninverting Configuration

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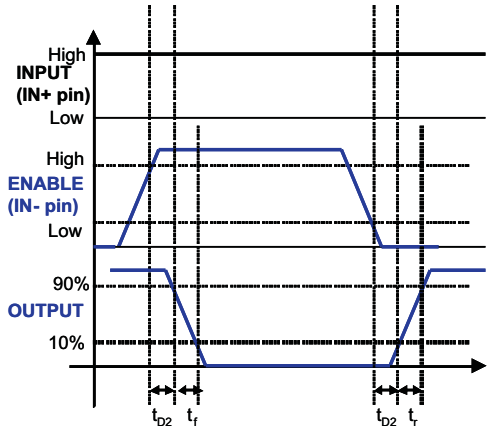
(PWM Input to IN– Pin (IN+ Pin Tied to VDD), Output Represents OUTH and OUTL Pins Tied Together in the UCC27511)

Figure 2. Inverting Configuration



(Enable and Disable Signal Applied to IN+ Pin, PWM Input to IN– Pin, Output Represents OUTH and OUTL Pins Tied Together in the UCC27511)

Figure 3. Enable and Disable Function Using IN+ Pin



(Enable and Disable Signal Applied to IN– Pin, PWM Input To IN+ Pin, Output Represents OUTH and OUTL Pins Tied Together in the UCC27511)

Figure 4. Enable and Disable Function Using IN– Pin

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8.7 Typical Characteristics

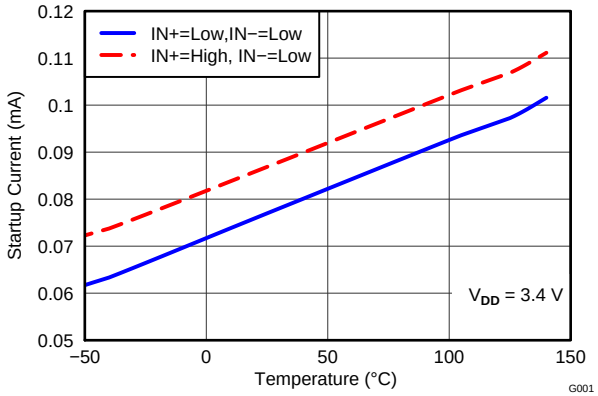


Figure 5. Start-Up Current vs Temperature

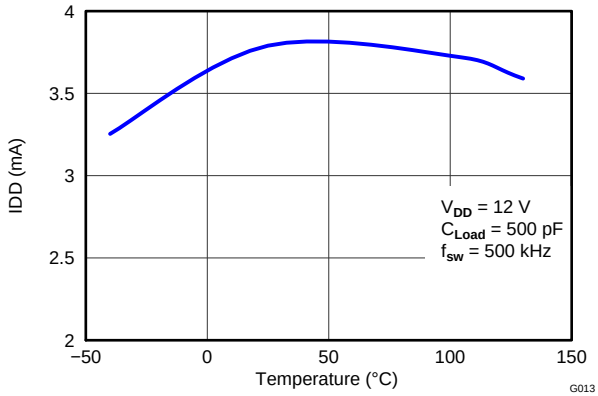


Figure 6. Operating Supply Current vs Temperature (Output Switching)

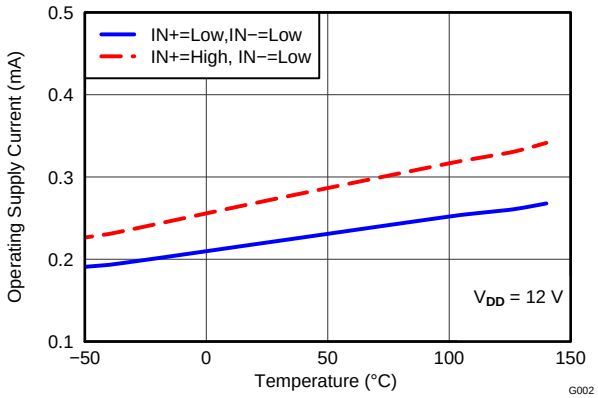


Figure 7. Supply Current vs Temperature (Output In DC On/Off Condition)

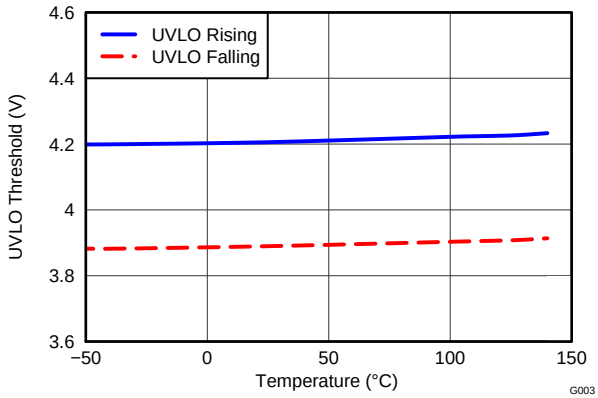


Figure 8. UVLO Threshold Voltage vs Temperature

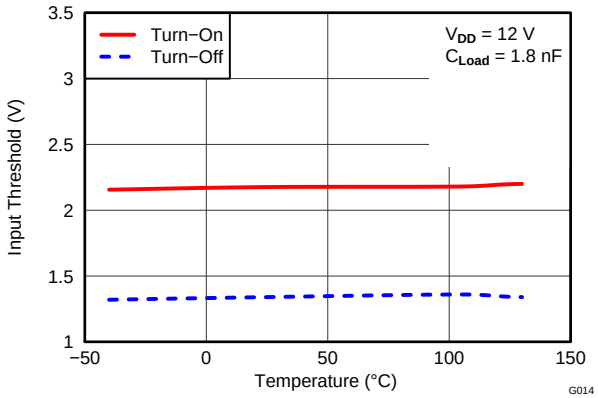


Figure 9. Input Threshold vs Temperature

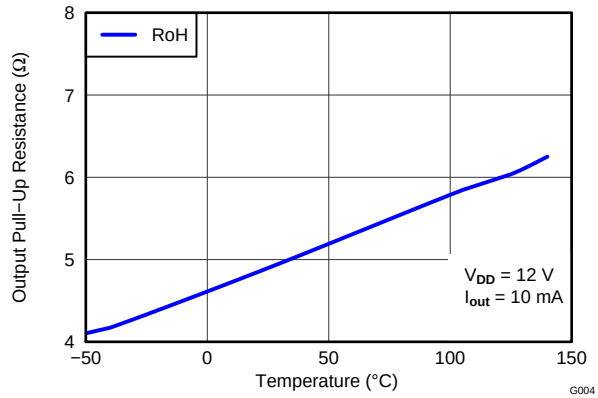


Figure 10. Output Pullup Resistance vs Temperature

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Typical Characteristics (continued)

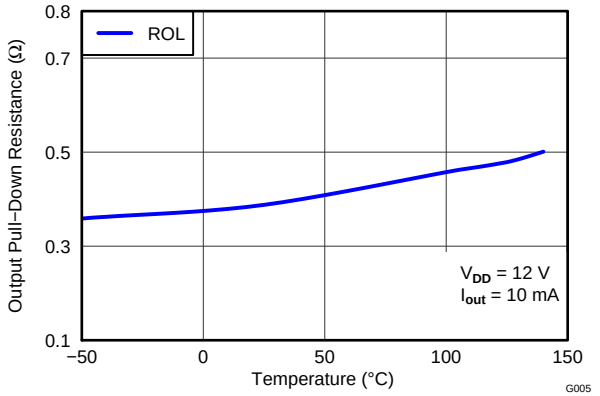


Figure 11. Output Pulldown Resistance vs Temperature

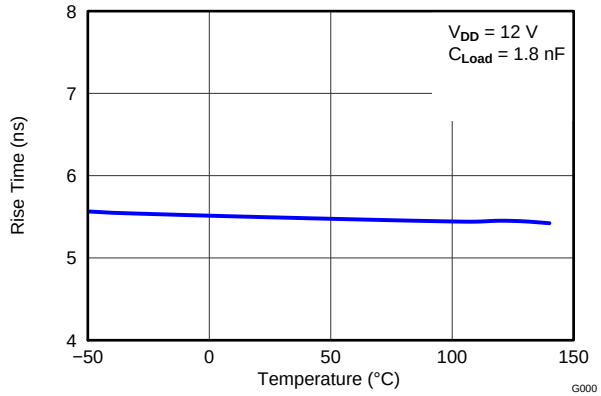


Figure 12. Rise Time vs Temperature

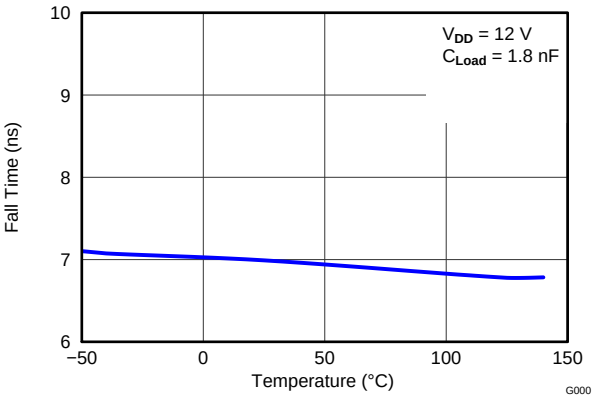


Figure 13. Fall Time vs Temperature

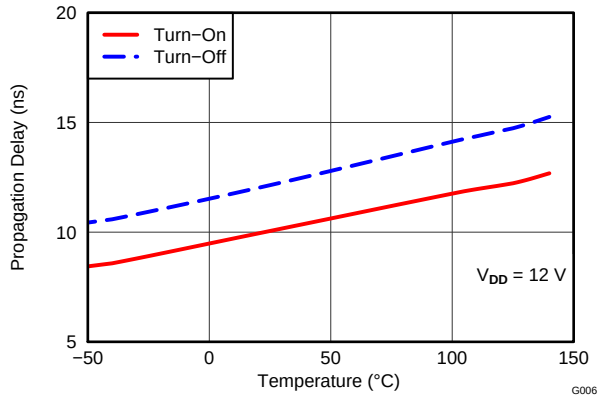


Figure 14. Input to Output Propagation Delay vs Temperature

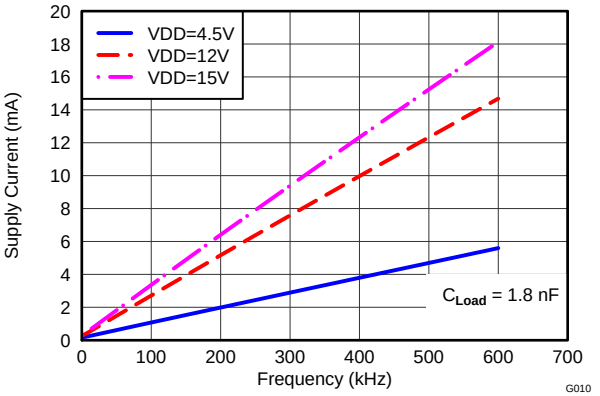


Figure 15. Operating Supply Current vs Frequency

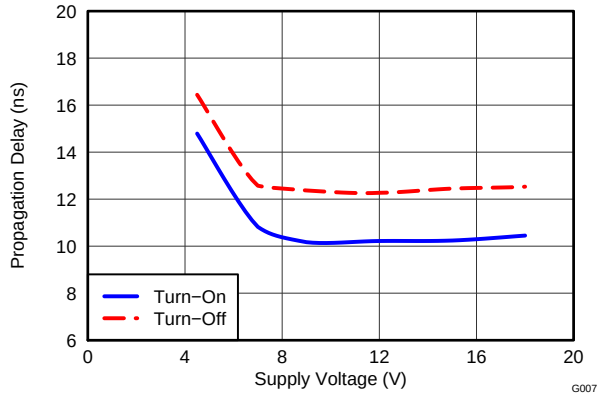


Figure 16. Propagation Delays vs Supply Voltage

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Typical Characteristics (continued)

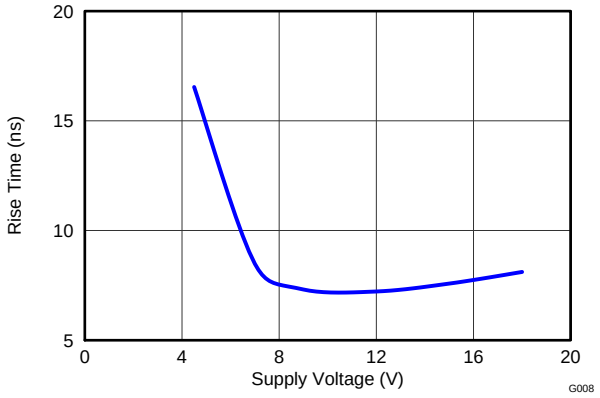


Figure 17. Rise Time vs Supply Voltage

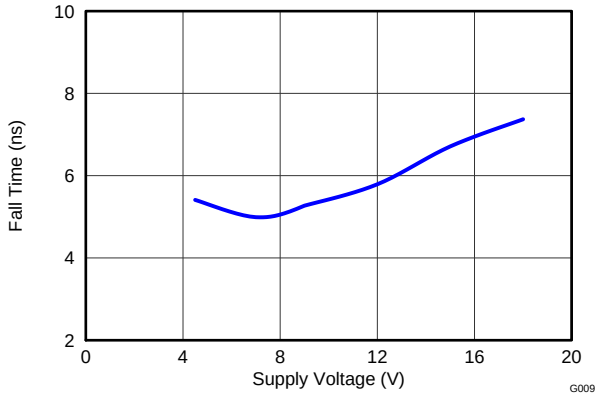


Figure 18. Fall Time vs Supply Voltage

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9 Detailed Description

9.1 Overview

The UCC27511/2 single-channel high-speed low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC27511 device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical).

The UCC27511 device provides 4-A source, 8-A sink (asymmetrical drive) peak-drive current capability. Strong sink capability in asymmetrical drive boosts immunity against parasitic, Miller turnon effect. The UCC27511 device also features a unique split output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This unique pin arrangement allows the user to apply independent turnon and turnoff resistors to the OUTH and OUTL pins (respectively) and easily control the switching slew rates.

Alternatively the OUTH and OUTL pins can be tied together, which results in a typical gate driver output configuration where the source and sink currents are delivered from the same pin. In case of UCC27511 device, the state of the device's output is simply determined by the combined states of the OUTH and OUTL pins when tied together. Output high implies that OUTH pin is pulled close to V_{DD} pin bias voltage while OUTL pin is in high-impedance state. Similarly output low implies that OUTL pin is pulled close to the GND pin while OUTH pin is in high-impedance state. OUTH pulled to VDD, while OUTL pulled to GND pin simultaneously is not a valid state for the device.

The UCC27511 device is designed to operate over a wide V_{DD} range of 4.5 to 18 V and wide temperature range of –40°C to 140°C. Internal undervoltage lockout (UVLO) circuitry on the V_{DD} pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

The UCC27511 device features a dual-input design which offers flexibility of implementing both inverting (IN– pin) and noninverting (IN+ pin) configuration with the same device. Either the IN+ or IN– pin can be used to control the state of the driver output. The unused input pin can be used for enable and disable functions. For system robustness, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when the input pins are in floating condition. Therefore the unused input pin is not left floating and must be properly biased to ensure that driver output is in enabled for normal operation.

The input pin threshold of the UCC27511A-Q1 device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

9.2 Functional Block Diagram

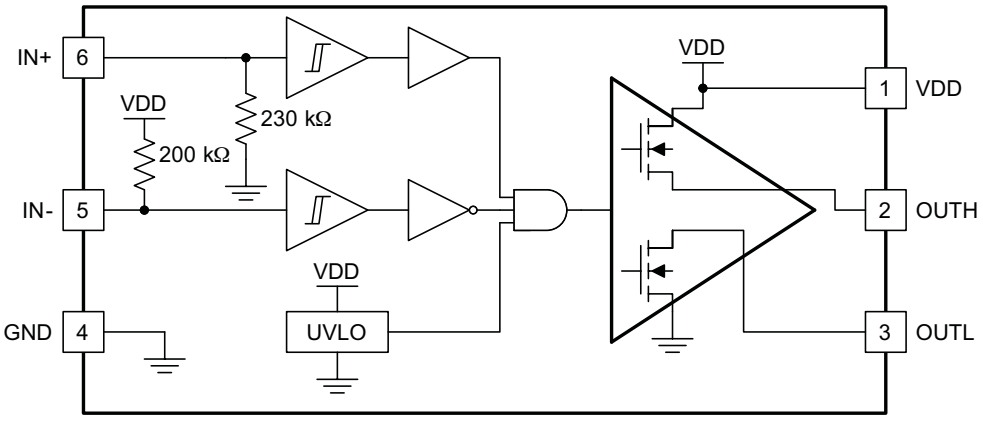


Figure 19. UCC27511 Functional Block Diagram

Functional Block Diagram (continued)

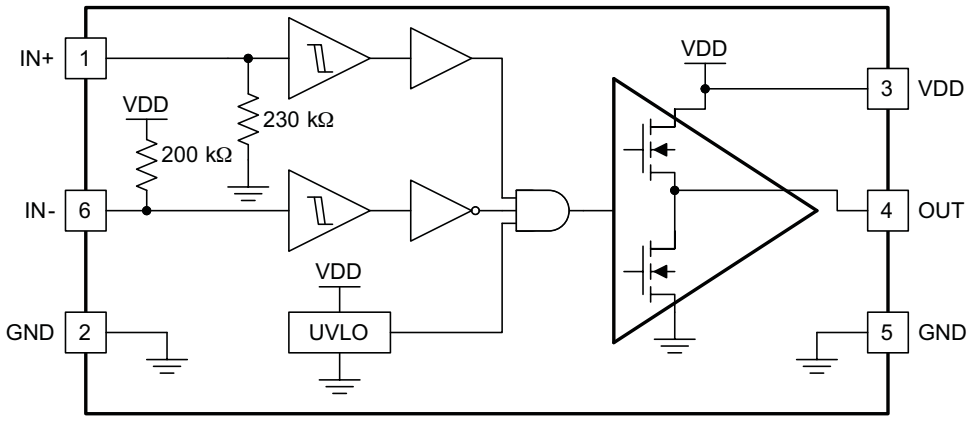


Figure 20. UCC27512 Functional Block Diagram

9.3 Feature Description

In the following sections with respect to UCC27511, the term *output*, or *OUT* refers to the combined state that results when the OUTH pin is tied directly to the OUTL pin. As stated earlier, *output high*, or *OUT high* refers to the state when the OUTH pin is pulled close to V_{DD} pin bias voltage while the OUTL pin is in high-impedance state. Similarly *output low* or *OUT low* implies that the OUTL pin is pulled close to the GND pin while the OUTH pin is in high-impedance state.

9.3.1 V_{DD} and Undervoltage Lockout

The UCC27511 and UCC27512 devices have internal Undervoltage LockOut (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition (for example when V_{DD} voltage less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis prevents chatter when low V_{DD} supply voltages have noise from the power supply and also when there are droops in the V_{DD} bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide band-gap power-semiconductor devices.

For example, at power up, the UCC27511 and UCC27512 driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the noninverting operation (PWM signal applied to IN+ pin) shown in Figure 21, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting operation (PWM signal applied to IN- pin) shown in Figure 22 the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input. In both cases, the unused input pin must be properly biased to enable the output. Note that in these devices the output turns to high state only if IN+ pin is high and IN- pin is low after the UVLO threshold is reached.

Since the driver draws current from the V_{DD} pin to bias all internal circuits, for the best high-speed circuit performance, two V_{DD}-bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the V_{DD} to GND pins of the gate driver. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

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Feature Description (continued)

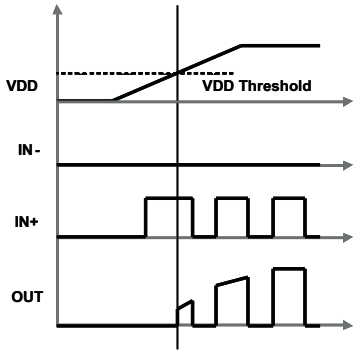


Figure 21. Powerup (Noninverting Drive)

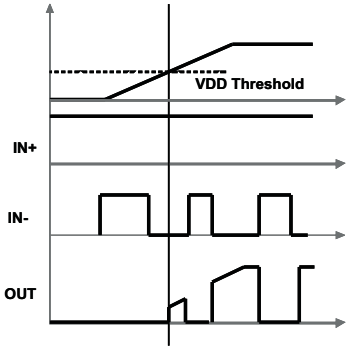


Figure 22. Powerup (Inverting Drive)

9.3.2 Operating Supply Current

The UCC27511 and UCC27512 feature very low quiescent I_{DD} currents. The typical operating-supply current in Undervoltage LockOut (UVLO) state and fully-on state (under static and switching conditions) are summarized in Figure 5, Figure 6 and Figure 7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 7) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching, and finally any current related to pullup resistors on the unused input pin. For example, when the inverting input pin is pulled low additional current is drawn from V_{DD} supply through the pullup resistors (refer to for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the IDD current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load is provided in Figure 15. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

9.3.3 Input Stage

The input pins of the UCC27511 and UCC27512 devices are based on a TTL and CMOS compatible input-threshold logic that is independent of the V_{DD} supply voltage. With a typicalyl high threshold of 2.2 V and a typically low threshold of 1.2 V, the logic-level thresholds can be conveniently driven with PWM control signals derived from 3.3-V and 5-V digital-power controllers. Wider hysteresis (1 V typical) offers enhanced noise immunity compared to traditional TTL-logic implementations, where the hysteresis is typically less than 0.5 V. This device also feature tight control of the input-pin threshold-voltage levels which eases system design considerations and ensures stable operation across temperature. The very-low input capacitance on these pins reduces loading and increases switching speed.

Whenever any of the input pins are in a floating condition, the output of the respective channel is held in the low state. This function is achieved using V_{DD}-pullup resistors on all the inverting inputs (IN– pin) or GND-pulldown resistors on all the noninverting input pins (IN+ pin), (see the).

The device also features a dual-input configuration with two input pins available to control the state of the output. The user has the flexibility to drive the device using either a noninverting input pin (IN+) or an inverting input pin (IN–). The state of the output pin is dependent on the bias on both the IN+ and IN– pins. For additional clarification, refer to the I/O-logic truth table (Table 3) and the typical application diagrams, (Figure 25 and Figure 26).

When an input pin is selected for PWM drive, the other input pin (the *unused* input pin) must be properly biased in order to enable the output. As previously stated, the *unused* input pin cannot remain in a floating condition because whenever any input pin is left in a floating condition the output is disabled. Alternatively, the *unused* input pin can effectively be used to implement an enable or disable function. The following explains this function:

- In order to drive the device in a noninverting configuration, apply the PWM-control input signal to IN+ pin. In this case, the *unused* input pin, IN–, must be biased low (such as tied to GND) in order to enable the output.
  - Alternately, the IN– pin is used to implement the enable or disable function using an external logic signal.

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Feature Description (continued)

OUT is disabled when IN– is biased high and OUT is enabled when IN– is biased low.

- In order to drive the device in an inverting configuration, apply the PWM-control input signal to IN– pin. In this case, the *unused* input pin, IN+, must be biased high (such as tied to V_{DD}) in order to enable the output.
  - Alternately, the IN+ pin is used to implement the enable or disable function using an external logic signal. OUT is disabled when IN+ is biased low and OUT is enabled when IN+ is biased high.
- Finally, note that the output pin can be driven into a high state **only** when the IN+ pin is biased high and the IN– input is biased low.

The input stage of the driver is preferably driven by a signal with a short rise or fall time. Use caution whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout that is not optimal:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. The differential voltage between input pins and GND is modified and triggers an unintended change of output state because of fast 13-ns propagation delay which can ultimately result in high-frequency oscillations that increase power dissipation and pose a risk of damage to the device.
- A 1-V input-threshold hysteresis boosts noise immunity compared to most other industry standard drivers.
- In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor (1 nF) between the input pin and GND pin very close to the driver device may be necessary which helps to convert the differential mode noise with respect to the input-logic circuitry into common-mode noise and avoid unintended change of output state.

If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate-driver device package and transferring the power dissipation into the external resistor.

9.3.4 Enable Function

As mentioned earlier, an enable and disable function is easily implemented in UCC27511 and UCC27512 devices using the *unused* input pin. When the IN+ pin is pulled down to GND or the IN– pin is pulled down to V_{DD}, the output is disabled. Thus the IN+ pin can be used like an enable pin that is based on active-high logic, while the IN– pin can be used like an enable pin that is based on active-low logic.

9.3.5 Output Stage

Figure 23 shows the output stage of the UCC27511 and UCC27512 devices. The UCC27511 and UCC27512 devices feature a unique architecture on the output stage which delivers the highest peak-source current when the peak source current is most needed during the Miller plateau region of the power switch turnon transition (when the power-switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-channel and P-channel MOSFET devices. By turning on the N-channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turnon.

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Feature Description (continued)

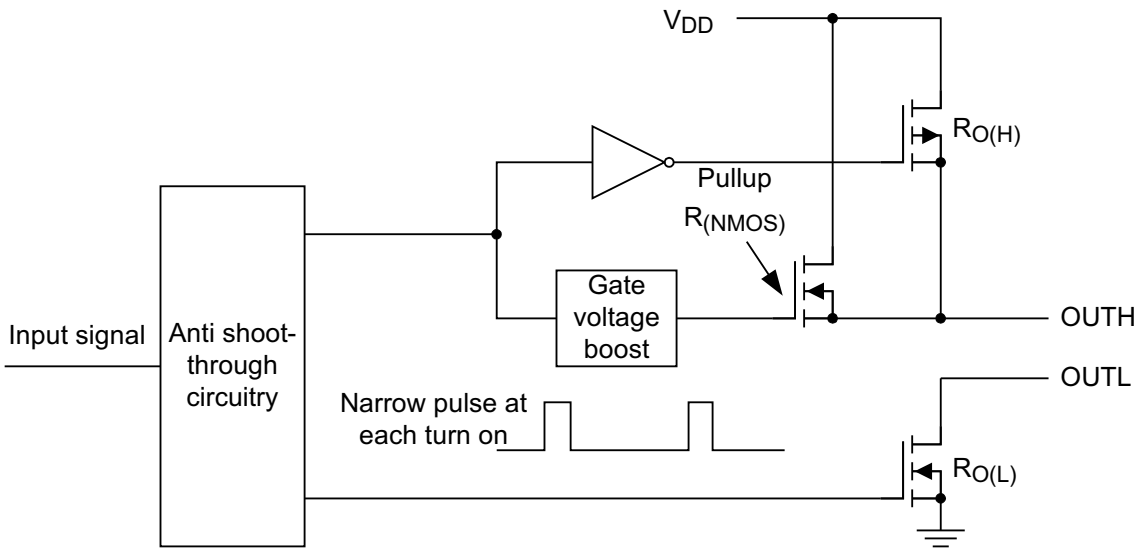


Figure 23. UCC27511 Gate Driver Output Structure

The $R_{O(H)}$ parameter (see the *Electrical Characteristics* table) is a DC measurement and is representative of the on-resistance of the P-channel device only, because the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by $R_{O(H)}$ parameter. The pulldown structure is composed of a N-channel MOSFET only. The $R_{O(L)}$ parameter (see the *Electrical Characteristics* table), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In the UCC27511 and UCC27512 devices, the effective resistance of the hybrid pullup structure is approximately 2.7 × $R_{O(L)}$.

The UCC27511 device features a unique split output configuration where the gate-drive current is sourced through the OUTH pin and sunk through the OUTL pin. This unique pin arrangement allows users to apply independent turnon and turnoff resistors to the OUTH and OUTL pins respectively and easily control the turnon and turnoff switching dV/dt. This pin arrangement, along with the low pulldown impedance of the output driver stage, is especially useful in applications where a high C × dV/dt Miller turnon immunity is needed (such as with GaN power switches, SR MOSFETs and other applications) and the OUTL pin can be directly tied to the gate of the power device.

The UCC27511 and UCC27512 devices are capable of delivering 4-A source, 8-A sink (asymmetrical drive) at V_{DD} equal to 12 V. Strong sink capability in asymmetrical drive results in a very-low pulldown impedance in the driver output stage which boosts immunity against parasitic, Miller turnon (C × dV/dt turnon) effect, especially where the low gate-charge MOSFETs or emerging wide band-gap GaN-power switches are used.

An example of a situation where the Miller turnon effect is a concern is synchronous rectification (SR). In an SR application, the dV/dt occurs on the MOSFET drain when the MOSFET is already held in off state by the gate driver. The current discharging the $C_{(GD)}$ Miller capacitance during this dV/dt is shunted by the pulldown stage of the driver. If the pulldown impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turnon. This phenomenon is shown in Figure 24. The UCC27511 and UCC27512 device offers a best-in-class, 0.375-Ω (typ) pulldown impedance boosting immunity against Miller turnon.

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Feature Description (continued)

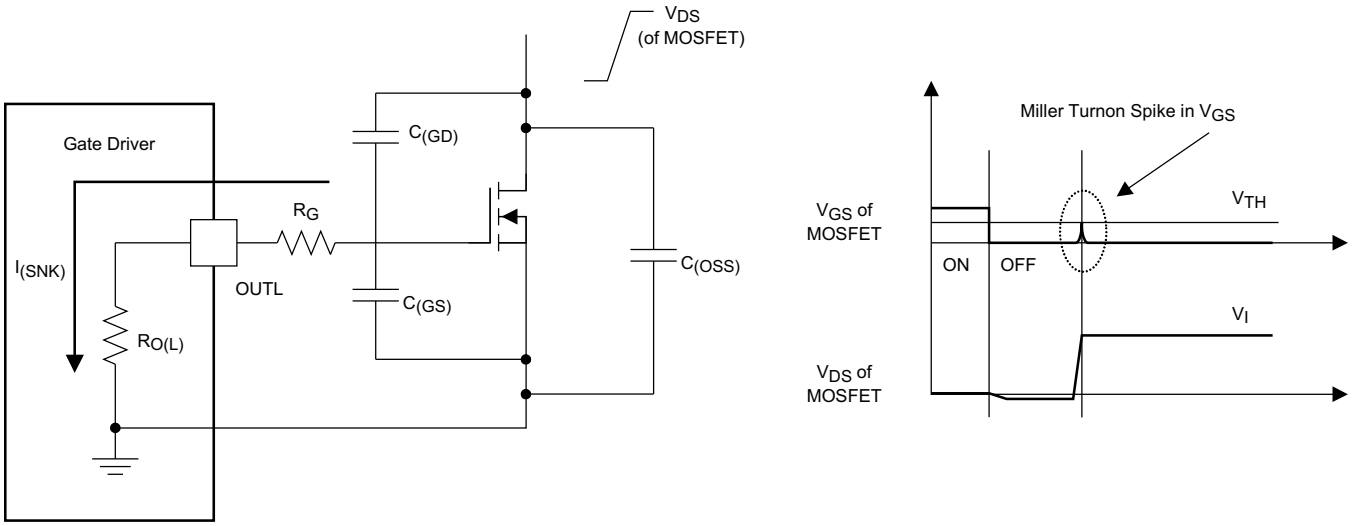


Figure 24. Very-Low Pulldown Impedance in UCC27511 and UCC27512, 4-A and 8-A Asymmetrical Drive (Output Stage Mitigates Miller Turnon Effect)

The driver-output voltage swings between the V_{DD} and GND pins which provides rail-to-rail operation as a result of the MOS-output stage which delivers very-low dropout. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. In many cases, external Schottky diode clamps are eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

9.3.6 Low Propagation Delays

The UCC27511 and UCC27512 driver devices feature best-in-class input-to-output propagation delay of 13 ns (typ) at V_{DD} = 12 V, which promises the lowest level of pulse transmission distortion available from industry-standard gate-driver devices for high-frequency switching applications. As seen in Figure 14, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

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9.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See the *V_{DD} and Undervoltage Lockout* section for information on UVLO operation mode. In the normal mode the output state is dependent on states of the IN+ and IN– pins. Table 3 lists the output states for different input pin combinations.

Table 3. Device Logic Table

IN+ PIN	IN- PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together in the UCC27511)
L	L	High impedance	L	L
L	H	High impedance	L	L
H	L	H	High impedance	H
H	H	High impedance	L	L
x(1)	Any	High impedance	L	L
Any	x(1)	High impedance	L	L

(1) x = Floating Condition

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

High-current gate-driver devices are required in switching-power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver employs between the PWM output of controllers and the gates of the power-semiconductor devices. Further, gate drivers are indispensable when having the PWM controller directly drive the gates of the switching devices is impossible. With advent of digital power, this situation will be often encountered since the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power since they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low V_{DD} voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance low-cost component count and board-space reduction and simplified system design.

10.2 Typical Application

Typical application diagrams of UCC27511 and UCC27512 devices are shown below illustrating use in non-inverting and inverting driver configurations. The UCC27511 device features a unique split output configuration where the gate-drive current is sourced through OUTH pin and sunk through OUTL pin. This unique pin arrangement allows user to apply independent turn-on and turn-off resistors to the OUTH and OUTL pins respectively and easily control the turn-on and turn-off switching dV/dt. This pin arrangement, along with the low pulldown impedance of the output driver stage, is especially handy in applications where a high C x dV/dt Miller turnon immunity is needed (such as with GaN power switches, SR MOSFETs, and so forth) and OUTL pin can be directly tied to the gate of the power device.

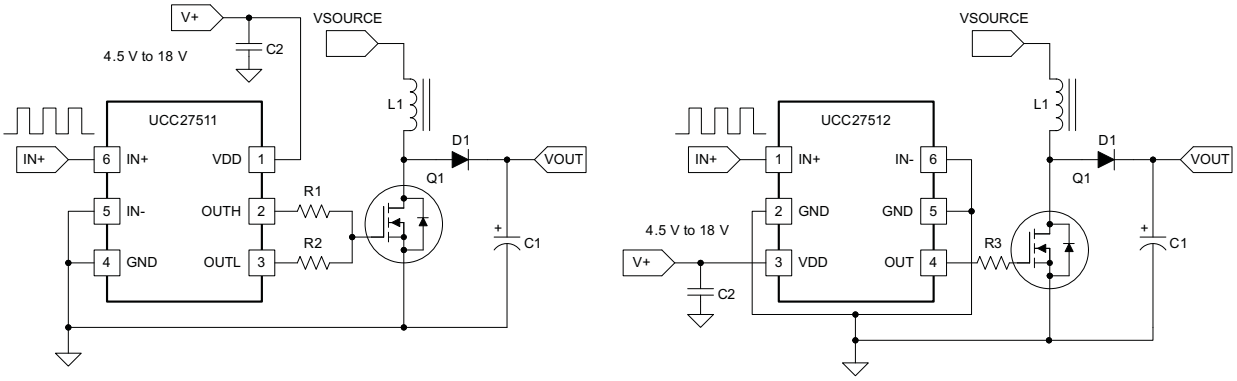


Figure 25. Using Noninverting Input (IN– Is Grounded to Enable Output)

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Typical Application (continued)

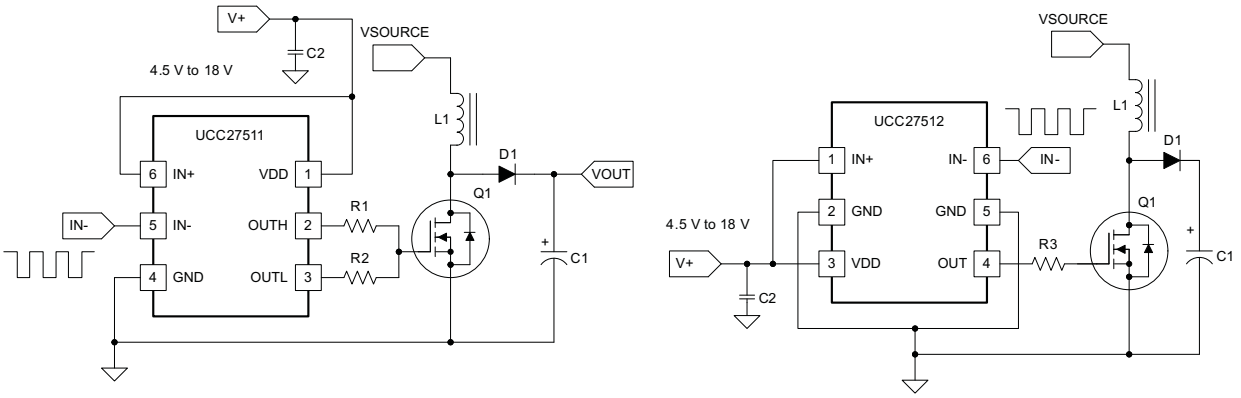


Figure 26. Using Inverting Input (IN+ Is Tied to V_{DD} Enable Output)

NOTE

The UCC27512 features two ground pins, pin 2 and pin 5. TI recommends tying both pins together using PCB trace as close as possible to the device.

10.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type.

10.2.2 Detailed Design Procedure

10.2.2.1 Input-to-Output Logic

The design should specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the non-inverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be chosen. The UCC27511 and UCC27512 devices can be configured in either an inverting or noninverting input-to-output configuration using the IN– or IN+ pins respectively. To configure the device for use in inverting mode, tie the IN+ pin to V_{DD} and apply the input signal to the IN– pin. For the noninverting configuration, tie the IN– pin to GND and apply the input signal to the IN+ pin.

10.2.2.2 Input Threshold Type

The type of Input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC27511 and UCC27512 devices feature a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the V_{DD} supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the *Electrical Characteristics* table for the actual input threshold voltage levels and hysteresis specifications for the UCC27511 and UCC27512 devices.

10.2.2.3 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pin of the device should never exceed the values listed in the *Recommended Operating Conditions* table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the V_{DD} bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC27511 and UCC27512 devices can be used to drive a variety of power switches, such as Si MOSFETs (for example, V_{GS} = 4.5 V, 10 V, 12 V), IGBTs (V_{GE} = 15 V, 18 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

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Typical Application (continued)

10.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turn-on event (from 400 V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (Q_{GD} parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$.

In order to achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the Q_{GD} charge in 20 ns or less. In other words a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC27511 and UCC27512 gate driver is capable of providing 4-A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 2.4x overdrive capability provides an extra margin against part-to-part variations in the Q_{GD} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations.

However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × I_{PEAK} × time) would equal the total gate charge of the power MOSFET (Q_G parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

10.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers an enable and disable function achieves this requirement. The UCC27511 and UCC27512 devices offer 2 input pins, IN+ and IN–, both of which control the state of the output as listed in Table 3. Based on whether an inverting or noninverting input signal is provided to the driver, the appropriate input pin can be selected as the primary input for controlling the gate driver. The other *unused* input pin can be conveniently used for the enable and disable functionality. If the design does not require an enable function, the unused input pin can be tied to either the V_{DD} pin (in case IN+ is the unused pin), or GND (in case IN– is unused pin) in order to ensure it does not affect the output status.

10.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27511 and UCC27512 devices feature industry best-in-class 13-ns (typical) propagation delays which ensures very little pulse distortion and allows operation at very high-frequencies. See the table for the propagation and switching characteristics of the UCC27511 and UCC27512 devices.

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Typical Application (continued)

10.2.2.7 Thermal Information

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is listed in the table. For detailed information regarding the table, please refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (SPRA953).

The UCC27511 device is offered in a SOT-23, 6-pin package (DBV). The section lists the thermal performance metrics related to SOT-23 package. The ψ_{JT} and ψ_{JB} metrics are used when estimating the die temperature during actual application measurements.

Heat removal occurs primarily through the leads of the device and the PCB traces connected to the leads.

10.2.2.8 Power Dissipation

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27511 and UCC27512 features very low quiescent currents (less than 1 mA, refer Figure 7) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out).
- Switching frequency.
- Use of external gate resistors.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver (2)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by Equation 3.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when charging a capacitor which is calculated using the equation, $Q_G = C_{LOAD}$ x V_{DD}, to provide Equation 4 for power.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (4)$$

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Typical Application (continued)

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated in Equation 5.

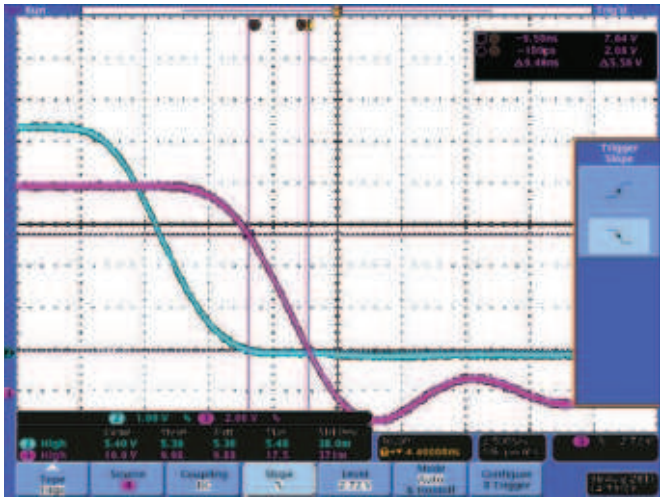
$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure) = 2.7 x R_{OL} (5)

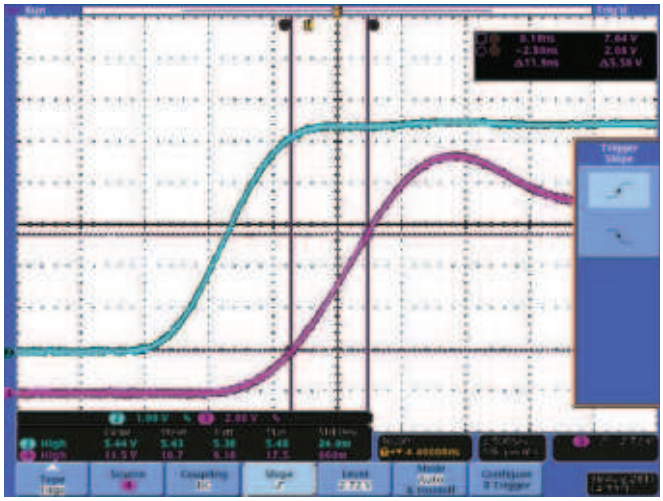
10.2.3 Application Curves

Figure 27 and Figure 28 show the typical switching characteristics of the UCC27511 device.



V_{DD} = 10 V $C_{(LOAD)}$ = 1 nF

Figure 27. Typical Turnon Waveform



V_{DD} = 10 V $C_{(LOAD)}$ = 1 nF

Figure 28. Typical Turnoff Waveform

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11 Power Supply Recommendations

The bias supply voltage range for which the UCC27511 and UCC27512 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. Therefore, ensuring that, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown.

During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup, the device does not begin operation until the V_{DD} pin voltage has exceeded above the $V_{(ON)}$ threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTH pin is also supplied through the same V_{DD} pin is important. As a result, every time a current is sourced out of the output pins (OUTH), a corresponding current pulse is delivered into the device through the V_{DD} pin. Thus ensuring that local bypass capacitors are provided between the V_{DD} and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low ESR, ceramic surface mount capacitor is a must. TI recommends to have 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device and another surface-mount capacitor of few microfarads added in parallel.

12 Layout

12.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27511 and UCC27512 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher V_{DD} voltages, the peak-current capability is even higher (4-A/8-A peak current is at V_{DD} = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit-layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the V_{DD}-bypass capacitors between V_{DD} and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from V_{DD} during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current-loop paths (driver device, power MOSFET and V_{DD} bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances – during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller, and so forth, at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals

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Layout Guidelines (continued)

during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

- In noisy environments, tying the unused Input pin of UCC27511 and UCC27512 to V_{DD} (in case of IN+) or GND (in case of IN-) using short traces in order to ensure that the output is enabled and to prevent noise from causing malfunction in the output may be necessary.
- The UCC27512 device offers two ground pins, pin 2 and pin 5. Shorting the two pins together using the PCB trace is extremely important. The shortest trace should be located as close as possible to the device.

12.2 Layout Example

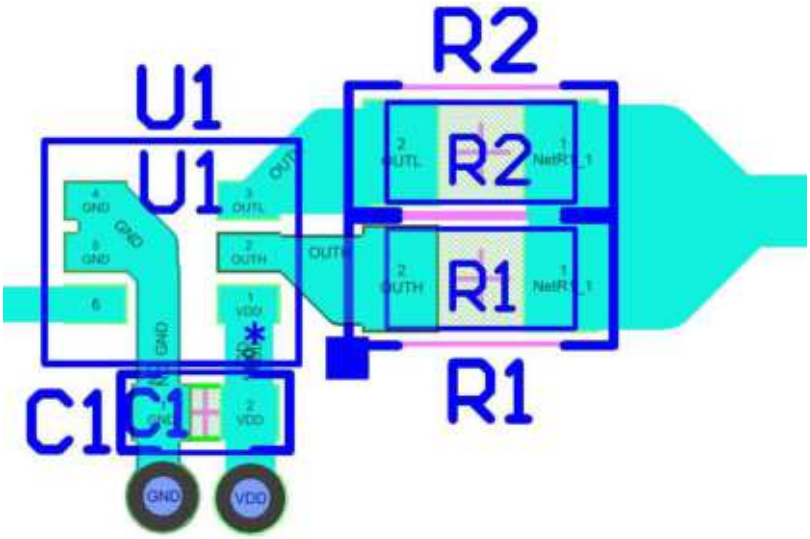


Figure 29. UCC27511 Layout Example

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13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27511	Click here	Click here	Click here	Click here	Click here
UCC27512	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27511DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27511DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27511DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27511DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27511DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27511DBVT.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27511DBVTG4	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27511DBVTG4.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27511DBVTG4.B	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7511
UCC27512DRSR	Active	Production	SON (DRS) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27512
UCC27512DRSR.A	Active	Production	SON (DRS) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27512
UCC27512DRST	Active	Production	SON (DRS) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27512
UCC27512DRST.A	Active	Production	SON (DRS) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 140	27512

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27512 :

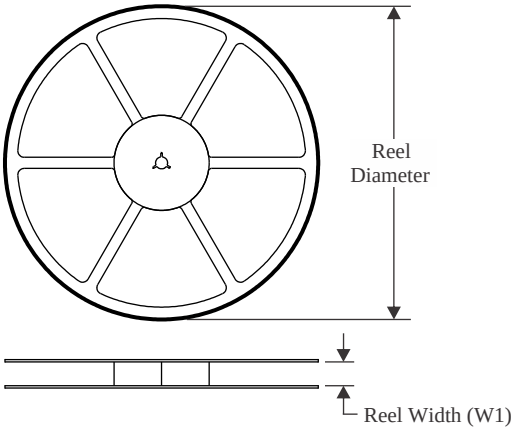
- Enhanced Product : UCC27512-EP

NOTE: Qualified Version Definitions:

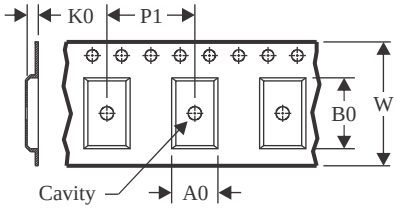
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

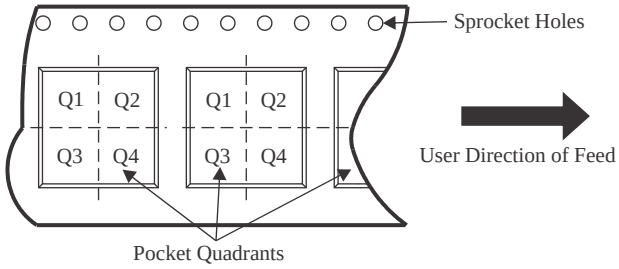


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

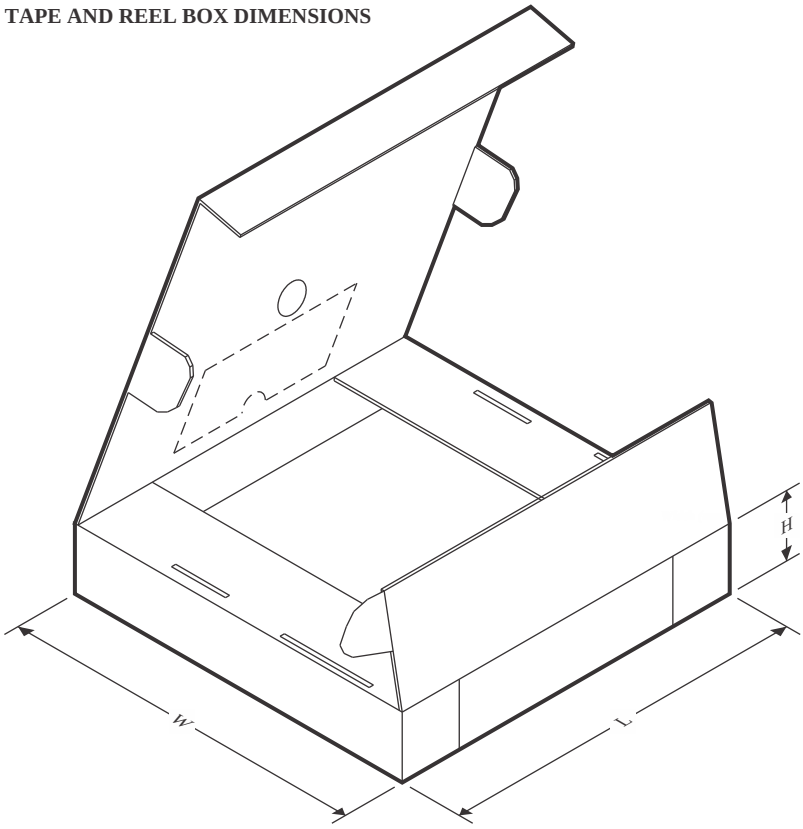
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27511DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27511DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27511DBVTG4	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27512DRSR	SON	DRS	6	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27512DRST	SON	DRS	6	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

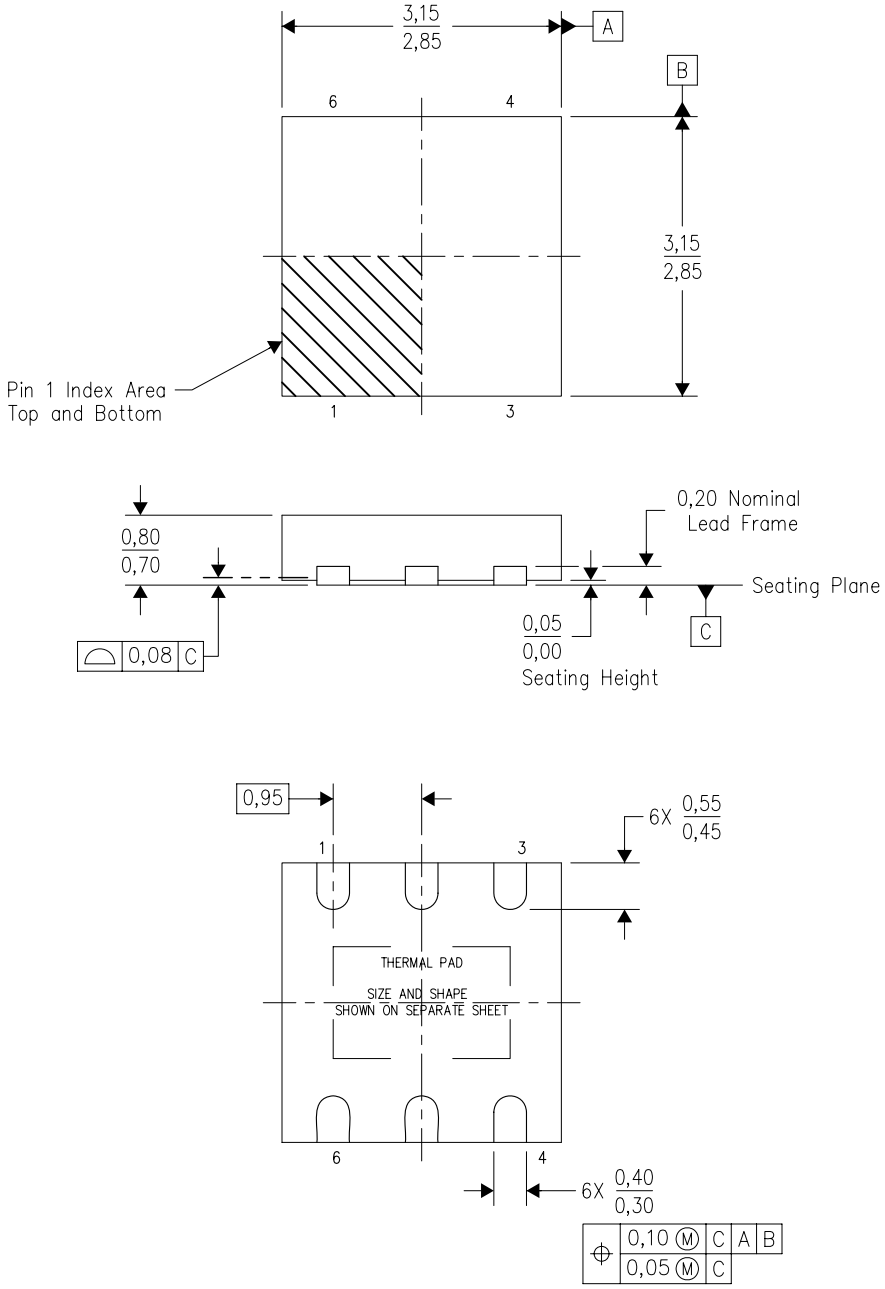
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27511DBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
UCC27511DBVT	SOT-23	DBV	6	250	200.0	183.0	25.0
UCC27511DBVTG4	SOT-23	DBV	6	250	200.0	183.0	25.0
UCC27512DRSR	SON	DRS	6	3000	346.0	346.0	33.0
UCC27512DRST	SON	DRS	6	250	210.0	185.0	35.0

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206219/F 07/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

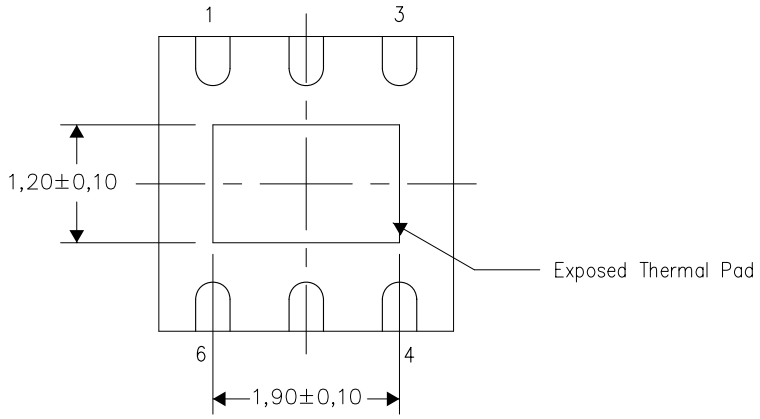
DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



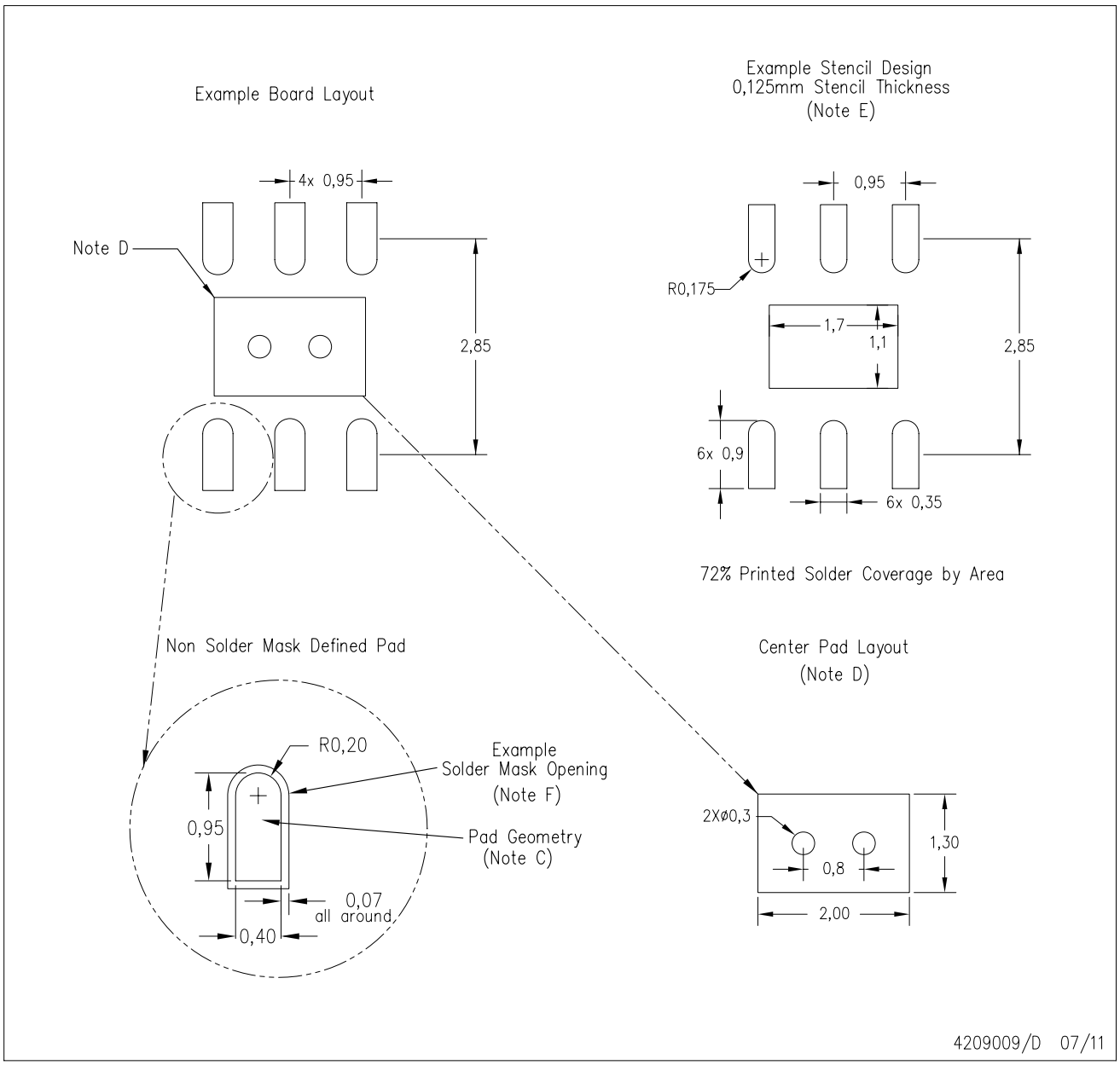
Bottom View

Exposed Thermal Pad Dimensions

4207663/E 07/11

NOTE: All linear dimensions are in millimeters

DRS (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



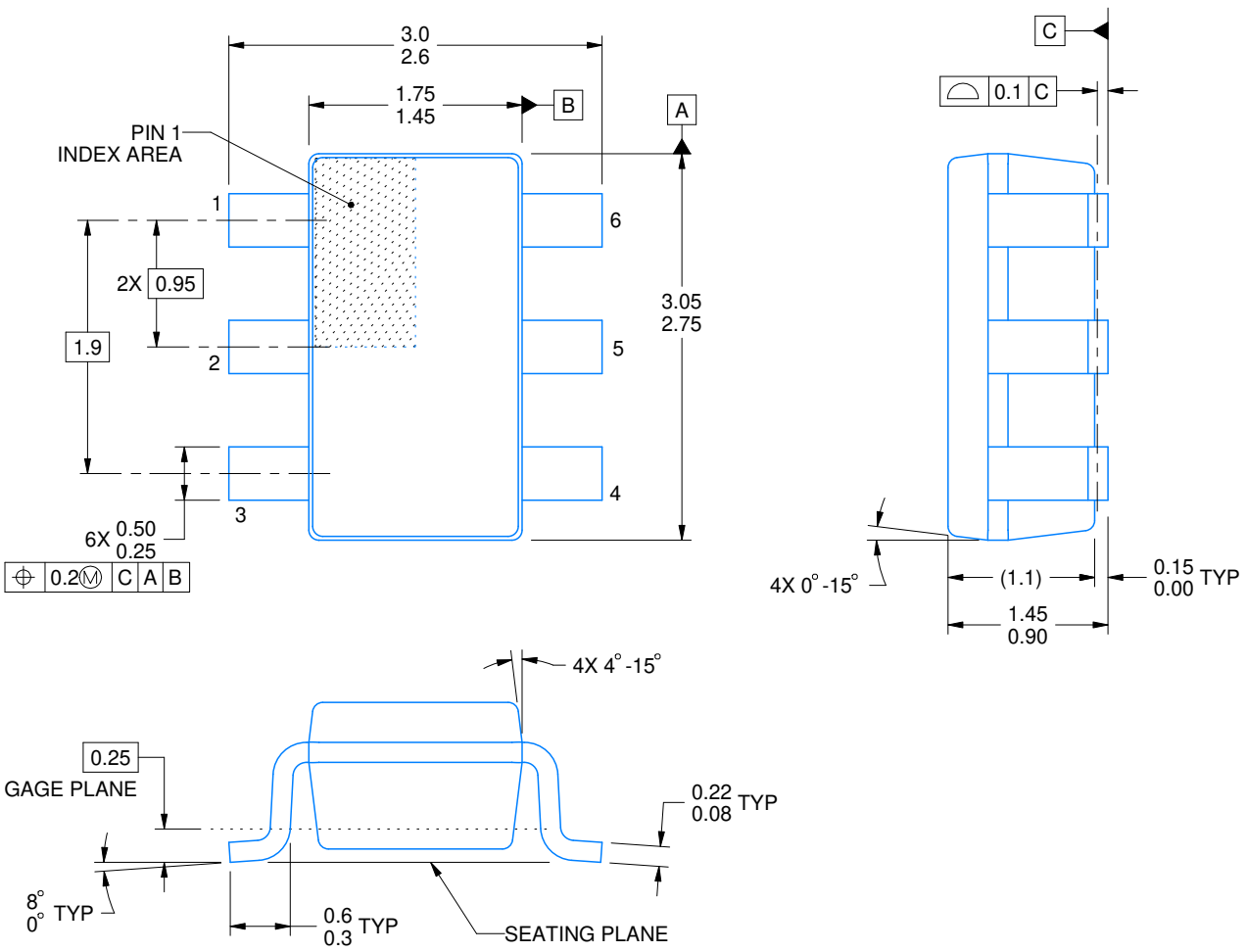
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

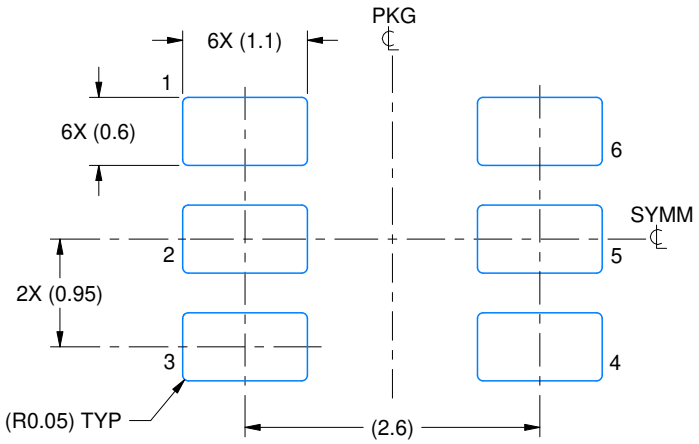
SMALL OUTLINE TRANSISTOR



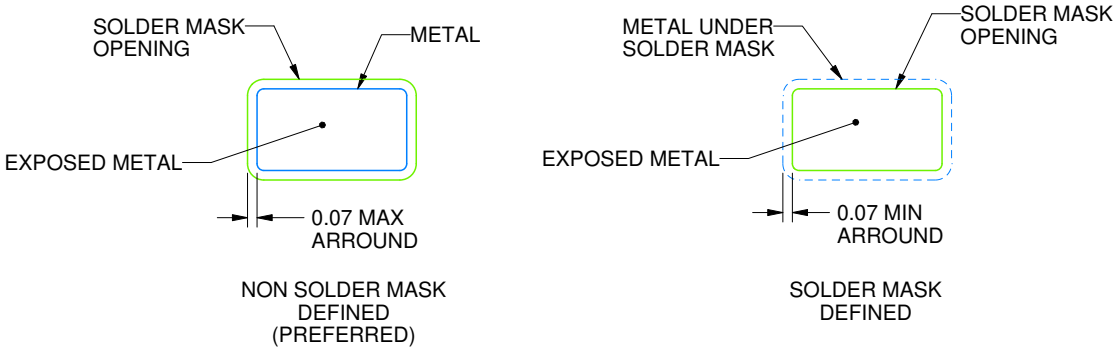
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

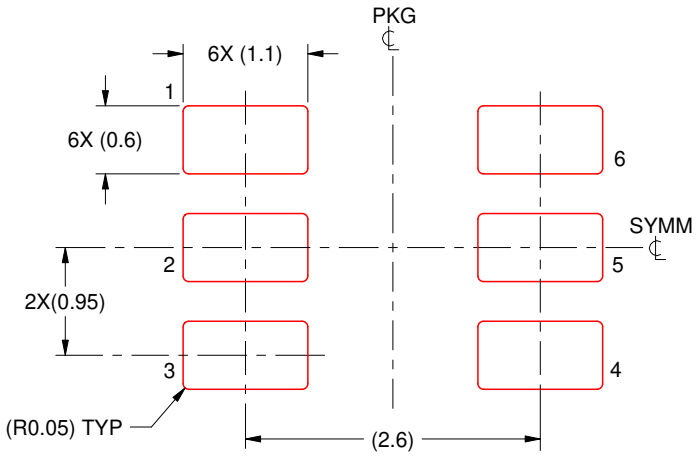


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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