UCC28019A 8-Pin Continuous Conduction Mode (CCM) PFC Controller

1 Features

- 8-Pin Solution Reduces External Components
- Wide-Range Universal AC Input Voltage
- Fixed 65-kHz Operating Frequency
- Maximum Duty Cycle of 98% (typ.)
- Output Over/Undervoltage Protection
- Input Brown-Out Protection
- Cycle-by-Cycle Peak Current Limiting
- Open Loop Detection
- Low-Power User-Controlled Standby Mode

2 Applications

- CCM Boost Power Factor Correction Power Converters in the 100 W to >2 kW Range
- Digital TV
- Home Electronics
- White Goods and Industrial Electronics
- Server and Desktop Power Supplies

3 Description

The UCC28019A 8-pin active Power Factor Correction (PFC) controller uses the boost topology operating in Continuous Conduction Mode (CCM). The controller is suitable for systems in the 100 W to >2 kW range over a wide-range universal ac line input. Start-up current during undervoltage lockout is less than 200 μA. The user can control low power standby mode by pulling the VSENSE pin below 0.77 V.

Low-distortion wave shaping of the input current using average current mode control is achieved without input line sensing, reducing the external component count. Simple external networks allow for flexible compensation of the current and voltage control loops. The switching frequency is internally fixed and trimmed to better than ±5% accuracy at 25°C. Fast 1.5-A peak gate current drives the external switch.

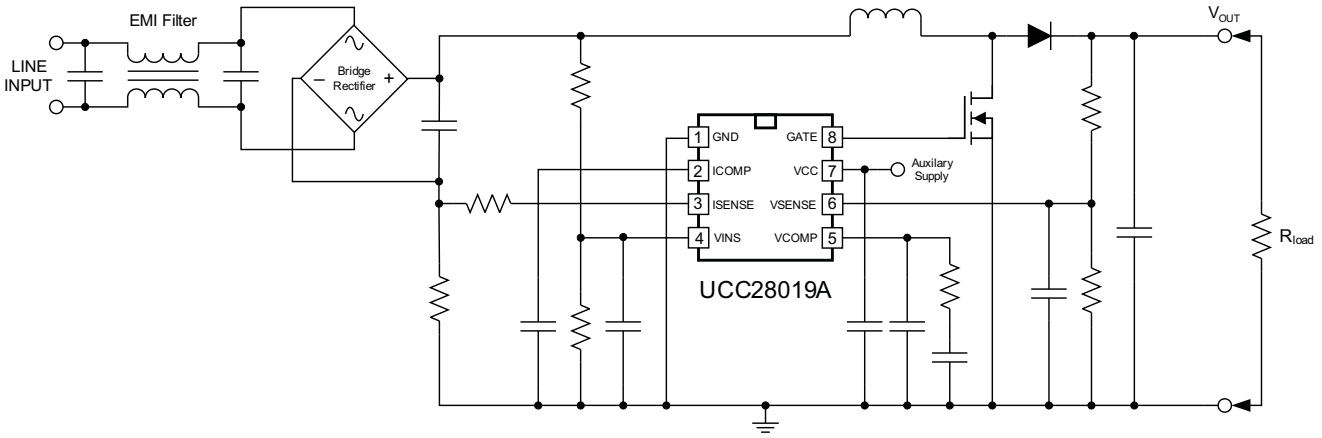
Numerous system-level protection features include peak current limit, soft over-current, open-loop detection, input brown-out, and output over/undervoltage. Soft-start limits boost current during start-up. A trimmed internal reference provides accurate protection thresholds and a regulation set-point. An internal clamp limits the gate drive voltage to 12.5 V.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28019A	SOIC (8)	3.91 mm × 4.9 mm
	PDIP (8)	6.35 mm × 9.81 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features 1
2 Applications 1
3 Description 1
4 Revision History 2
5 Pin Configuration and Functions 3
6 Specifications 4
6.1 Absolute Maximum Ratings 4
6.2 ESD Ratings 4
6.3 Recommended Operating Conditions 4
6.4 Thermal Information 4
6.5 Electrical Characteristics 5
6.6 Typical Characteristics 7
7 Detailed Description 10
7.1 Overview 10
7.2 Functional Block Diagram 11
7.3 Feature Description 12
7.4 Device Functional Modes 19
8 Application and Implementation 20
8.1 Application Information 20
8.2 Typical Application 21
9 Power Supply Recommendations 40
9.1 Bias Supply 40
10 Layout 41
10.1 Layout Guidelines 41
10.2 Layout Example 42
11 Device and Documentation Support 43
11.1 Device Support 43
11.2 Documentation Support 43
11.3 Community Resources 43
11.4 Trademarks 43
11.5 Electrostatic Discharge Caution 43
11.6 Glossary 43
12 Mechanical, Packaging, and Orderable Information 44

4 Revision History

Changes from Revision C (August 2015) to Revision D **Page**

- Changed VCOMP and ICOMP MAX value from 7 V to 7.5 V. 4
- Added VCOMP and ICOMP note. 4

Changes from Revision B (April 2009) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

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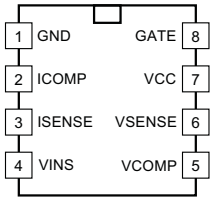
5 Pin Configuration and Functions

D, P Package
8-Pin SOIC, 8-Pin PDIP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO. SOIC, PDIP		
GND	1	—	Ground: device ground reference.
ICOMP	2	O	Current loop compensation: Transconductance current amplifier output. A capacitor connected to GND provides compensation and averaging of the current sense signal in the current control loop. The controller is disabled if the voltage on ICOMP is less than 0.6 V.
ISENSE	3	I	Inductor current sense: Input for the voltage across the external current sense resistor, which represents the instantaneous current through the PFC boost inductor. This voltage is averaged by the current amplifier to eliminate the effects of ripple and noise. Soft Over Current (SOC) limits the average inductor current. Cycle-by-cycle Peak Current Limit (PCL) immediately shuts off the GATE drive if the peak-limit voltage is exceeded. An internal 1.5-μA current source pulls ISENSE above 0.1 V to shut down PFC operation if this pin becomes open-circuited. Use a 220-Ω resistor between this pin and the current sense resistor to limit inrush-surge currents into this pin.
VINS	4	I	Input ac voltage sense: A filtered resistor-divider network connects from this pin to the rectified-mains node. Input Brown-Out Protection (IBOP) detects when the system ac-input voltage is above a user-defined normal operating level, or below a user-defined “brown-out” level. At startup the controller is disabled until the VINS voltage exceeds a threshold of 1.5 V, initiating a soft start. The controller is also disabled if VINS drops below the brown-out threshold of 0.8 V. Operation will not resume until both VINS and VSENSE voltages exceed their enable thresholds, initiating another soft start.
VCOMP	5	O	Voltage loop compensation: Transconductance voltage error amplifier output. A resistor-capacitor network connected from this pin to GND provides compensation. VCOMP is held at GND until VCC, VINS, and VSENSE all exceed their threshold voltages. Once these conditions are satisfied, VCOMP is charged until the VSENSE voltage reaches 99% of its nominal regulation level. When Enhanced Dynamic Response (EDR) is engaged, a higher transconductance is applied to VCOMP to reduce the charge time for faster transient response. Soft Start is programmed by the capacitance on this pin. The EDR higher transconductance is inhibited during Soft Start.
VSENSE	6	I	Output voltage sense: An external resistor-divider network connected from this pin to the PFC output voltage provides feedback sensing for regulation to the internal 5-V reference voltage. A small capacitor from this pin to GND filters high-frequency noise. Standby mode disables the controller and discharges VCOMP when the voltage at VSENSE drops below the enable threshold of 0.8 V. An internal 100-nA current source pulls VSENSE to GND for Open-Loop Protection (OLP), including pin disconnection. Output Over-Voltage Protection (OVP) disables the GATE output when VSENSE exceeds 105% of the reference voltage. Enhanced Dynamic Response (EDR) rapidly returns the output voltage to its normal regulation level when a system line or load step causes VSENSE to fall below 95% of the reference voltage.
VCC	7		Device supply: External bias supply input. Under-Voltage Lockout (UVLO) disables the controller until VCC exceeds a turn-on threshold of 10.5 V. Operation continues until VCC falls below the turn-off (UVLO) threshold of 9.5 V. A ceramic by-pass capacitor of 0.1 μF minimum value should be connected from VCC to GND as close to the device as possible for high frequency filtering of the VCC voltage.
GATE	8	O	Gate drive: Integrated push-pull gate driver for one or more external power MOSFETs. Typical 2.0-A sink and 1.5-A source capability. Output voltage is typically clamped at 12.5 V.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range unless otherwise noted. Unless noted, all voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

		MIN	MAX	UNIT
Input voltage range	VCC, GATE	–0.3	22	V
	VINS, VSENSE,	–0.3	7	V
	VCOMP, ICOMP(2)	–0.3	7.5	V
	ISENSE	–24	7	V
Input current range	VSENSE, ISENSE	–1	1	mA
Lead temperature, T_{SOL}	Soldering, 10s		300	°C
Junction temperature, T_J	Operating	–55	150	°C
	Storage	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.
(2) The VCOMP and ICOMP pin can go to 7.5 V ±6% due to internal drive circuitry. Absolute maximum rating is 7 V when an external bias is applied to the pin, with the source current limited below 50 µA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VCC input voltage from a low-impedance source	VCC_{OFF} + 1 V	21	V
Operating junction temperature, T_J	-40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC28019A		UNIT
		P (PDIP)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.8	113.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	61.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.0	53.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.5	15.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.9	52.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Unless otherwise noted, VCC=15 V_{DC}, 0.1 µF from VCC to GND, -40°C ≤ T_J = T_A ≤ 125°C. All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
VCC Bias Supply						
$ICC_{PRESTART}$	ICC pre-start current	VCC = VCC_{ON} – 0.1 V	25	100	200	µA
ICC_{STBY}	ICC standby current	VSENSE = 0.5 V	1	2.2	2.9	mA
ICC_{ON_load}	ICC operating current	VSENSE = 4.5 V, C_{GATE} = 4.7 nF	4	7.5	10	mA
Under Voltage Lockout (UVLO)						
VCC_{ON}	VCC turn on threshold		10	10.5	11	V
VCC_{OFF}	VCC turn off threshold		9	9.5	10	V
	UVLO hysteresis		0.8	1	1.2	V
Oscillator						
f_{SW}	Switching frequency	T_A = 25°C	61.7	65	68.3	kHz
		-25°C ≤ T_A ≤ 125°C	59	65	71	kHz
		-40°C ≤ T_A ≤ 125°C	57		71	kHz
PWM						
D_{MIN}	Minimum duty cycle	VCOMP = 0 V, VSENSE = 5 V, ICOMP = 6.4 V			0%	
D_{MAX}	Maximum duty cycle	VSENSE = 4.95 V	94%	98%	99.3%	
$t_{OFF(min)}$	Minimum off time	VSENSE = 3 V, ICOMP = 1 V	100	250	600	ns
System Protection						
V_{SOC}	ISENSE threshold, Soft Over Current (SOC)		-0.66	-0.73	-0.79	V
V_{PCL}	ISENSE threshold, Peak Current Limit (PCL)		-1	-1.08	-1.15	V
I_{ISOP}	ISENSE bias current, ISENSE Open-Pin Protection (ISOP)	ISENSE = 0 V		-2.1	-4.0	µA
V_{ISOP}	ISENSE threshold, ISENSE Open-Pin Protection (ISOP)	ISENSE = open pin		0.082		V
V_{OLP}	VSENSE threshold, Open Loop Protection (OLP)	ICOMP = 1 V, ISENSE = -0.1 V, VCOMP = 1 V	0.77	0.82	0.86	V
	Open Loop Protection (OLP) Internal pull-down current	VSENSE = 0.5 V		100	250	nA
V_{UVD}	VSENSE threshold, output Under-Voltage Detection (UVD) (1)		4.63	4.75	4.87	V
V_{OVP}	VSENSE threshold, output Over-Voltage Protection (OVP)	ISENSE = -0.1 V	5.12	5.25	5.38	V
$V_{INSBROWNOUT_th}$	Input Brown-Out Detection (IBOP) high-to-low threshold		0.76	0.82	0.88	V
$V_{INSENABLE_th}$	Input Brown-Out Detection (IBOP) low-to-high threshold		1.4	1.5	1.6	V
I_{VINS_0V}	VINS bias current	VINS = 0 V		0	±0.1	µA
	ICOMP threshold, external overload protection			0.6		V

(1) Not production tested. Characterized by design.

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Electrical Characteristics (continued)

Unless otherwise noted, VCC=15 V_{DC}, 0.1 µF from VCC to GND, -40°C ≤ T_J = T_A ≤ 125°C. All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Current Loop						
g_{mi}	Transconductance gain	T_A = 25°C	0.75	0.95	1.15	mS
	Output linear range(1)			±50		µA
	ICOMP voltage during OLP	VSENSE = 0.5 V	3.7	4	4.3	V
Voltage Loop						
V_{REF}	Reference voltage	-40°C ≤ T_A ≤ 125°C	4.9	5	5.1	V
g_{mv}	Transconductance gain without EDR		-31.5	-42	-52.5	µS
$g_{mv\text{-}EDR}$	Transconductance gain under EDR	VSENSE = 4.65 V		-440		µS
	Maximum sink current under normal operation	VSENSE = 6 V, VCOMP = 4 V	21	30	38	µA
	Source current under soft start	VSENSE = 4 V, VCOMP = 2.5 V	-21	-30	-38	µA
	Maximum source current under EDR operation	VSENSE = 4 V, VCOMP = 2.5 V		-300		µA
		VSENSE = 4 V, VCOMP = 4 V		-170		µA
	Enhanced dynamic response VSENSE low threshold, falling(1)		4.63	4.75	4.87	V
	VSENSE input bias current	VSENSE = 5 V	20	100	250	nA
	VCOMP voltage during OLP	VSENSE = 0.5 V, I_{VCOMP} = 0.5 mA	0	0.2	0.4	V
	VCOMP rapid discharge current	VCOMP = 3 V, VCC = 0 V		0.77		mA
$V_{PRECHARGE}$	VCOMP precharge voltage	I_{VCOMP} = -100 µA, VSENSE = 5 V		1.76		V
$I_{PRECHARGE}$	VCOMP precharge current	VCOMP = 1.0 V		-1		mA
	VSENSE threshold, end of soft start	Initial start up		4.95		V
GATE Driver						
	GATE current, peak, sinking(1)	C_{GATE} = 4.7 nF		2		A
	GATE current, peak, sourcing(1)	C_{GATE} = 4.7 nF		-1.5		A
	GATE rise time	C_{GATE} = 4.7 nF, GATE = 2 V to 8 V	8	40	60	ns
	GATE fall time	C_{GATE} = 4.7 nF, GATE = 8 V to 2 V	8	25	40	ns
	GATE low voltage, no load	I_{GATE} = 0 A		0	0.05	V
	GATE low voltage, sinking	I_{GATE} = 20 mA		0.3	0.8	V
	GATE low voltage, sourcing	I_{GATE} = -20 mA		-0.3	-0.8	V
	GATE low voltage, sinking, device OFF	VCC = 5 V, I_{GATE} = 5 mA	0.2	0.75	1.2	V
		VCC = 5 V, I_{GATE} = 20 mA	0.2	0.9	1.5	V
	GATE high voltage	VCC = 20 V, C_{GATE} = 4.7 nF	11.0	12.5	14.0	V
		VCC = 11 V, C_{GATE} = 4.7 nF	9.5	10.5	11.0	V
		VCC = VCC_{OFF} + 0.2 V, C_{GATE} = 4.7 nF	8.0	9.4	10.2	V

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6.6 Typical Characteristics

Unless otherwise noted, VCC = 15 V_{DC}, 0.1 µF from VCC to GND, -40°C ≤ T_J = T_A ≤ 125°C. All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

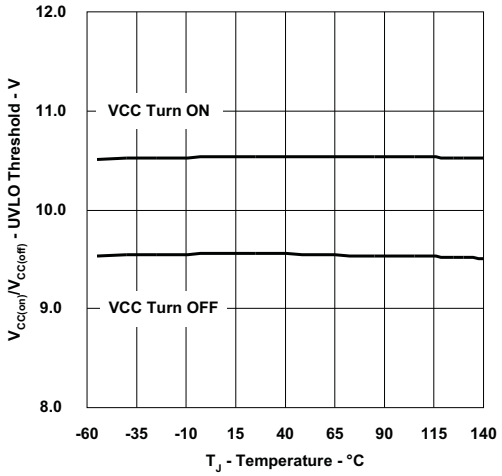

Figure 1. UVLO Thrasholds vs Temperature

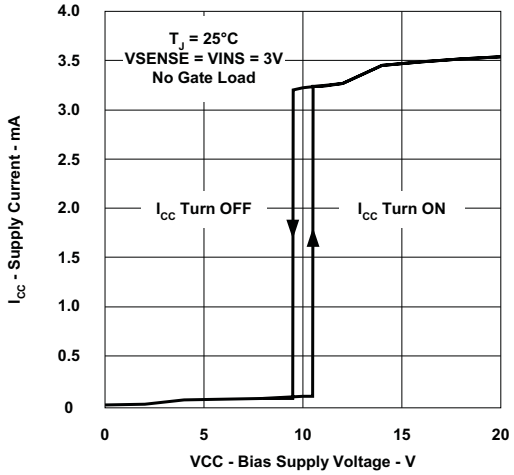

Figure 2. Supply Current vs Bias Supply Voltage

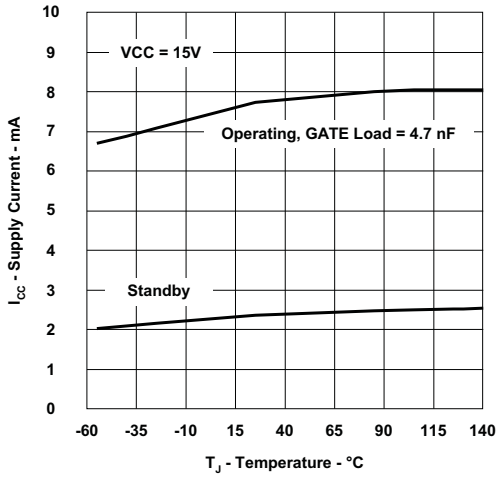

Figure 3. Supply Current vs Temperature

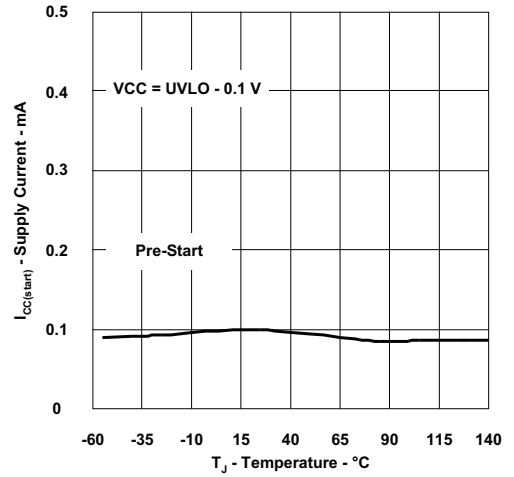

Figure 4. Supply Current vs Temperature

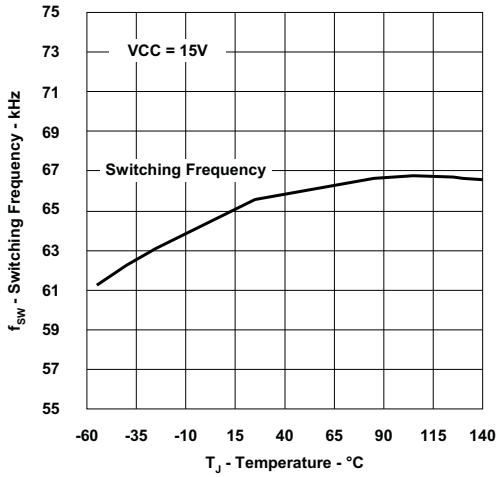

Figure 5. Oscillator Frequency vs Temperature

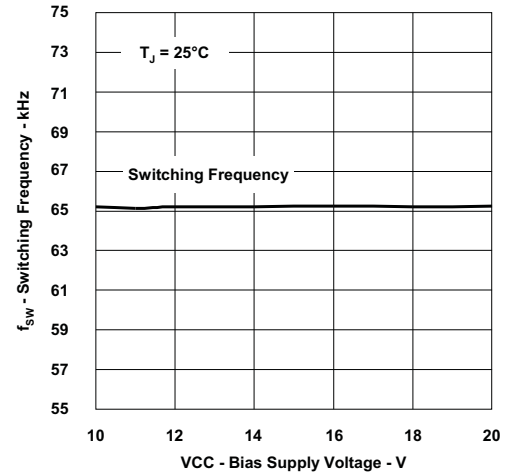

Figure 6. Oscillator Frequency vs Bias Supply Voltage

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Typical Characteristics (continued)

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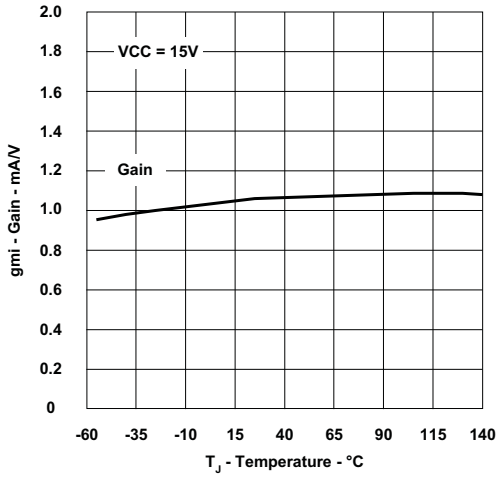

Figure 7. Current Averaging Amplifier Transconductance vs Temperature

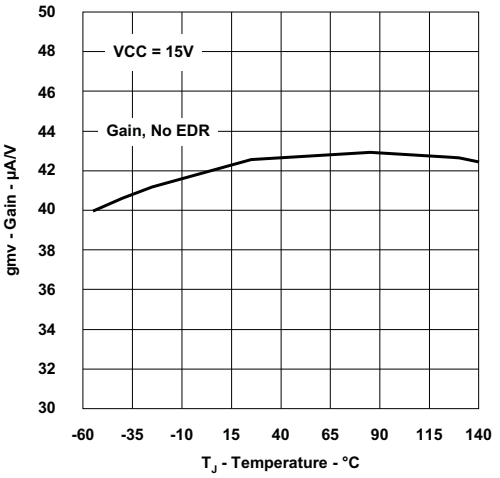

Figure 8. Voltage Error Amplifier Transconductance vs Temperature

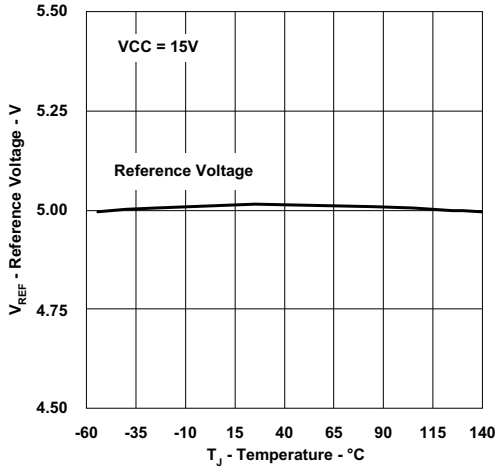

Figure 9. Reference Voltage vs Temperature

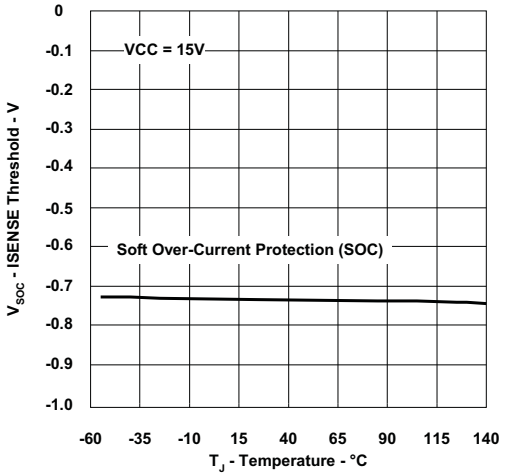

Figure 10. ISENSE Threshold vs Temperature

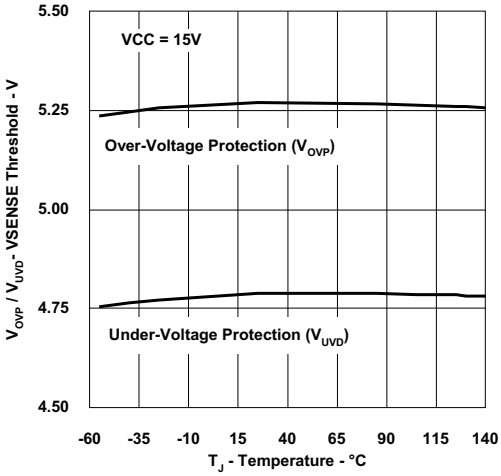

Figure 11. VSENSE Threshold vs Temperature

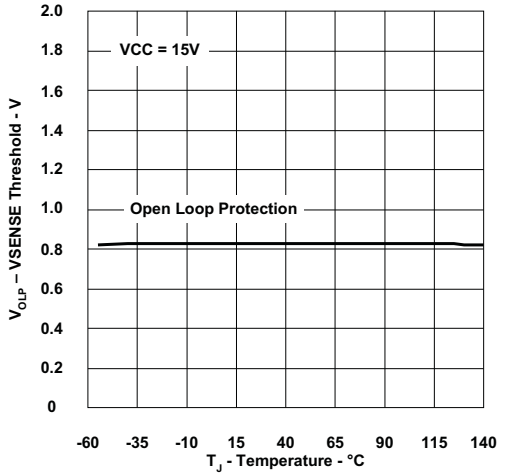

Figure 12. VSENSE Threshold vs Temperature

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Typical Characteristics (continued)

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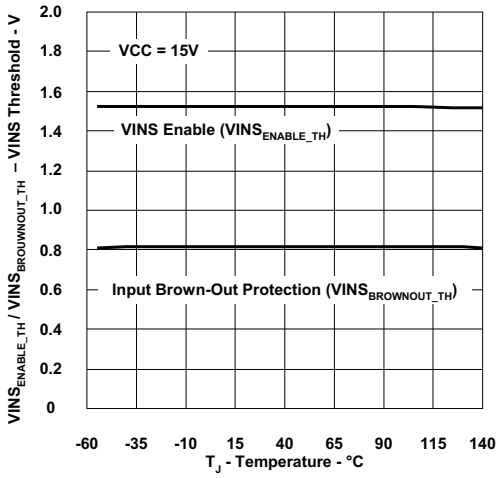

Figure 13. VINS Threshold vs Temperature

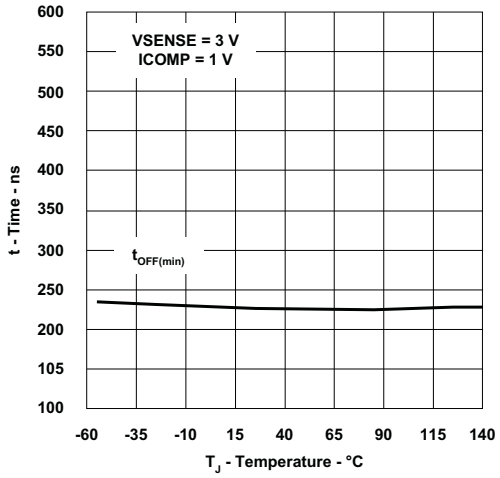

Figure 14. Minimum Off Time vs Temperature

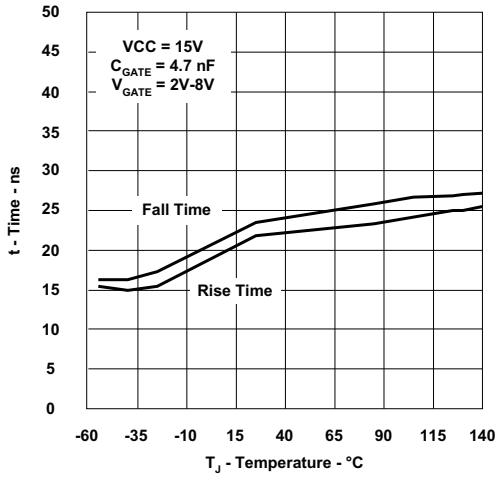

Figure 15. Gate Drive Switching vs Temperature

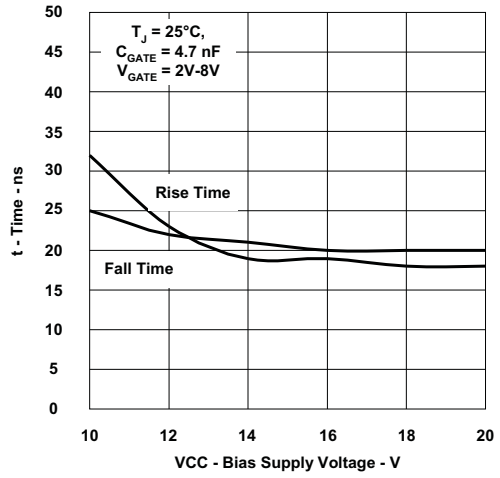

Figure 16. Gate Drive Switching vs Bias Supply Voltage

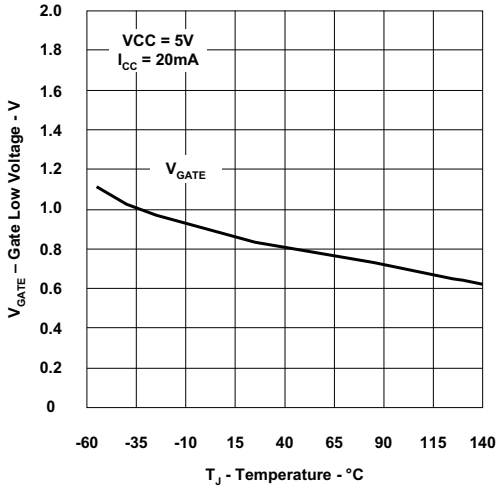

Figure 17. Gate Low Voltage With Device Off vs Temperature

7 Detailed Description

7.1 Overview

The UCC28019A is a switch-mode controller used in boost converters for power factor correction operating at a fixed frequency in continuous conduction mode. The UCC28019A requires few external components to operate as an active PFC pre-regulator. Its trimmed oscillator provides a nominal fixed switching frequency of 65 kHz, ensuring that both the fundamental and second harmonic components of the conducted-EMI noise spectrum are below the EN55022 conducted-band 150 kHz measurement limit.

Its tightly-trimmed internal 5-V reference voltage provides for accurate output voltage regulation over the typical world-wide 85-265VAC mains input range from zero to full output load.

Regulation is accomplished in two loops. The inner current loop shapes the average input current to match the sinusoidal input voltage under continuous inductor current conditions. Under light load conditions, depending on the boost inductor value, the inductor current may go discontinuous but still meet Class-D requirements of EN61000-3-2 despite the higher harmonics. The outer voltage loop regulates the PFC output voltage by generating a voltage on VCOMP (dependent upon the line and load conditions) which determines the internal gain parameters for maintaining a low-distortion steady-state input current wave-shape.

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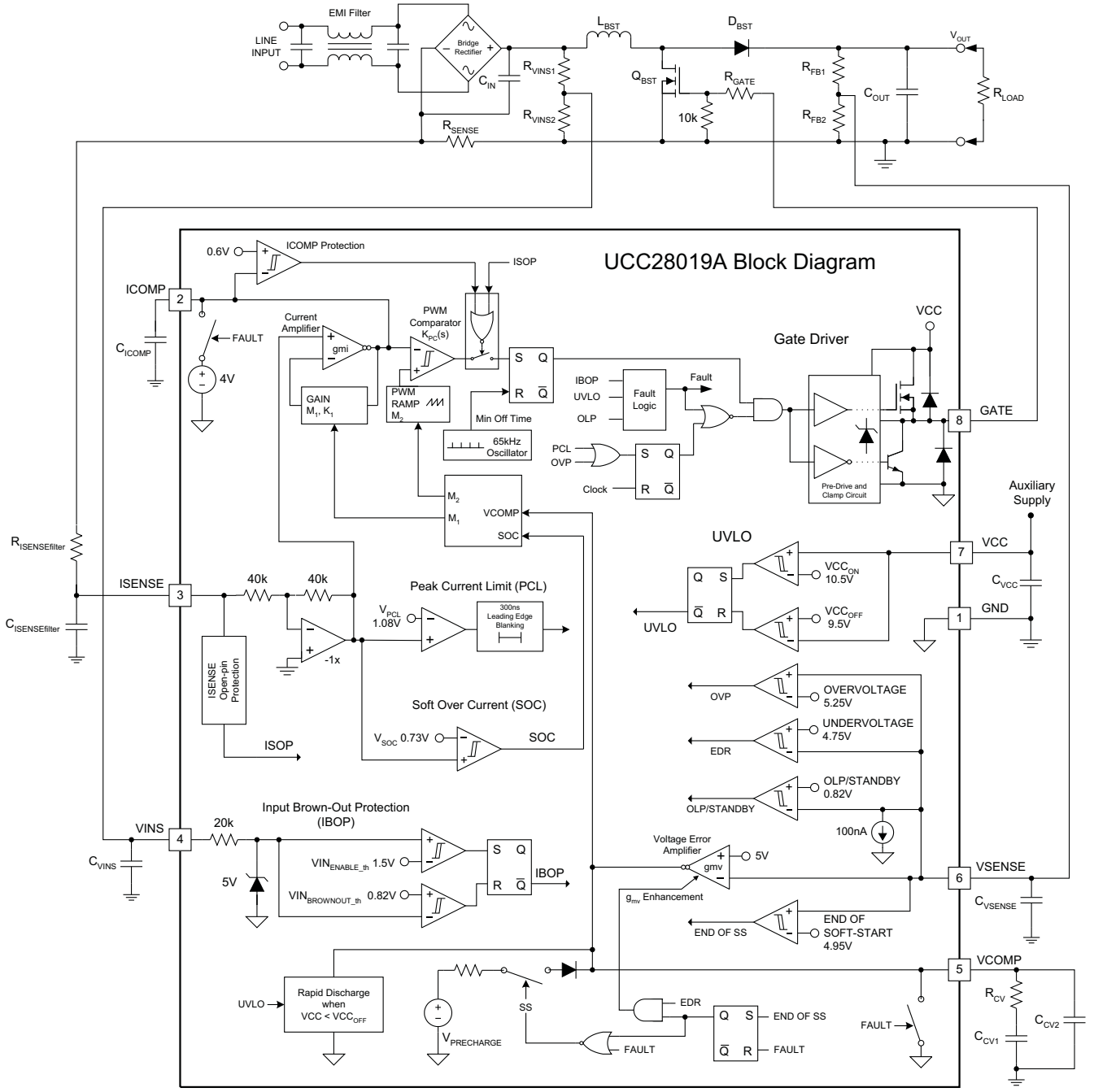
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft-Start

Soft Start controls the rate of rise of VCOMP in order to obtain a linear control of the increasing duty cycle as a function of time. VCOMP, the output of the voltage loop transconductance amplifier, is pulled low during UVLO, IBOP, and OLP (Open-Loop Protection)/STANDBY. Once the fault condition is released, an initial pre-charge source rapidly charges VCOMP to about 1.9 V. After that point, a constant 30 μA of current is sourced into the compensation components causing the voltage on this pin to ramp linearly until the output voltage reaches 85% of its final value. At this point, the sourcing current decreases until the output voltage reaches 99% of its final rated voltage. The Soft-Start time is controlled by the voltage error amplifier compensation capacitor values selected, and is user programmable based on desired loop crossover frequency. Once the output voltage exceeds 99% of rated voltage, the pre-charge source is discountinued and EDR is no longer inhibited.

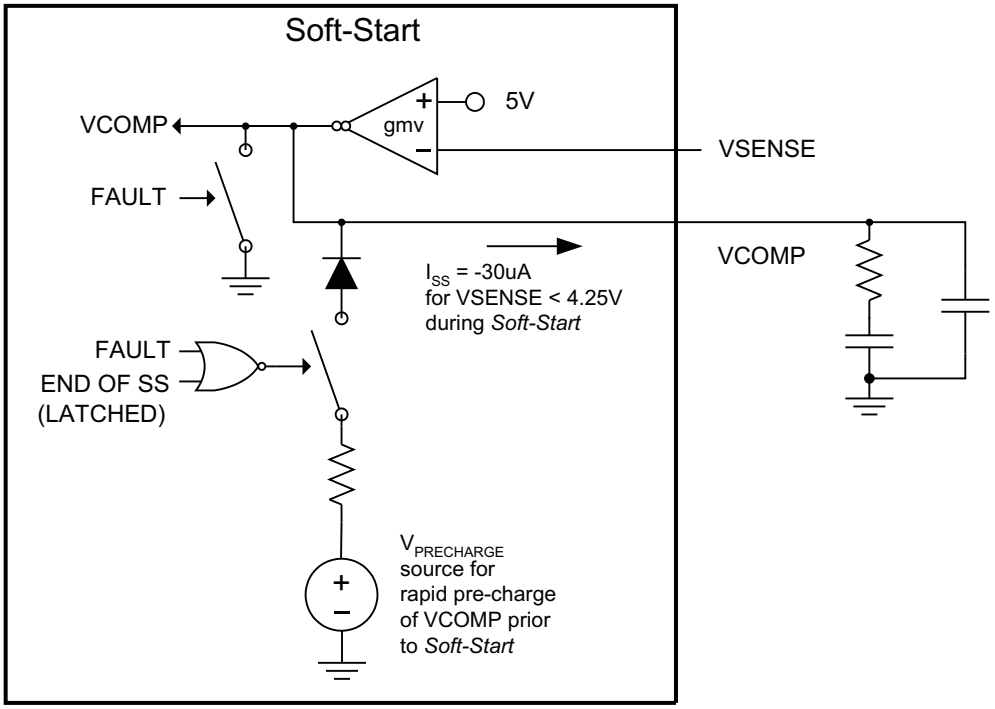


Figure 18. Soft Start

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Feature Description (continued)

7.3.2 System Protection

System-level protection features help keep the converter within safe operating limits.

7.3.2.1 VCC Undervoltage Lockout (UVLO)

During startup, Under-Voltage Lockout (UVLO) keeps the device in the off state until VCC rises above the 10.5-V enable threshold, VCC_{ON}. With a typical 1 V of hysteresis on UVLO to increase noise immunity, the device turns off when VCC drops to the 9.5-V disable threshold, VCC_{OFF}.

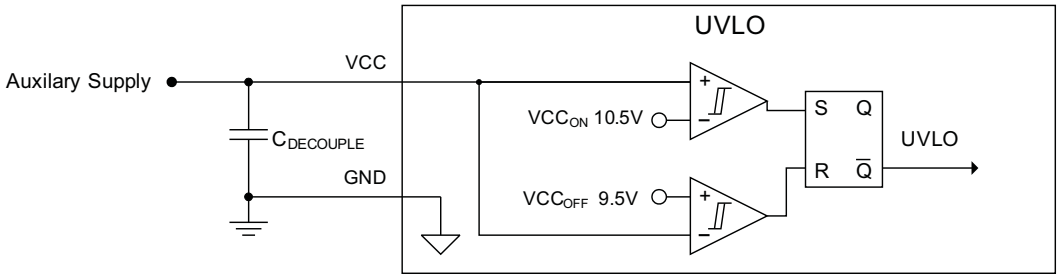

Figure 19. UVLO

If, during a brief ac-line dropout, the VCC voltage falls below the level necessary to bias the internal FAULT circuitry, the UVLO condition enables a special rapid discharge circuit which continues to discharge the VCOMP capacitors through a low impedance despite a complete lack of VCC. This helps to avoid an excessive current surge should the ac-line return while there is still substantial voltage stored on the VCOMP capacitors. Typically, these capacitors can be discharged to less than 1.2 V within 150 ms of loss of VCC.

7.3.2.2 Input Brown-Out Protection (IBOP)

The sensed line-voltage input, VINS, provides a means for the designer to set the desired mains RMS voltage level at which the PFC pre-regulator should start-up, $V_{ACturnon}$, as well as the desired mains RMS level at which it should shut down, $V_{ACturnoff}$. This prevents unwanted sustained system operation at or below a brown-out voltage, where excessive line current could overheat components. In addition, because VCC bias is not derived directly from the line voltage, IBOP protects the circuit from low line conditions that may not trigger the VCC UVLO turn-off.

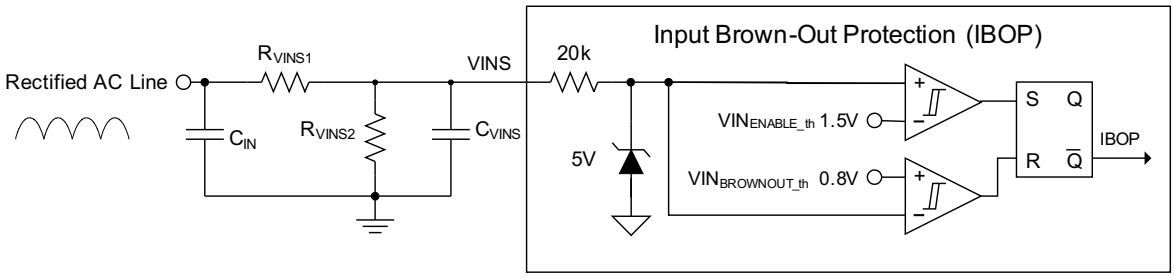

Figure 20. Input Brown-Out Protection

Feature Description (continued)

Input line voltage is sensed directly from the rectified ac mains voltage through a resistor-divider filter network providing a scaled and filtered value at the VINS input. IBOP will put the device into standby mode when VINS falls (high to low) below 0.8 V, $VINS_{BROWNOUT_th}$. The device comes out of standby when VINS rises (low to high) above 1.5 V, $VINS_{ENABLE_th}$. Bias current sourced from VINS, I_{VINS_0V}, is less than 0.1 μA. With a bias current this low, there is little concern for any set-point error caused by this current flowing through the sensing network. The highest praticable value resistance for this network should be chosen to minimize power dissipation, especially in applications requiring low standby power. Be aware that higher resistance values are more susceptible to noise pickup, but low-noise PCB layout techniques can help mitigate this. Also, depending on the resistor type used and its voltage rating, R_{VINS1} should be implemented with multiple resistors in series to reduce voltage stresses.

First, select R_{VINS1} based on choosing the highest reasonable resistance value available for typical applications.

Then select R_{VINS2} based on this value:

$$R_{VINS2} = R_{VINS1} \frac{VINS_{ENABLE_th}}{\sqrt{2}V_{ACturnon} - VINS_{ENABLE_th}} \tag{1}$$

Power dissipated in the resistor network is:

$$P_{VINS} = \frac{V_{IN(RMS)}^{2}}{R_{VINS1} + R_{VINS2}} \tag{2}$$

The filter capacitor, C_{VINS}, has two functions. First, to attenuate the voltage ripple to levels between the enable and brown-out threshold to prevent ripple on VINS from falsely triggering IBOP when the converter is operating at low line. Second, C_{VINS} delays the brown-out protection operation for a desired number of line-half-cycle periods while still having a good response to an actual brown-out event.

The capacitor is chosen so that it will discharge to the $VINS_{BROWNOUT_th}$ level after a delay of N number of line ½-cycles to accommodate ac-line dropout ride-through requirements.

$$C_{VINS} = \frac{-t_{dischrg}}{R_{VINS2}\, ln\left(\frac{VINS_{BROWNOUT_th}}{0.9V_{ACmin}\frac{R_{VINS2}}{R_{VINS1} + R_{VINS2}}}\right)} \tag{3}$$

Where,

$$t_{dischrg} = \frac{1}{2f_{LINE}} N \tag{4}$$

and V_{ACmin} is the lowest normal operating rms input voltage.

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Feature Description (continued)

7.3.2.3 Output Overvoltage Protection (OVP)

$V_{OUT(OVP)}$ is the output voltage exceeding 5% of the rated value, causing VSENSE to exceed a 5.25-V threshold (5-V reference voltage + 5%), V_{OVP}. The normal control loop is bypassed and the GATE output is disabled until VSENSE falls below 5.25 V. $V_{OUT(OVP)}$ is 420 V in a system with a 400-V rated output, for example.

7.3.2.4 Open Loop Protection/Standby (OLP/Standby)

If the output voltage feedback components were to fail and disconnect (open loop) the signal from the VSENSE input, then it is likely that the voltage error amp would increase the GATE output to maximum duty cycle. To prevent this, an internal pull-down forces VSENSE low. If the output voltage falls below 16% of its rated voltage, causing VSENSE to fall below 0.8 V, the device is put in standby, a state where the PWM switching is halted and the device is still on but draws standby current below 2.9 mA. This shutdown feature also gives the designer the option of pulling VSENSE low with an external switch.

7.3.2.5 ISENSE Open-Pin Protection (ISOP)

If the current feedback components were to fail and disconnect (open loop) the signal to the ISENSE input, then it is likely that the PWM stage would increase the GATE output to maximum duty cycle. To prevent this, an internal pull-up source drives ISENSE above 0.1 V so that a detector forces a state where the PWM switching is halted and the device is still on but draws standby current below 2.9 mA. This shutdown feature avoids continual operation in OVP and severely distorted input current.

7.3.2.6 Output Undervoltage Detection (UVD) and Enhanced Dynamic Response (EDR)

During normal operation, small perturbations on the PFC output voltage rarely exceed 5% deviation and the normal voltage control loop gain drives the output back into regulation. For large changes in line or load, if the output voltage drop exceeds -5%, an output under-voltage is detected (UVD) and Enhanced Dynamic Response (EDR) acts to speed up the slow response of the low-bandwidth voltage loop. During EDR, the transconductance of the voltage error amplifier is increased approximately 16 times to speed charging of the voltage-loop compensation capacitors to the level required for regulation. EDR is removed when VSENSE > 4.75 V. The EDR feature is not activated until soft start is completed.

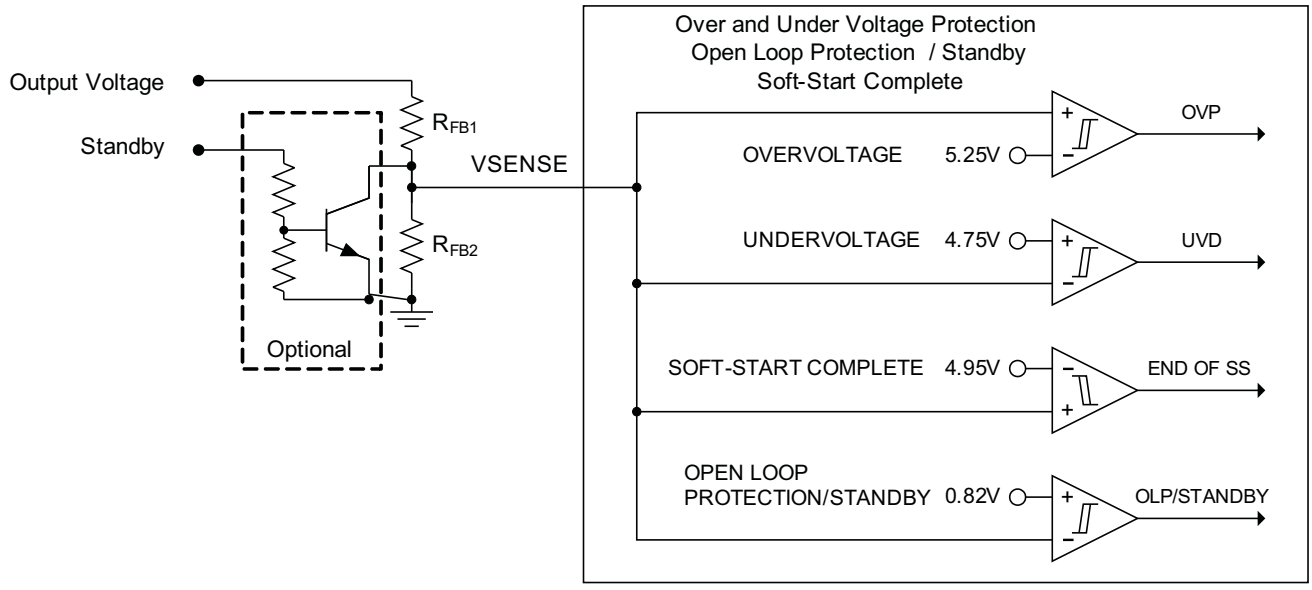

Figure 21. OVP, UVD, OLP/ Standby, Soft Start Complete

Feature Description (continued)

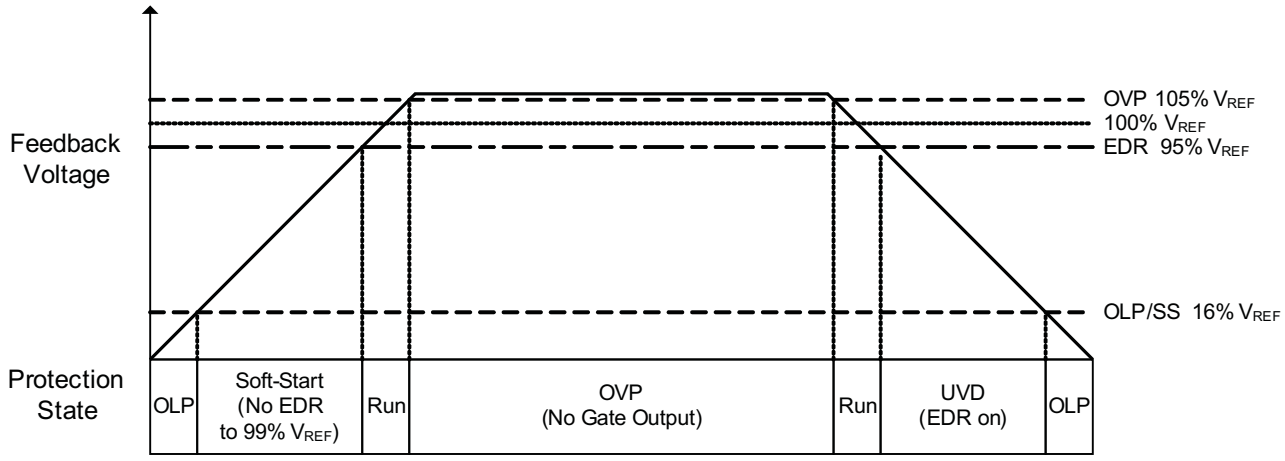

Figure 22. Soft Start and Protection States

7.3.2.7 Over-Current Protection

Inductor current is sensed by R_{ISENSE}, a low value resistor in the return path of input rectifier. The other side of the resistor is tied to the system ground. The voltage is sensed on the rectifier side of the sense resistor and is always negative. The voltage at ISENSE is buffered by a fixed gain of -1.0 to provide a positive internal signal to the current functions. There are two over-current protection features; Soft Over-Current (SOC) protects against an overload on the output and Peak Current Limit (PCL) protects against inductor saturation.

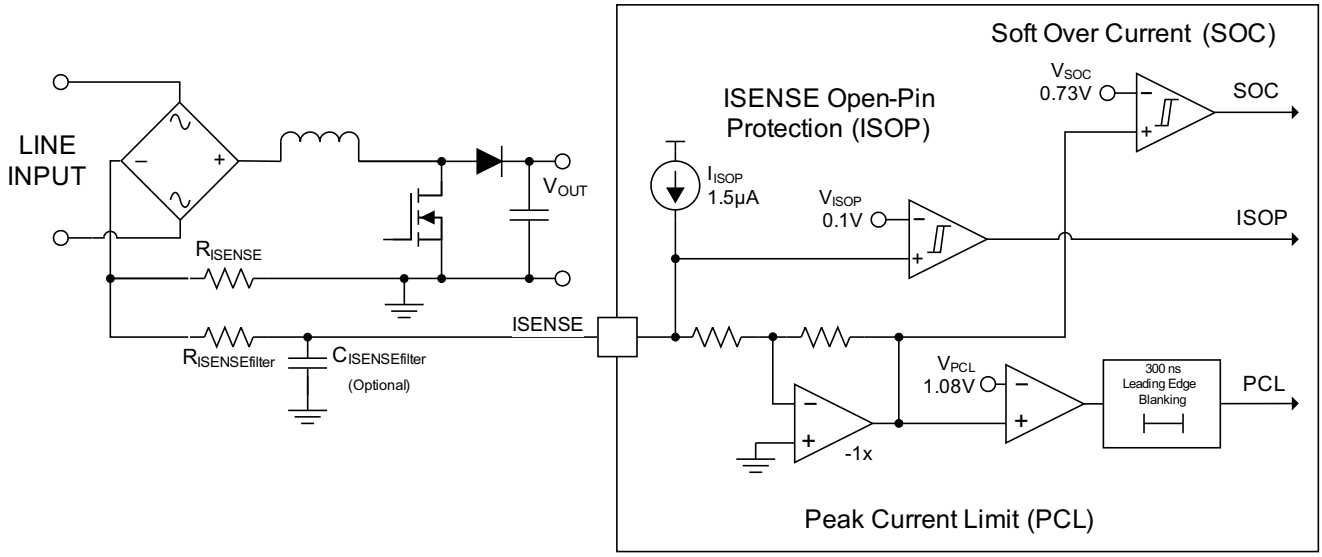

Figure 23. Soft Over Current/ Peak Current Limit

7.3.2.8 Soft Over Current (SOC)

Soft Over-Current (SOC) limits the input current. SOC is activated when the current sense voltage on ISENSE reaches -0.73 V, affecting the internal VCOMP level, and the control loop is adjusted to reduce the PWM duty cycle.

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Feature Description (continued)

7.3.2.9 Peak Current Limit (PCL)

Peak Current Limit (PCL) operates on a cycle-by-cycle basis. When the current sense voltage on ISENSE reaches -1.08 V, PCL is activated, immediately terminating the active switch cycle. PCL is leading-edge blanked to improve noise immunity against false triggering.

7.3.2.10 Current Sense Resistor, R_{ISENSE}

The current sense resistor, R_{ISENSE}, is sized using the minimum threshold value of Soft Over Current (SOC), $V_{SOC(min)}$ = 0.66 V. To avoid triggering this threshold during normal operation, resulting in a decreased duty-cycle, the resistor is sized for an overload current of 10% more than the peak inductor current,

$$R_{ISENSE} \leq \frac{V_{SOC(min)}}{1.1 I_{L_PEAK(max)}} \tag{5}$$

Since R_{ISENSE} sees the average input current, worst-case power dissipation occurs at input low-line when input current is at its maximum. Power dissipated by the sense resistor is given by:

$$P_{RISENSE} = (I_{IN_RMS(max)})^2 R_{ISENSE} \tag{6}$$

Peak Current Limit (PCL) protection turns off the output driver when the voltage across the sense resistor reaches the PCL threshold, V_{PCL}. The absolute maximum peak current, I_{PCL}, is given by:

$$I_{PCL} = \frac{V_{PCL}}{R_{ISENSE}} \tag{7}$$

7.3.3 Gate Driver

The GATE output is designed with a current-optimized structure to directly drive large values of total MOSFET gate capacitance at high turn-on and turn-off speeds. An internal clamp limits voltage on the MOSFET gate to 12.5 V (typical). When VCC voltage is below the UVLO level, the GATE output is held in the Off state. An external gate drive resistor, R_{GATE}, can be used to limit the rise and fall times and dampen ringing caused by parasitic inductances and capacitances of the gate drive circuit and to reduce EMI. The final value of the resistor depends upon the parasitic elements associated with the layout and other considerations. A 10-kΩ resistor close to the gate of the MOSFET, between the gate and ground, discharges stray gate capacitance and helps protect against inadvertent dv/dt-triggered turn-on.

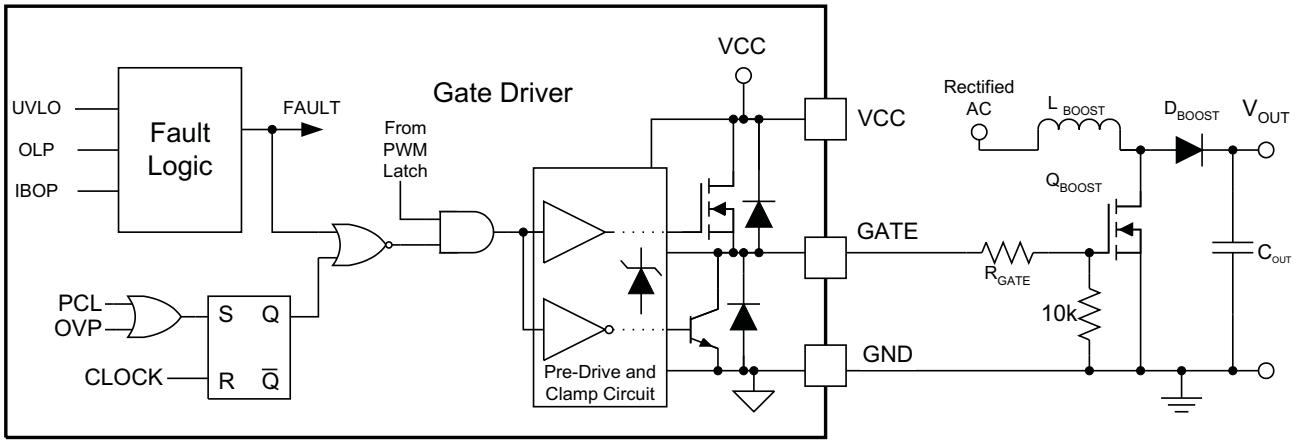

Figure 24. Gate Driver

Feature Description (continued)

7.3.4 Current Loop

The overall system current loop consists of the current averaging amplifier stage, the pulse width modulator (PWM) stage, the external boost inductor stage and the external current sensing resistor.

7.3.5 ISENSE and ICOMP Functions

The negative polarity signal from the current sense resistor is buffered and inverted at the ISENSE input. The internal positive signal is then averaged by the current amplifier (g_{mi}), whose output is the ICOMP pin. The voltage on ICOMP is proportional to the average inductor current. An external capacitor to GND is applied to the ICOMP pin for current loop compensation and current ripple filtering. The gain of the averaging amplifier is determined by the internal VCOMP voltage. This gain is non-linear to accommodate the world-wide ac-line voltage range.

ICOMP is connected to 4V internally whenever the device is in a Fault or Standby condition.

7.3.6 Pulse Width Modulator

The PWM stage compares the ICOMP signal with a periodic ramp to generate a leading-edge-modulated output signal which is High whenever the ramp voltage exceeds the ICOMP voltage. The slope of the ramp is defined by a non-linear function of the internal VCOMP voltage.

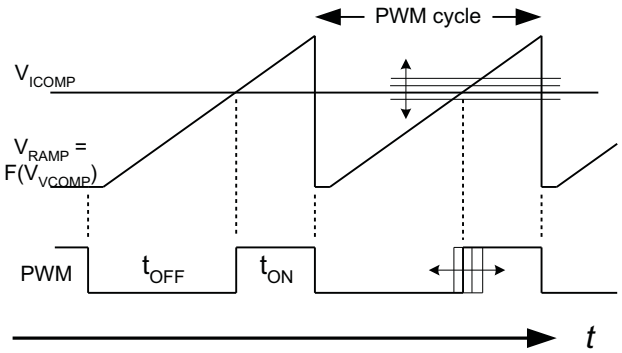

Figure 25. PWM Generation

The PWM output signal always starts Low at the beginning of the cycle, triggered by the internal clock. The output stays Low for a minimum off-time, t_{OFF_min}, after which the ramp rises linearly to intersect the ICOMP voltage. The ramp-ICOMP intersection determines t_{OFF}, and hence D_{OFF}. Since $D_{OFF} = V_{IN}/V_{OUT}$ by the boost-topology equation, and since VIN is sinusoidal in wave-shape, and since ICOMP is proportional to the inductor current, it follows that the control loop forces the inductor current to follow the input voltage wave-shape to maintain boost regulation. Therefore, the average input current is also sinusoidal in wave-shape.

7.3.7 Control Logic

The output of the PWM comparator stage is conveyed to the GATE drive stage, subject to control by various protection functions incorporated into the device. The GATE output duty-cycle may be as high as 99%, but will always have a minimum off-time t_{OFF_min}. Normal duty-cycle operation can be interrupted directly by OVP and PCL on a cycle-by-cycle basis. UVLO, IBOP and OLP/Standby also terminate the GATE output pulse, and further inhibit output until the SS operation can begin.

7.3.8 Voltage Loop

The outer control loop of the PFC controller is the voltage loop. This loop consists of the PFC output sensing stage, the voltage error amplifier stage, and the non-linear gain generation.

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Feature Description (continued)

7.3.9 Output Sensing

A resistor-divider network from the PFC output voltage to GND forms the sensing block for the voltage control loop. The resistor ratio is determined by the desired output voltage and the internal 5-V regulation reference voltage.

Like the VINS input, the very low bias current at the VSENSE input allows the choice of the highest practicable resistor values for lowest power dissipation and standby current. A small capacitor from VSENSE to GND serves to filter the signal in a high-noise environment. This filter time constant should generally be less than 100 μs.

7.3.10 Voltage Error Amplifier

The transconductance error amplifier (g_{mv}) generates an output current proportional to the difference between the voltage feedback signal at VSENSE and the internal 5-V reference. This output current charges or discharges the compensation network capacitors on the VCOMP pin to establish the proper VCOMP voltage for the system operating conditions. Proper selection of the compensation network components leads to a stable PFC pre-regulator over the entire ac-line range and 0-100% load range. The total capacitance also determines the rate-of-rise of the VCOMP voltage at soft start, as discussed earlier.

The amplifier output VCOMP is pulled to GND during any Fault or Standby condition to discharge the compensation capacitors to an initial zero state. Usually, the large capacitor has a series resistor which delays complete discharge for their respective time constant (which may be several hundred milliseconds). If VCC bias voltage is quickly removed after UVLO, the normal discharge transistor on VCOMP loses drive and the large capacitor could be left with substantial voltage on it, negating the benefit of a subsequent soft start. The UCC28019A incorporates a parallel discharge path which operates without VCC bias, to further discharge the compensation network after VCC is removed.

When output voltage perturbations greater than ±5% appear at the VSENSE input, the amplifier moves out of linear operation. On an over-voltage, the OVP function acts directly to shut off the GATE output until VSENSE returns within ±5% of regulation. On an under-voltage, the UVD function invokes EDR which immediately increases the voltage error amplifier transconductance to about 440 μS. This higher gain facilitates faster charging of the compensation capacitors to the new operating level.

7.3.11 Non-Linear Gain Generation

The voltage at VCOMP is used to set the current amplifier gain and the PWM ramp slope. This voltage is buffered internally and is then subject to modification by the SOC function, as discussed earlier.

Together the current gain and the PWM slope adjust to the different system operating conditions (set by the ac-line voltage and output load level) as VCOMP changes, to provide a low-distortion, high-power-factor input current wave-shape following that of the input voltage.

7.4 Device Functional Modes

This device has no functional modes.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC28019A is a switch-mode controller used in boost converters for power factor correction operating at a fixed frequency in continuous conduction mode. The UCC28019A requires few external components to operate as an active PFC pre-regulator. The operating switching frequency is fixed at 65 kHz.

The internal 5-V reference voltage provides for accurate output voltage regulation over the typical world-wide 85-V_{AC} to 265-V_{AC} mains input range from zero to full output load. The usable system load ranges from 100 W to few kW.

Regulation is accomplished in two loops. The inner current loop shapes the average input current to match the sinusoidal input voltage under continuous inductor current conditions. Under light-load conditions, depending on the boost inductor value, the inductor current may go discontinuous but still meet Class-A/D requirements of IEC 61000-3-2 despite the higher harmonics. The outer voltage loop regulates the PFC output voltage by generating a voltage on VCOMP (dependent upon the line and load conditions) which determines the internal gain parameters for maintaining a low-distortion, steady-state, input-current wave shape.

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8.2 Typical Application

Figure 26 illustrates the design process and component selection for a continuous conduction mode power factor correction boost converter utilizing the UCC28019A. The target design is a universal input, 350-W PFC designed for an ATX supply application. This design process is directly tied to the UCC28019A Design Calculator (SLUC117) spreadsheet that can be found in the Tools section of the UCC28019A product folder on the Texas Instruments website.

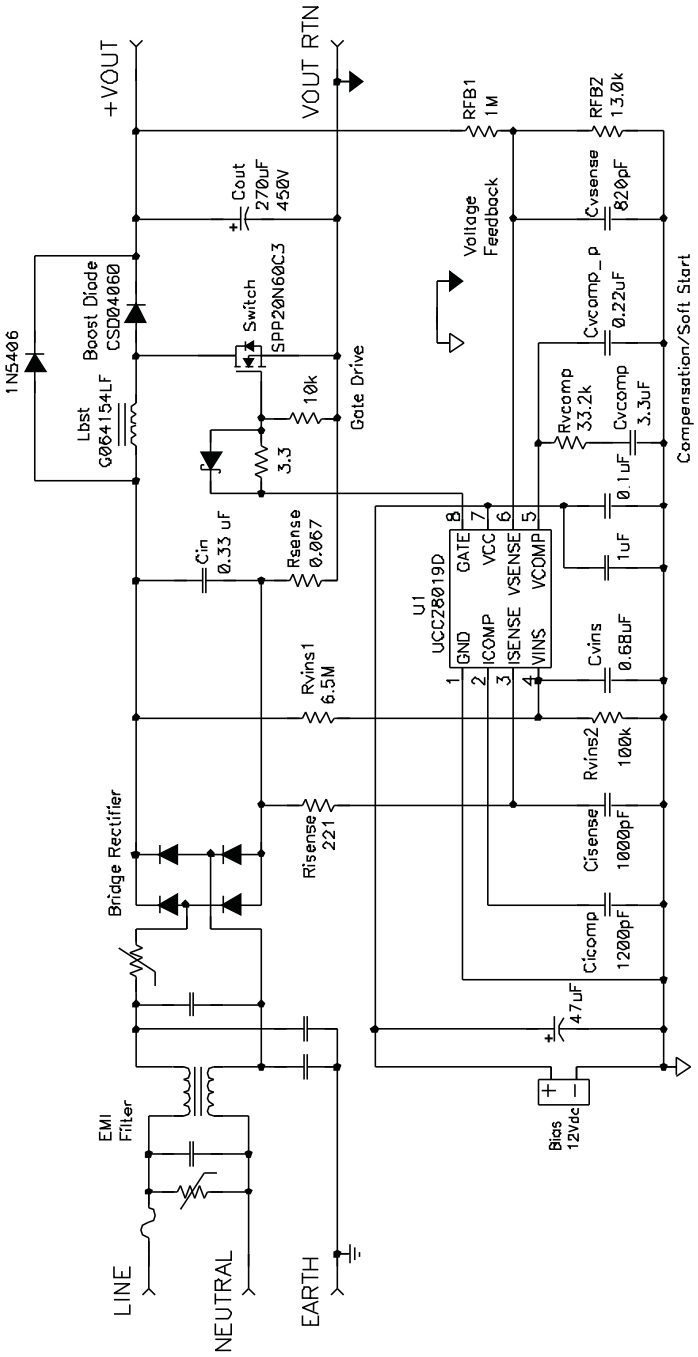

Figure 26. Design Example Schematic

Typical Application (continued)

8.2.1 Design Requirements

Design goal parameters for a continuous conduction mode power factor correction boost converter utilizing the UCC28019A.

Table 1. Design Goal Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Input characteristics						
V_{IN}	Input voltage		85	115	265	VAC
f_{LINE}	Input frequency		47		63	Hz
	Brown out voltage	$V_{AC(on)}$, I_{OUT} = 0.9 A		75		V_{AC}
		$V_{AC(off)}$, I_{OUT} = 0.9 A		65		V_{AC}
Output characteristics						
V_{OUT}	Output voltage	85 VAC ≤ V_{IN} ≤ 265 VAC, 47 Hz ≤ f_{LINE} ≤ 63 Hz 0 A ≤ I_{OUT} ≤ 0.9 A	380	390	402	V_{DC}
$V_{RIPPLE(SW)}$	High frequency output voltage ripple	V_{IN} = 115 VAC, f_{LINE} = 60 Hz, I_{OUT} = 0.9 A			3.9	V_{PP}
		V_{IN} = 230 VAC , f_{LINE} = 50 Hz, I_{OUT} = 0.9 A			3.9	V_{PP}
$V_{RIPPLE(f_LINE)}$	Line frequency output voltage ripple	V_{IN} = 115 VAC, f_{LINE} = 60 Hz, I_{OUT} = 0.9 A			19.5	V_{PP}
		V_{IN} = 230 VAC, f_{LINE} = 50 Hz, I_{OUT} = 0.9 A			19.5	V_{PP}
I_{OUT}	Output load current	85 VAC ≤ V_{IN} ≤ 265 VAC, 47 Hz ≤ f_{LINE} ≤ 63 Hz			0.9	A
P_{OUT}	Output power				350	W
$V_{OUT(OVP)}$	Output over voltage protection			410		V
$V_{OUT(UVP)}$	Output under voltage protection			370		V
Control loop characteristics						
f_{SW}	Switching frequency	T_J = 25°C	61.7	65	68.3	kHz
$f_{(CO)}$	Control loop bandwidth	V_{IN} = 162 VDC, I_{OUT} = 0.45 A		14		Hz
	Phase margin	V_{IN} = 162 VDC, I_{OUT} = 0.45 A		70		degrees
PF	Power factor	V_{IN} = 115 VAC, I_{OUT} = 0.9 A	0.98			
THD	Total harmonic distortion	V_{IN} = 115 VAC, f_{LINE} = 60 Hz, I_{OUT} = 0.9 A		4.3%	10%	
		V_{IN} = 230 VAC, f_{LINE} = 50 Hz, I_{OUT} = 0.9 A		6.6%	10%	
η	Full load efficiency	V_{IN} = 115 VAC, f_{LINE} = 60 Hz, I_{OUT} = 0.9 A	0.95			
T_{AMB}	Ambient temperature				50	°C

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8.2.2 Detailed Design Procedure

8.2.2.1 Current Calculations

First, determine the maximum average output current, $I_{OUT(max)}$:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}} \tag{8}$$

$$I_{OUT(max)} = \frac{350W}{390V} \cong 0.9A \tag{9}$$

The maximum input RMS line current, $I_{IN_RMS(max)}$, is calculated using the parameters from Table 1 and the efficiency and power factor initial assumptions:

$$I_{IN_RMS(max)} = \frac{P_{OUT(max)}}{\eta V_{IN(min)} PF} \tag{10}$$

$$I_{IN_RMS(max)} = \frac{350W}{0.92 \times 85V \times 0.99} = 4.52A \tag{11}$$

Based upon the calculated RMS value, the maximum peak input current, $I_{IN_PEAK(max)}$, and the maximum average input current, $I_{IN_AVG(max)}$, assuming the waveform is sinusoidal, can be determined.

$$I_{IN_PEAK(max)} = \sqrt{2} I_{IN_RMS(max)} \tag{12}$$

$$I_{IN_PEAK(max)} = \sqrt{2} \times 4.52A = 6.39A \tag{13}$$

$$I_{IN_AVG(max)} = \frac{2I_{IN_PEAK(max)}}{\pi} \tag{14}$$

$$I_{IN_AVG(max)} = \frac{2 \times 6.39A}{\pi} = 4.07A \tag{15}$$

8.2.2.2 Bridge Rectifier

Assuming a forward voltage drop, V_{F_BRIDGE}, of 0.95 V across the rectifier diodes, BR1, the power loss in the input bridge, P_{BRIDGE}, can be calculated:

$$P_{BRIDGE} = 2V_{F_BRIDGE} I_{IN_AVG(max)} \tag{16}$$

$$P_{BRIDGE} = 2 \times 0.95V \times 4.07A = 7.73W \tag{17}$$

8.2.2.3 Input Capacitor

Note that the UCC28019A is a continuous conduction mode controller and as such the inductor ripple current should be sized accordingly. High inductor ripple current has an impact on the CCM/DCM boundary and results in higher light-load THD, and also affects the choices for R_{SENSE} and C_{ICOMP} values. Allowing an inductor ripple current, I_{RIPPLE}, of 20% and a high frequency ripple voltage factor, ΔV_{RIPPLE_IN}, of 6%, the minimum input capacitor value, C_{IN}, is calculated by first determining the input ripple current, I_{RIPPLE}, and the input ripple voltage, $V_{IN_RIPPLE(max)}$:

$$I_{RIPPLE} = \Delta I_{RIPPLE} I_{IN_PEAK(max)} \tag{18}$$

$$\Delta I_{RIPPLE} = 0.2 \tag{19}$$

$$I_{RIPPLE} = 0.2 \times 6.39A = 1.28A \tag{20}$$

$$V_{IN_RIPPLE(max)} = \Delta V_{RIPPLE_IN} V_{IN_RECTIFIED(min)} \tag{21}$$

$$\Delta V_{RIPPLE_IN} = 0.06 \tag{22}$$

$$V_{IN_RECTIFIED} = \sqrt{2} V_{IN} \tag{23}$$

$$V_{IN_RECTIFIED(min)} = \sqrt{2} \times 85V = 120.2V \tag{24}$$

$$V_{IN_RIPPLE(max)} = 0.06 \times 120.2V = 7.21V \tag{25}$$

The value for the input x-capacitor can now be calculated:

$$C_{IN} = \frac{I_{RIPPLE}}{8 f_{SW} V_{IN_RIPPLE(max)}} \tag{26}$$

$$C_{IN} = \frac{1.28A}{8 \times 65kHz \times 7.21V} = 0.341\mu F \tag{27}$$

A 0.33 µF, 275 VAC ex-2 film capacitor was selected for C_{IN}.

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8.2.2.4 Boost Inductor

The boost inductor, L_{BST}, is selected after determining the maximum inductor peak current, $I_{L_PEAK(max)}$:

$$I_{L_PEAK(max)} = I_{IN_PEAK(max)} + \frac{I_{RIPPLE}}{2} \tag{28}$$

$$I_{L_PEAK(max)} = 6.39A + \frac{1.28A}{2} = 7.03A \tag{29}$$

The minimum value of the boost inductor is calculated based upon a worst case duty cycle of 0.5:

$$L_{BST(min)} \geq \frac{V_{OUT} D(1-D)}{f_{SW(typ)} I_{RIPPLE}} \tag{30}$$

$$L_{BST(min)} \geq \frac{390V \times 0.5(1-0.5)}{65kHz \times 1.28A} \geq 1.17mH \tag{31}$$

The actual value of the boost inductor that will be used is 1.25 mH.

The maximum duty cycle, $DUTY_{(max)}$, can be calculated and will occur at the minimum input voltage:

$$DUTY_{(max)} = \frac{V_{OUT} - V_{IN_RECTIFIED(min)}}{V_{OUT}} \tag{32}$$

$$V_{IN_RECTIFIED(min)} = \sqrt{2} \times 85V = 120V \tag{33}$$

$$DUTY_{(max)} = \frac{390V - 120V}{390V} = 0.692 \tag{34}$$

8.2.2.5 Boost Diode

The diode losses are estimated based upon the forward voltage drop, V_F, at 125°C and the reverse recovery charge, Q_{RR}, of the diode. This design uses a silicon-carbide diode. Although somewhat more expensive, it essentially eliminates the reverse recovery losses because Q_{RR} is equal to 0nC.

$$P_{DIODE} = V_{F_125C} I_{OUT(max)} + 0.5 f_{SW(typ)} V_{OUT} Q_{RR} \tag{35}$$

$$V_{F_125C} = 1.5V \tag{36}$$

$$Q_{RR} = 0nC \tag{37}$$

$$P_{DIODE} = 1.5V \times 0.897A + 0.5 \times 65kHz \times 390V \times 0nC = 1.35W \tag{38}$$

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8.2.2.6 Switching Element

The conduction losses of the switch are estimated using the $R_{DS(on)}$ of the FET at 125°C , found in the FET data sheet, and the calculated drain to source RMS current, I_{DS_RMS}:

$$P_{COND} = I_{DS_RMS}^2 R_{DSon(125C)} \tag{39}$$

$$R_{DSon(125C)} = 0.35\Omega \tag{40}$$

$$I_{DS_RMS} = \frac{P_{OUT(max)}}{V_{IN_RECTIFIED(min)}} \sqrt{2 - \frac{16 V_{IN_RECTIFIED(min)}}{3\pi V_{OUT}}} \tag{41}$$

$$I_{DS_RMS} = \frac{350W}{120V} \sqrt{2 - \frac{16 \times 120V}{3\pi \times 390V}} = 3.54A \tag{42}$$

$$P_{COND} = 3.54A^2 \times 0.35\Omega = 4.38W \tag{43}$$

The switching losses are estimated using the rise time, (t_r), and fall time, (t_f), of the gate, and the output capacitance losses.

For the selected device:

$$t_r = 5.0\ ns, t_f = 4.5\ ns \tag{44}$$

$$C_{OSS} = 780\,pF \tag{45}$$

$$P_{SW} = f_{SW(typ)}(0.5 V_{OUT} I_{IN-PEAK(max)} \left(t_r + t_f\right) + 0.5 C_{OSS} V_{OUT}^2) \tag{46}$$

$$P_{SW} = 65kHz(0.5 \times 390V \times 6.39A\left(5n + 4.5ns\right) + 0.5 \times 780\,pF \times 390V^2) = 4.626W \tag{47}$$

Total FET losses:

$$P_{COND} + P_{SW} = 4.38W + 4.626W = 9.007W \tag{48}$$

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8.2.2.7 Sense Resistor

To accommodate the gain of the internal non-linear power limit, R_{SENSE} is sized such that it will trigger the soft over-current at 25% higher than the maximum peak inductor current using the minimum SOC threshold, V_{SOC}, of ISENSE.

$$R_{SENSE} = \frac{V_{SOC}}{I_{L_PEAK(max)} \times 1.25} \tag{49}$$

$$R_{SENSE} = \frac{0.66V}{7.03A \times 1.25} = 0.075\Omega \tag{50}$$

Using a parallel combination of available standard value resistors, the sense resistor is chosen.

$$R_{SENSE} = 0.067\Omega \tag{51}$$

The power dissipated across the sense resistor, P_{Rsense}, must be calculated:

$$P_{Rsense} = I^2_{IN_RMS(\max)} R_{SENSE} \tag{52}$$

$$P_{Rsense} = (4.52A)^2 \times 0.067\Omega = 1.37W \tag{53}$$

The peak current limit, PCL, protection feature will be triggered when current through the sense resistor results in the voltage across R_{SENSE} to be equal to the V_{PCL} threshold. For a worst case analysis, the maximum V_{PCL} threshold is used:

$$I_{PCL} = \frac{V_{PCL}}{R_{SENSE}} \tag{54}$$

$$I_{PCL} = \frac{1.15V}{0.067\Omega} = 17.16A \tag{55}$$

To protect the device from inrush current, a standard 220-Ω resistor, R_{ISENSE}, is placed in series with the ISENSE pin. A 1000-pF capacitor, C_{ISENSE}, is placed close to the device to improve noise immunity on the ISENSE pin.

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8.2.2.8 Output Capacitor

The output capacitor, C_{OUT}, is sized to meet holdup requirements of the converter. Assuming the downstream converters require the output of the PFC stage to never fall below 300 V, $V_{OUT_HOLDUP(min)}$, during one line cycle, $t_{HOLDUP} = 1/f_{LINE(min)}$, the minimum calculated value for the capacitor is:

$$C_{OUT(min)} \geq \frac{2P_{OUT}t_{HOLDUP}}{V_{OUT}^2 - V_{OUT_HOLDUP(min)}^2} \tag{56}$$

$$C_{OUT(min)} \geq \frac{2 \times 350W \times 21.28ms}{390V^2 - 300V^2} \geq 240\mu F \tag{57}$$

It is advisable to de-rate this capacitor value by 20%; the actual capacitor used is 270 µF.

Setting the maximum peak-to-peak output ripple voltage to be less than 5% of the output voltage will ensure that the ripple voltage will not trigger the output over-voltage or output under-voltage protection features of the controller. The maximum peak-to-peak ripple voltage, occurring at twice the line frequency, and the ripple current of the output capacitor are calculated:

$$V_{OUT_RIPPLE(pp)} < 0.05V_{OUT} \tag{58}$$

$$V_{OUT_RIPPLE(pp)} < 0.05 \times 390V < 19.5V_{PP} \tag{59}$$

$$V_{OUT_RIPPLE(pp)} = \frac{I_{OUT}}{\pi(2f_{LINE(min)})C_{OUT}} \tag{60}$$

$$V_{OUT_RIPPLE(pp)} = \frac{0.9A}{\pi(2 \times 47Hz) \times 270\mu F} = 11.26V \tag{61}$$

The required ripple current rating at twice the line frequency is equal to:

$$I_{Cout_2fline} = \frac{I_{OUT(max)}}{\sqrt{2}} \tag{62}$$

$$I_{Cout_2fline} = \frac{0.9A}{\sqrt{2}} = 0.635A \tag{63}$$

There will also be a high frequency ripple current through the output capacitor:

$$I_{Cout_HF} = I_{OUT(max)}\sqrt{\frac{16V_{OUT}}{3\pi V_{IN_RECTIFIED(min)}} - 1.5} \tag{64}$$

$$I_{Cout_HF} = 0.9A\sqrt{\frac{16 \times 390V}{3\pi \times 120V} - 1.5} = 1.8A \tag{65}$$

The total ripple current in the output capacitor is the combination of both and the output capacitor must be selected accordingly:

$$I_{Cout_RMS(total)} = \sqrt{I_{Cout_2fline}^2 + I_{Cout_HF}^2} \tag{66}$$

$$I_{Cout_RMS(total)} = \sqrt{0.635A^2 + 1.8A^2} = 1.9A \tag{67}$$

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8.2.2.9 Output Voltage Set Point

For low power dissipation and minimal contribution to the voltage set point error, it is recommended to use 1 MΩ for the top voltage feedback divider resistor, R_{FB1}. Multiple resistors in series are used due to the maximum allowable voltage across each. Using the internal 5-V reference, V_{REF}, select the bottom divider resistor, R_{FB2}, to meet the output voltage design goals.

$$R_{FB2} = \frac{V_{REF} R_{FB1}}{V_{OUT} - V_{REF}} \tag{68}$$

$$R_{FB2} = \frac{5V \times 1M\Omega}{390V - 5V} = 13.04k\Omega \tag{69}$$

Using 13 kΩ for R_{FB2} results in a nominal output voltage set point of 391 V.

The over-voltage protection, OVD, will be triggered when the output voltage exceeds 5% of its nominal set-point:

$$V_{OUT(OVP)} = VSENSE_{OVP}\left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}}\right) \tag{70}$$

$$V_{OUT(OVP)} = 5.25V \times \left(\frac{1M\Omega + 13k\Omega}{13k\Omega}\right) = 410.7V \tag{71}$$

The under-voltage detection, UVD, will be triggered when the output voltage falls below 5% of its nominal set-point:

$$V_{OUT(UVD)} = VSENSE_{UVD}\left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}}\right) \tag{72}$$

$$V_{OUT(UVD)} = 4.75V \times \left(\frac{1M\Omega + 13k\Omega}{13k\Omega}\right) = 371.6V \tag{73}$$

A small capacitor on VSENSE must be added to filter out noise. Limit the value of the filter capacitor such that the RC time constant is less than 0.1 ms so as not to significantly reduce the control response time to output voltage deviations. With careful layout, the noise on this design is minimal, so an RC time constant of 0.01 ms was all that was needed:

$$C_{VSENSE} = \frac{0.01ms}{R_{FB2}} \tag{74}$$

$$C_{VSENSE} = \frac{0.01ms}{13k\Omega} = 769pF \tag{75}$$

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8.2.2.10 Loop Compensation

The selection of compensation components, for both the current loop and the voltage loop, is made easier by using the UCC28019A Design Calculator spreadsheet that can be found in the Tools section of the UCC28019A product folder on the Texas Instruments website. The current loop is compensated first by determining the product of the internal loop variables, M_1M_2, using the internal controller constants K_1 and K_{FQ}:

$$M_1M_2 = \frac{I_{OUT(max)} V_{OUT}^2 R_{SENSE} K_1}{\eta^2 V_{IN_RMS}^2 K_{FQ}} \tag{76}$$

$$K_{FQ} = \frac{1}{f_{SW(typ)}} \tag{77}$$

$$K_{FQ} = \frac{1}{65kHz} = 15.385\mu s \tag{78}$$

$$K_1 = 7 \tag{79}$$

$$M_1M_2 = \frac{0.9A \times 391V^2 \times 0.067\Omega \times 7}{0.92^2 \times 115V^2 \times 15.385\mu s} = 0.374\frac{V}{\mu s} \tag{80}$$

The VCOMP operating point is found on Figure 27. The Design Calculator spreadsheet enables the user to iteratively select the appropriate VCOMP value.

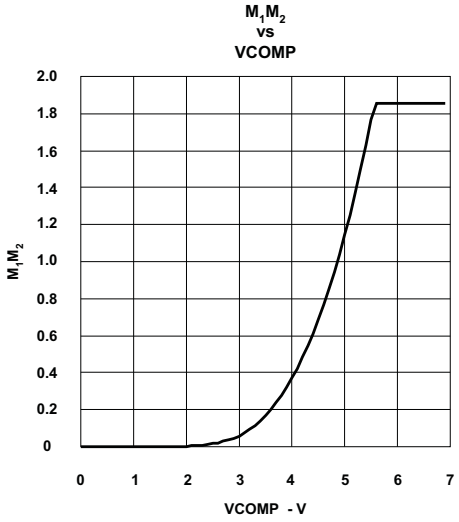

Figure 27. M_1M_2 vs. VCOMP

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For the given M_1M_2 of 0.374 V/µs, the VCOMP is approximately equal to 4, as shown in Figure 27.

The individual loop factors, M_1 which is the current loop gain factor, and M_2 which is the voltage loop PWM ramp slope, are calculated using the following conditions:

The M_1 current loop gain factor:

- if : 0 < VCOMP < 2

$$then: M_1 = 0.064 \tag{81}$$

- if : 2 ≤ VCOMP < 3

$$then: M_1 = 0.139 \times VCOMP - 0.214 \tag{82}$$

- if : 3 ≤ VCOMP < 5.5

$$then: M_1 = 0.279 \times VCOMP - 0.632 \tag{83}$$

- if : 5.5 ≤ VCOMP < 7

$$then: M_1 = 0.903 \tag{84}$$

In this example:

$$VCOMP = 4$$
$$M_1 = 0.279 \times 4 - 0.632 = 0.484 \tag{85}$$

The M_2 PWM ramp slope:

- if : 0 < VCOMP < 1.5

$$then: M_2 = 0 \frac{V}{\mu s} \tag{86}$$

- if : 1.5 ≤ VCOMP < 5.6

$$then: M_2 = 0.1223 \times (VCOMP - 1.5)^2 \frac{V}{\mu s} \tag{87}$$

- if : 5.6 ≤ VCOMP < 7

$$then: M_2 = 2.056 \frac{V}{\mu s} \tag{88}$$

In this example:

$$VCOMP = 4$$
$$M_2 = 0.1223 \times (4 - 1.5)^2 \frac{V}{\mu s} = 0.764 \frac{V}{\mu s} \tag{89}$$

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Verify that the product of the individual gain factors is approximately equal to the M_1M_2 factor determined above, if not, reselect VCOMP and recalculate M_1M_2.

$$M_1 \times M_2 = 0.484 \times 0.764 \frac{V}{\mu s} = 0.37 \frac{V}{\mu s} \tag{90}$$

$$0.37 \frac{V}{\mu s} \cong M_1 M_2 = 0.372 \frac{V}{\mu s} \tag{91}$$

The non-linear gain variable, M_3, can now be calculated:

- if : 0 < VCOMP < 3

$$then: M_3 = 0.0510 \times VCOMP^2 - 0.1543 \times VCOMP - 0.1167 \tag{92}$$

- if : 3 ≤ VCOMP < 7

$$then: M_3 = 0.1026 \times VCOMP^2 - 0.3596 \times VCOMP + 0.3085 \tag{93}$$

In this example:

$$VCOMP = 4$$

$$M_3 = 0.1026 \times 4^2 - 0.3596 \times 4 + 0.3085 = 0.512 \tag{94}$$

The frequency of the current averaging pole, f_{IAVG}, is chosen to be at 9.5 kHz. The required capacitor on ICOMP, C_{ICOMP}, for this is determined using the transconductance gain, g_{mi}, of the internal current amplifier:

$$C_{ICOMP} = \frac{g_{mi} M_1}{K_1 2\pi f_{IAVG}} \tag{95}$$

$$C_{ICOMP} = \frac{0.95mS \times 0.484}{7 \times 2 \times \pi \times 9.5kHz} = 1100pF \tag{96}$$

Using a 1200 pF capacitor for C_{ICOMP} results in a current averaging pole frequency of 8.7 kHz:

$$f_{IAVG} = \frac{g_{mi} M_1}{K_1 2\pi C_{ICOMP}} \tag{97}$$

$$f_{IAVG} = \frac{0.95mS \times 0.484}{7 \times 2 \times \pi \times 1200pF} = 8.7kHz \tag{98}$$

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The transfer function of the current loop can be plotted:

$$G_{CL}(f) = \frac{K_1 R_{SENSE} V_{OUT}}{K_{FQ} M_1 M_2 L_{BST}} \times \frac{1}{s(f) + \frac{s(f)^2 K_1 C_{ICOMP}}{g_{mi} M_1}} \quad (99)$$

$$G_{CLdB}(f) = 20 log\left(\left|G_{CL}(f)\right|\right) \quad (100)$$

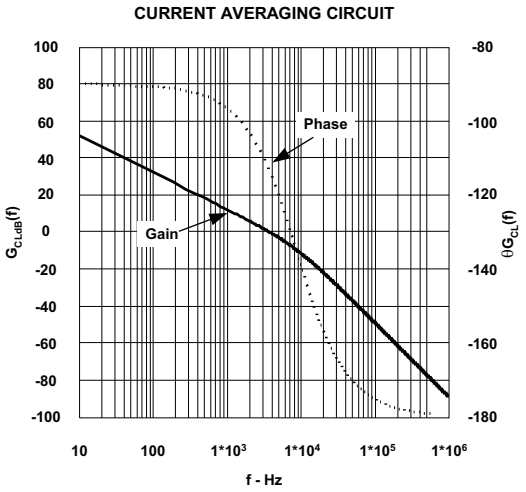

Figure 28. Bode Plot of the Current Averaging Circuit.

The open loop of the voltage transfer function, $G_{VL}(f)$ contains the product of the voltage feedback gain, G_{FB}, and the gain from the pulse width modulator to the power stage, G_{PWM_PS}, which includes the pulse width modulator to power stage pole, f_{PWM_PS}. The plotted result is shown in Figure 29.

$$G_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \tag{101}$$

$$G_{FB} = \frac{13k\Omega}{1M\Omega + 13k\Omega} = 0.013 \tag{102}$$

$$f_{PWM_PS} = \frac{1}{2\pi \frac{K_1 R_{SENSE} V_{OUT}^3 C_{OUT}}{K_{FQ} M_1 M_2 V_{IN(typ)}^2}} \tag{103}$$

$$f_{PWM_PS} = \frac{1}{2\pi \frac{7 \times 0.067\Omega \times 391V^3 \times 270\mu F}{15.385\mu s \times 0.484 \times 0.764 \frac{V}{\mu s} \times 115V^2}} = 1.581Hz \tag{104}$$

$$G_{PWM_PS}(f) = \frac{\frac{M_3 V_{OUT}}{M_1 M_2 \times 1\mu s}}{1 + \frac{s(f)}{2\pi f_{PWM_PS}}} \tag{105}$$

$$G_{VL}(f) = G_{FB} G_{PWM_PS}(f) \tag{106}$$

$$G_{VLdB}(f) = 20 log\left(\left|G_{VL}(f)\right|\right) \tag{107}$$

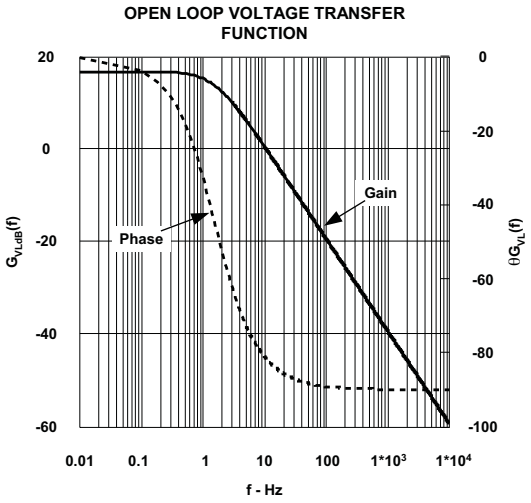

Figure 29. Bode Plot of the Open Loop Voltage Transfer Function

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The voltage error amplifier is compensated with a zero, f_{ZERO}, at the f_{PWM_PS} pole and a pole, f_{POLE}, placed at 20 Hz to reject high frequency noise and roll off the gain amplitude. The overall voltage loop crossover, f_V, is desired to be at 10 Hz. The compensation components of the voltage error amplifier are selected accordingly.

$$f_{ZERO} = \frac{1}{2\pi R_{VCOMP} C_{VCOMP}} \tag{108}$$

$$f_{POLE} = \frac{1}{2\pi \frac{R_{VCOMP} C_{VCOMP} C_{VCOMP_P}}{C_{VCOMP} + C_{VCOMP_P}}} \tag{109}$$

$$G_{EA}(f) = gmv \left[\frac{1 + s(f) R_{VCOMP} C_{VCOMP}}{\left(C_{VCOMP} + C_{VCOMP_P}\right) s(f) \left[1 + s(f) \left(\frac{R_{VCOMP} C_{VCOMP} C_{VCOMP_P}}{C_{VCOMP} + C_{VCOMP_P}} \right) \right]} \right] \tag{110}$$

$$f_V = 10 Hz \tag{111}$$

From Figure 29, and the Design Calculator spreadsheet, the open loop gain of the voltage transfer function at 10 Hz is approximately 0.667 dB. Estimating that the parallel capacitor, C_{VCOMP_P}, is much smaller than the series capacitor, C_{VCOMP}, the unity gain will be at f_V, and the zero will be at f_{PWM_PS}, the series compensation capacitor is determined:

$$C_{VCOMP} = \frac{gmv \frac{f_V}{f_{PWM_PS}}}{10^{\frac{G_{VLdB}(f)}{20}} \times 2\pi f_V} \tag{112}$$

$$C_{VCOMP} = \frac{42\mu S \times \frac{10Hz}{1.581Hz}}{10^{\frac{0.667dB}{20}} \times 2 \times \pi \times 10Hz} = 3.92\mu F \tag{113}$$

A 3.3-µF capacitor is used for C_{VCOMP}.

$$R_{VCOMP} = \frac{1}{2\pi f_{ZERO} C_{VCOMP}} \tag{114}$$

$$R_{VCOMP} = \frac{1}{2 \times \pi \times 1.581Hz \times 3.3\mu F} = 30.51k\Omega \tag{115}$$

A 33.2-kΩ resistor is used for R_{VCOMP}.

$$C_{VCOMP_P} = \frac{C_{VCOMP}}{2\pi f_{POLE} R_{VCOMP} C_{VCOMP} - 1} \tag{116}$$

$$C_{VCOMP_P} = \frac{3.3\mu F}{2 \times \pi \times 20Hz \times 33.2k\Omega \times 3.3\mu F - 1} = 0.258\mu F \tag{117}$$

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A 0.22-µF capacitor is used for C_{VCOMP_P}.

The total closed loop transfer function, G_{VL_total}, contains the combined stages and is plotted in Figure 30.

$$G_{VL_total}(f) = G_{FB}(f)G_{PWM_PS}(f)G_{EA}(f) \quad (118)$$

$$G_{VL_totaldB}(f) = 20\log\left(\left|G_{VL_total}(f)\right|\right) \quad (119)$$

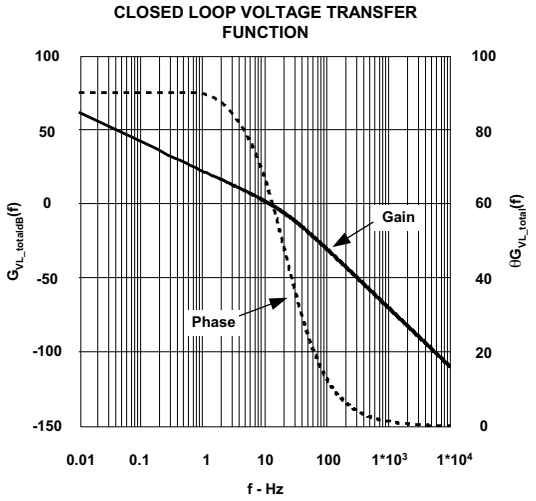

Figure 30. Closed Loop Voltage Bode Plot

8.2.2.11 Brown Out Protection

Select the top divider resistor into the VINS pin so as not to contribute excessive power loss. The extremely low bias current into VINS means the value of R_{VINS1} could be hundreds of megaOhms. For practical purposes, a value less than 10 MΩ is usually chosen. Assuming approximately 150 times the input bias current through the resistor dividers will result in an R_{VINS1} that is less than 10 MΩ , so as to not contribute excessive noise, and still maintain minimal power loss. The brown out protection will turn off the gate drive when the input falls below the user programmable minimum voltage, $V_{AC(off)}$, and turn on when the input rises above $V_{AC(on)}$.

$$I_{VINS} = 150 \times I_{VINS_0V} \tag{120}$$

$$I_{VINS} = 150 \times 0.1\mu A = 15\mu A \tag{121}$$

$$V_{AC(on)} = 75V \tag{122}$$

$$V_{AC(off)} = 65V \tag{123}$$

$$R_{VINS1} = \frac{\sqrt{2} \times V_{AC(on)} - V_{F_BRIDGE} - VINS_{ENABLE_th(max)}}{I_{VINS}} \tag{124}$$

$$R_{VINS1} = \frac{\sqrt{2} \times 75V - 0.95V - 1.6V}{15\mu A} = 6.9M\Omega \tag{125}$$

A 6.5-M resistance is chosen.

$$R_{VINS2} = \frac{VINS_{ENABLE_th(max)} \times R_{VINS1}}{\sqrt{2} \times V_{AC(on)} - VINS_{ENABLE_th(max)} - V_{F_BRIDGE}} \tag{126}$$

$$R_{VINS2} = \frac{1.6V \times 6.5M\Omega}{\sqrt{2} \times 75V - 1.6V - 0.95V} = 100k\Omega \tag{127}$$

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The capacitor on VINS, C_{VINS}, is selected so that it's discharge time is greater than the output capacitor hold up time. C_{OUT} was chosen to meet one-cycle hold-up time so C_{VINS} will be chosen to meet 2.5 half-line cycles.

$$t_{CVINS_dischrg} = \frac{N_{HALF_CYCLES}}{2 \times f_{LINE(min)}} \tag{128}$$

$$t_{CVINS_dischrg} = \frac{2.5}{2 \times 47Hz} = 25.6ms \tag{129}$$

$$C_{VINS} = \frac{-t_{CVINS_dischrg}}{R_{VINS2} \times ln\left[\frac{VINS_{BROWNOUT_th(min)}}{0.9 \times V_{IN_RMS(min)} \times \left(\frac{R_{VINS2}}{R_{VINS1} + R_{VINS2}}\right)}\right]} \tag{130}$$

$$C_{VINS} = \frac{-25.6ms}{100k\Omega \times ln\left[\frac{0.76V}{0.9 \times 85V \times \left(\frac{100k\Omega}{6.5M\Omega + 100k\Omega}\right)}\right]} = 0.63\mu F \tag{131}$$

8.2.3 Application Curves

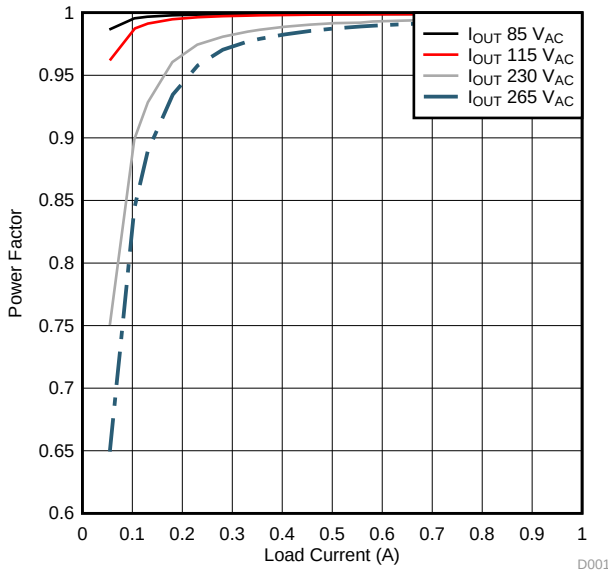

Figure 31. Power Factor vs. Load Current

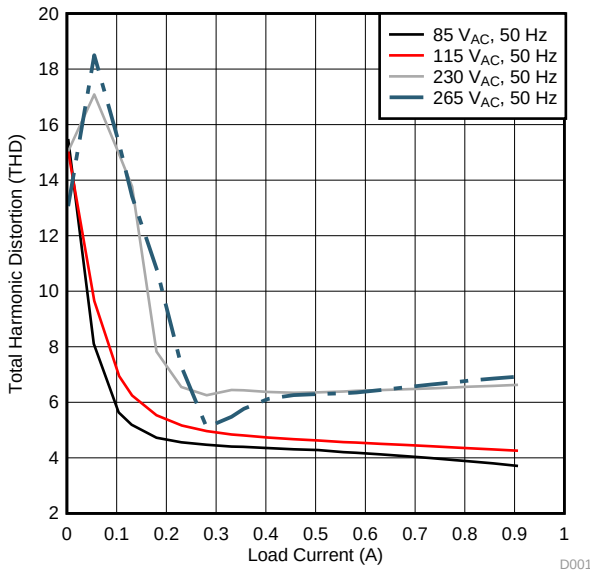

Figure 32. Total Harmonic Distortion vs. Load Current

9 Power Supply Recommendations

9.1 Bias Supply

The UCC28019A operates from an external bias supply. It is recommended that the device be powered from a regulated auxiliary supply.

NOTE

This device is not intended to be used from a bootstrap bias supply. A bootstrap bias supply is fed from the input high voltage through a resistor with sufficient capacitance on VCC to hold up the voltage on VCC until current can be supplied from a bias winding on the boost inductor. For that reason, the minimal hysteresis on VCC would require an unreasonable value of hold-up capacitance.

During normal operation, when the output is regulated, current drawn by the device includes the nominal run current plus the current supplied to the gate of the external boost switch. Decoupling of the bias supply must take switching current into account in order to keep ripple voltage on VCC to a minimum. A ceramic capacitor of 0.1 μF minimum value from VCC to GND with short, wide traces is recommended.

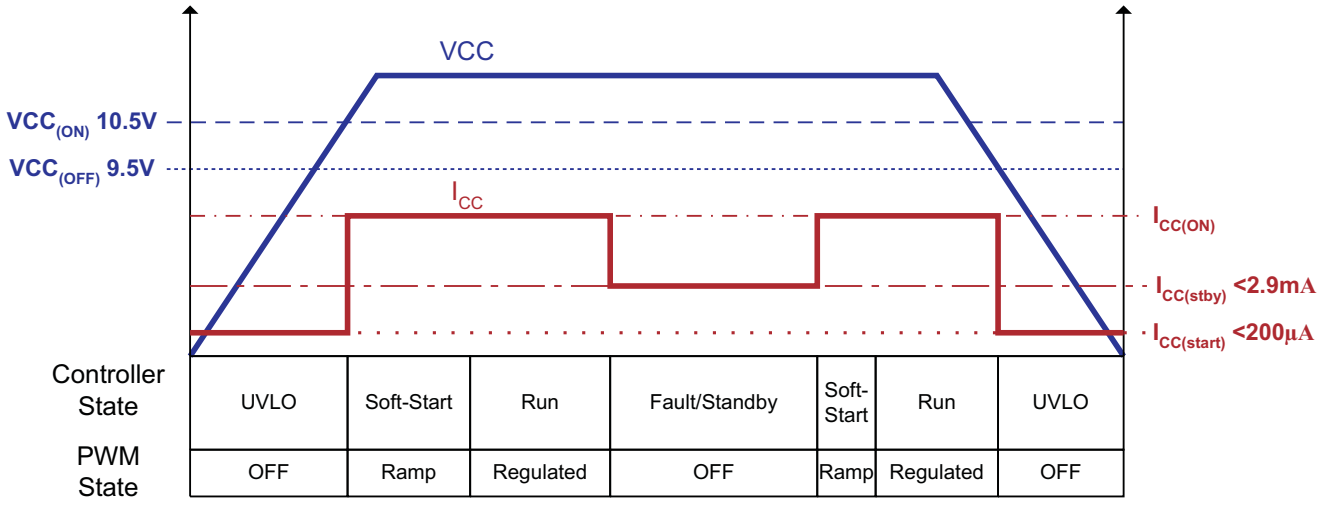

Figure 33. Device Supply States

The device bias operates in several states. During startup, VCC Under-Voltage Lock-Out (UVLO) sets the minimum operational dc input voltage of the controller. There are two UVLO thresholds. When the UVLO turn-on threshold is exceeded, the PFC controller turns ON. If the VCC voltage falls below the UVLO turn-off threshold, the PFC controller turns off. During UVLO, current drawn by the device is minimal. After the device turns on, Soft Start (SS) is initiated and the boost inductor current is ramped up in a controlled manner to reduce the stress on the external components and avoids output voltage overshoot. During Soft Start and after the output is in regulation, the device draws its normal run current. If any of several fault conditions is encountered or if the device is put in Standby with an external signal, the device draws a reduced standby current.

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10 Layout

10.1 Layout Guidelines

As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. The pin out of the UCC28019A is ideally suited for separating the high di/dt induced noise on the power ground from the low current quiet signal ground required for adequate noise immunity. A star point ground connection at the GND pin of the device can be achieved with a simple cut out in the ground plane of the printed circuit board. As shown in Figure 34, the capacitors on ISENSE, VINS, VCOMP, and VSENSE must all be returned directly to the quiet portion of the ground plane, indicated by Signal GND, and not the high current return path of the converter, shown as the Power GND. Because the example circuit in Figure 34 uses surface mount components, the ICOMP capacitor, C10, has its own dedicated return to the GND pin.

Table 2. Layout Components

REFERENCE DESIGNATOR	FUNCTION
U1	UCC28019A
Q1	Main switch
R1	R_{GATE}
R5	Pull-down resistor on GATE
C13, C14	VCC bypass capacitors
C10	ICOMP compensation, C_{ICOMP}
R6	Inrush current limiting resistor, R_{ISENSE}
C11	I_{SENSE} filter, C_{ISENSE}
R12, R13, R14	R_{FB1} on VSENSE
R18	R_{FB2} on VSENSE
C16	C_{VSENSE}
R16, C17, C15	VCOMP compensation components, R_{VCOMP}, C_{VCOMP}, C_{VCOMP_P}
C12, R17	C_{VINS}, R_{VINS2} on VINS
D2	Boost diode

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Layout Guidelines (continued)

10.2 Layout Example

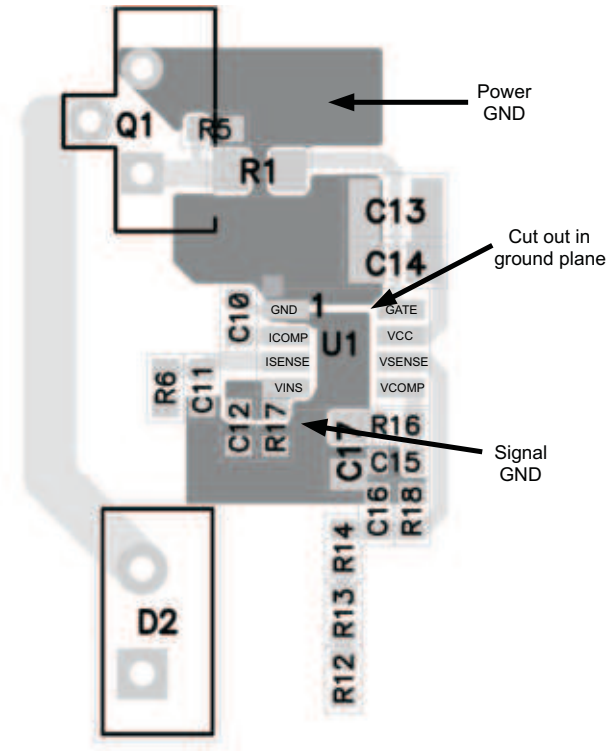

Figure 34. Recommended Layout for the UCC28019A

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Related Products

The following parts have characteristics similar to the UCC28019A and may be of interest.

Table 3. Related Products

DEVICE	DESCRIPTION
UCC28019	8-Pin CCM PFC Controller
UCC3817/18	Full-Feature PFC Controller
UC2853A	8-Pin CCM PFC Controller

11.2 Documentation Support

11.2.1 Related Documentation

These references, additional design tools, and links to additional references, including design software and models may be found on the web at www.power.ti.com under Technical Documents.

1. Design Spreadsheet, UCC28019A Design Calculator, SLUC117

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28019AD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28019A
UCC28019AD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28019A
UCC28019ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28019A
UCC28019ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28019A
UCC28019ADR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28019A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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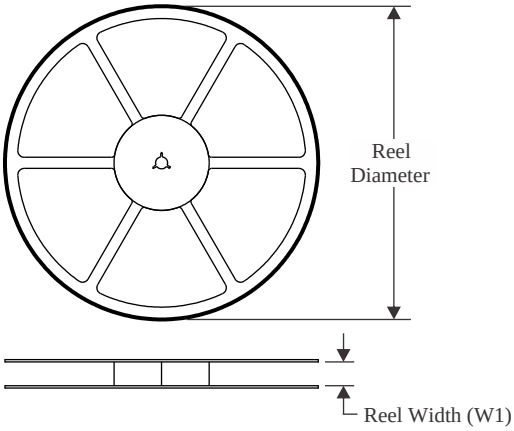
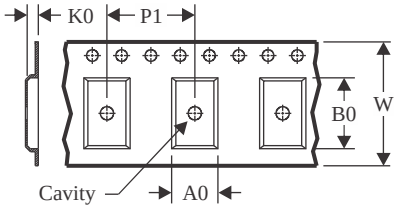
TAPE AND REEL INFORMATION

REEL DIMENSIONS

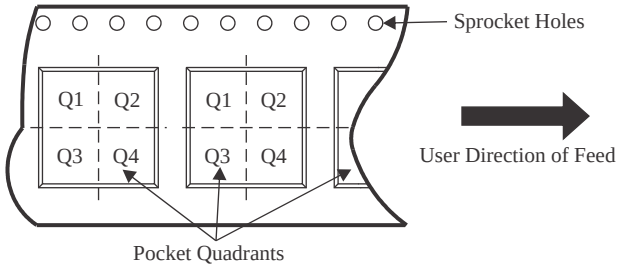


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

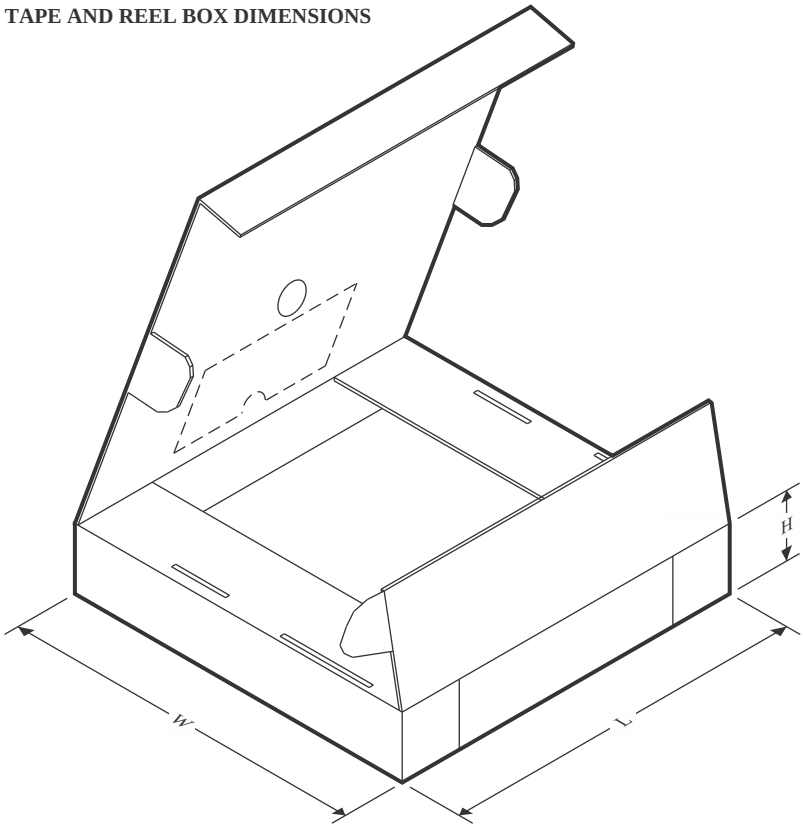
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28019ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

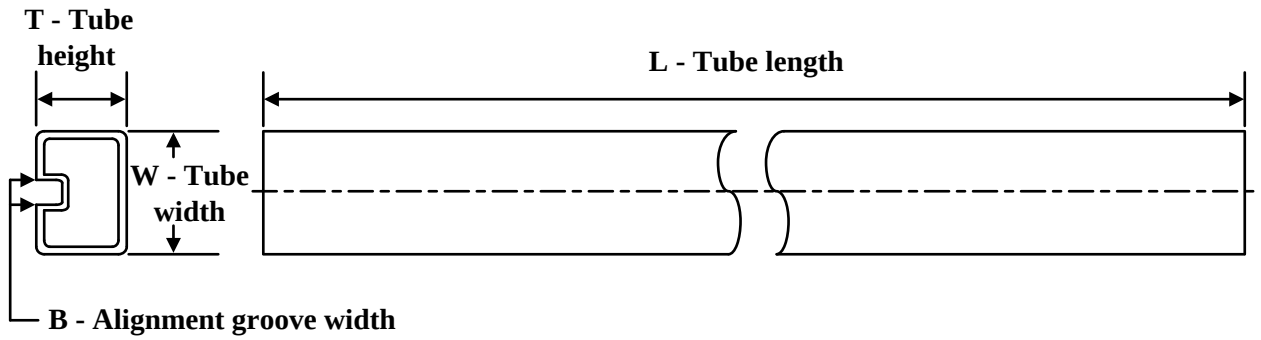
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28019ADR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28019AD	D	SOIC	8	75	507	8	3940	4.32
UCC28019AD.A	D	SOIC	8	75	507	8	3940	4.32

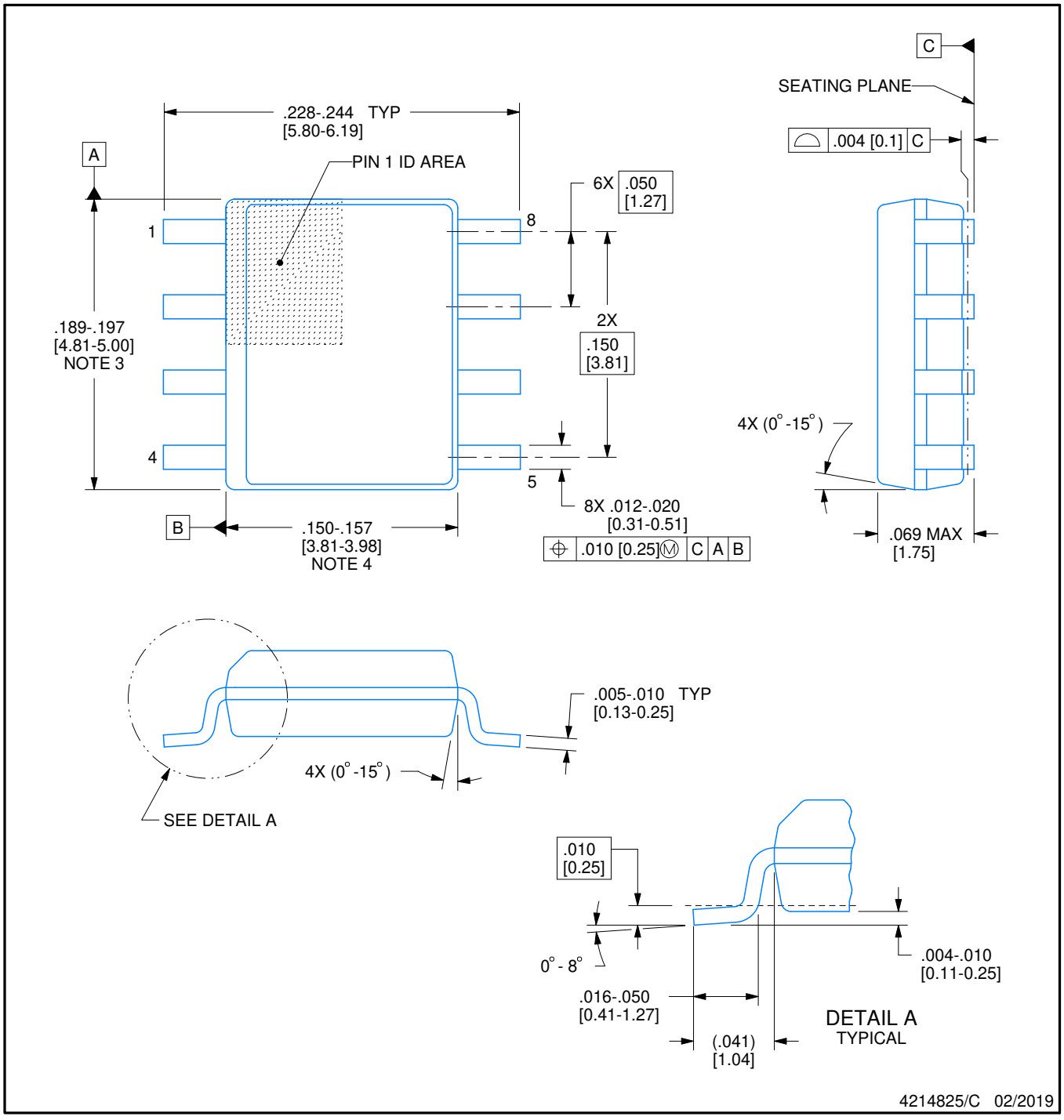


PACKAGE OUTLINE

D0008A

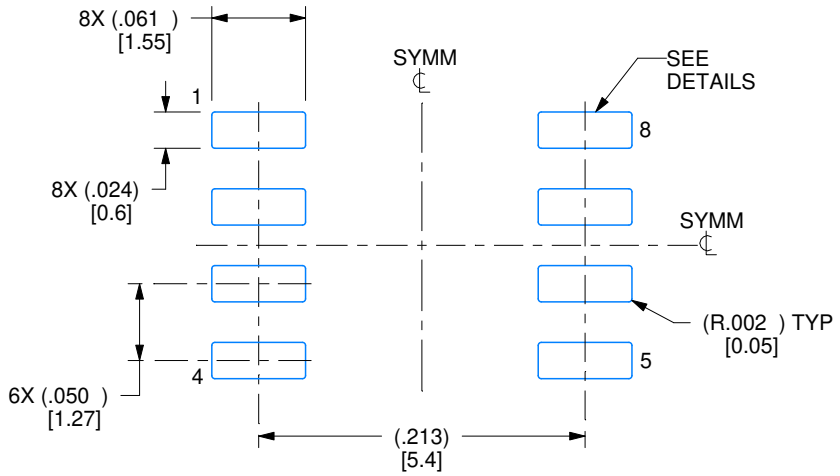
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

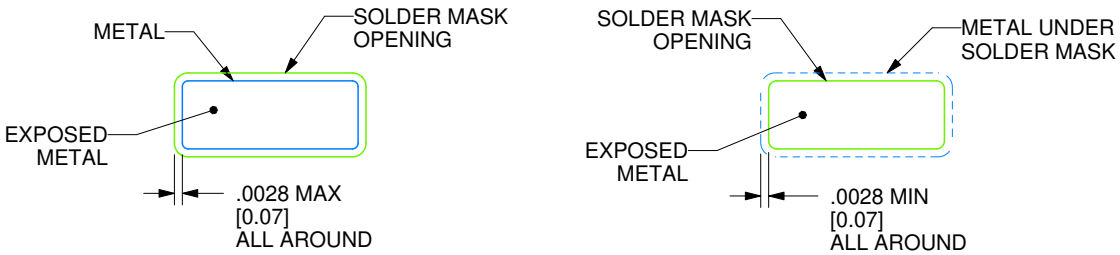


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

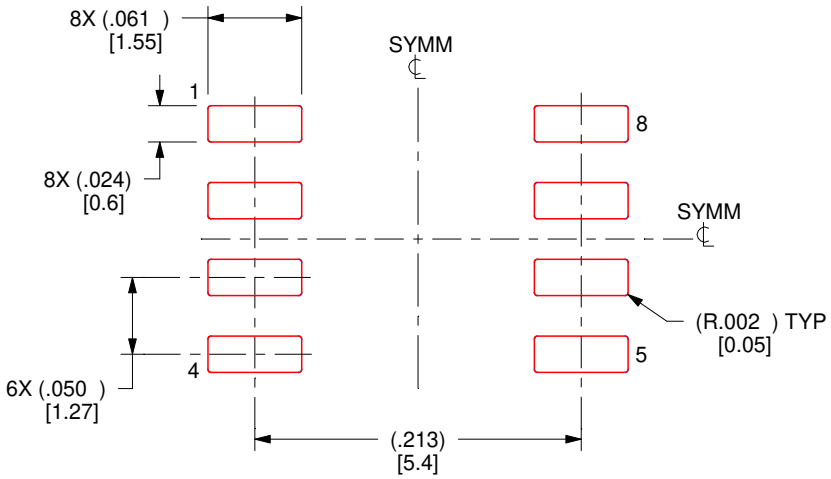
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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