UCC28064A Natural Interleaving™ Transition-Mode PFC Controller with High Light-Load Efficiency

1 Features

- Input filter and output capacitor ripple-current reduction
  - Reduced current ripple for higher system reliability and smaller bulk capacitor
  - Reduced EMI filter size
- High light-load efficiency
  - User adjustable phase management with input voltage compensation
  - Burst mode operation with adjustable burst threshold
  - Helps enable compliance to EUP Lot6 Tier II, CoC Tier II and DOE Level VI standards
- Sensorless current-shaping simplifies board layout and improves efficiency
- Input line feed-forward for fast line transient response
- Inrush-safe current limiting:
  - Prevents MOSFET conduction during inrush
  - Eliminates CCM operation and reverse recovery events in output rectifier
- Operating temperature range –40°C to +125°C in a 16-pin SOIC package
- Create a Custom Design Using the UCC28064A With the WEBENCH® Power Designer

2 Applications

- HD, U-HD, and LED TVs
- All-in-one PC
- Gaming
- Adapters
- Home audio systems

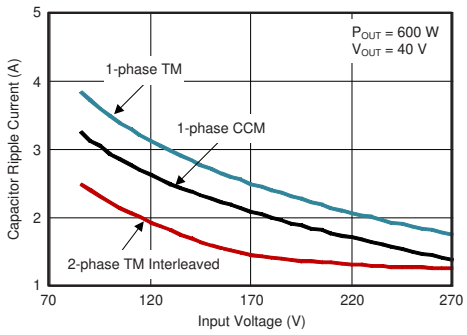
3 Description

The UCC28064A interleaved PFC controller has higher power ratings than previously possible. The device uses a Natural Interleaving™ technique. Both channels operate as masters (there is no slave channel) synchronized to the same frequency. This approach enables faster response time, excellent phase-to-phase on-time matching, and transition mode operation for each channel. The device has a burst mode function to get high light-load efficiency. Burst mode eliminates the need to turn off the PFC during light load operation to meet standby power targets. Burst mode eliminates the need for an auxiliary flyback converter when paired with UCC25630x LLC controller and the UCC24624 synchronous rectifier controller.

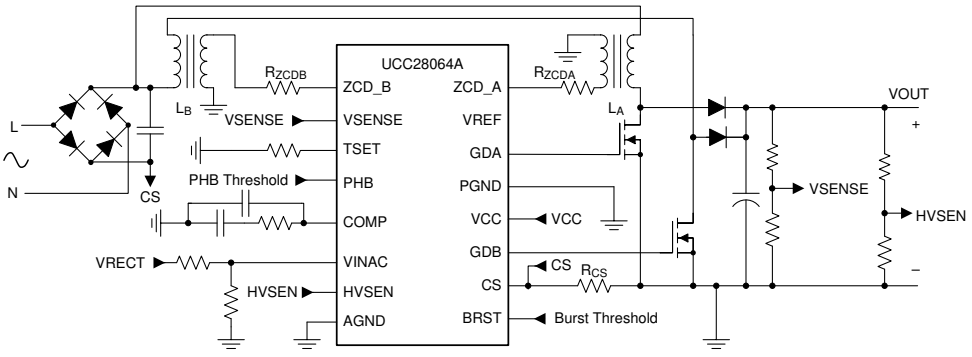
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28064A	SOIC (16)	9.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2018) to Revision B	Page
• Changed Simplified Application diagram.	1

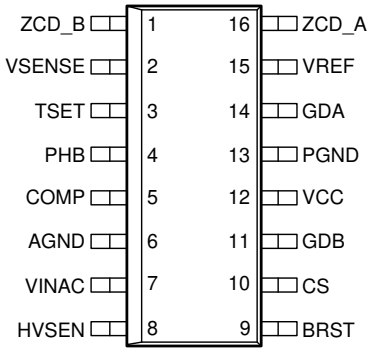
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5 Description (Continued)

Expanded system level protections features include input brownout and dropout recovery, output over-voltage, open-loop, overload, soft-start, phase-fail detection, and thermal shutdown. The additional fail-safe over-voltage protection (OVP) feature protects against shorts to an intermediate voltage that, if undetected, could lead to catastrophic device failure. Advanced non-linear gain results in rapid, yet smooth response to line and load transient events. Special line-dropout handling avoids significant current disruption. Strong reduction of bias current when not switching during burst mode operation, improves stand-by performance.

6 Pin Configuration and Functions

D Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	6	-	Analog ground
BRST	9	I	Burst mode threshold input
COMP	5	O	Error amplifier output
CS	10	I	Current sense input
GDA	14	O	Phase A gate driver output
GDB	11	O	Phase B gate driver output
HVSEN	8	I	High voltage output sense
PGND	13	-	Power ground
PHB	4	I	Phase B enable disable threshold input
TSET	3	I	Timing set
VCC	12	-	Bias supply input
VINAC	7	I	Input AC voltage sense
VSENSE	2	I	Error amplifier input
VREF	15	O	Voltage reference output
ZCDA	16	I	Phase A zero current detection input
ZCDB	1	I	Phase B zero current detection input

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7 Specifications

7.1 Absolute Maximum Ratings

All voltages are with respect to GND, −40°C < T_J = T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

			MIN	MAX	UNIT
	Continuous input voltage	VCC (1)	−0.5	21	V
		COMP (2), PHB, HVSEN (3), VINAC (3), VSENSE (3), TSET, BRST	–0.5	7	
		ZCDA, ZCDB	–0.5	4	
		CS (4)	–0.5	3	
		GDA, GDB (5)	–0.5	VCC + 0.3	
	Continuous input current	VCC		20	mA
		ZCDA, ZCDB		±5	
		GDA, GDB (5)	–25	25	
		VREF	–2		
	Peak input current	CS	–30		mA
T_J	Operating junction temperature		–40	125	°C
T_{SOL}	Soldering 10 s			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Voltage on VCC is internally clamped. VCC may exceed the continuous absolute maximum input voltage rating if the source is current limited below the absolute maximum continuous VCC input current level.
(2) In normal use, COMP is connected to capacitors and resistors and is internally limited in voltage swing.
(3) In normal use, VINAC, VSENSE, and HVSEN are connected to high-value resistors and are internally limited in negative-voltage swing. Although not recommended for extended use, VINAC, VSENSE, and HVSEN can survive input currents as high as -10mA from negative voltage sources, and input currents as high as +0.5mA from positive voltage sources.
(4) In normal use, CS is connected to a series resistor to limit peak input current during brief system line-inrush conditions. In these situations, negative voltage on CS may exceed the continuous absolute maximum rating.
(5) No GDA or GDB current limiting is required when driving a power MOSFET gate. However, a small series resistor may be required to damp resonant ringing due to stray inductance.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

All voltages are with respect to GND, −40°C < T_J = T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

	MIN	MAX	UNIT
VCC input voltage from a low-impedance source	14	21	V
VCC input current from a high-impedance source	8	18	mA
VINAC input voltage	0	6	V
VREF load current	0	–2	mA
ZCDA, ZCDB series resistor	20	80	kΩ
TSET resistor to program PWM on-time	66.5	400	kΩ
HVSEN input voltage	0.8	4.5	V
PHB Phase management threshold voltage	0	2	V
BRST Burst mode threshold voltage	0	V_{PHB} - 0.6 V	V

7.4 Thermal Information

THERMAL METRIC		UCC28064A SOIC (D) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	91.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(2)	52.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance(3)	48.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter(4)	14.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter(5)	48.3	°C/W

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDECstandard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Electrical Characteristics

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 0V, BRST = 0V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40°C < T_J = T_A < 125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC BIAS SUPPLY						
VCC_{SHUNT}	VCC shunt voltage(1)	I_{VCC} = 10 mA	22	24	26	V
$I_{VCC(UVLO)}$	VCC current, UVLO	VCC = 9.3 V prior to turn on		125	200	µA
$I_{VCC(stby)}$	VCC current, disabled	VSENSE = 0 V		150	210	µA
$I_{VCC(on)}$	VCC current, enabled	VSENSE = 2 V		5	8	mA
$I_{VCC(BURST)}$	VCC current burst mode no switching	V_{COMP} < V_{BURST}		650	850	µA
UNDERVOLTAGE LOCKOUT (UVLO)						
VCC_{ON}	VCC turnon threshold	VCC rising	9.45	10.35	11.1	V
VCC_{OFF}	VCC turnoff threshold	VCC falling	8.8	9.6	10.7	V
ΔVCC_{UVLO}	UVLO Hysteresis	VCC_{ON} - VCC_{OFF}	0.68	0.8	0.9	V
REFERENCE						

(1) Excessive VCC input voltage and current will damage the device. This clamp will not protect the device from an unregulated bias supply. If an unregulated bias supply is used, a series-connected Fixed Positive-Voltage Regulator such as the UA78L15A is recommended. See the Absolute Maximum Ratings table for the limits on VCC voltage, current, and junction temperature.

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 0V, BRST = 0V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40°C < T_J = T_A < 125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REF}	VREF output voltage, no load	I_{VREF} = 0 mA	5.82	6.00	6.18	V
ΔV_{REF_LOAD}	VREF change with load	0 mA ≤ I_{VREF} ≤ −2 mA	-6	-1		mV
ΔV_{REF_VCC}	VREF change with VCC	12 V ≤ VCC ≤ 20 V		2	10	mV
ERROR AMPLIFIER						
VSENSEreg25	VSENSE input regulation voltage	T_A = 25°C	5.85	6	6.15	V
VSENSEreg	VSENSE input regulation voltage		5.82	6	6.18	V
I_{VSENSE}	VSENSE input bias current	In regulation	50	100	150	nA
V_{ENAB}	VSENSE enable threshold, rising		1.15	1.25	1.35	V
	VSENSE enable hysteresis		0.02	0.07	0.15	V
V_{COMP_CLMP}	COMP high voltage, clamped	VSENSE = VSENSEreg – 0.3 V	4.70	4.95	5.10	V
V_{COMP_SAT}	COMP low voltage, saturated	VSENSE = VSENSEreg + 0.3 V		0.03	0.125	V
g_{M1}	VSENSE to COMP transconductance, small signal	0.99(VSENSEreg) < VSENSE < 1.01(VSENSEreg), COMP = 3 V	40	55	70	µS
$V_{SENSE_gM2_SINK}$	VSENSE high-going threshold to enable COMP large signal gain, percent	Relative to VSENSEreg, COMP = 3 V	3.25	5	6.75	%
$V_{SENSE_gM2_SOURCE}$	VSENSE low-going threshold to enable COMP large signal gain, percent	Relative to VSENSEreg, COMP = 3 V	–6.75	−5	−3.25	%
g_{M2_SOURCE}	VSENSE to COMP transconductance, large signal	VSENSE = VSENSEreg – 0.4 V , COMP = 3 V	210	290	370	µS
g_{M2_SINK}	VSENSE to COMP transconductance, large signal	VSENSE = VSENSEreg + 0.4 V, COMP = 3 V	210	290	370	µS
$I_{COMP_SOURCE_MAX}$	COMP maximum source current	VSENSE = 5 V, COMP = 3 V	-170	-125	-80	µA
$R_{COMPDCHG}$	COMP discharge resistance	HVSEN = 5.2 V, COMP = 3 V	1.6	2	2.4	kΩ
I_{DODCHG}	COMP discharge current during Dropout	VSENSE = 5 V, VINAC = 0.3 V, COMP = 1V	3.2	4	4.8	µA
V_{LOW_OV}	VSENSE overvoltage threshold, rising	Relative to VSENSEreg	6.5	8	9.5	%
$\Delta V_{LOW_OV_HYST}$	VSENSE overvoltage hysteresis	Relative to V_{LOW_OV}	-3	-2	-1.5	%
V_{HIGH_OV}	VSENSE 2nd overvoltage threshold, rising	Relative to VSENSEreg	9.3	11	12.7	%
SOFT START						
V_{SSTHR}	COMP Soft-Start threshold, falling	VSENSE = 1.5 V	10	23	35	mV
$I_{SS,FAST}$	COMP Soft-Start current, fast	SS-state, V_{ENAB} < VSENSE < VREF/2	-170	-125	-80	µA
$I_{SS,SLOW}$	COMP Soft-Start current, slow	SS-state, VREF/2 < VSENSE < 0.88VREF	-20	-16	-11.5	µA
K_{EOSS}	VSENSE End-of-Soft-Start threshold factor	Percent of VSENSEreg	96.5%	98.3%	99.8%	
OUTPUT MONITORING						
$V_{HV_OV_FLT}$	HVSEN threshold to overvoltage fault	HVSEN rising	4.64	4.87	5.1	V
$V_{HV_OV_CLR}$	HVSEN threshold to overvoltage clear	HVSEN falling	4.45	4.67	4.8	V
GATE DRIVE						

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 0V, BRST = 0V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40°C < T_J = T_A < 125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GDx_H}	GDA, GDB output voltage, high	I_{GDA}, I_{GDB} = −100 mA	10.7	12.4	15	V
R_{GDx_H}	GDA, GDB on-resistance, high	I_{GDA}, I_{GDB} = −100 mA		8.8	16.7	Ω
V_{GDx_L}	GDA, GDB output voltage, low	I_{GDA}, I_{GDB} = 100 mA		0.18	0.32	V
R_{GDx_L}	GDA, GDB on-resistance, low	I_{GDA}, I_{GDB} = 100 mA		2	3.2	Ω
$V_{GDx_H_VCCH}$	GDA, GDB output voltage high, clamped	VCC = 20 V, I_{GDA}, I_{GDB} = −5 mA	11.8	13.5	15	V
$V_{GDx_H_VCCL}$	GDA, GDB output voltage high, low VCC	VCC = 12 V, I_{GDA}, I_{GDB} = −5 mA	10	10.5	11.5	V
$V_{GDx_L_UVLO}$	GDA, GDB output voltage, UVLO	VCC = 3.0 V, I_{GDA}, I_{GDB} = 2.5 mA		100	200	mV
t_{GDx_RISE}	Rise time	1 V to 9 V, C_{LOAD} = 1 nF		18	30	ns
t_{GDx_FALL}	Fall time	9 V to 1 V, C_{LOAD} = 1 nF		12	25	ns
ZERO CURRENT DETECTOR						
V_{ZCDx_TRIG}	ZCDA, ZCDB voltage threshold, falling		0.8	1	1.2	V
V_{ZCDx_ARM}	ZCDA, ZCDB voltage threshold, rising		1.5	1.7	1.9	V
$V_{ZCDx_CLMP_H}$	ZCDA, ZCDB clamp, high	I_{ZCDA} = +2 mA, I_{ZCDB} = +2 mA	2.6	3	3.4	V
$V_{ZCDx_CLMP_L}$	ZCDA, ZCDB clamp, low	I_{ZCDA} = −2 mA, I_{ZCDB} = −2 mA	-0.40	−0.2	0	V
I_{ZCDx}	ZCDA, ZCDB input bias current	ZCDA = 1.4 V, ZCDB = 1.4 V	-0.5	0	0.5	µA
t_{ZCDx_DEL}	ZCDA, ZCDB delay to GDA, GDB outputs	From ZCDx input falling to 1 V to respective gate drive output rising 10%		50	100	ns
t_{ZCDx_BLNK}	ZCDA, ZCDB blanking time	From GDx rising to GDx falling		100		ns
CURRENT SENSE						
I_{CS}	CS input bias current, dual-phase	At rising threshold	-200	-166	-120	µA
V_{CS_DPh}	CS current-limit rising threshold, dual-phase		-0.22	-0.2	-0.18	V
V_{CS_SPh}	CS current-limit rising threshold, single-phase	PHB = 6 V	-0.183	-0.166	-0.149	V
V_{CS_RST}	CS current-limit reset falling threshold		-0.025	–0.015	-0.002	V
t_{CS_DEL}	CS current-limit response time	From CS exceeding threshold−0.05 V to GDx dropping 10%		60	100	ns
t_{CS_BLNK}	CS blanking time	From GDx rising and falling edges		100		ns
VINAC INPUT						
I_{VINAC}	VINAC input bias current, above brownout	VINAC = 2 V	-0.5	0	0.5	µA
V_{BOTHR}	VINAC brownout threshold		1.33	1.45	1.6	V
t_{BODLY}	VINAC brownout filter time	VINAC below the brownout threshold for the brownout filter time	500	640	810	ms
t_{BORST}	VINAC brownout reset time	VINAC above the brownout threshold for the brownout reset time after Brown out event	300	450	600	ms
I_{BOHYS}	VINAC brownout hysteresis current	VINAC = 1 V for > t_{BODLY}	1.6	1.95	2.25	µA
V_{DODET}	VINAC dropout detection threshold	VINAC falling	0.310	0.35	0.38	V
t_{DODLY}	VINAC dropout filter time	VINAC below the dropout detection threshold for the dropout filter time	3.5	5	7	ms

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Electrical Characteristics (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 0V, BRST = 0V, R_{TSET} = 133 kΩ, all voltages are with respect to GND, all outputs unloaded, −40°C < T_J = T_A < 125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DOCLR}	VINAC dropout clear threshold	VINAC rising	0.67	0.71	0.75	V
PULSE-WIDTH MODULATOR						
K_{TL}	On-time factor, two phases operating, low VINAC_PK	VINAC=1.6V, VCOMP=4V(2)	3.0	4.15	5.3	µs/V
K_{TH}	On-time factor, two phases operating, high VINAC_PK	VINAC= 5V, VCOMP = 4V(2)	0.36	0.43	0.5	µs/V
K_{TSL}	On-time factor, single-phase operating, low VINAC_PK	VINAC=1.6V, VCOMP = 1.5V, PHB = 2V(2)	6.1	8.3	10.5	µs/V
K_{TSH}	On-time factor, single-phase operating, high VINAC_PK	VINAC= 5V, VCOMP = 1.5V, PHB=2V(2)	0.73	0.87	1.01	µs/V
t_{ZCC_I}	Zero-crossing distortion correction additional on time	COMP = 0.5 V, VINAC = 0.1 V	15	23.6	32.2	µs
t_{ZCC_II}	Zero-crossing distortion correction additional on time	COMP = 0.5 V, VINAC = 1.6 V	0.7	1.1	1.5	µs
t_{MIN}	Minimum Switching period	R_{TSET} = 133 kΩ, VCOMP = 0.3, VINAC = 3 V(2)	1.9	2.7	3.5	µs
t_{START}	PWM restart time	ZCDA = ZCDB = 2 V(3)	160	210	265	µs
t_{ONMAX_L}	Maximum FET on time at low VINAC	VSENSE = 5.8 V, VINAC=1.6V	15.1	20.4	26.2	µs
t_{ONMAX_H}	Maximum FET on time at High VINAC	VSENSE = 5.8 V, VINAC= 5V	1.5	2	2.4	µs
t_{ONMAX_SL}	Maximum FET on time at low VINAC, Single Phase operation.	VSENSE = 5.8V, VINAC=1.6V, PHB = 6V	11.8	16	20.2	µs
t_{ONMAX_SH}	Maximum FET on time at hgih VINAC, single phase operation	VSENSE = 5.8V, VINAC=5 V, PHB = 6V	1.37	1.66	1.95	µs
$\Delta t_{ONMAX_AB_L}$	Phase B to phase A on-time matching error	VSENSE = 5.8 V, VINAC=1.6V	–6		6	%
$\Delta t_{ONMAX_AB_H}$	Phase B to phase A on-time matching error	VSENSE = 5.8 V, VINAC= 5V	-6		6	%
ΔV_{BRST_HYST}	BRST Hysteresis, COMP voltage rising	BRST = 1V, VINAC = 1.5 V	30	50	70	mV
ΔV_{PHB_HYST}	PHB Hysteresis COMP voltage rising	PHB = 3V, VINAC = 2.5 V	80	150	210	mV
I_{PHB_RANGE}	PHB pin sourced current when high input voltage	VINAC = 3.75V, PHB = 2V	2	3	4.1	µA
I_{BRST_RANGE}	BRST pin sourced current when high input voltage	VINAC = 3.75V, BRST = 2V	2	3	4.1	µA
$V_{VINAC_RANGE_THF}$	VINAC range falling threshold	PHB = 2V, BRST = 2V	2.95	3.15	3.3	V
ΔV_{INAC_RANGE}	VINAC range Hysteresis at rising edge	PHB = 2V, BRST=2V	300	350	400	mV
THERMAL SHUTDOWN						
T_J	Thermal shutdown temperature	Temperature rising(4)		160		°C
T_J	Thermal restart temperature	Temperature falling(4)		140		°C

(2) Gate drive on-time is proportional to (VCOMP – 0.125 V). The on-time proportionality factor, KT, scales linearly with the value of RTSET and is different in two-phase and single-phase modes. The minimum switching period is proportional to RTSET.
(3) An output on-time is generated at both GDA and GDB if both ZCDA and ZCDB negative-going edges are not detected for the restart time. In single-phase mode, the restart time applies for the ZCDA input and the GDA output.
(4) Thermal shutdown occurs at temperatures higher than the normal operating range. Device performance above the normal operating temperature is not specified or assured.

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7.6 Typical Characteristics

V_{VCC} = 16 V, V_{AGND} = V_{PGND} = 0 V, V_{VINAC} = 3 V, V_{VSENSE} = 6 V, V_{HVSEN} = 3 V, V_{PHB} = 0 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, T_J = 25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

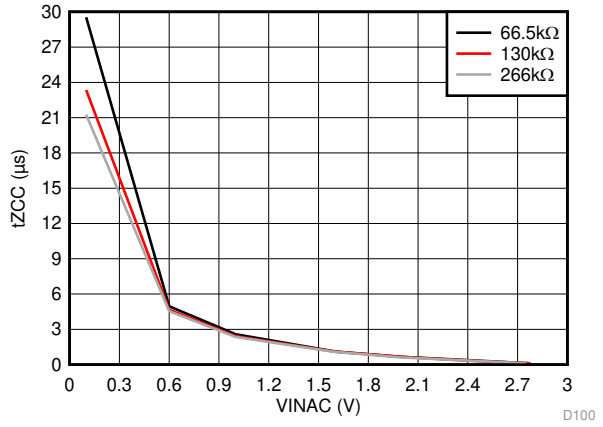


Figure 1. RTSET Resistance and Zero-Crossing Distortion Correction Additional On Time

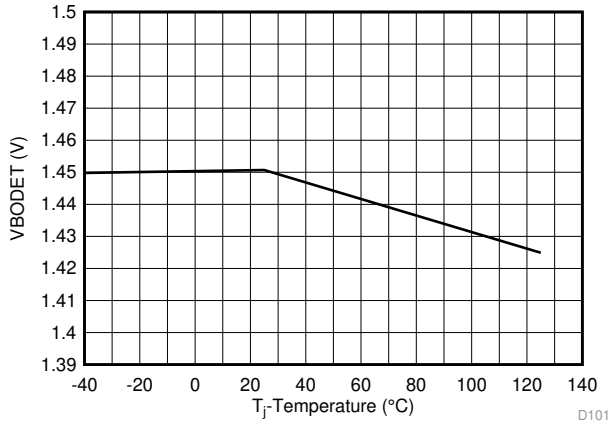


Figure 2. VINAC Brownout Detection Threshold

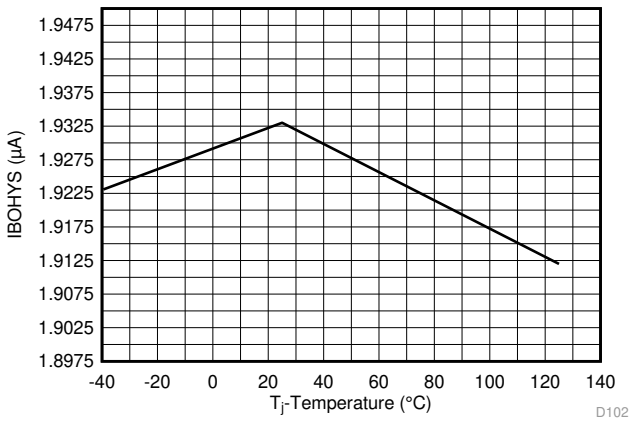


Figure 3. VINAC Brownout Hysteresis Current

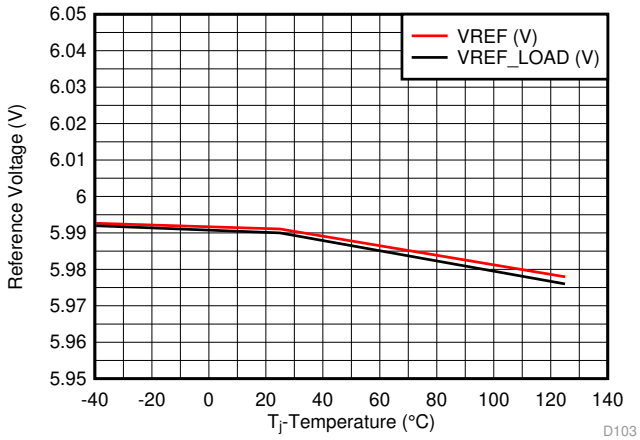


Figure 4. VREF Output Voltage

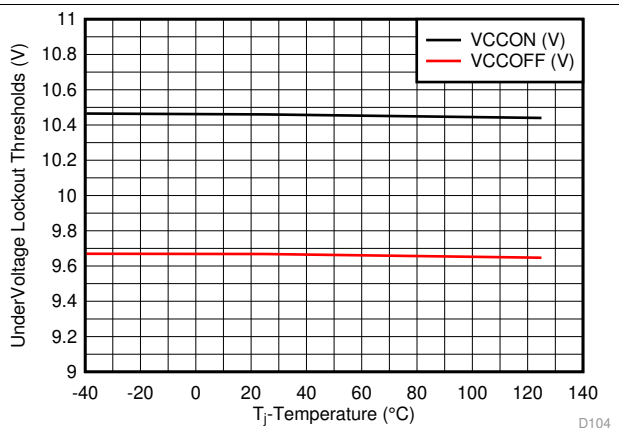


Figure 5. UVLO On Off Thresholds

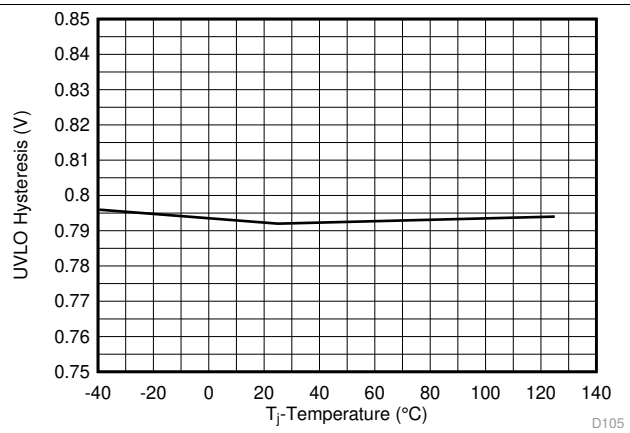


Figure 6. UVLO Hysteresis

Typical Characteristics (continued)

V_{VCC} = 16 V, V_{AGND} = V_{PGND} = 0 V, V_{VINAC} = 3 V, V_{VSENSE} = 6 V, V_{HVSEN} = 3 V, V_{PHB} = 0 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, T_J = 25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

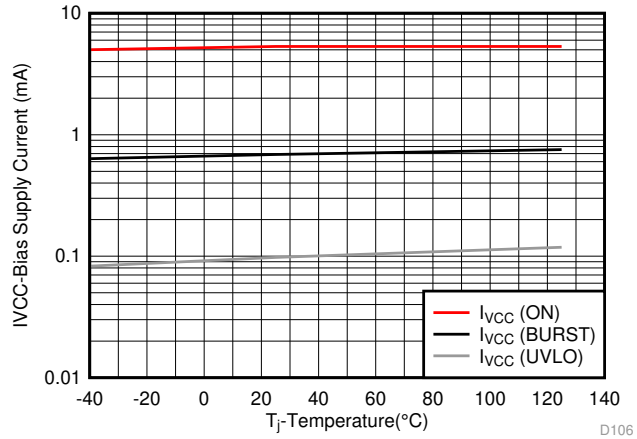
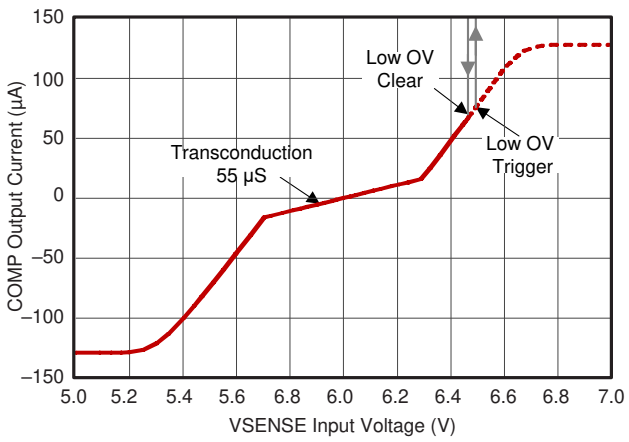


Figure 7. VCC Bias Supply Current



Soft-start period completed

Figure 8. Error Amplifier Output Current vs Input Voltage

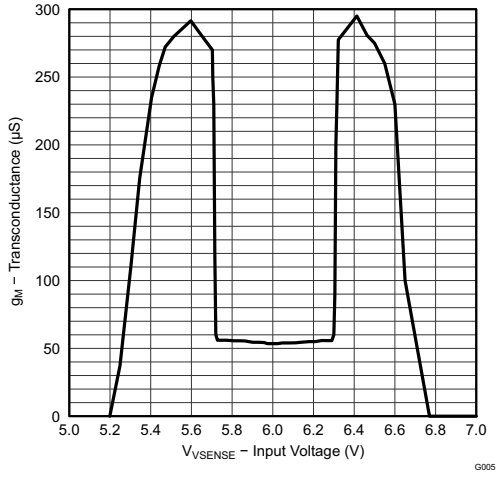


Figure 9. Error Amplifier Transconductance vs VSENSE

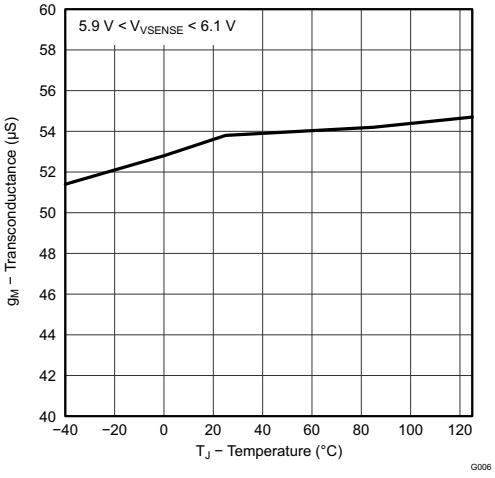


Figure 10. Error Amplifier Transconductance vs Temperature

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Typical Characteristics (continued)

V_{VCC} = 16 V, V_{AGND} = V_{PGND} = 0 V, V_{VINAC} = 3 V, V_{VSENSE} = 6 V, V_{HVSEN} = 3 V, V_{PHB} = 0 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, T_J = 25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

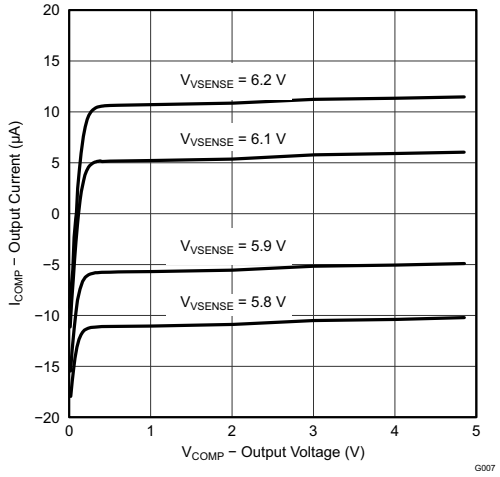


Figure 11. Error Amplifier Output Current vs Output Voltage

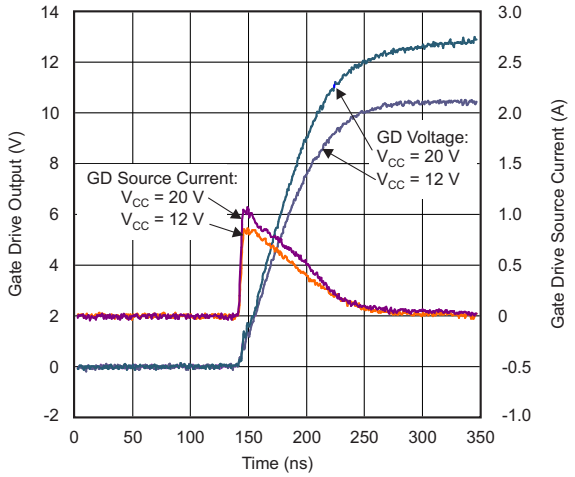


Figure 12. Gate Drive Rising vs Time

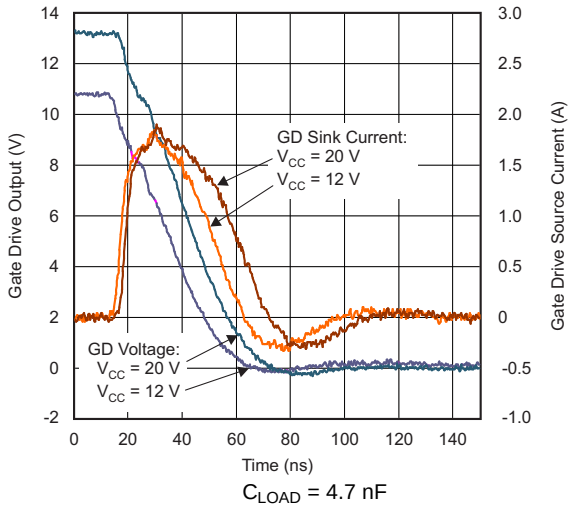


Figure 13. Gate Drive Falling vs Time

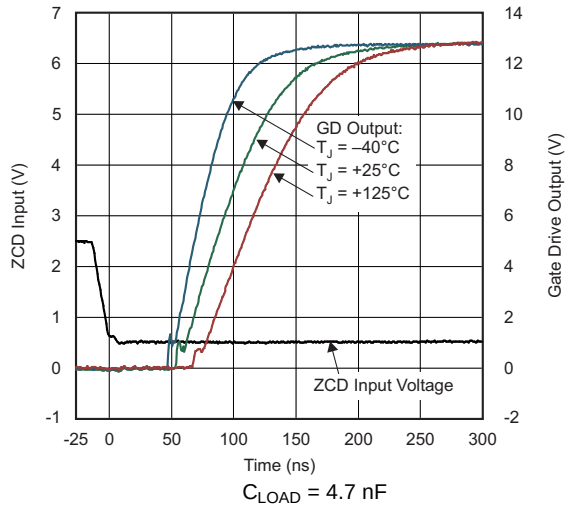


Figure 14. Gate Drive Rising and Delay From ZCD Input vs Time

Typical Characteristics (continued)

V_{VCC} = 16 V, V_{AGND} = V_{PGND} = 0 V, V_{VINAC} = 3 V, V_{VSENSE} = 6 V, V_{HVSEN} = 3 V, V_{PHB} = 0 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, T_J = 25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

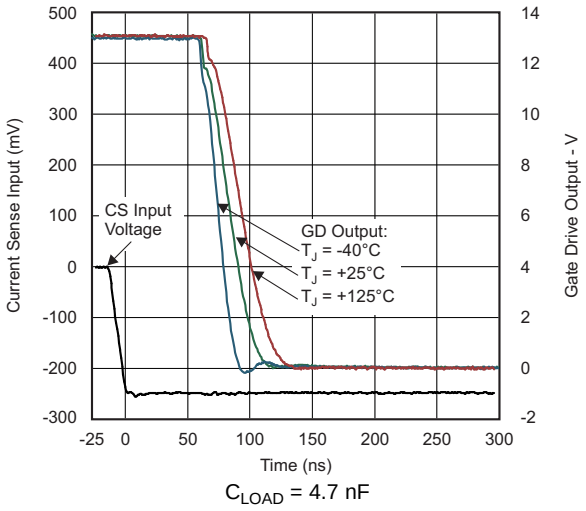


Figure 15. Gate Drive Falling and Delay From CS Input vs Time

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8 Detailed Description

8.1 Overview

Transition mode (TM) control is a popular choice for the boost power factor correction topology at lower power levels. Some advantages of this control method are its lower complexity in achieving high power factor and because lower cost boost diode with higher reverse recovery current specification may be used. In TM control MOSFET is turned on always when no current is flowing into diode. Interleaved Transition Mode Control retains this benefit and generally extends the applicability up to much higher power levels while simultaneously conferring the interleaving benefits of reduced input and output ripple current and system thermal optimization.

In UCC28064A, burst mode was introduced respect its predecessor (UCC28063) to achieve higher efficiency in light load conditions. Input voltage feed-forward and threshold adjustment is also available to ensure the user can optimize performance across line and load conditions. When operating single phase on time of the switching phase is doubled with the purpose of compensating the missing power from the not switching phase. In this way for the same COMP value the converter should provide the same output power regardless if operating single phase mode or dual phase mode. Unfortunately this is not always the case. Component variations and MOSFETs turn-off delay can lead to big differences (for the same COMP voltage) in the output power delivery. The *Phase Management and Light-Load Operation* section will discuss some ways to deal with the variations.

Line voltage feed-forward compensation provides several benefits: it maintains constant bandwidth of the control loop versus line voltage variation, avoids high current in the MOSFETs, inductors, and line filter when line transitions from low to high happens, and helps to keep simple Phase Management control because the COMP pin voltage is almost proportional to Load. Burst Mode enables high efficiency at light load and soft-on and soft-off in burst mode reduces risk of audible noise. The optimal load current at which the converter should enter burst mode can be different for different input voltages. These thresholds can be customized by the user.

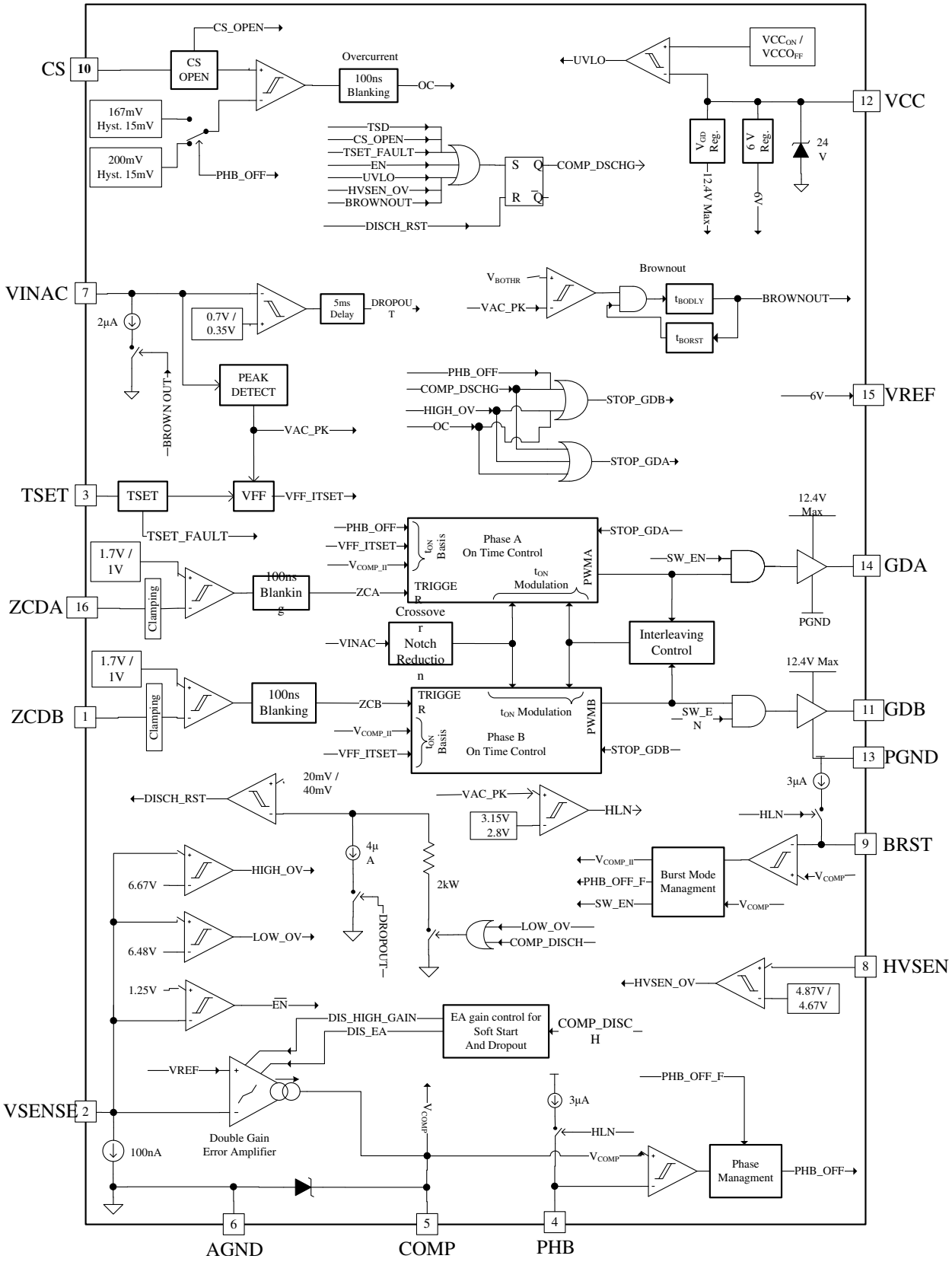
Interleaving control and phase management facilitates high efficiency 80+ and Energy Star designs with reduced input and output ripple. The Natural Interleaving method allows TM operation and achieves 180 degrees between the phases by On-time management. Moreover Natural interleaving method does not rely on tight tolerance requirements on the inductors. Negative current sensing is implemented on the total input current instead of just the MOSFET current which prevents MOSFET switching during inrush surges or in any mode where the inductor current may enter in continuous conduction mode (CCM). This prevents reverse recovery conduction events between the MOSFET and output rectifier.

Independent output voltage sense circuits with their separate fault management behaviors provide a high degree of redundancy against PFC stage over-voltage. Brownout, over voltage protection on HVSEN pin (HVSENSE OV), under voltage lockout (UVLO), and device over-temperature faults will all cause a complete Soft-Start cycle. Other faults such as short duration AC Drop-Out, minor over-voltage or cycle-by-cycle over-current cause a live recovery process to initiate by pulling down the COMP pin or by terminating the pulses early.

The error amplifier transconductance is designed to allow smaller compensation components and optimum transient response for large changes in line or load. The Soft-Start process is carefully optimized. A complete Soft-Start is implemented. It is dependent on the output voltage sense to speed up start-up from low AC line and to minimize the effect of excessive capacitance on the COMP pin during start-up into no-load. If some faults events are triggered COMP pin is fast pulled down to zero. This complete discharge of COMP aids with preventing excessive currents on recovery from an AC Brown-Out event.

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8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Principles of Operation

The UCC28064A device contains the control circuits for two parallel-connected boost pulse-width modulated (PWM) power converters. The boost PWM power converters ramp current in the boost inductors for a time period proportional to the voltage on the error amplifier output (COMP pin). Each power converter then turns off the power MOSFET until current in the boost inductor decays to zero (as sensed on the zero current detection inputs, ZCDA and ZCDB). After the inductor demagnetizes, the power converter starts another cycle. This cycle process produces a triangular waveform of current, with peak current set by the on-time and the instantaneous power mains input voltage, $V_{IN}(t)$ value, as shown in Equation 1.

$$I_{PEAK} = \frac{V_{IN} \times t_{ON}}{L} \tag{1}$$

The average line current is exactly equal to half of the peak line current, as shown in Equation 2.

$$I_{PEAK} = \frac{V_{IN} \times t_{ON}}{2 \times L} \tag{2}$$

When the t_{ON} and L values are essentially constant during an AC-line period, the resulting triangular current waveform during each switching cycle has an average value proportional to the instantaneous value of the rectified AC-line voltage. This architecture results in a resistive input impedance characteristic at the line frequency and a near-unity power factor.

8.3.2 Natural Interleaving

Under normal operating conditions, the UCC28064A device regulates the relative phasing of the channel A and channel B inductor currents to be approximately 180°. This greatly reduces the switching-frequency ripple currents seen at the line-filter and output capacitors, compared to the ripple current of each individual converter. This design allows a reduction in the size and cost of input and output filtering. The phase-control function differentially modulates the on-times of the A and B channels based on their phase and frequency relationship. The Natural Interleaving method allows the converter to achieve 180° phase-shift and transition-mode operation for both phases without tight requirements on boost inductor tolerance.

Ideally, the best current-sharing is achieved when both inductors are exactly the same value. Typically the inductances are not the same, so the current-sharing of the A and B channels is proportional to the inductor tolerance. Also, switching delays and resonances of each channel typically differ slightly, and the controller allows some necessary phase-error deviation from 180° to maintain equal switching frequencies. Optimal phase balance occurs if the individual power stages and the on-times are well matched. Mismatches in inductor values do not affect the phase relationship.

Interleaving may not be ideal under all conditions. In particular a loss of interleaving may be experienced at light loads near the zero crossings. In some cases there may be insufficient current to trigger a large enough signal to trip the zero crossing detectors. In addition the turn off delay in the MOSFET may dominate the overall on-time at very light loads. This creates a very limited ability for the controller to correct for phase errors in the system.

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Feature Description (continued)

8.3.3 On-Time Control, Maximum Frequency Limiting, Restart Timer and Input Voltage Feed-Forward compensation

Gate-drive on-time varies proportionately with the error-amplifier output voltage (V_{COMP}) and inversely proportional to the squared value of the peak of the rectified input voltage sensed through VINAC pin as stated by equation (3). In equation (3) it is shown that the on-time is inversely proportionally to the value of resistor R_{TSET} connected between pin TSET and pin AGND. In order to calculate on-time, Equation (4) can be used. Parameter K_T is function of the rectified peak input voltage sensed by pin VINAC as reported in graph of Figure 16. In this graph 3 curves are reported for three different values of R_{TSET}. Two values of parameter K_T are reported in the electrical specs table for two values of VINAC: K_{TL} and K_{TH} corresponding at the VINAC = 1.6V and VINAC = 5V and R_{TSET} = 133kΩ. Because voltage on VINAC is proportional to the line rectified voltage, for t_{ON} calculation purposes we refer to the peak value of this voltage that is obtained through an internal peak detect. K_T is inversely proportional to the squared value of VINAC peak value so it is the t_{ON} time realizing the so called voltage feed-forward compensation. The Voltage Feed-forward function modifies the MOSFET on time according to line voltage so, ideally output power delivered does not change if line voltage changes. When operating in single phase mode K_T is called K_{TS} and its value is doubled.

$$t_{ON} = \propto \frac{(V_{COMP} - 125\ mV)}{V_{INAC\ PK}{}^2 \times R_{TSET}} \tag{3}$$

The COMP pin voltage value is clamped at 4.95 V, so the maximum on time can be calculated by Equation 4.

$$t_{ON} = (V_{COMP} - 125\ mV) \times K_T(V_{INAC}) \tag{4}$$

Figure 16 shows the values of K_T versus the peak voltage value on VINAC pin.

The maximum switching frequency of each phase is limited by minimum-period timers. If the inductor current decays to zero before the minimum-period timer elapses, the next turn on will be delayed, resulting in discontinuous phase current.

A restart timer ensures starting under all circumstances by restarting both phases if the ZCD input of either phase has not transitioned from high-to-low within approximately 210 µs.

The minimum switching period, $T_{(MIN)}$, is inversely proportional to the time-setting resistor R_{TSET} (the resistor from the TSET pin to ground).

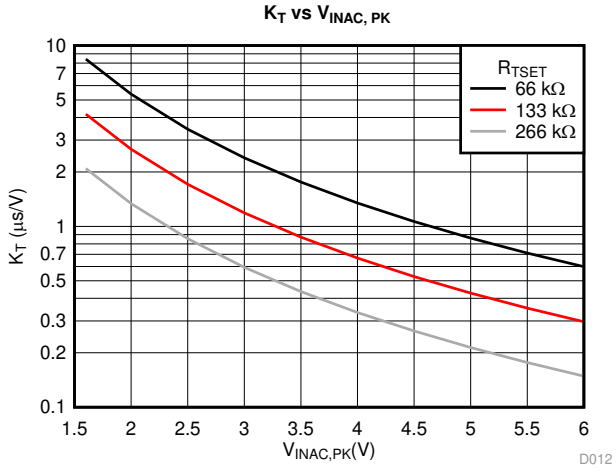


Figure 16. K_T vs Peak Voltage

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Feature Description (continued)

8.3.4 Distortion Reduction

Due to the parasitic resonance between the drain-source capacitance of the switching MOSFET and the boost inductor, conventional transition-mode PFC circuits may not be able to absorb power from the input line when the input voltage is near zero. This limitation increases total harmonic distortion as a result of ac-line current waveform distortion in the form of flat spots. To help reduce line-current distortion, the UCC28064A increases switching MOSFET on-time when the input voltage is near 0 V to improve the power absorption capability and compensate for this effect.

Figure 1 in the *Typical Characteristics* section shows the increase in on-time with respect to VINAC voltage. Excessive filtering of the VINAC signal will nullify this function. In cases where small inductances are used (< 250 µH) the increased MOSFET on time can be excessive, increasing distortion instead of decreasing. If this is the case the external circuit shown in *Figure 17* can help limit this effect.

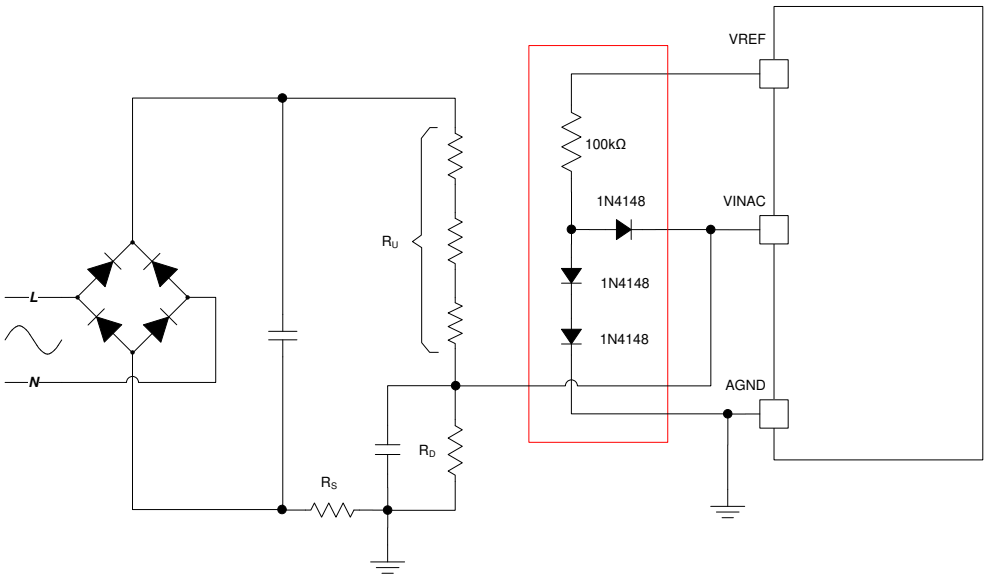


Figure 17. External Circuit to improve THD in case of Low inductance

8.3.5 Zero-Current Detection and Valley Switching

In transition-mode PFC circuits, the MOSFET turns on when the boost inductor current reaches zero. Because of the resonance between the boost inductor and the parasitic capacitance at the MOSFET drain node, part of the energy stored in the MOSFET junction capacitor can be recovered, reducing switching losses. Furthermore, when the rectified input voltage is less than half of the output voltage, all the energy stored in the MOSFET junction capacitor can be recovered and zero-voltage switching (ZVS) can be realized. By adding an appropriate delay, the MOSFET can be turned on at the valley of its resonating drain voltage (valley-switching). In this way, the energy recovery can be maximized and switching loss is minimized.

The optimal time delay is generally derived empirically, but a good starting point is a value equal to 25% of the resonant period of the drain circuit. The delay can be realized by a simple RC filter, as shown in Figure 18, but the delay time increases slightly as the input voltage nears the output voltage. Because the ZCD pin is internally clamped, a more accurate delay can also be realized by using the circuit shown in Figure 19.

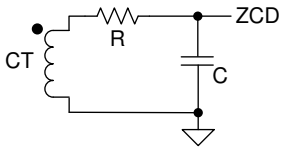


Figure 18. Simple RC Delay Circuit

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Feature Description (continued)

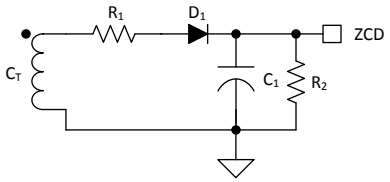


Figure 19. More Accurate Time Delay Circuit

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Feature Description (continued)

8.3.6 Phase Management and Light-Load Operation

It is challenging to maintain high efficiency under all loading conditions. When operating in light-load, switching losses may dominate over conduction losses and the efficiency may be improved if one phase is turned off. Turning off a phase at light load is especially valuable for meeting light-load efficiency standards. This is a major benefit of interleaved PFC and it is especially valuable for meeting 80+ design requirements.

In order to ensure smooth operation when removing or adding a phase, some additional considerations are required. When the number of phases operating is changed from 2 to 1 the overall switching frequency is reduced by a factor of 2. If everything else is held constant this will also reduce the energy delivered to the load by a factor of 2. In order to maintain the same power delivery to the output, it is necessary to increase the on-time when performing such a transition. A similar situation exists when a phase is added. In other words, when going from 1 phase to 2 phases, the on-time should decrease in order to have smooth continuous power delivery. If everything is ideal, the amount by which the system has to increase/decrease the on-time is a factor of 2. Since 1 phase needs to deliver twice the energy as each phase when both phases are operating, doubling the on-time would seem to make the most sense (or cutting it in half if going from 1 phase to 2 phases). While this works well in many cases there are real world examples where this fails to provide a sufficiently smooth phase shedding/adding operation. In order to resolve this conflict the circuit in Figure 20 can be utilized to program a custom on-time for both 1 phase and 2 phase operation. The circuit operates by monitoring the gate drive of phase 2 (GDB). When this signal is active the resistor R_{TSET} configures the on-time. When the gate drive is absent the on-time is configured by the parallel combination of R_{TSET} and R_{TSET_II}. The capacitors C_{FIL} and C_{HOLD} can be adjusted to set up custom delays in the phase shedding/adding process.

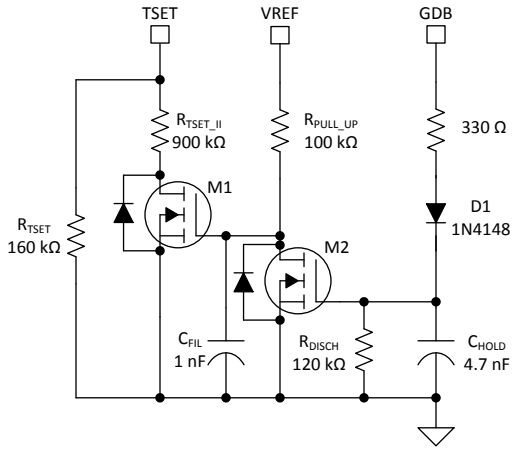


Figure 20. External circuit for Enhanced Phase Shedding

In the case where the 2x factor is sufficient, the UCC28064A can manage this phase shedding/adding process without the need of the circuit in Figure 20.The PHB input can be used to set the load value when the UCC28064A has to operate in single-phase mode. The UCC28064A internally compares the voltage fed to PHB pin with the COMP pin voltage. If COMP is below PHB channel B will stop switching and the channel A on-time will automatically double to compensate the missing power from channel B. When operating in single phase mode in order to avoid risk of inductor saturation an internal clamp ensures the on time never can exceed the maximum on-time you will have when operating in dual phase mode. The device will resume dual-phase mode when the COMP pin voltage exceeds PHB voltage plus the PHB hysteresis. In order to avoid voltage ripple on the COMP pin causing the system to oscillate between one and two phases a time delay filter is present. In order to change from normal operation to single phase mode the COMP voltage should stay below PHB pin voltage for 14 line half cycles. The filter does not apply for the opposite transition. When the COMP pin voltage exceeds PHB pin voltage plus the hysteresis, channel B is immediately turned on and the channel A on-time is halved.

At start up, the output voltage can be very close to the peak line voltage. The inductor current value during the off time will decrease very slowly and it is possible systems will operate in CCM for a few switching cycles. In order to avoid high current, during soft start, the system is forced to work with both phases on even if the COMP pin voltage is below PHB pin voltage. In two phase mode the on-time of each phase is one half of the on time of phase A when Phase B is off so this mitigates the risk of high CCM currents.

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Feature Description (continued)

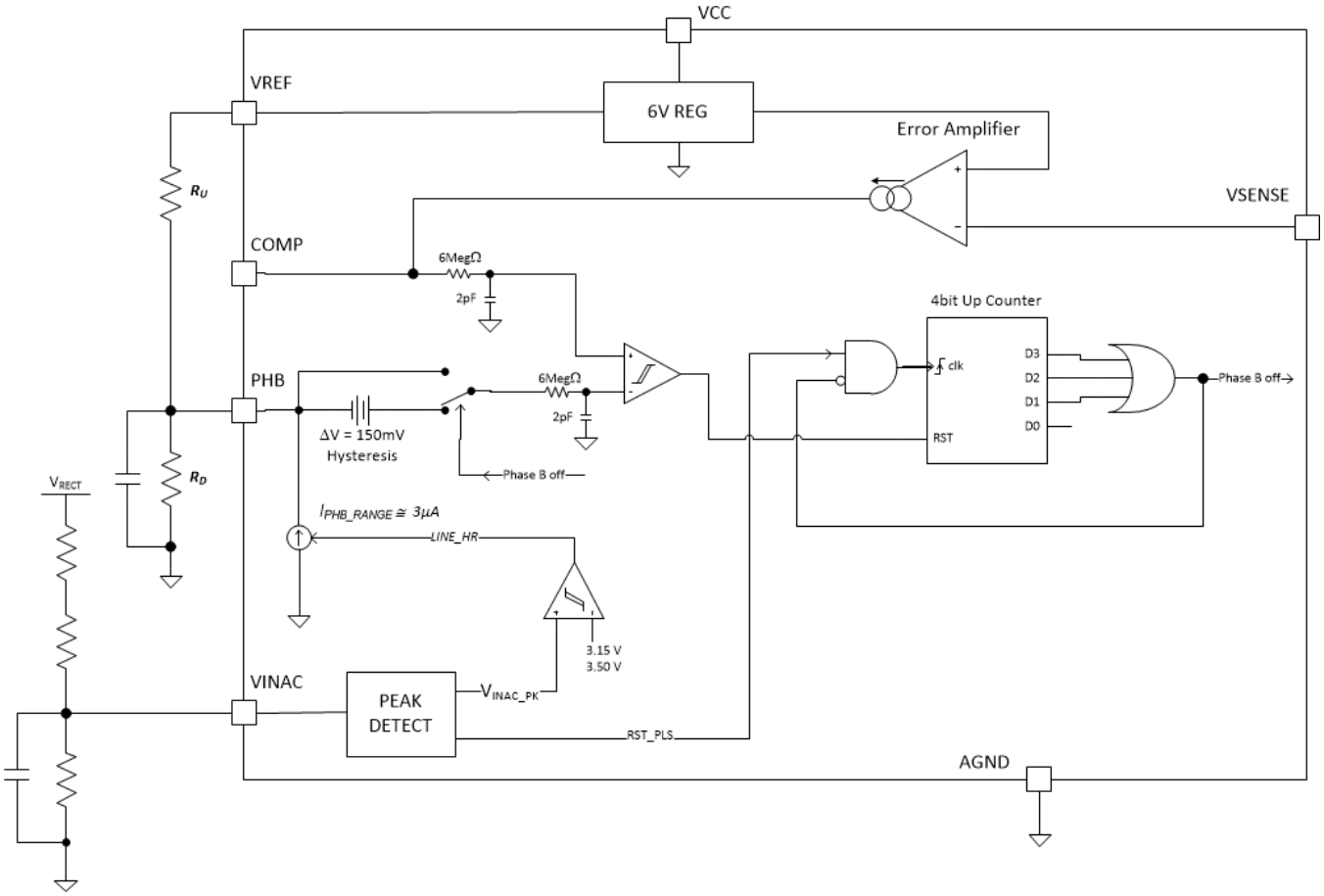


Figure 21. Phase Management Block Diagram

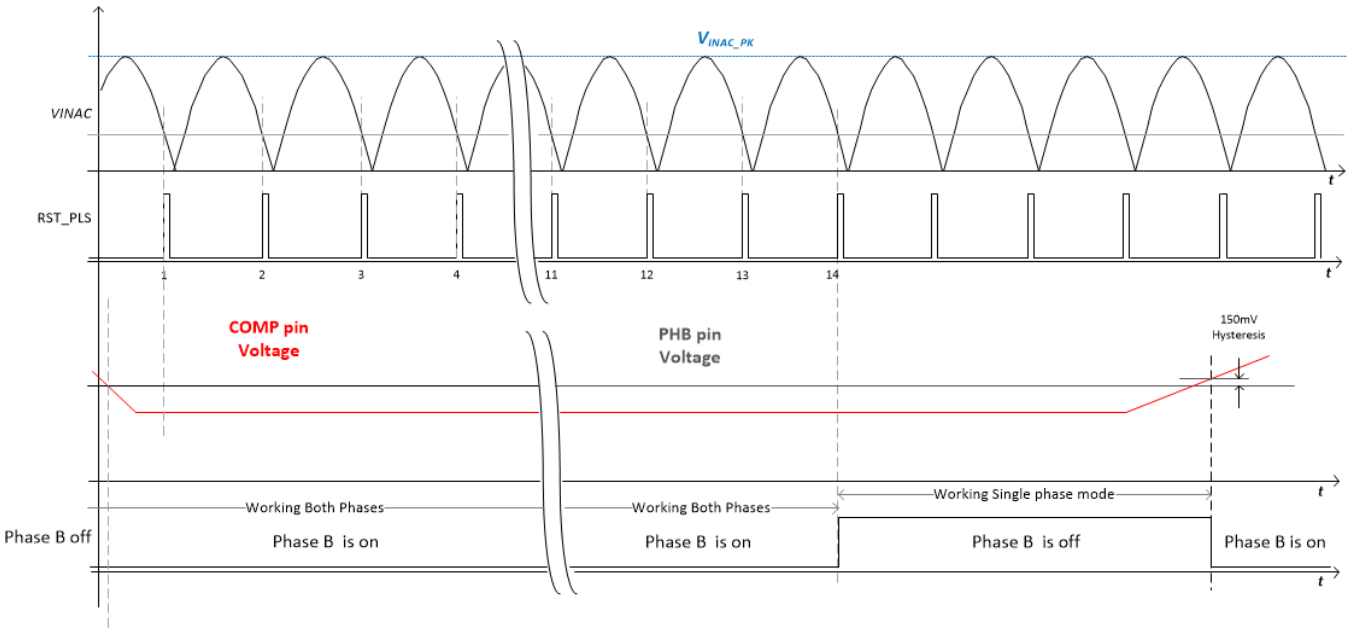


Figure 22. Phase Management Time Diagram

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Feature Description (continued)

The voltage on the PHB pin can be set using a simple resistor divider connected to the V_{REF} pin. Another important feature, that allows optimization of phase management is that it is possible to set different thresholds wether the PFC input voltage is in the range of 90 to 132 V_{RMS} (US mains) or in the range of 180 to 265 V_{RMS} (European mains). If the peak voltage sensed by the V_{INAC} pin exceeds 3.5V the converter assumes that the input voltage is in the range of 180 to 265 V_{RMS} and starts sourcing from PHB a small current (3µA typically) that increases the voltage on PHB pin.

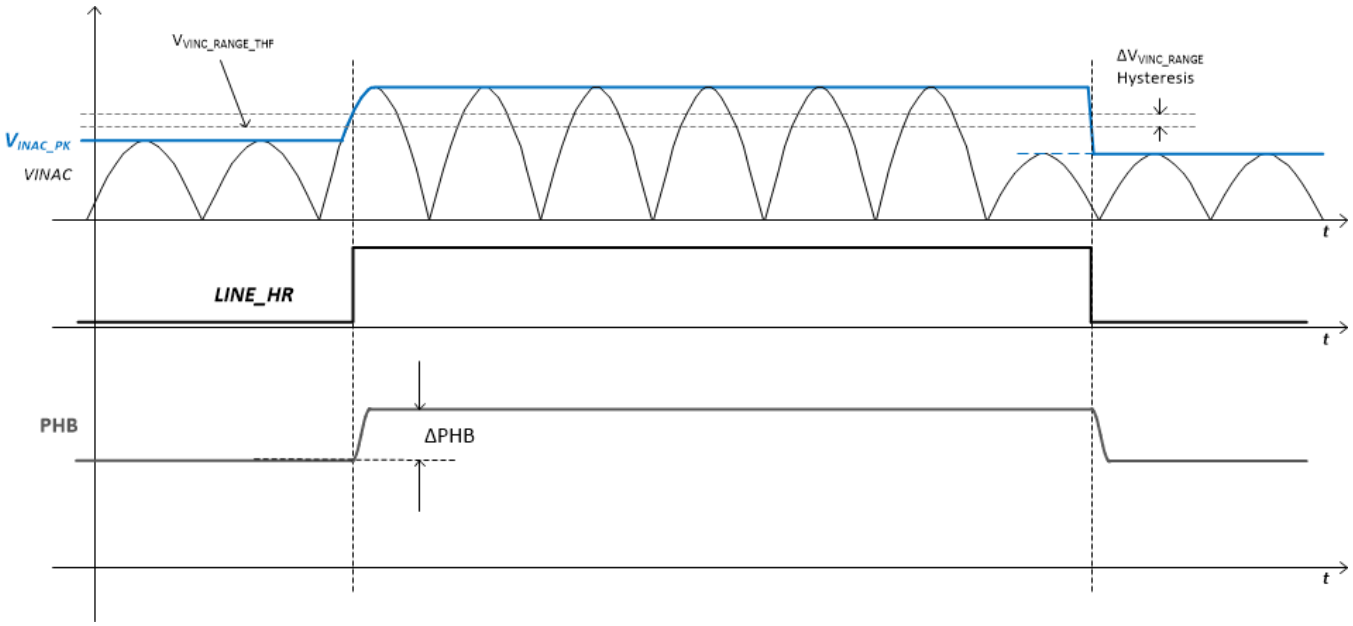


Figure 23. Change Phase Management Thresholds

Use Equation 5 and Equation 6 to calculate PHB thresholds.

$$V_{PHB_LR} = \frac{R_D}{R_U + R_D} \times V_{REF} \tag{5}$$

$$V_{PHB_HR} = \frac{R_D}{R_U + R_D} \times V_{REF} + \frac{R_D \times R_U}{R_U + R_D} \times I_{PHB_RANGE} \tag{6}$$

The load value at which the system moves between single phase and dual phase modes of operation is part of the system specification. The formulas to calculate resistor divider resistance values that allows us to get the desired thresholds are reported below.

$$R_U = \frac{\Delta V_{PHB} \times V_{REF}}{V_{PHB_LR} \times I_{PHB_RANGE}} \tag{7}$$

$$R_D = \frac{\Delta V_{PHB} \times V_{REF}}{(V_{REF} - V_{PHB_LR}) \times I_{PHB_RANGE}}$$

where

Feature Description (continued)

- R_D is the lower resistor of the resistor divider that provides voltage to PHB pin that is supplied by V_{REF}
- R_U is the upper resistor of the resistor divider.

$$\Delta V_{PHB} = V_{PHB_HR} - V_{PHB_LR} \tag{8}$$

(9)

PHB thresholds are selected by the user according to the load value where they want to turn off Phase B. So assuming we want to turn off Phase B when the load goes below P_{OUT_PHB} we can calculate the threshold using equation (10). We can use the same equation in order to calculate the two thresholds V_{PHB_HR} and V_{PHB_LR} once provided the two different load values, for US range and EU range where Phase B has to be turned off. Of course main EU range PHB_OFF load value has to be greater than main US range PHB_OFF load value. A reasonable range of load values is from 20% to 30% of converter rated power.

$$V_{PHB} = \frac{(4.825\ V)}{V_{REF}} \times \frac{P_{OUT\ (PHB)}}{P_{OUT\ (MAX)}} + 125\ mV \tag{10}$$

When the COMP voltage goes below the burst mode threshold the device is forced to work in single phase mode so if the COMP pin voltage drops below the burst threshold it is possible that the time delay filtering is not respected. Moreover it is recommended that PHB pin voltage is at least 600mV higher than BRST pin voltage.

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Feature Description (continued)

8.3.7 Burst Mode Operation

To further improve light load efficiency burst mode operation can be used. In this case the burst mode threshold is fed to BRST pin by an external source that could be a simple resistor divider connected to the V_{REF} pin. If COMP pin voltage goes below the BRST pin voltage the converter stops switching. When the COMP voltage exceeds BRST pin voltage plus hysteresis, the converter restarts switching.

In order to have a smooth transition between switching and not switching and vice-versa burst soft-on and burst soft-off features are added. So when the COMP voltage goes below BRST voltage switching is not stopped immediately, but there will be eight additional switching cycles where FET on time is decreased gradually. In similar way when COMP voltage exceeds BRST voltage plus hysteresis a soft-on period occurs where the on time is increased gradually to a value that corresponds to the present COMP voltage in eight switching cycles.

When the load decreases the device is intended to operate in single phase mode starting from 35% to 15% of rated load and goes to burst mode at lower load values when single phase operation is activated. If the PHB threshold is lower than the Burst mode threshold, single phase operation is forced during soft-on and soft-off periods of burst mode.

Similar to the PHB feature the burst mode threshold has two different levels depending if the PFC input voltage is in the range of 90 to 132 V_{RMS} (US main) or in the range of 180 to 265 V_{RMS} (European main). If the peak voltage on VINAC pin peak voltage exceeds 3.5 V (typ.) a small current (3 µA typically) is provided from BRST pin. If a resistor divider is used to set the BRST pin voltage this current will raise the voltage.

Use Equation 11 and Equation 12 to calculate the resistor divider that sets the Burst Mode thresholds. These equations are identical to the equations used to calculate the PHB resistor divider.

R_U and R_D are the upper and the lower resistence of the resistor divider connected to VREF pin.

$$R_U = \frac{\Delta V_{PHB} \times V_{REF}}{V_{PHB_LR} \times I_{PHB_RANGE}} \tag{11}$$

$$R_D = \frac{\Delta V_{BRST} \times V_{REF}}{(V_{REF} - V_{BRST\ (LR)}) \times I_{BRST\ (RANGE\ )}} \tag{12}$$

8.3.8 External Disable

The UCC28064A can be externally disabled by pulling the VSENSE pin to ground with an open-drain or open-collector driver. When disabled, the device supply current drops significantly and COMP is actively pulled low. This disable method forces the device into standby mode and minimizes its power consumption. When VSENSE is released, the device enters soft-start mode.

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Feature Description (continued)

8.3.9 Improved Error Amplifier

The voltage error amplifier is a transconductance amplifier. Voltage-loop compensation is connected from the error amplifier output, COMP, to analog ground, AGND. The recommended Type-II compensation network is shown in Figure 24. For loop-stability purposes, the compensation network values are calculated based on small-signal perturbations of the output voltage using the nominal transconductance (gain) of 55 µS.

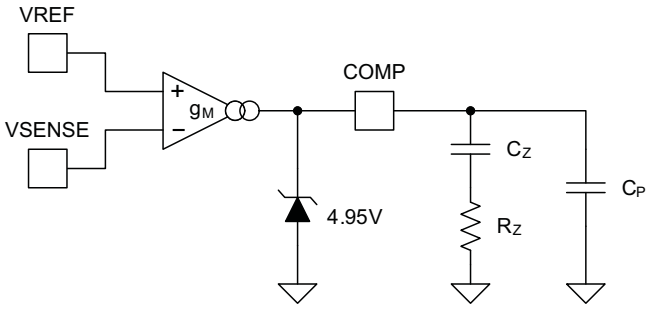
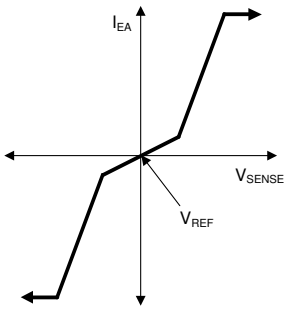


Figure 24. Transconductance Error Amplifier With Typical Compensation Network

To improve the transient response to large perturbations, the error amplifier gain increases by a factor of around 5X when the error amplifier input deviates more than ±5% from the nominal regulation voltage, VSENSEreg. This increase allows faster charging and discharging of the compensation components following sudden load-current increases or decreases.



Basic voltage error amplifier transconductance curve showing small-signal and large-signal gain sections, with maximum current limitations.

Figure 25. Basic Voltage-Error Amplifier Transconductance Curve

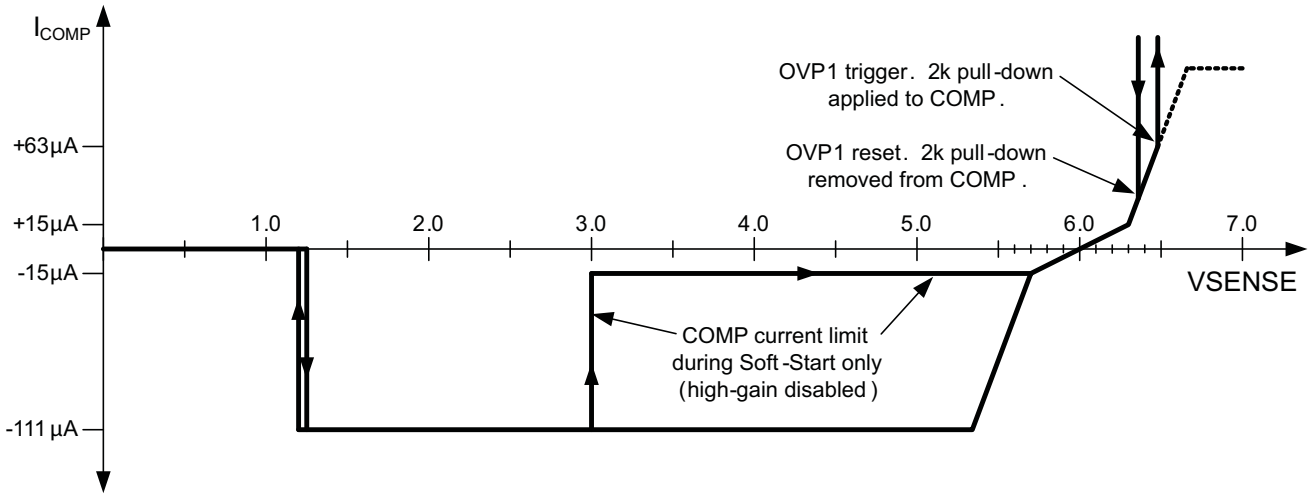
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Feature Description (continued)

8.3.10 Soft Start

Soft-start is a process for boosting the output voltage of the PFC converter from the peak of the ac-line input voltage to the desired regulation voltage under controlled conditions. Instead of a dedicated soft-start pin, the UCC28064A uses the voltage error amplifier as a controlled current source to increase the PWM duty-cycle by way of increasing the COMP voltage. To avoid excessive start-up time-delay when the ac-line voltage is low, a higher current is applied until VSENSE exceeds 3 V at which point the current is reduced to minimize the tendency for excess COMP voltage at no-load start-up.

The PWM gradually ramps from zero on-time to normal on-time as the compensation capacitor from COMP to AGND charges from zero to near its final value. This process implements a soft-start, with timing set by the output current of the error amplifier and the value of the compensation capacitors. Soft-start ends when VSENSE pin voltage exceeds 95% of VSENSEreg. During soft-start the device will operate with both phases on and even if the COMP voltage is below the BRST pin voltage the device will not stop switching. In the event of a HVSEN failsafe OVP, brownout, external-disable, UVLO fault, or other protection faults, COMP is actively discharged and the UCC28064A will soft-start after the triggering event is cleared. Even if a fault event happens very briefly, the fault is latched into the soft-start state and soft-start is delayed until COMP is fully discharged to 20 mV and the fault is cleared. See Figure 26 for details on the COMP current. See Figure 27 which illustrates an example of typical system behavior during soft-start.



Expanded COMP output current curve including voltage error amplifier transconductance and modifications applicable to soft-start and overvoltage conditions.

Figure 26. Expanded COMP pin Output Current Curve

Feature Description (continued)

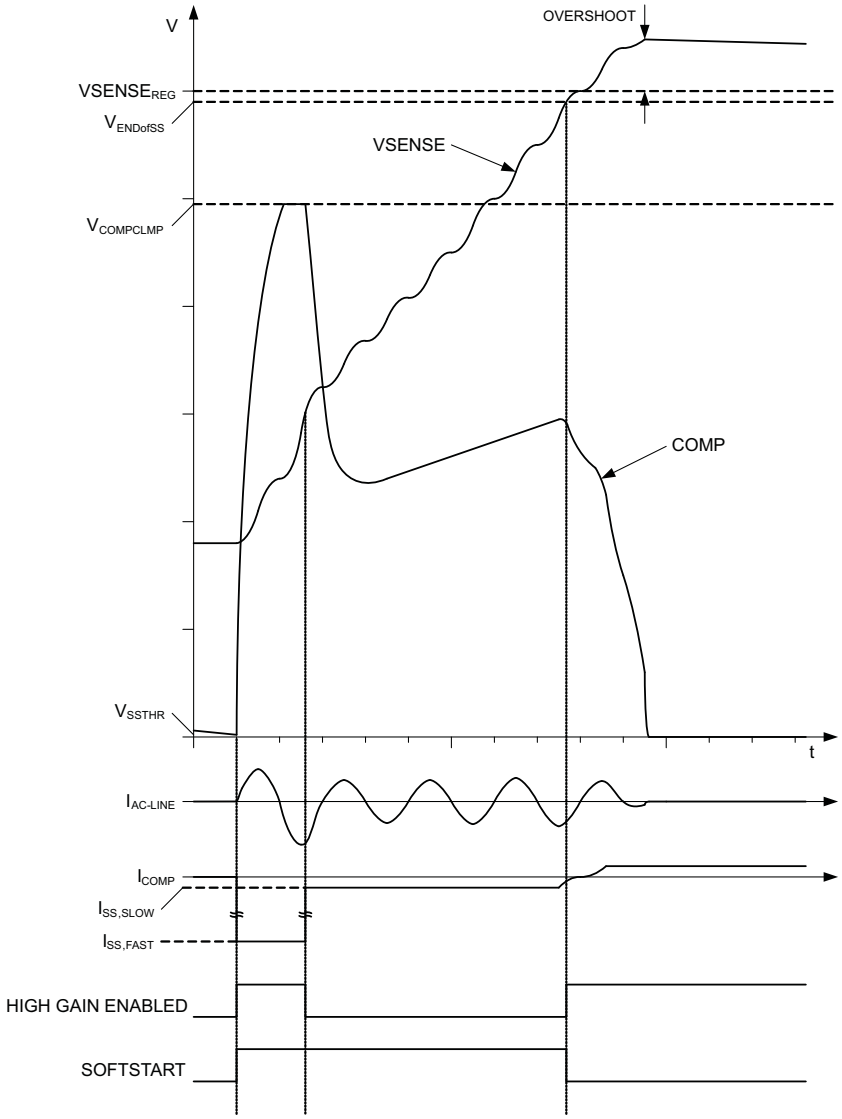


Figure 27. Soft-Start Timing with System Behavior

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Feature Description (continued)

8.3.11 Brownout Protection

As the power line RMS voltage decreases, RMS input current must increase to maintain a constant output voltage for a specific load. Brownout protection helps prevent excess system thermal stress (due to the higher RMS input current) from exceeding a safe operating level. Power-line voltage is sensed at VINAC pin. When the VINAC fails to exceed the brownout threshold for the brownout filter time (t_{BODLY}), a brownout condition is detected and both gate drive outputs are turned off. During brownout, COMP is actively pulled low and soft-start condition is initiated. When VINAC rises above the brownout threshold, the power stage soft-starts as COMP rises with controlled current.

The brownout threshold and its hysteresis are set by the voltage-divider ratio and resistor values. Brownout protection is based on VINAC peak voltage; the threshold and hysteresis are also based on the line peak voltage. Hysteresis is provided by a 2-μA current-sink (I_{BOHYS}) enabled whenever Brownout protection is activated. As soon as the Brownout protection is activated an additional timer is started that counts the t_{BORST} time. During this time the device is forced to stay in a Brownout condition. So, during t_{BORST} time, the device is not allowed to switch, COMP is pulled low and the 2-uA current sink (I_{BOHYS}) is active regardless of the voltage on VINAC pin. After t_{BORST} is elapsed the device can exit from Brownout condition only if VINAC pin exceeds V_{BOTHR} threshold. When the device operates in burst mode, several blocks inside the IC are turned off to reduce IC current consumption. The Brownout management block is also turned off. Each time the system stops switching, because of burst mode, the Brownout filter timer is reset. So if the system is operating in burst mode, the Brownout protection, generally is not triggered. The main purpose of Brownout is to avoid excess system thermal stress. When the system is operating in burst-mode the load is low enough to avoid thermal stress. The peak VINAC voltage can be easily translated into an RMS value. Example resistor values for the voltage divider are 8.61 MΩ ±1% from the rectified input voltage to VINAC and 133 kΩ ±1% from VINAC to ground. These resistors set the typical thresholds for RMS line voltages, as shown in Table 1.

Table 1. Brownout Thresholds (For Conditions Stated in the Text)

THRESHOLD	AC-LINE VOLTAGE (RMS)
Falling	67 V
Rising	81 V

Equation 13 and Equation 14 can be used to calculate the VINAC divider-resistors values based on desired brownout and brown-in voltage levels. V_{AC_OK} is the desired RMS turnon voltage, V_{AC_BO} is the desired RMS turnoff brownout voltage, and V_{LOSS} is total series voltage drop due to wiring, EMI-filter, and bridge-rectifier impedances at V_{AC_BO}. V_{BOTHR}, and I_{BOHYS} are found in the data-tables of this datasheet.

$$R_A = \left[\frac{\sqrt{2} \times \left(V_{AC_{OK}} - V_{AC_{BO}}\right)}{I_{BOHYS}}\right] \quad (13)$$

$$R_B = \frac{R_A}{\left(\frac{\sqrt{2} \times V_{AC_{BO}} - V_{LOSS}}{V_{BOTHR}} - 1\right)} \quad (14)$$

When standard values for the VINAC divider-resistors R_A and R_B are selected, the actual turn-on and brownout threshold RMS voltages for the ac-line can be back-calculated with Equation 15 and Equation 16:

$$V_{AC_{BO}} = \frac{1}{\sqrt{2}} \times \left[\left(1 + \frac{R_A}{R_B}\right) \times V_{BOTHR} + V_{LOSS}\right] \quad (15)$$

$$V_{AC_{OK}} = \frac{1}{\sqrt{2}} \times \left[\frac{R_B + R_A}{R_B} \times V_{BOTHR} + R_A \times I_{BOHYS}\right] \quad (16)$$

An example of the timing for the brownout function is illustrated in Figure 28.

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8.3.12 Line Dropout Detection

It is often the case that the AC-line voltage momentarily drops to zero or nearly zero, due to transient abnormal events affecting the local AC-power distribution network. Referred to as AC-line dropouts (or sometimes as line-dips) the duration of such events usually extends to only 1 or 2 line cycles. During a dropout, the down-stream power conversion stages depend on sufficient energy storage in the PFC output capacitance, which is sized to provide the ride-through energy for a specified hold-up time. Typically while the PFC output voltage is falling, the voltage-loop error amplifier output rises in an attempt to maintain regulation. As a consequence, excess duty-cycle is commanded when the AC-line voltage returns and high peak current surges may saturate the boost inductors with possible overstress and audible noise.

The UCC28064A incorporates a dropout detection feature which suspends the action of the error amplifier for the duration of the dropout. If the VINAC voltage falls below 0.35 V for longer than 5 ms, a dropout condition is detected and the error amplifier output is turned off. In addition, a 4-μA pull down current is applied to COMP to gently discharge the compensation network capacitors. In this way, when the AC-line voltage returns, the COMP voltage (and corresponding duty-cycle setting) remains very near or even slightly below the level it was before the dropout occurred. Current surges due to excess duty-cycle, and their undesired attendant effects, are avoided. The dropout condition is cancelled and the error amplifier resumes normal operation when VINAC rises above 0.71 V.

Based on the VINAC divider-resistor values calculated for Brownout in the previous section, the input RMS voltage thresholds for dropout detection V_{AC_DO} and dropout clearing V_{DO_CLR} can be determined using Equation 17 and Equation 18, below.

$$V_{AC_DO} = \frac{V_{DODET}\left(\frac{R_A}{R_B} + 1\right) + V_{LOSS}}{\sqrt{2}} \quad (17)$$

$$V_{DO_CLR} = \frac{V_{DOCLR}\left(\frac{R_A}{R_B} + 1\right) + V_{LOSS}}{\sqrt{2}} \quad (18)$$

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Avoid excessive filtering of the VINAC signal, or dropout detection may be delayed or defeated. An RC time-constant of ≤ 100 s. should provide good performance. Figure 29 shows an example of the timing for the dropout function.

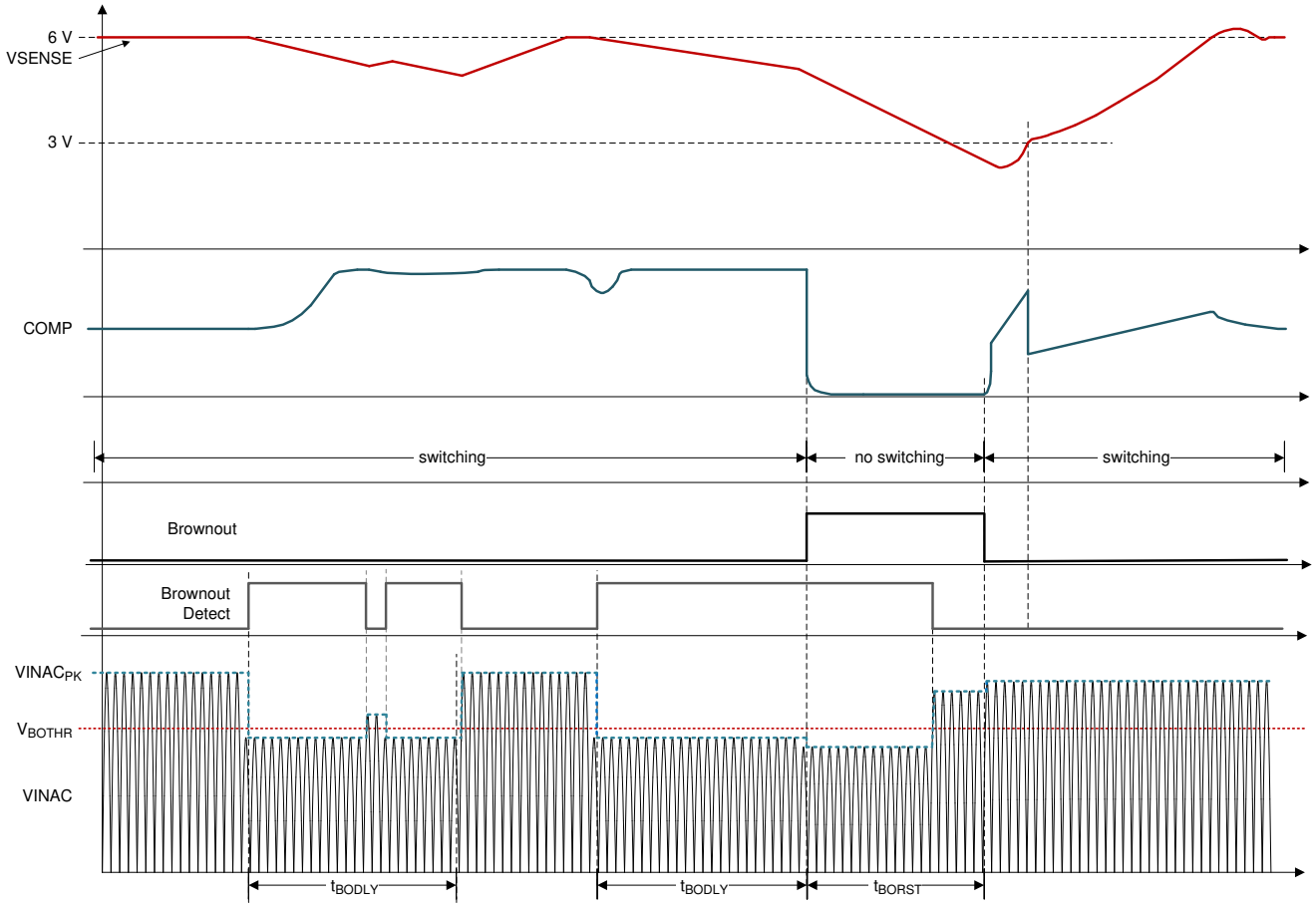


Figure 28. AC-Line Brownout Timing and System Behavior

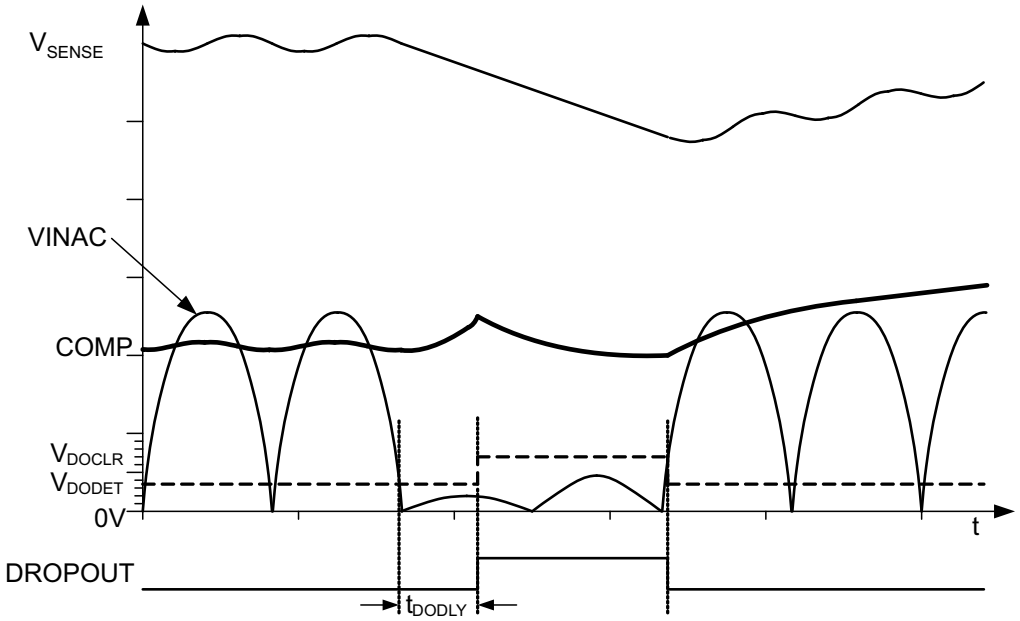


Figure 29. AC-Line Dropout Timing With Illustrative System Behavior

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8.3.13 VREF

VREF is an output which supplies a well-regulated reference voltage to circuits within the device as well as serving as a limited source for external circuits. This output must be bypassed to GND with a low-impedance 0.1-μF or larger capacitor placed as close to the VREF and GND pins as possible. Current draw by external circuits should not exceed 2mA and should not be pulsing.

The VREF output is disabled under the following conditions: when VCC is in UVLO, or when VSENSE is below the Enable threshold. This output can only source current and is unable to accept current into the pin.

8.3.14 VCC

VCC is usually connected to a bias supply of between 14 V and 21 V. To minimize switching ripple voltage on VCC, it should be bypassed with a low-impedance capacitor as close to the VCC and GND pins as possible. The capacitance should be sized to adequately decouple the peak currents due to gate-drive switching at the highest operating frequency. When powered from a poorly-regulated low-impedance supply, an external zener diode is recommended to prevent excessive current into VCC.

The undervoltage-lockout (UVLO) condition is when VCC voltage has not yet reached the turn-on threshold or has fallen below the turn-off threshold, having already been turned on. While in UVLO, the VREF output and most circuits within the device are disabled and VCC current falls significantly below the normal operating level. The same situation applies when VSENSE is below its Enable threshold. This helps minimize power loss during pre-power up and standby conditions.

8.3.15 System Level Protections

8.3.15.1 Failsafe OVP - Output Over-voltage Protection

Failsafe OVP prevents any single failure from allowing the output to boost above safe levels. Redundant paths for output voltage sensing provide additional protection against output over-voltage. Over-voltage protection is implemented through two independent paths: VSENSE and HVSEN.

VSENSE pin voltage is compared with two levels of over-voltage. If the lower one, V_{LOW_OV},is exceeded the COMP pin is discharged by an internal 2-kΩ resistance until the output voltage falls below V_{LOW_OV} reduced of 2% to provide hysteresis ($\Delta V_{LOW_OV_HYST}$). If also the higher over-voltage threshold is exceeded in addition to activate the 2-kΩ pull down switching is soon disabled. In order to re-enable the switching the sensed voltage has to fall below V_{LOW_OV} reduced of 2%. Additional over-voltage protection can be implemented on HVSEN pin through a separate resistor divider to monitor output voltage. An over-voltage is detected if HVSEN pin voltage exceeds $V_{HV_OV_FLT}$ an as consequence device stops switching and the 2-kΩ pull down is activated. The pull down 2-kΩ pull down is removed only if HVSEN pin goes below $V_{HV_OV_CLR}$ threshold and the COMP pin is fully discharged to 20 mV. Both conditions needs to be true before the soft-start can begin.

The converter shuts down if either input senses a severe over-voltage condition. The output voltage can still remain below a safe limit if either sense path fails. The device is re-enabled when both sense inputs fall back into their normal ranges. At that time, the gate drive outputs will resume switching under PWM control. A low-level over-voltage on VSENSE does not trigger soft-start, an higher-level over voltage on VSENSE additionally shuts off the gate-drive outputs until the OV clears, but still does not trigger a soft-start. However, an over-voltage detected on HVSEN does trigger a full soft-start and the COMP pin is fully discharged to 20 mV before the soft-start can begin.

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8.3.15.2 Overcurrent Protection

Under certain conditions (such as inrush, brownout-recovery, and output over-load) the PFC power stage sees large currents. It is critical that the power devices be protected from switching during these conditions.

The conventional current-sensing method uses a shunt resistor in series with each MOSFET source leg to sense the converter currents, resulting in multiple ground points and high power dissipation. Furthermore, since no current information is available when the MOSFETs are off, the source-resistor current-sensing method results in repeated turn-on of the MOSFETs during overcurrent (OC) conditions. Consequently, the converter may temporarily operate in continuous conduction mode (CCM) and may experience failures induced by excessive reverse-recovery currents in the boost diodes or other abnormal stresses.

The UCC28064A uses a single resistor to continuously sense the combined total inductor (input) current. This way, turn-on of the MOSFETs is completely avoided when the inductor currents are excessive. The gate drive to the MOSFETs is inhibited until total inductor current drops to near zero, precluding reverse-recovery-induced failures (these failures are most likely to occur when the AC-line recovers from a brownout condition).

The nominal OC threshold voltage during two-phase operation is -200 mV, which helps minimize losses. This threshold is automatically reduced to -166 mV during single-phase operation, either by detection of a phase failure or because COMP is below PHB.

An OC condition immediately turns off both gate-drive outputs, but does not trigger a soft-start and does not modify the error amplifier operation. The overcurrent condition is cleared when the total inductor current-sense voltage falls below the OC-clear threshold (–15 mV).

Following an overcurrent condition, both MOSFETs are turned on simultaneously once the input current drops to near zero. Because the two phase currents are temporarily operating in-phase, the current-sense resistance should be chosen so that OC protection is not triggered with twice the maximum current peak value of either phase to allow quick return to normal operation after an overcurrent event. Automatic phase-shift control will re-establish interleaving within a few switching cycles.

8.3.15.3 Open-Loop Protection

If the feedback loop is disconnected from the device, a 100-nA current source internal to the UCC28064A pulls the VSENSE pin voltage towards ground. When VSENSE falls below 1.20 V, the device becomes disabled. When disabled, the bias supply current decreases, both gate-drive outputs and COMP are actively pulled low, and a soft-start condition is initiated. The device is re-enabled when VSENSE rises above 1.25 V. At that time, the gate drive outputs will begin switching under soft-start PWM control.

If the resistor connected from AGND pin and VSENSE pin (Low resistor of the resistor divider used to sense output voltage from VSENSE pin) opens, the VSENSE voltage will be pulled high. When VSENSE rises above the 2nd-level over-voltage protection threshold, both gate drive outputs are shut off and COMP is actively pulled low. The device is re-enabled when VSENSE falls below the OV-clear threshold. The VSENSE input can tolerate a limited amount of current into the device under abnormally high input voltage conditions. Refer to the Absolute Maximum Ratings table near the beginning of this datasheet for details.

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8.3.15.4 VCC Undervoltage Lock-Out (UVLO) Protection

VCC must rise above the turn-on threshold for the controller to begin functioning. If VCC drops below the UVLO threshold during operation, both gate-drive outputs are actively pulled low, COMP is actively pulled low, and a soft-start condition is triggered. VCC must again rise above the turn-on threshold for the PWM function to restart in soft-start mode.

8.3.15.5 Phase-Fail Protection

The UCC28064A detects failure of either of the phases by monitoring the sequence of ZCD pulses. During normal two-phase operation, if one ZCD input remains idle for longer than approximately 400 µs while the other ZCD input switches normally, the over-current threshold is reduced to the value used for single phase operation (V_{CS_SPh}). During normal single-phase operation, phase failure is not monitored. Phase failure is also not monitored when COMP is below approximately 250 mV.

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8.3.15.6 CS - Open, TSET - Open and Short Protection

In the event that CS input becomes open-circuited, the UCC28064A detects this condition and will shutdown the outputs and trigger a full soft start condition. In the event that TSET input becomes either open-circuited or short-circuited to GND, the UCC28064A detects these conditions and will shutdown the outputs and trigger a full-soft-start condition. Normal operation will resume (with a soft start) when the fault clears.

8.3.15.7 Thermal Shutdown Protection

Overloading of the gate-drive outputs, VREF, or both can dissipate excess power within the device which may raise the internal temperature of the circuits beyond a safe level. Even normal power dissipation can generate excess heat if the thermal impedance is too high or the ambient temperature is too high. When the UCC28064A detects an internal over-temperature condition it will shutdown the outputs and trigger a full soft-start condition. When the internal device junction temperature has cooled below the thermal hysteresis temperature, operation will resume under soft-start control.

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8.3.15.8 Fault Logic Diagram

Figure 30 depicts the fault-handling logic involving VSENSE, COMP, and several internal states. It should be noted that recovery from any fault except OC if the soft start is not triggered, will result in single phase soft-on operation (8 switching cycles).

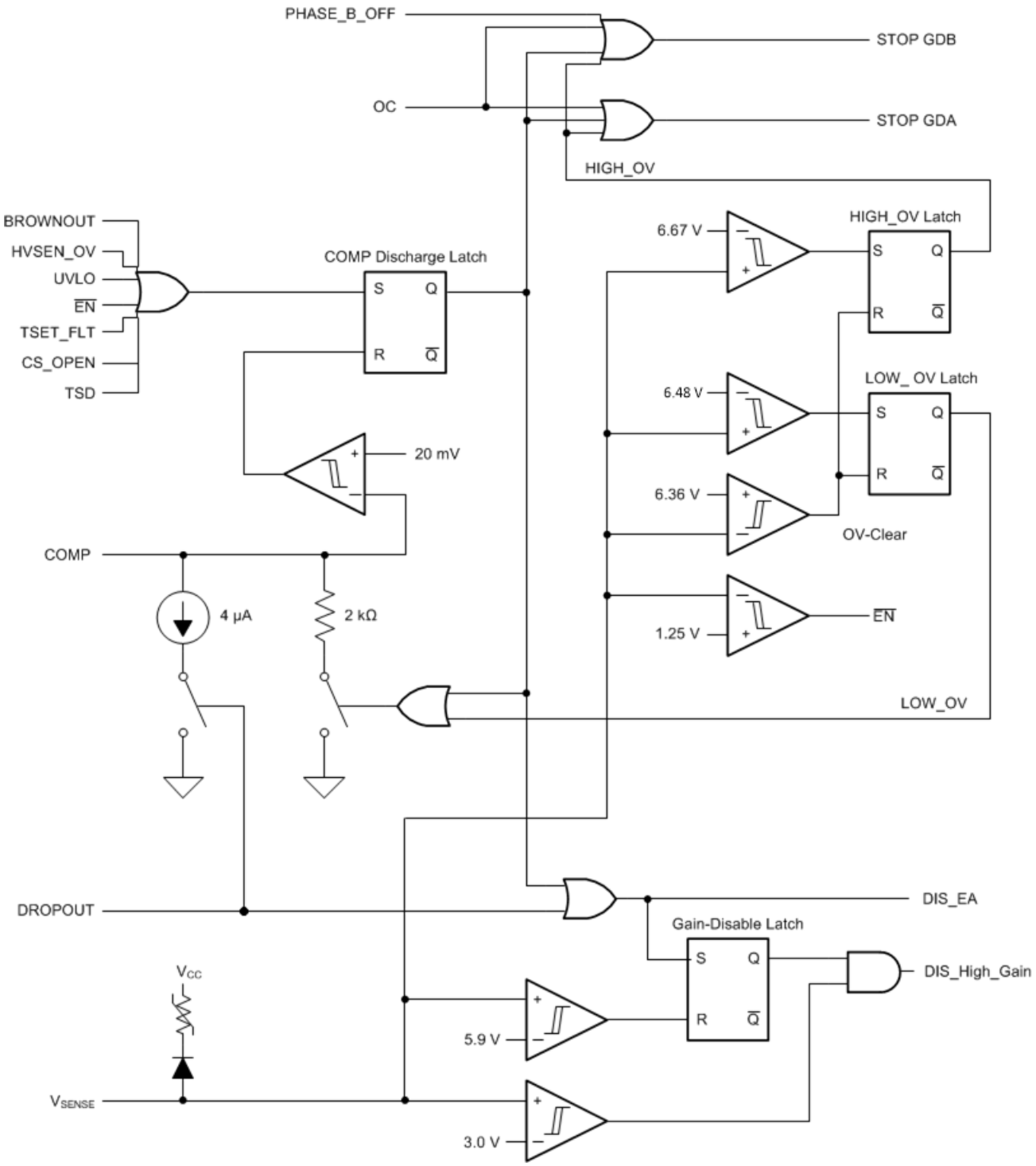


Figure 30. Fault Logic With VSENSE Detections and Error Amplifier Control

8.4 Device Functional Modes

The controller is primarily intended for set up as a dual phase interleaved PFC which utilizes inductor demagnetization information based on inductor sense winding voltages which are routed to ZCDA and ZCDB to trigger the start of a switching cycle.

The functionality may be extended in a couple of ways:

Phase-B Enable and Disable: When the voltage on COMP is below the voltage on the PHB pin, Phase B and the Phase Fail Detector will be disabled. The on-time for Phase-A will be doubled to compensate the Phase-B missing power. When the voltage on COMP is greater than the PHB pin voltage, two phase mode is enabled. Connect PHB to a resistor divider sourced by VREF to set a threshold for COMP pin and obtain an automatic light load efficiency management feature. Because when PHB voltage is higher then COMP voltage, the on-time is doubled, in order to avoid risk of inductor saturation an internal clamp ensures the on-time never can exceed dual phase mode maximum on-time.

PFC Stage Enable and Disable Control: Controller operation is enabled when VSENSE voltage exceeds the 1.25-V enable threshold. The primary disable method should be by pulling VSENSE low by an open drain or open collector logic output. This will disable the outputs and significantly reduce VCC current. Releasing VSENSE will initiate a soft-start. Avoid any PCB traces which would couple any noise into this node.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This control device is generally applicable to the control of AC-DC power supplies which require Active Power Factor Correction off Universal AC line. Applications using this device generally meet the Class-D equipment input current harmonics standards per EN61000-3-2. This standard applies to equipment with rated Powers higher than 75W. The device brings two phase interleaved control capability to the Transition Mode Boost and hence will be generally a very good choice for cost optimized applications in the 150W to 800W space, or to even lower powers that wish to leverage on the interleaving benefits of reduced filtering component size, lower profile solutions and distributed thermal management.

9.2 Typical Application

Figure 31 shows an example of the UCC28064A PFC controller in a two-phase interleaved, transition-mode PFC pre-regulator.

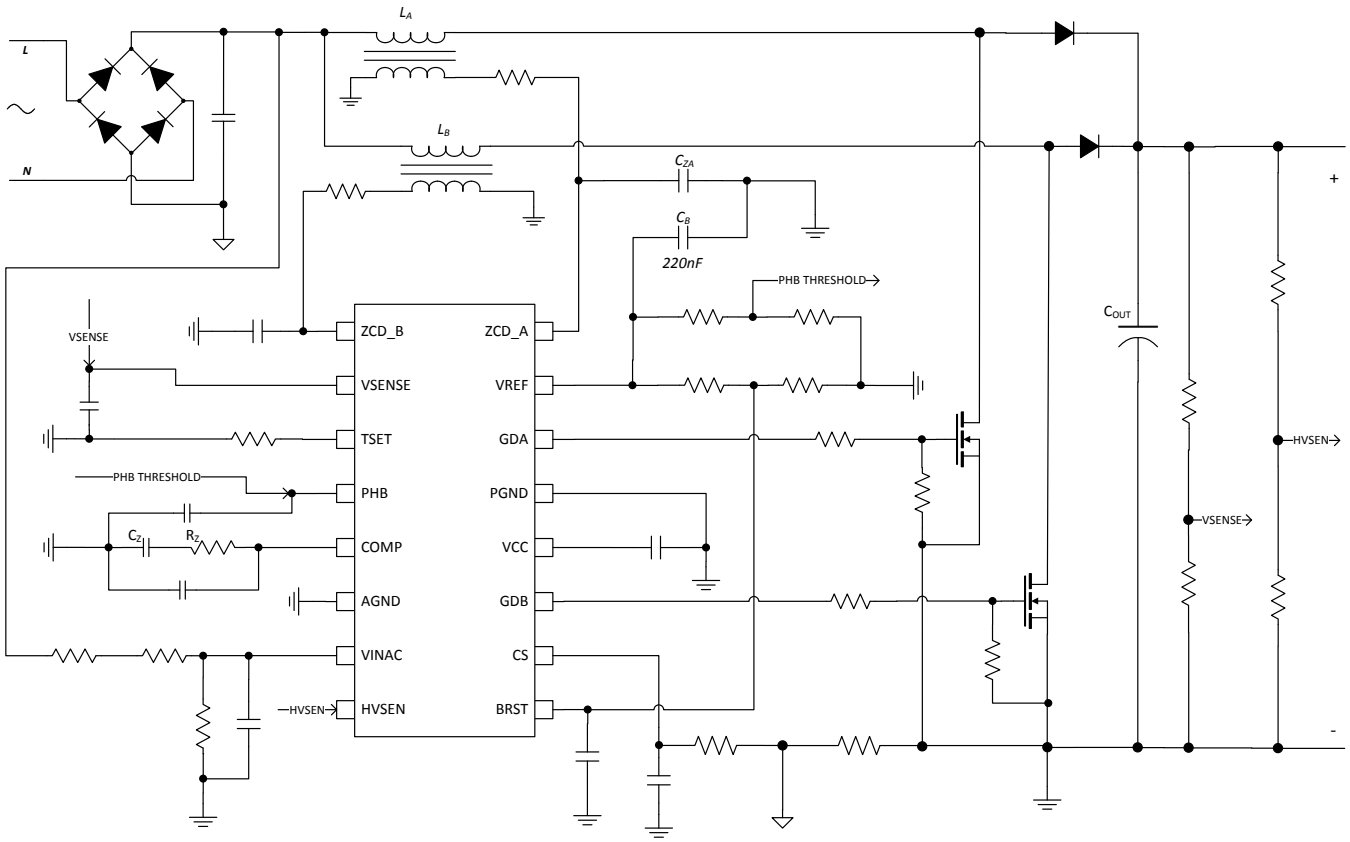


Figure 31. Typical Interleaved Transition-Mode PFC Preregulator

Typical Application (continued)

9.2.1 Design Requirements

The specifications for this design were chosen based on the power requirements of a typical 300-W LCD TV. Table 2 lists these specifications.

Table 2. Design Specifications

DESIGN PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	RMS input voltage	85 (VIN_MIN)		265 (VIN_MAX)	VRMS
V_{OUT}	Output voltage		390		V
f_{LINE}	AC-line frequency	47		63	Hz
PF	Power factor at maximum load	0.90			
P_{OUT}				300	W
η	Full-load efficiency		92%		
f_{MIN}	Minimum switching frequency	45			kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28064A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

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9.2.2.2 Inductor Selection

The boost inductor is selected based on the minimum switching requirements. Operating at the boundary between DCM and CCM the minimum switching frequency will be at maximum power and at the peak of the line. It is possible that the minimum switching frequency can occur at minimum line or at maximum line. Equation 20.

$$L_H = \frac{\eta \times {V_{IN_MAX}}^2 \times (V_{OUT} - \sqrt{2} \times V_{IN_MAX})}{f_{MIN} \times V_{OUT} \times P_{OUT_MAX}} = \frac{0.92 \times (264V)^2 \times (390 - \sqrt{2} \times 264V)}{27kHz \times 390V \times 300W} = 338\mu H \quad (19)$$

$$L_L = \frac{\eta \times {V_{IN_MIN}}^2 \times (V_{OUT} - \sqrt{2} \times V_{IN_MIN})}{f_{MIN} \times V_{OUT} \times P_{OUT_MAX}} = \frac{0.92 \times (85V)^2 \times (390 - \sqrt{2} \times 85V)}{27kHz \times 390V \times 300W} = 568\mu H \quad (20)$$

In order to be sure that converters operates always above the desired (f_{MIN}) we will select the minimum value between L_H that would be the value we have if we consider the minimum occurs at maximum input voltage and L_L that would be the value we have if we consider that minimum switching frequency occurs at minimum Line voltage. For this design example, f_{MIN} is set to 27 kHz in order to be always above the audible range. For a 2-phase interleaved design, L1 and L2 are determined by minimum between L_H and $L_L$as stated in formula (19) here belowEquation 21.

$$L1 = L2 = \min(L_H, L_L) \cong 340\mu H \quad (21)$$

The inductor for this design would have a peak current (I_{LPEAK}) of 5.4 A, as shown in Equation 22, and an RMS current (I_{LRMS}) of 2.2 A, as shown in Equation 23.

$$I_{LPEAK} = \frac{P_{OUT}\sqrt{2}}{V_{IN_MIN} \times \eta} = \frac{300\,W\sqrt{2}}{85\,V \times 0.92} \approx 5.4\,Apk \quad (22)$$

$$I_{LRMS} = \frac{I_{LPEAK}}{\sqrt{6}} = \frac{5.4\,A}{\sqrt{6}} \approx 2.2\,Arms \quad (23)$$

This converter uses constant on time (T_{ON}) and zero-current detection (ZCD) to set up the converter timing. Auxiliary windings on L1 and L2 detect when the inductor currents are zero. Selecting the turns ratio using Equation 24 ensures that there will be at least 2 V at the peak of high line to reset the ZCD comparator after every switching cycle.

The turns-ratio of each auxiliary winding is:

$$\frac{N_P}{N_s} = \frac{V_{OUT} - V_{IN_MAX}\sqrt{2}}{2\,V} = \frac{390\,V - 265\,V\sqrt{2}}{2\,V} \approx 8 \quad (24)$$

9.2.2.3 ZCD Resistor Selection R_{ZA}, R_{ZB}

The minimum value of the ZCD resistors is selected based on the internal clamps maximum current ratings of 3 mA, as shown in Equation 25.

$$R_{ZA} = R_{ZB} \geq \frac{V_{OUT}N_S}{N_P \times 3\,mA} = \frac{390\,V}{8 \times 3\,mA} \approx 16.3\,k\Omega \quad (25)$$

In this design the ZCD resistors are set to 20 kΩ, as shown in Equation 26.

$$R_{ZA} = R_{ZB} = 20\,k\Omega \quad (26)$$

9.2.2.4 HVSEN

According to R_E and R_F resistor values, the Failsafe OVP threshold will be set according to Equation 27

$$V_{OV_FAILSAFE} = \frac{4.87\,V\,(R_E + R_F)}{R_F} = \frac{4.87\,V\,(8.22M\Omega + 82.5k\Omega)}{82.5k\Omega} \approx 490\,V \quad (27)$$

9.2.2.5 Output Capacitor Selection

The output capacitor (C_{OUT}) is selected based on holdup requirements, as shown in Equation 28.

$$C_{OUT} \geq \frac{2\frac{P_{OUT}}{\eta}\frac{1}{f_{LINE}}}{V_{OUT}^{2} - (V_{OUT_MIN})^{2}} = \frac{2\frac{300\,W}{0.92}\frac{1}{47\,Hz}}{390\,V^{2} - (252\,V)^{2}} \approx 156\,\mu F \tag{28}$$

Two 100-µF capacitors were used in parallel for the output capacitor.

$$C_{OUT} = 200\,\mu F \tag{29}$$

For this size capacitor, the low-frequency peak-to-peak output voltage ripple (V_{RIPPLE}) is approximately 14 V, as shown in Equation 30:

$$V_{RIPPLE} = \frac{2 \times P_{OUT}}{\eta}\frac{1}{V_{OUT} \times 4\pi \times f_{LINE} \times C_{OUT}} = \frac{2 \times 300\,W}{0.92 \times 390\,V \times 4\pi \times 47\,Hz \times 200\,\mu F} \approx 14\,Vpk \tag{30}$$

In addition to holdup requirements, a capacitor must be selected so that it can withstand the low-frequency RMS current (I_{COUT_100Hz}) and the high-frequency RMS current (I_{COUT_HF}); see Equation 31 to Equation 33. High-voltage electrolytic capacitors generally have both a low- and a high-frequency RMS current ratings on the product data sheets.

$$I_{COUT_100Hz} = \frac{P_{OUT}}{V_{OUT} \times \eta \times \sqrt{2}} = \frac{300\,W}{390\,V \times 0.92 \times \sqrt{2}} = 0.591\ Arms \tag{31}$$

$$I_{COUT_HF} = \sqrt{\left(\frac{P_{OUT}\,2\sqrt{2}}{2 \times \eta \times V_{IN_MIN}}\sqrt{\frac{4\sqrt{2}V_{IN_MIN}}{9\pi V_{OUT}}}\right)^{2} - \left(I_{COUT_100Hz}\right)^{2}} \tag{32}$$

$$I_{COUT_HF} = \sqrt{\left(\frac{300\,W \times 2\sqrt{2}}{2 \times 0.92 \times 85\,V}\sqrt{\frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}}\right)^{2} - (0.591A)^{2}} \approx 0.966\,Arms \tag{33}$$

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9.2.2.6 Selecting R_S For Peak Current Limiting

The UCC28064A peak limit comparator senses the total input current and is used to protect the MOSFETs during inrush and over-load conditions. For reliability, the peak current limit (I_{PEAK}) threshold in this design is set for 120% of the nominal maximum current that will be observed during power up, as shown in Equation 34.

$$I_{PEAK} = \frac{2P_{OUT}\sqrt{2}(1.2)}{\eta \times V_{IN_MIN}} = \frac{2 \times 300\,W\sqrt{2} \times 1.2}{0.92 \times 85\,V} \approx 13\,A \tag{34}$$

A standard 15-mΩ metal-film current-sense resistor will be used for current sensing, as shown in Equation 35. The estimated power loss of the current-sense resistor (P_{RS}) is less than 0.25 W during normal operation, as shown in Figure 8.

$$R_S = \frac{200\,mV}{I_{PEAK}} = \frac{200\,mV}{13\,A} \approx 15\,m\Omega \tag{35}$$

$$P_{RS} = \left(\frac{P_{OUT}}{V_{IN_MIN} \times \eta}\right)^2 R_S = \left(\frac{300\,W}{85\,V \times 0.92}\right)^2 \times 15\,m\Omega \approx 0.22\ W \tag{36}$$

The most critical parameter in selecting a current-sense resistor is the surge rating. The resistor needs to withstand a short-circuit current larger than the current required to open the fuse (F1). I^2t (ampere-squared-seconds) is a measure of thermal energy resulting from current flow required to melt the fuse, where I^2t is equal to RMS current squared times the duration of the current flow in seconds. A 4-A fuse with an I^2t of 14 A^2s was chosen to protect the design from a short-circuit condition. To ensure the current-sense resistor has high-enough surge protection, a 15-mΩ, 500-mW, metal-strip resistor was chosen for the design. The resistor has a 2.5-W surge rating for 5 seconds. This result translates into 833 A^2s and has a high-enough I^2t rating to survive a short-circuit before the fuse opens, as described in Equation 37.

$$I^2t = \frac{2.5\,W}{0.015\,\Omega} \times 5s = 833\,A^2s \tag{37}$$

9.2.2.7 Power Semiconductor Selection (Q1, Q2, D1, D2)

The selection of Q1, Q2, D1, and D2 are based on the power requirements of the design. For an explanation of how to select power semiconductor components for transition-mode PFC preregulators, refer to *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-regulator*.

The MOSFET (Q1, Q2) pulsed-drain maximum current is shown in Equation 38:

$$I_{DM} \geq I_{PEAK} = 13\,A \tag{38}$$

The MOSFET (Q1, Q2) RMS current calculation is shown in Equation 39:

$$I_{DS} = \frac{I_{PEAK}}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}\,V_{IN_MIN}}{9\pi \times V_{OUT}}} = \frac{13\,A}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \approx 2.3\,A \tag{39}$$

To meet the power requirements of the design, IRFB11N50A 500-V MOSFETs were chosen for Q1 and Q2.

The boost diode (D1, D2) RMS current is shown in Equation 40:

$$I_D = \frac{I_{PEAK}}{2}\sqrt{\frac{4\sqrt{2} \times V_{IN_MIN}}{9\pi \times V_{OUT}}} = \frac{13\,A}{2}\sqrt{\frac{4\sqrt{2} \times 85\,V}{9\pi \times 390\,V}} \approx 1.4\,A \tag{40}$$

To meet the power requirements of the design, MURS360T3, 600-V diodes were chosen for D1 and D2.

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9.2.2.8 Brownout Protection

Resistor R_A and R_B are selected to activate brownout protection at ~75% of the specified minimum-operating input voltage. Resistor R_A programs the brownout hysteresis comparator, which is selected to provide 17 V (~12 V_{RMS}) of hysteresis. Calculations for R_A and R_B are shown in Equation 41 through Equation 44.

$$R_A = \frac{\text{Hysteresis}}{2\mu A} = \frac{17\,V}{2\mu A} = 8.5M\Omega \tag{41}$$

To meet voltage requirements, three 2.87-MΩ resistors were used in series for R_A.

$$R_A = 3 \times 2.87M\Omega = 8.61M\Omega \tag{42}$$

$$R_B = \frac{1.4\,V \times R_A}{V_{IN_MIN} \times 0.75\sqrt{2} - 1.4\,V} = \frac{1.4\,V \times 8.61M\Omega}{85\,V \times 0.75\sqrt{2} - 1.4\,V} = 135.8k\Omega \tag{43}$$

Select a standard value for R_B.

$$R_B = 133k\Omega \tag{44}$$

In this design example, brownout becomes active (shuts down PFC) when the input drops below 67 V_{RMS} for longer than 680 ms and deactivates (restarts with a full soft start) if, after that the t_{BORST} time is elapsed, the input reaches 81 V_{RMS}.

9.2.2.9 Converter Timing

The MOSFET on-time T_{ON} depends on value of the selected inductance on load value, represented by COMP pin voltage and by the converter AC input voltage Equation 45. To ensure proper operation, the timing must be set based on the highest boost inductance ($L1_{MAX}$) and output power (P_{OUT}) at minimum operating AC input Voltage. Because the input voltage is sensed by VINAC pin the on time setting needs to take into account of the selected resistor divider that provide voltage at VINAC pin. In this design example, the boost inductor could be as high as 390 µH.

Let's call K_{BO} the ratio:Equation 49.

$$K_{BO} = \frac{R_A + R_B}{R_B} = \frac{8.61M\Omega + 133k\Omega}{133k\Omega} = 65.74 \tag{45}$$

the Maximum on time at full load (P_{OUT} = 300W) and minimum input voltage ($85V_{AC}$) is given by formula;

$$t_{ON_MAX} = \frac{P_{OUT} \times L}{\eta \times \left(V_{IN_MIN}\right)^2} = \frac{(300W) \times (340\mu H)}{0.92 \times (85V)^2} = 15.34\mu s \tag{46}$$

The value of the resistor R_T connected to TSET pin to set the on time timers is the minimum of R_{TH} and R_{TL} provided by formulas (46) and (47)

$$R_T = \min(R_{TL}, R_{TH}) \tag{47}$$

$$R_{TH} = \frac{K_{TH_MIN} \times (5V)^2 \times (133k\Omega) \times (4.825V)}{\left(\frac{\sqrt{2} \times V_{IN_MIN}}{K_{BO}}\right)^2 \times t_{ON_MAX}} \tag{48}$$

$$R_{TL} = \frac{K_{TL_MIN} \times (1.6V)^2 \times (133k\Omega) \times (4.825V)}{\left(\frac{\sqrt{2} \times V_{IN_MIN}}{K_{BO}}\right)^2 \times t_{ON_MAX}} \tag{49}$$

Where the values of K_{TL_min} and K_{TH_min} are the minimum values of K_{TL} and K_{TH} parameters reported on the electrical characteristic table at page 7 of this datasheet.

The selected value for R_T is 115 kΩ.

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9.2.2.10 Programming V_{OUT}

Resistor R_C is selected to minimize loading on the power line when the PFC is disabled. Construct resistor R_C from two or more resistors in series to meet high-voltage requirements. Resistor R_D is then calculated based on R_C, the reference voltage, V_{REF}, and the required output voltage, V_{OUT}. Based on the values shown in Equation 50 to Equation 53, the primary output overvoltage protection threshold should be as shown in Equation 54:

$$R_C = 2.74\,M\Omega + 2.74\,M\Omega + 3.01\,M\Omega = 8.49\,M\Omega \quad (50)$$

$$V_{REF} = 6\ V \quad (51)$$

$$R_D = \frac{V_{REF} \times R_C}{V_{OUT} - V_{REF}} = \frac{6\,V \times 8.49\,M\Omega}{390\,V - 6\,V} = 132.7\,k\Omega \quad (52)$$

Select a standard value for R_D.

$$R_D = 133\,k\Omega \quad (53)$$

$$V_{OVP} = 6.48\,V\frac{R_C + R_D}{R_D} = 6.48\,V\frac{8.49\,M\Omega + 133\,k\Omega}{133\,k\Omega} = 420.1V \quad (54)$$

9.2.2.11 Voltage Loop Compensation

Resistor R_Z is sized to attenuate low-frequency ripple to less than 2% of the voltage amplifier output range. This value ensures good power factor and low harmonic distortion on the input current. The voltage on the COMP pin needs to stay above 250 mV to maintain normal operation. If COMP falls below this threshold switching will stop.

The transconductance amplifier small-signal gain is shown in Equation 55:

$$g_m = 50\,\mu S \quad (55)$$

The voltage-divider feedback gain is shown in Equation 56:

$$H = \frac{V_{REF}}{V_{OUT}} = \frac{6\,V}{390\,V} \approx 0.015 \quad (56)$$

The value of R_Z is calculated as shown in Equation 57:

$$R_Z = \frac{100\,mV}{V_{RIPPLE} \times H \times g_m} = \frac{100\,mV}{14\,V \times 0.015 \times 50\,\mu S} = 9.52\ k\Omega \quad (57)$$

C_Z is then set to add 45° phase margin at 1/5th of the line frequency, as shown in Equation 58:

$$C_Z = \frac{1}{2\pi \times \frac{f_{LINE}}{5} \times R_Z} = \frac{1}{2\pi \times \frac{47\,Hz}{5} \times 9.52\,k\Omega} = 1.78\,\mu F \quad (58)$$

C_P is sized to attenuate high-frequency switching noise, as shown in Equation 59:

$$C_p = \frac{1}{2\pi \times \frac{f_{MIN}}{2} \times R_Z} = \frac{1}{2\pi \times \frac{45\,kHz}{2} \times 9.52\,k\Omega} = 770\,pF \quad (59)$$

Standard values should be chosen for R_Z, C_Z and C_P, as shown in Equation 60 to Equation 62.

$$R_Z = 9.53\,k\Omega \quad (60)$$

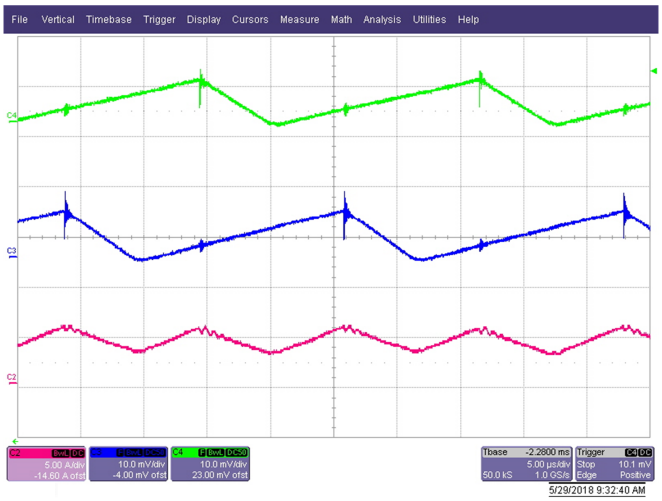
$$C_Z = 2.2\,\mu F \quad (61)$$

$$C_P = 820\,pF \quad (62)$$

9.2.3 Application Curves

9.2.3.1 Input Ripple Current Cancellation with Natural Interleaving

Figure 32 through Figure 34 show the input current (CH2), Inductor Ripple Currents (CH3, CH4) versus rectified line voltage. From these graphs, it can be observed that natural interleaving reduces the overall magnitude of input (and output) ripple current caused by the individual inductor current ripples.

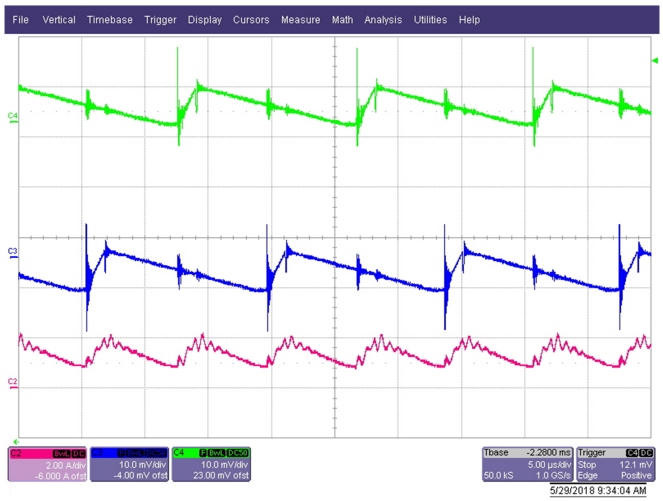


CH2 = Input Current

CH4 = Phase B Inductor Current

CH3 = Phase A Inductor Current

Figure 32. Inductor and Input Ripple Current at 85 V_{RMS} at Peak of Line Voltage

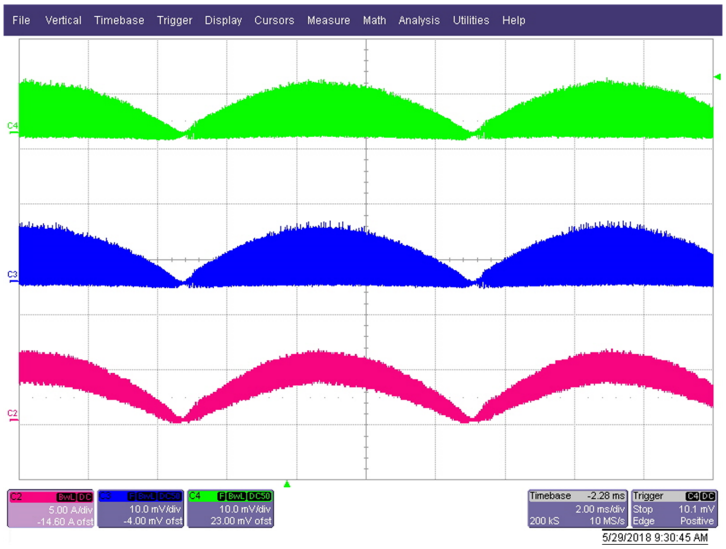


CH2 = Input Current

CH4 = Phase B Inductor Current

CH3 = Phase A Inductor Current

Figure 33. Inductor and Input Ripple Current at 265 V_{RMS} Input at Peak Line Voltage



CH2 = Input Current

CH4 = Phase B Inductor Current

CH3 = Phase A Inductor Current

Figure 34. Inductor and Input Ripple Current at V_{IN} = 85 V_{RMS}, P_{OUT} = 300 W

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9.2.3.2 Brownout Protection

The UCC28064A has a brownout protection that shuts down both gate drives (GDA and GDB) when the VINAC pin detects that the RMS input voltage is too low. Figure 35.



CH1 = V_{GDA} CH2 = V_{GDB}

CH3 = V_{OUT} CH3 = V_{IN}

Figure 35. UCC28064A Response to a Line Brownout Event at 115 V_{RMS}

10 Power Supply Recommendations

The device receives all of its power through the VCC pin. This voltage should be as well regulated as possible through all of the operating conditions of the PFC stage. Consider creating the steady state bias for this stage from a downstream DC:DC stage which will in general be able to provide a bias winding with very well regulated voltage. This strategy will enhance the overall efficiency of the bias generation. A lower efficiency alternative will be to consider a series-connected fixed positive-voltage regulator such as the UA78L15A.

For all normal and abnormal operating conditions it is critically important that VCC remains within the recommended operating range for both Voltage and Input Current. VCC overvoltage may cause excessive power dissipation in the internal voltage clamp and undervoltage may cause inadequate drive levels for power MOSFETs, UVLO events (causing interrupted PFC operation) or inadequate headroom for the various on-chip linear regulators and references.

Note also that the high RMS and peak currents required for the MOSFET gate drives are provided through the device 13.5-V linear regulator, which does not have provision for the addition of external decoupling capacitance. For higher Powers, very high Q_G power MOSFETs or high switching frequencies, consider using external driver transistors, local to the power MOSFETs. These will reduce the device operating temperature and ensure that the VCC maximum input current rating is not exceeded.

Use decoupling capacitances between VREF and AGND and between VCC and PGND which are as local as possible to the device. These should have some ceramic capacitance which will provide very low ESR. PGND and AGND should ideally be star connected at the control device so that there is negligible DC or high frequency AC voltage difference between PGND and AGND. Use values for decoupling capacitors similar to or a little larger than those used in the EVM.

Pay close attention to start-up and shutdown VCC bias bootstrap arrangements so that these provide adequate regulated bias power as early as possible during power application and as late as possible during power removal. Ensure that these start-up bias bootstrap circuits do not cause unnecessary steady-state power drain.

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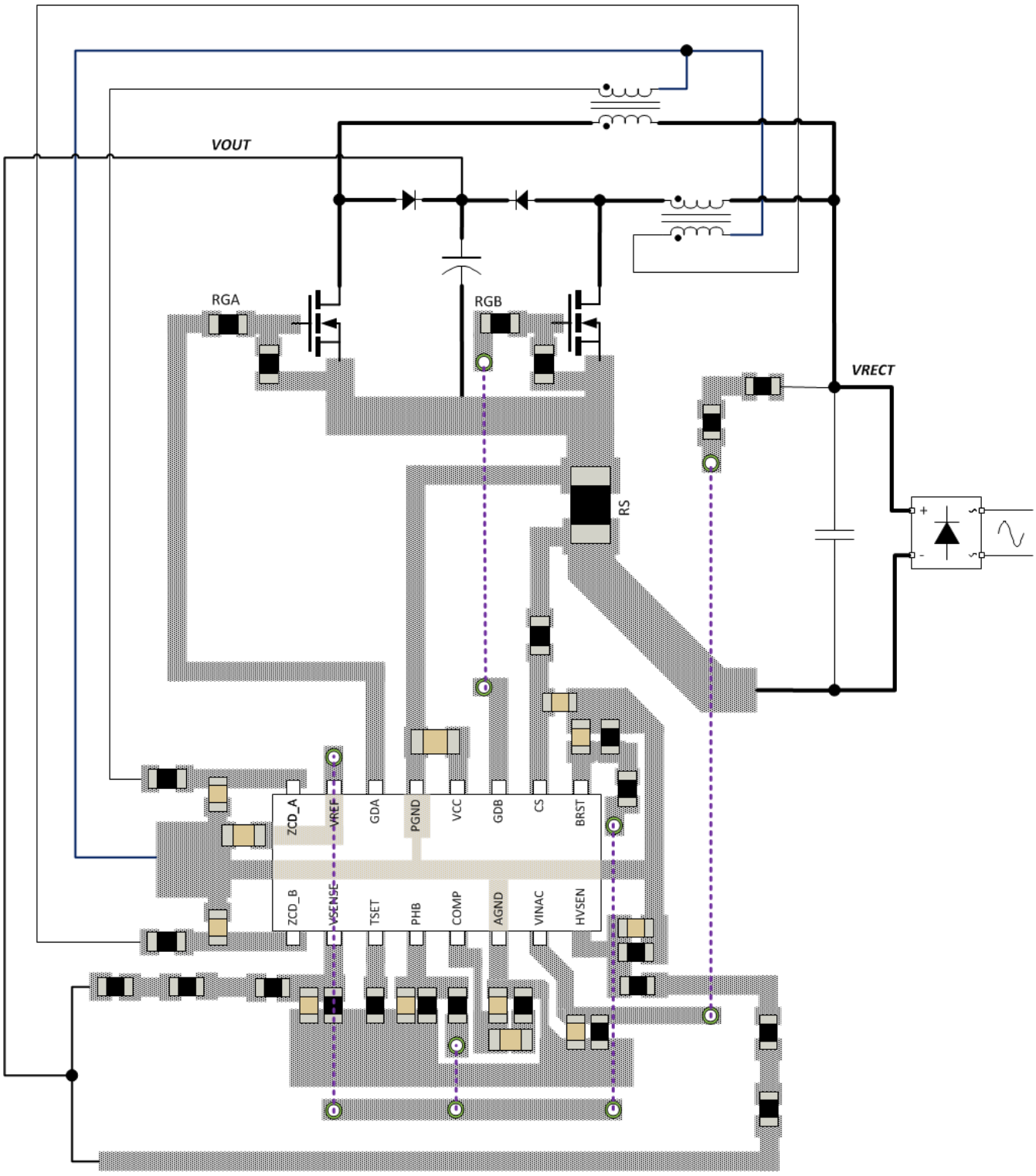
11 Layout

11.1 Layout Guidelines

Interleaved transition-mode PFC system architecture dramatically reduces input and output ripple current, allowing the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the input and output filter capacitors should be located after the two phase currents are combined together. Similar to other power management devices, when laying out the printed circuit board (PCB) it is important to use star grounding techniques and keep filter capacitors as close to device ground as possible. To minimize the interference caused by capacitive coupling from the boost inductor, the device should be located at least 1 in (25.4 mm) away from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements. Because of the precise timing requirement, timing-setting resistor R_T should be placed as close as possible to the TSET pin and returned to the analog ground pin with the shortest possible path. Figure 36 shows a recommended component placement and layout.

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11.2 Layout Example



Dotted line could be or a wire mounted on the top of the board or Top layer traces, assuming device and other traces are in the bottom layer.

Figure 36. Recommended PCB Layout

11.3 Package Option Addendum

11.3.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Qty	Eco Plan (2)	Lead/Ball Finish(3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking(5)(6)
UCC28064ADT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28064A
UCC28064ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28064A

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCC28064 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *UCC28064AEVM 300W Interleaved PFC Pre-regulator*
- *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-regulator*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28064ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28064A
UCC28064ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28064A
UCC28064ADR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28064A
UCC28064ADT	Active	Production	SOIC (D) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28064A
UCC28064ADT.A	Active	Production	SOIC (D) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28064A
UCC28064ADT.B	Active	Production	SOIC (D) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UCC28064A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

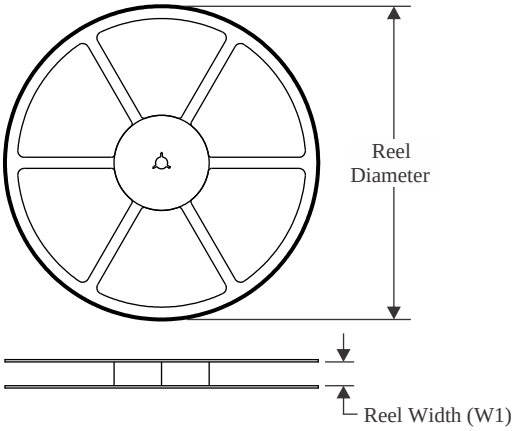
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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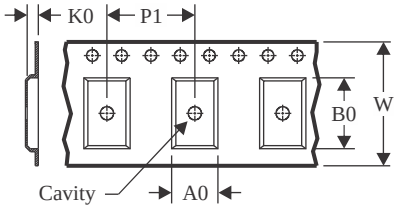
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

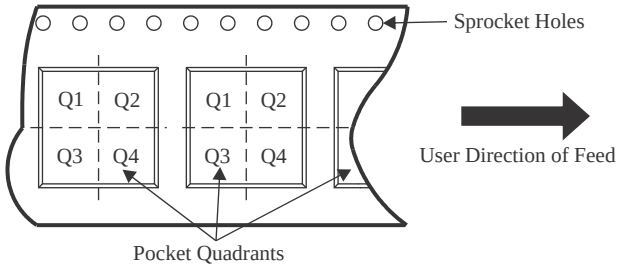


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

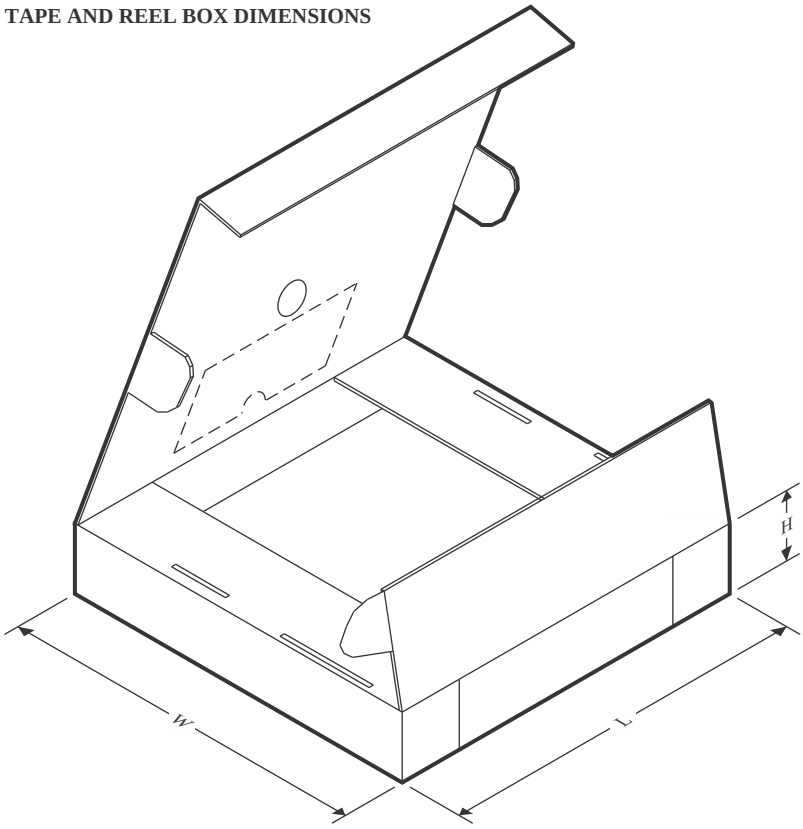
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28064ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC28064ADT	SOIC	D	16	250	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

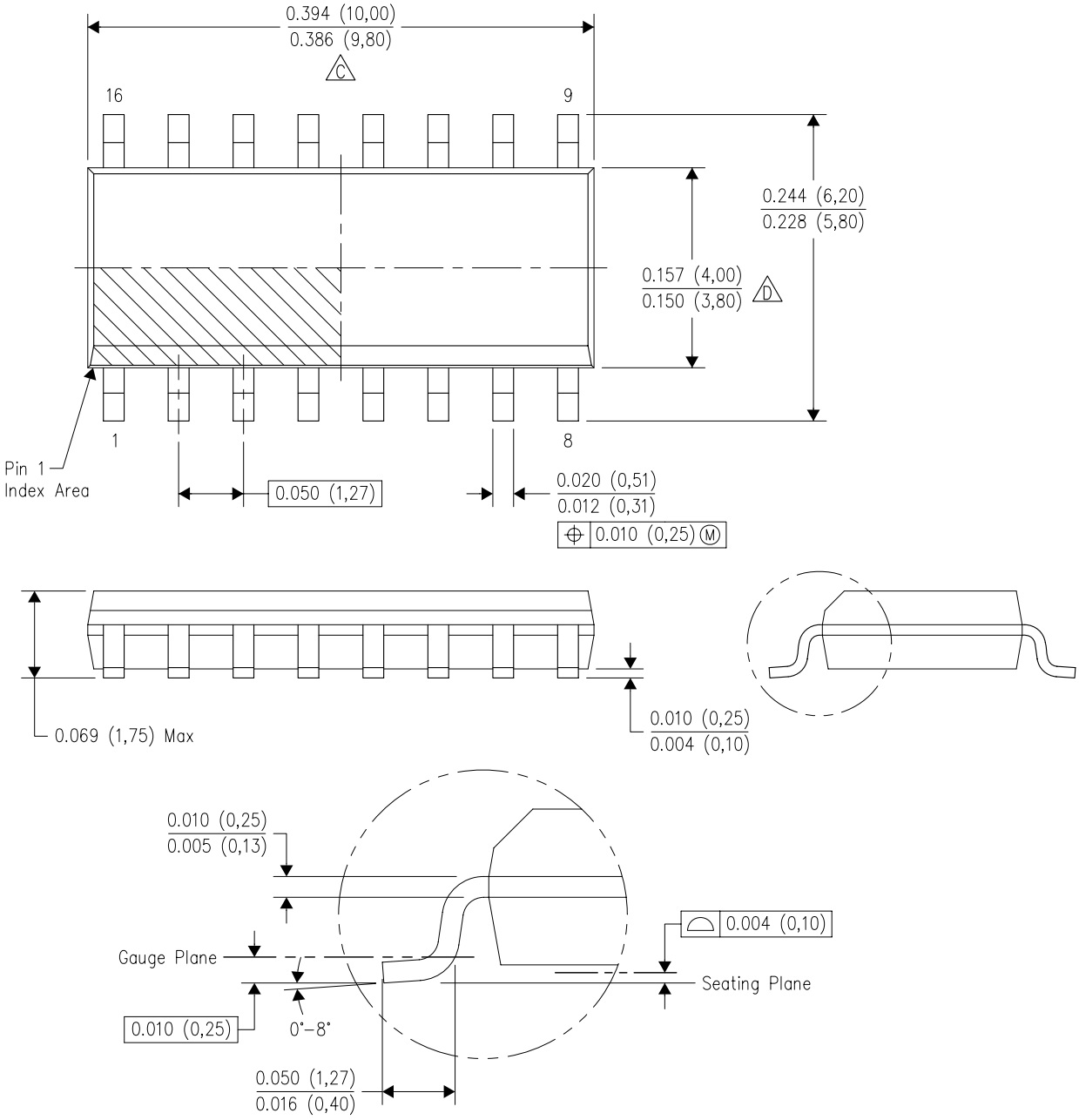
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28064ADR	SOIC	D	16	2500	353.0	353.0	32.0
UCC28064ADT	SOIC	D	16	250	340.5	336.1	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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