UCCx808A Low-Power Current-Mode Push-Pull PWM

1 Features

- Dual-output drive stages in push-pull configuration
- Current-sense discharge transistor to improve dynamic response
- 130µA typical starting current
- 1mA typical run current
- Operation to 1MHz
- Internal soft start
- On-chip error amplifier with 2MHz gain bandwidth product
- On-chip VDD clamping
- Output drive stages capable of 500mA peak source current, 1A peak sink current

2 Applications

- High-efficiency switch-mode power supplies
- Telecom DC/DC converters
- Point-of-load power modules
- Low-cost push-pull and half-bridge applications

3 Description

The UCCx808A devices are a family of BiCMOS push-pull, high-speed, low-power, pulse-width modulators. The UCCx808A contain all of the control and drive circuitry required for off-line or DC-to-DC fixed frequency current-mode switching power supplies with minimal external parts count.

The UCCx808A dual-output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60ns to 200ns depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

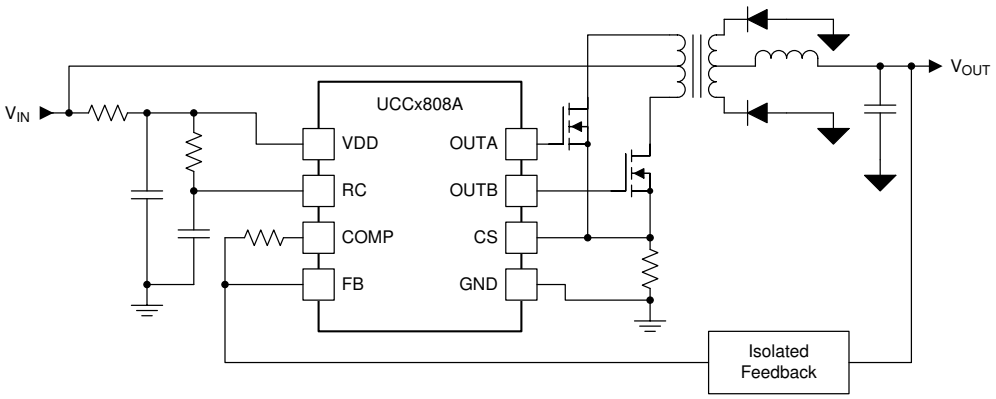
The UCCx808A family offers a variety of package options, temperature range options, and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for offline and battery-powered systems.

The UCCx808A are an enhanced version of the UCC3808 family. The significant difference is that the A versions feature an internal discharge transistor from the CS pin to ground, which is activated each clock cycle during the oscillator dead time. The feature discharges any filter capacitance on the CS pin during each cycle, and helps minimize filter capacitor values and current sense delay.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCC2808A-1, UCC2808A-2, UCC3808A-2	D (SOIC. 8)	4.9mm × 6mm
	PW (TSSOP, 8)	3mm × 6.4mm
UCC3808A-1	D (SOIC, 8)	4.9mm × 6mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

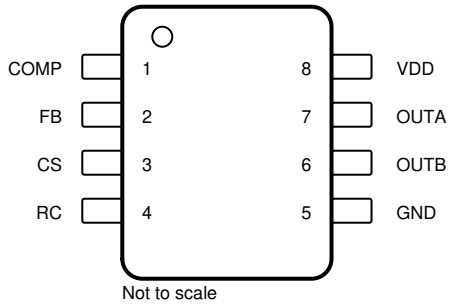


Figure 4-1. UCCx808A: D Package, 8-Pin SOIC (Top View)

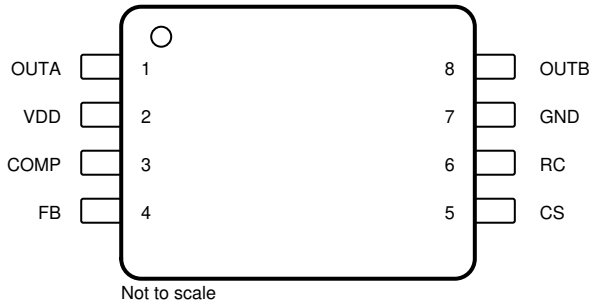


Figure 4-2. UCC2808A-x, UCC3808A-2: PW Package, 8-Pin TSSOP (Top View)

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	D (SOIC)	PW (TSSOP)		
COMP	1	3	O	COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCCx808A is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin both sources and sinks current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND. The UCCx808A family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.
CS	3	5	I	The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.
FB	2	4	I	The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.
GND	5	7	G	Reference ground and power ground for all functions. Because of high currents, and high-frequency operation of the UCC3808A, a low-impedance circuit board ground plane is highly recommended.
OUTA	7	1	O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current. The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This *dead time* between the two outputs, along with a slower output rise time than fall time, prevents the two outputs from simultaneous activity. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor. The high-current-output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This configuration means that in many cases, external Schottky-clamp diodes are not required.
OUTB	6	8	O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak-source current, and 1-A peak-sink current. The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This *dead time* between the two outputs, along with a slower output rise time than fall time, prevents the two outputs from simultaneous activity. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor. The high-current-output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This configuration means that in many cases, external Schottky-clamp diodes are not required.

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Table 4-1. Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	D (SOIC)	PW (TSSOP)		
RC	4	6	O	The oscillator programming pin. The UCC3808A oscillator tracks VDD and GND internally so that variations in power supply rails minimally affect frequency stability. *Section 6.2* shows the oscillator block diagram. Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula in Equation 1. The recommended range of timing resistors is between 10 kΩ and 200 kΩ and range of timing capacitors is between 100 pF and 1000 pF. Avoid timing resistors less than 10 kΩ. For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.
VDD	8	2	P	The power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current is calculated from Equation 2. To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1-µF decoupling capacitor is recommended.

(1) P = Power, G = Ground, I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
	Supply voltage (IDD ≤ 10 mA)			15	V
	Supply current			20	mA
	OUTA/OUTB source current (peak)			–0.5	A
	OUTA/OUTB sink current (peak)			1	A
	Analog inputs (FB, CS)		–0.3	VDD + 0.3 (not to exceed 6)	V
	Power dissipation at T_A = 25°C	P package		1	W
		D package		650	mW
		PW package		400	
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Currents are positive into, negative out of the specified terminal. Consult the packaging section of the *Power Supply Control Products Data Book* for thermal limitations and considerations of packages.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	UCCx808-1	13	14	V
		UCCx808-2	5	14	
T_J	Junction temperature	UCC2808-x	–40	85	°C
		UCC3808-x	0	70	

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 8 PINS	PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.7	157.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	97.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.7	9.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.5	95.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

T_A = 0°C to 70°C for the UCC3808A-x and –40°C to +85°C for the UCC2808A-x, VDD = 10 V[1], 1-µF capacitor from VDD to GND, R = 22 kΩ, C = 330 pF, and $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
	Oscillator frequency		175	194	213	kHz
	Oscillator amplitude/VDD[2]		0.44	0.5	0.56	V/V
ERROR AMPLIFIER						
	Input voltage	COMP = 2 V	1.95	2	2.05	V
	Input bias current		–1		1	µA
	Open loop voltage gain		60	80		dB
	COMP sink current	FB = 2.2 V, COMP = 1 V	0.3	2.5		mA
	COMP source current	FB = 1.3 V, COMP = 3.5 V	–0.2	–0.5		mA
PWM						
	Maximum duty cycle	Measured at OUTA or OUTB	48%	49%	50%	
	Minimum duty cycle	COMP = 0 V			0%	
CURRENT SENSE						
	Gain[3]		1.9	2.2	2.5	V/V
	Maximum input signal	COMP = 5 V[4]	0.45	0.5	0.55	V
	CS to output delay	COMP = 3.5 V, CS from 0 mV to 600 mV		100	200	ns
	CS source current		–200			nA
	CS sink current	CS = 0.5 V, RC = 5.5 V[5]	5	10		mA
	Over current threshold		0.7	0.75	0.8	V
	COMP to CS offset	CS = 0 V	0.35	0.8	1.2	V
OUTPUT						
	OUT low level	I = 100 mA		0.5	1	V
	OUT high level	I = –50 mA, VDD – OUT		0.5	1	V
	Rise time	C_L = 1 nF		25	60	ns
	Fall time	C_L = 1 nF		25	60	ns
UNDERVOLTAGE LOCKOUT						
	Start threshold	UCCx808A-1[1]	11.5	12.5	13.5	V
		UCCx808A-2	4.1	4.3	4.5	
	Minimum operating voltage after start	UCCx808A-1	7.6	8.3	9	V
		UCCx808A-2	3.9	4.1	4.3	
	Hysteresis	UCCx808A-1	3.5	4.2	5.1	V
		UCCx808A-2	0.1	0.2	0.3	
SOFT START						
	COMP rise time	FB = 1.8 V, rise from 0.5 V to 4 V		3.5	20	ms
OVERALL						
	Start-up current	VDD < start threshold		130	260	µA
	Operating supply current	FB = 0 V, CS = 0 V[1] [6]		1	2	mA
	VDD zener shunt voltage	IDD = 10 mA[7]	13	14	15	V

(1) For UCCx808A-1, set VDD above the start threshold before setting at 10 V.
(2) Measured at RC. Signal amplitude tracks VDD.
(3) Gain is defined by: $A = \Delta V_{COMP} / \Delta V_{CS}$, $0\ V \le V_{CS} \le 0.4\ V$.
(4) Parameter measured at trip point of latch with FB at 0 V.
(5) The internal current sink on the CS pin is designed to discharge an external filter capacitor, and is not intended to be a DC sink path.
(6) Does not include current in the external oscillator network.
(7) Start threshold and Zener shunt threshold track together.

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5.6 Typical Characteristics

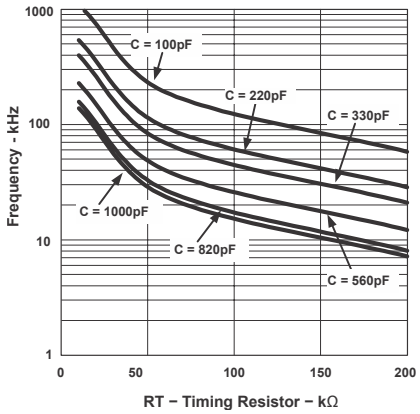


Figure 5-1. Oscillator Frequency vs External RC Values

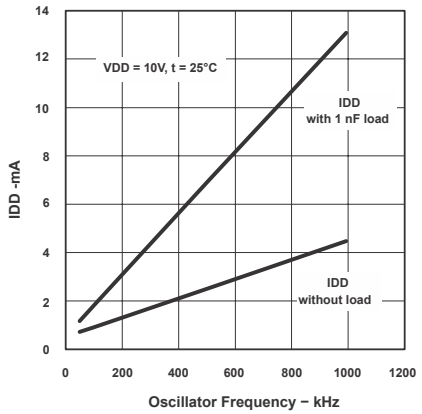


Figure 5-2. IDD vs Oscillator Frequency

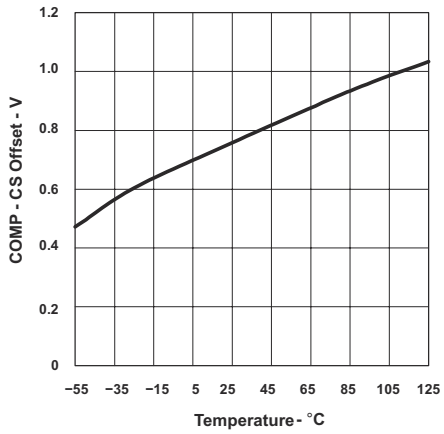


Figure 5-3. COMP to CS Offset vs Temperature

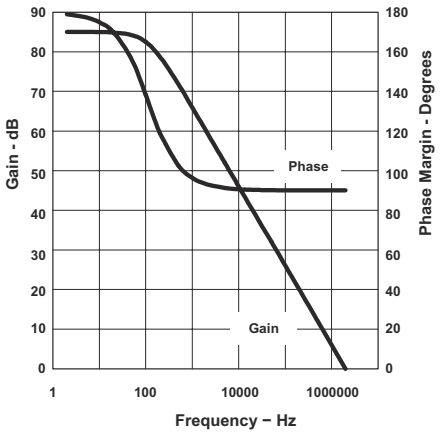


Figure 5-4. Error Amplifier Gain and Phase Response vs Frequency

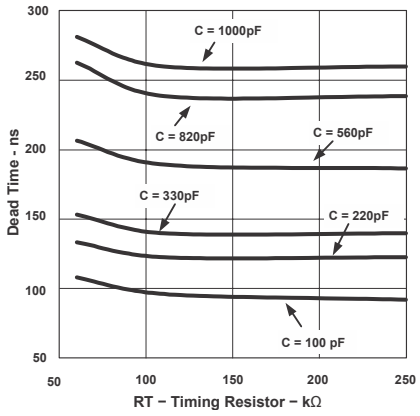


Figure 5-5. Output Dead Time vs External RC Values

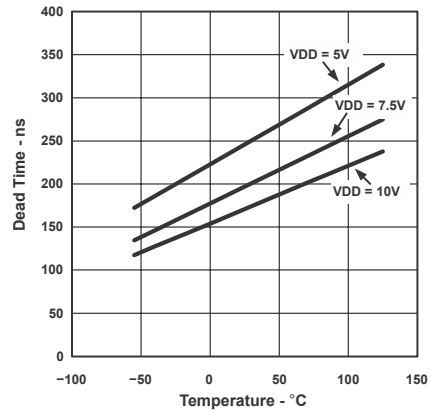


Figure 5-6. Dead Time vs Temperature

5.6 Typical Characteristics (continued)

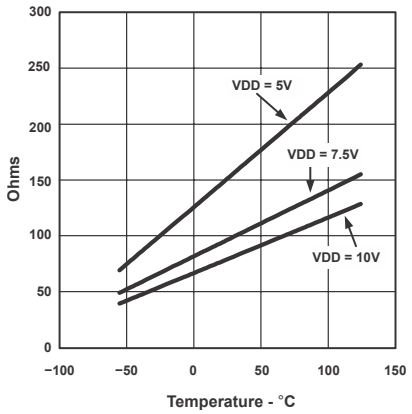


Figure 5-7. RC $R_{DS(on)}$ vs Temperature

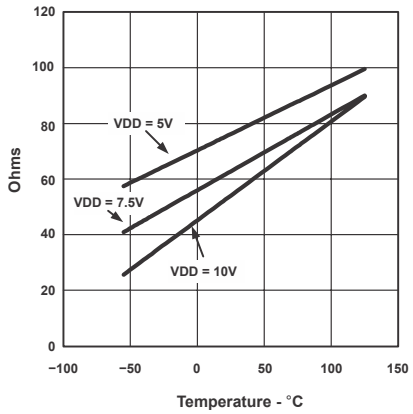


Figure 5-8. CS $R_{DS(on)}$ vs Temperature

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6 Detailed Description

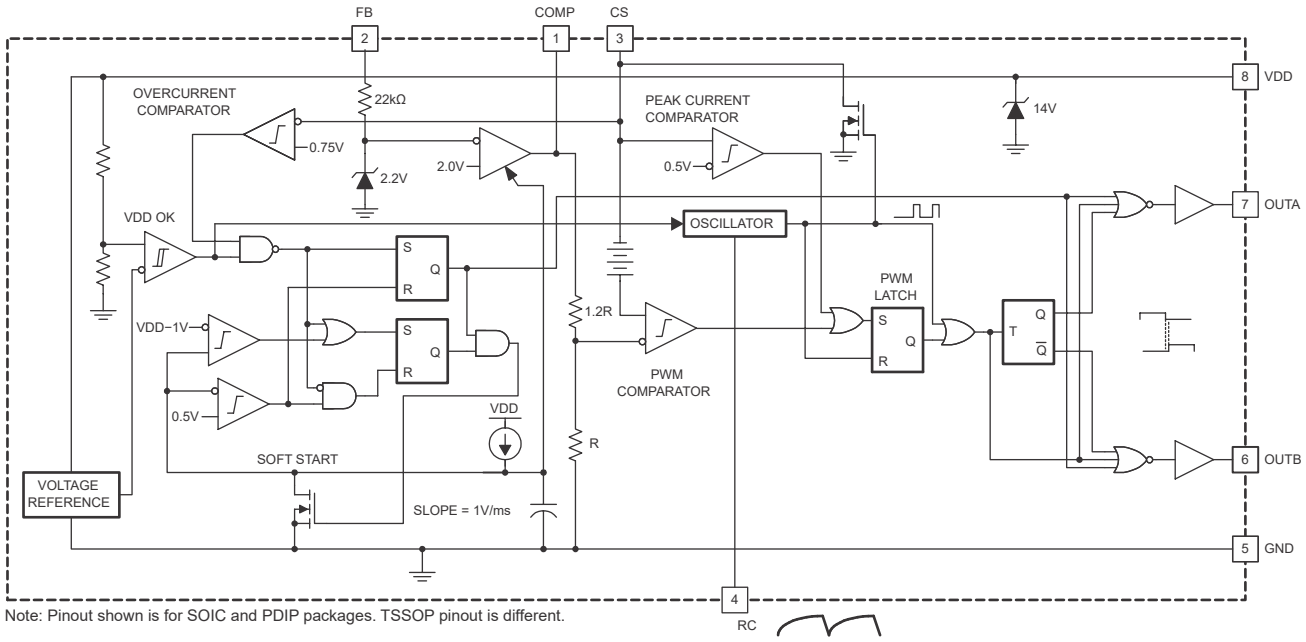
6.1 Overview

The UCCx808A-x device is a highly integrated, low-power current mode push-pull PWM controller. The controller employs low starting current and an internal control algorithm that offers accurate output voltage regulation in the presence of line and load variations. The UCCx808A-x family of parts has UVLO thresholds and hysteresis options for off-line and battery-powered systems.

Table 6-1. Undervoltage Lockout Levels

PART NUMBER	TURNON THRESHOLD	TURNOFF THRESHOLD
UCCx808A-1	12.5	8.3
UCCx808A-2	4.3	4.1

6.2 Functional Block Diagrams



Note: The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a 1/2 the oscillator frequency, with specified duty cycle of < 50% for both outputs.

Figure 6-1. Block Diagram

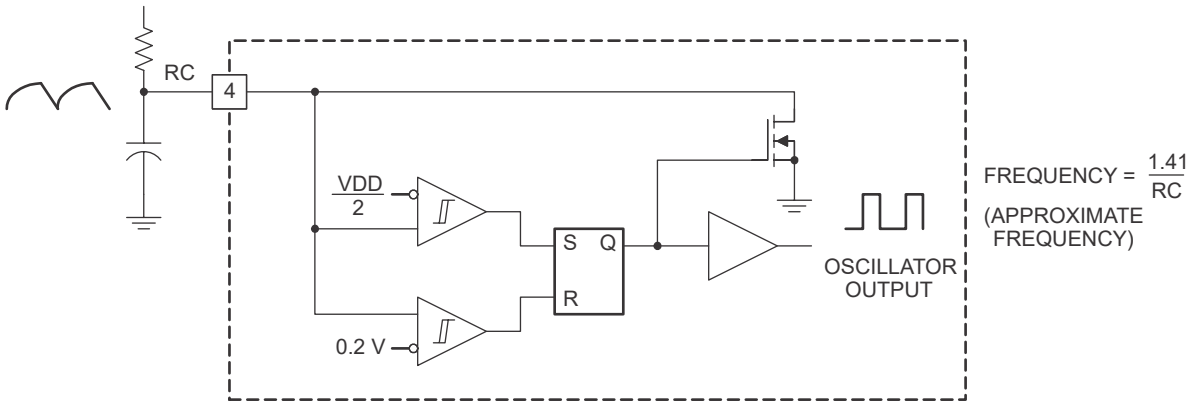


Figure 6-2. Block Diagram of Oscillator

6.3 Feature Description

6.3.1 Pin Descriptions

6.3.1.1 COMP

The COMP pin is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin both sources and sinks current. However, the error amplifier is internally current limited, so the zero duty cycle is externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

6.3.1.2 CS

The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft-start cycle.

6.3.1.3 FB

The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

6.3.1.4 GND

Reference ground and power ground for all functions. Because of high currents, and high-frequency operation of the UCC3808, a low-impedance printed-circuit board ground plane is highly recommended.

6.3.1.5 OUTA and OUTB

Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak source current, and 1-A peak sink current.

The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns, and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This provision means that in many cases, external Schottky clamp diodes are not required.

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6.3.1.6 RC

The oscillator programming pin. The oscillator of the UCC3808-x tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 6-2 shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). Equation 1 determines the approximate oscillator frequency.

$$f_{OSCILLATOR} = \frac{1.41}{RC} \quad (1)$$

where

- frequency is in Hz
- resistance in Ω
- capacitance in Farads

The recommended range of the timing resistors is between 10 kΩ and 200 kΩ, and range of the timing capacitors is between 100 pF and 1000 pF. Avoid timing resistors less than 10 kΩ.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

6.3.1.7 VDD

The power input connection for this device. Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), Equation 2 calculates the average OUT current.

$$I_{OUT} = Q_g \times f \quad (2)$$

where

- f is frequency

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. TI recommends a 1-µF decoupling capacitor.

6.4 Device Functional Modes

6.4.1 VCC

When VCC rises above 12.5 V (for the UCCx808A-1) or above 4.3 V (for the UCCx808-2) the device is enabled. When any fault conditions are cleared, a soft-start condition is initiated and the gate driver outputs begin switching.

When VCC drops below 8.3 V (for the UCCx808-1) or 4.1 V (for the UCCx808-2) the device enters the UVLO protection mode and both gate drivers are actively pulled low.

6.4.2 Push-Pull or Half-Bridge Function

The UCCx808A provide alternate 180° out-of-phase gate drive signals (OUTA and OUTB); therefore, these devices are an excellent choice to use as a controller for push-pull or half-bridge topologies. For half-bridge topology, the UCCx808A-x require a an external high side gate driver or pulse transformer on one or both of the OUTA and OUTB signals.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Figure 7-1 shows a 200-kHz push-pull application circuit with a full-wave rectifier. The output, V_O, provides 5 V at 50 W maximum and is electrically isolated from the input. Because the UCC3808A is a peak-current-mode controller, the 2N2907 emitter following amplifier (buffers the CT waveform) provides slope compensation that is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single-ground IC controller; therefore, use a 1-µF capacitor placed as close to the device as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady-state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 adjustable precision shunt regulator. Small-signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanical strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap; see also Figure 7-1. The main power transformer has a Magnetics Inc. ER28 size core made of P material for efficient operation at this frequency and temperature. The input voltage ranges from 36 Vdc to 72 Vdc.

7.2 Typical Application

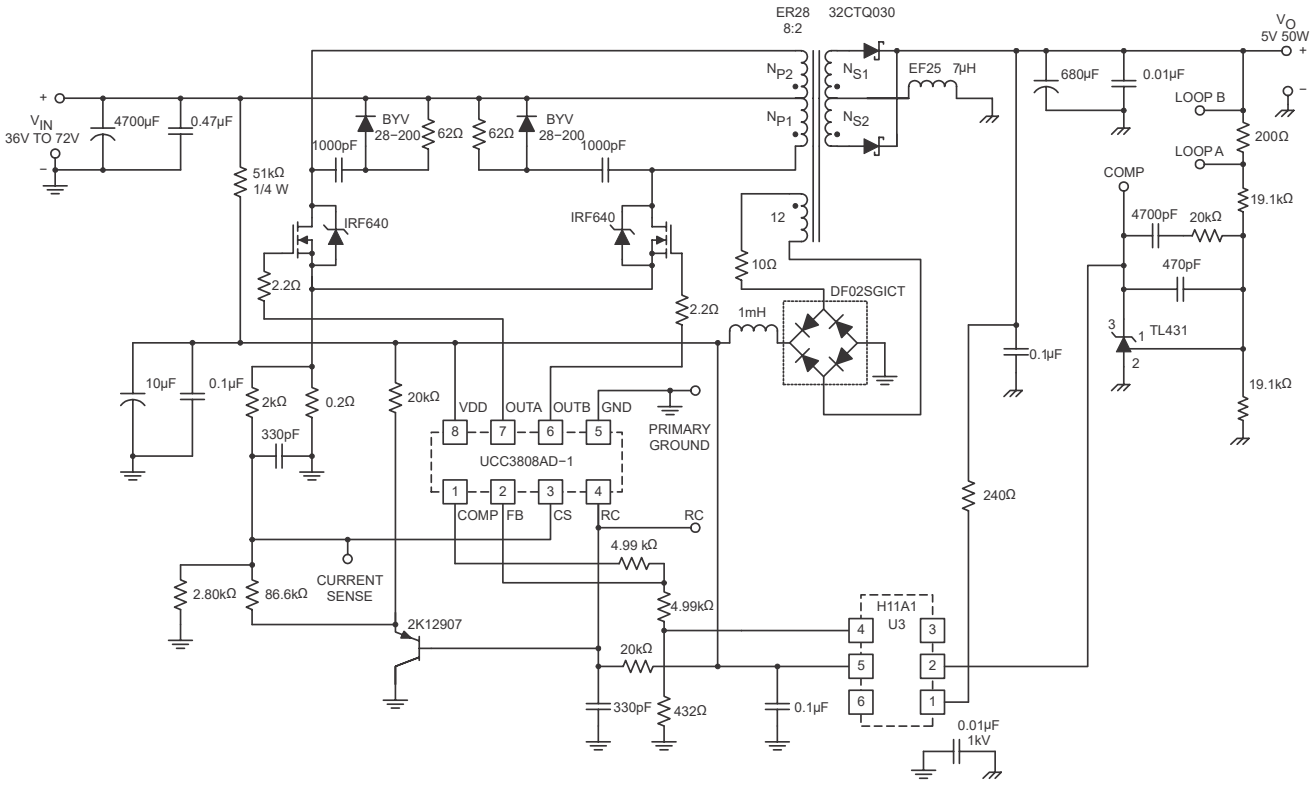


Figure 7-1. Typical Application Diagram: 48-Vin, 5-V, 50-W Output

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7.2.1 Design Requirements

Table 7-1 lists the design parameters for the UCC3808A-x.

Table 7-1. Design Parameters

PARAMETER	VALUE
Output voltage	5 V
Rated output power	50 W
Input DC voltage range	36 V to 72 V
Switching frequency	210 kHz

7.2.2 Detailed Design Procedure

The output, V_O, provides 5 V at 50 W maximum and is electrically isolated from the input. Because the UCC3808A is a peak current mode controller, the 2N2907 emitter follower amplifier buffers the oscillator waveform (RC pin) and provides slope compensation to the current sense (CS) input. This compensation is necessary for duty cycle ratios greater than 50%.

Capacitor decoupling is provided on the VDD pin. TI recommends using a minimum decoupling capacitance of 10-µF electrolytic and 0.1-µF ceramic. Place the ceramic capacitor as close to the VDD pin as possible. The UCC3808A is initially powered up from the 36-V to 72-V input supply. After the power supply has started, the bias supply is provided by an auxiliary winding on the main power transformer.

Isolation is provided by an optocoupler with regulation done on the secondary side using the TL431 precision programmable reference. The internal error amplifier of the UCC3808A is set up as a unity gain amplifier and the compensation network is provided on the secondary side.

Many choices exist for the output inductor depending on cost and size constraints. Design options are powdered iron, molypermalloy, or the ferrite core option used in this design. The power transformer is a low profile design, EFD25 size, using the Magnetics Inc. P material. This material is a good choice for low power loss at high switching frequency.

The switching frequency is set at 210 kHz with the RC network on the RC pin.

7.2.3 Application Curves

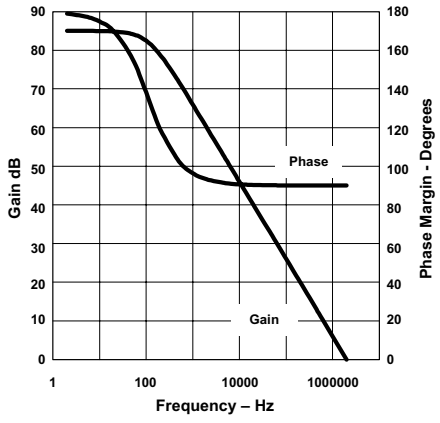


Figure 7-2. Error Amplifier Gain and Phase Response vs Frequency

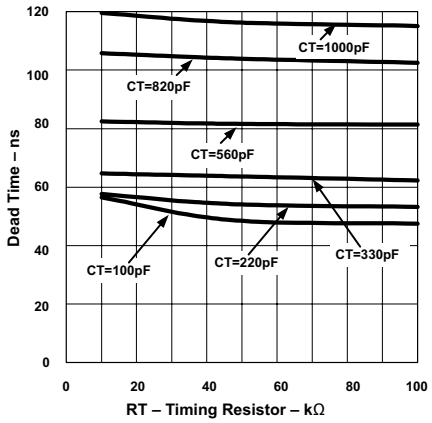


Figure 7-3. Dead Time vs Timing Resistor

7.3 Power Supply Recommendations

The VDD power pin for these devices requires the placement of electrolytic capacitor as energy storage capacitor because of the 1-A drive capability of the UCCx808A-x controller. A low-ESR noise decoupling capacitor is also required; place this capacitor as close as possible to the VDD and GND pins. Ceramic capacitors with stable dielectric characteristics over temperature are recommended. X7R is a good dielectric material for use here. TI recommends a 10-µF, 25-V electrolytic capacitor.

7.4 Layout

7.4.1 Layout Guidelines

1. Place the VDD capacitor as close as possible between the VDD pin and GND of the UCCx808A-x, tracked directly to both pins.
2. A small, external filter capacitor is recommended on the CS pin. Track the filter capacitor as directly as possible from the CS to GND pins.
3. The tracking and layout of the FB pin and connecting components is critical to minimizing noise pickup and interference. Reduce the total surface area of traces on the FB net to a minimum.
4. The OUTA and OUTB pins have a high-current source and sink capability. An external gate resistor is recommended to damp oscillations. A value of around a few Ohms is recommended. A pulldown resistor on the gate to source is recommended to prevent the MOSFET gate from floating on if there is an open-circuit fault in the gate drive path.

7.4.2 Layout Example

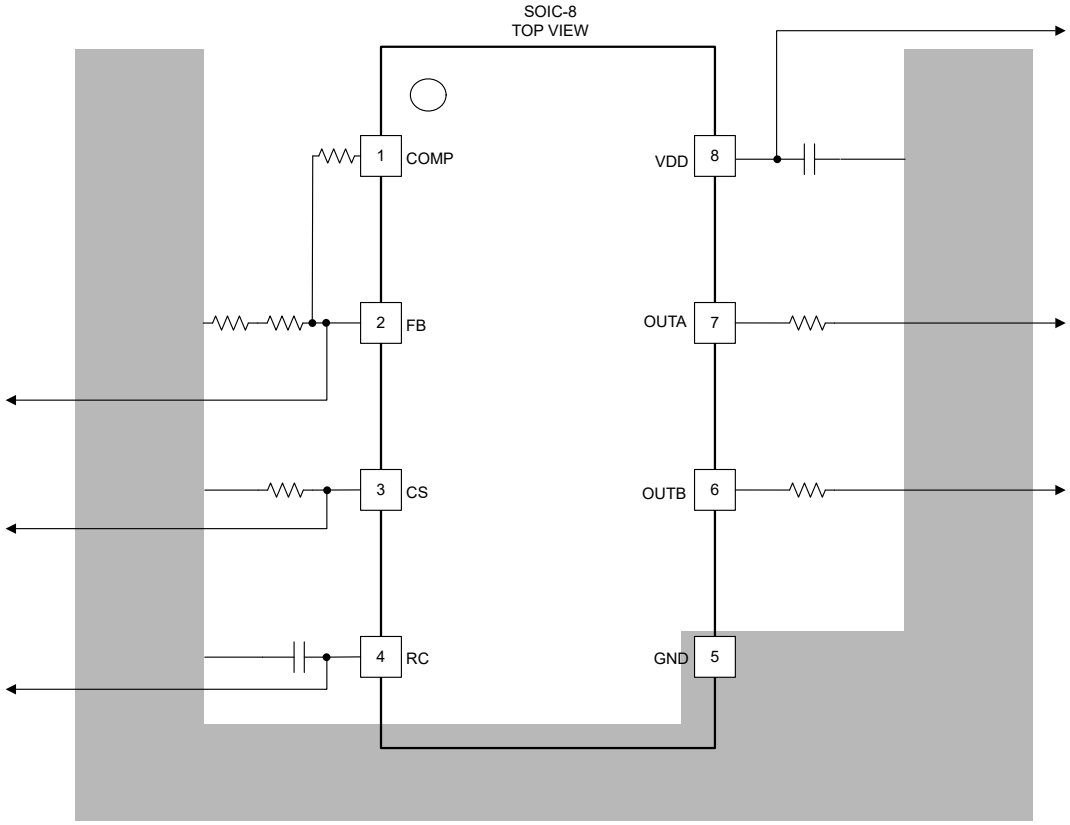


Figure 7-4. Recommended Layout

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following: *Power Supply Control Products Data Book*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2018) to Revision G (July 2025)	Page
• Deleted PDIP-related information	1
• Updated *ESD Ratings* to new limits	5
• Updated *Thermal Information*	5

Changes from Revision E (December 2016) to Revision F (July 2018)	Page
• Changed the *Simplified Application*	1
• Changed references of N package to P package (PDIP)	5

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Changes from Revision D (August 2002) to Revision E (October 2016)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted Lead temperature, soldering (10 s): 300°C maximum	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2808AD-1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2808A-1
UCC2808AD-2	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	2808A-2
UCC2808ADTR-1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1
UCC2808ADTR-1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1
UCC2808ADTR-1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-1
UCC2808ADTR-2	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2
UCC2808ADTR-2.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2
UCC2808ADTR-2G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808A-2
UCC2808APW-1	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	2808A1
UCC2808APW-2	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 85	2808A2
UCC2808APWTR-2	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 85	2808A2
UCC2808APWTR-2.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	2808A2
UCC3808AD-1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3808A-1
UCC3808AD-2	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	3808A-2
UCC3808ADTR-1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1
UCC3808ADTR-1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1
UCC3808ADTR-1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-1
UCC3808ADTR-2	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-2
UCC3808ADTR-2.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808A-2
UCC3808APW-2	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	0 to 70	3808A2
UCC3808APWTR-2	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	0 to 70	3808A2
UCC3808APWTR-2.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	0 to 70	3808A2
UCC3808APWTR-2G4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	0 to 70	3808A2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

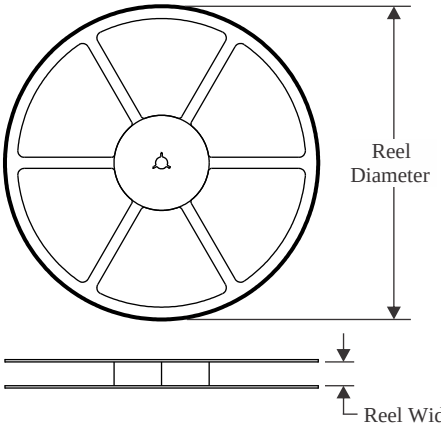
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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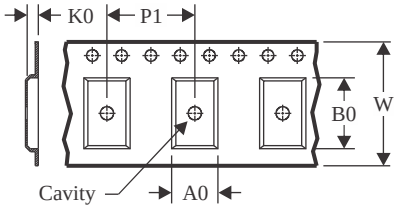
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

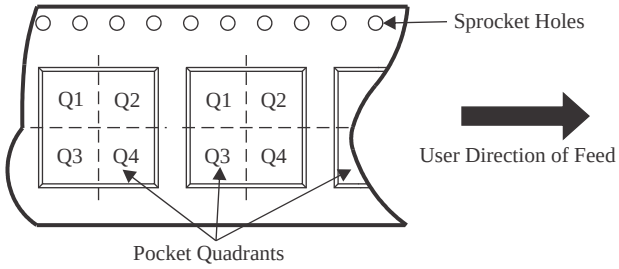


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

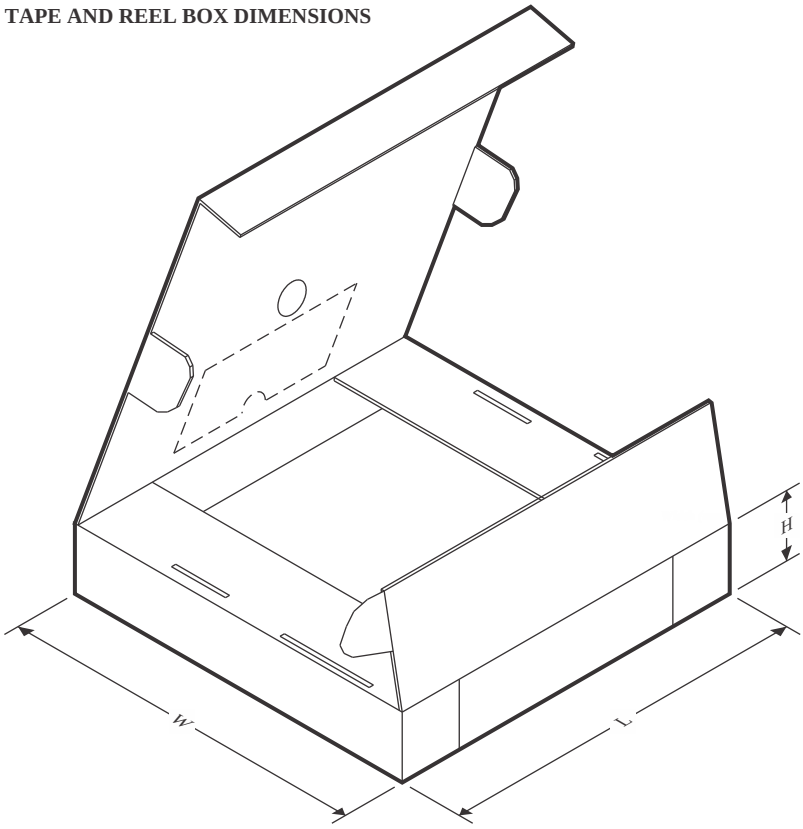
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808ADTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808ADTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808APWTR-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3808ADTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808ADTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808APWTR-2	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808ADTR-1	SOIC	D	8	2500	353.0	353.0	32.0
UCC2808ADTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC2808APWTR-2	TSSOP	PW	8	2000	353.0	353.0	32.0
UCC3808ADTR-1	SOIC	D	8	2500	353.0	353.0	32.0
UCC3808ADTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808APWTR-2	TSSOP	PW	8	2000	353.0	353.0	32.0

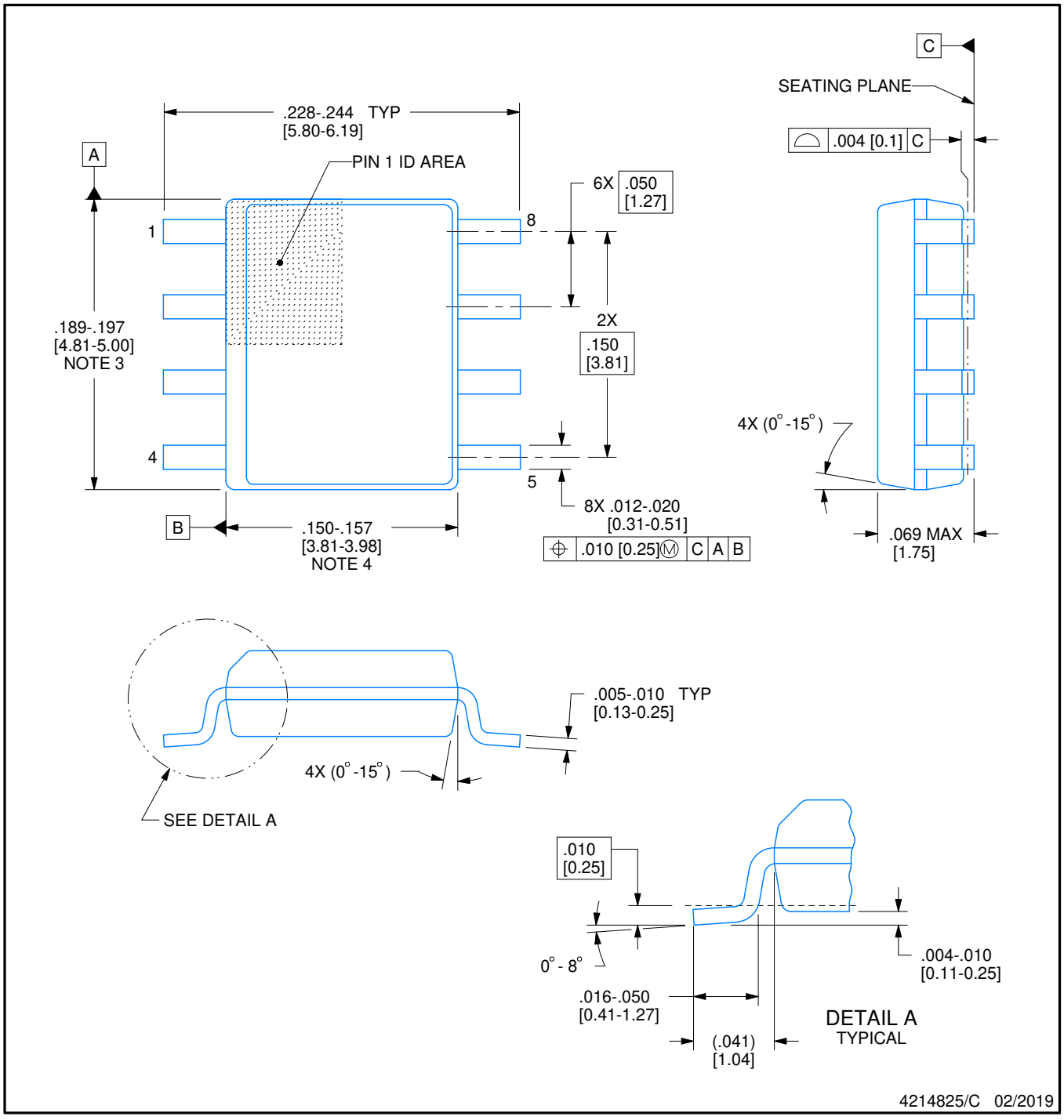


PACKAGE OUTLINE

D0008A

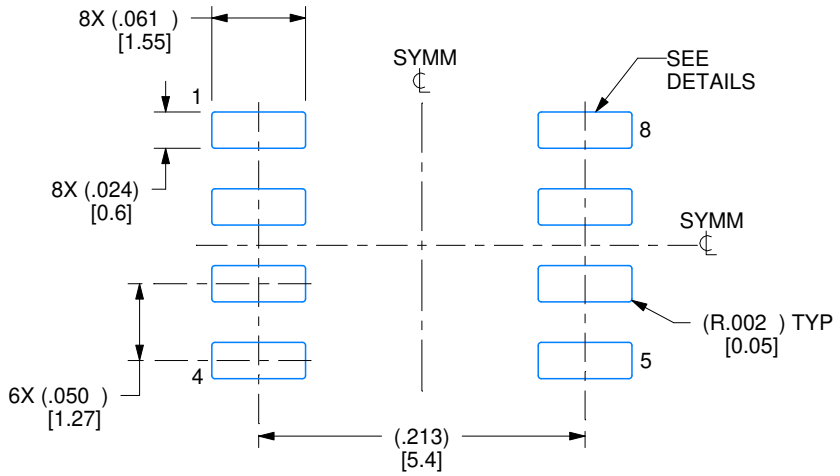
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

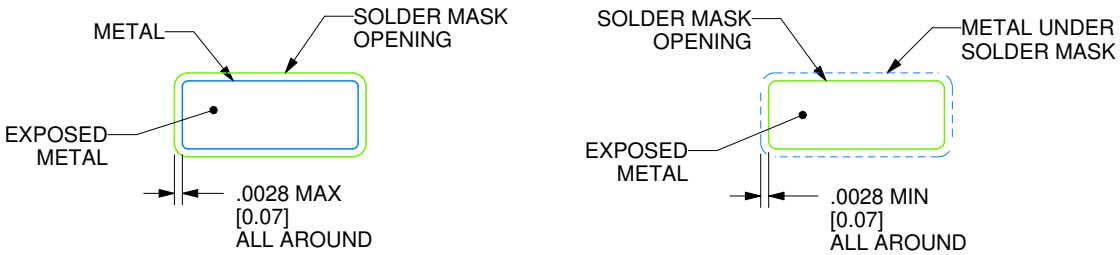


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

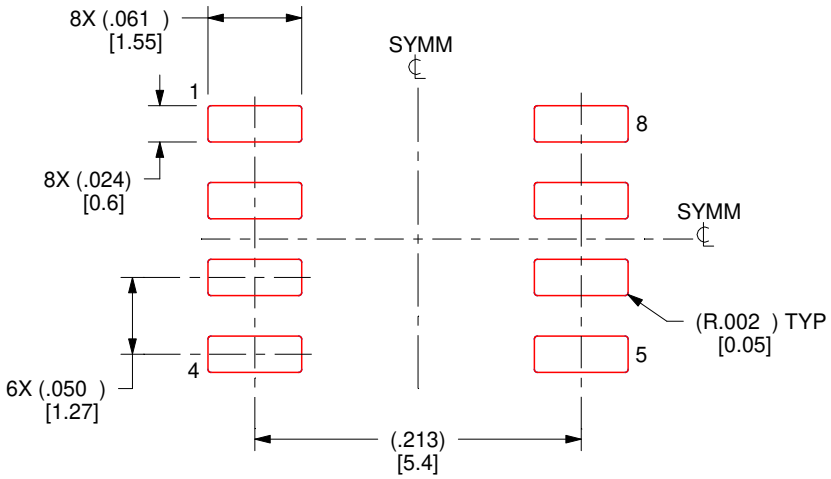
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

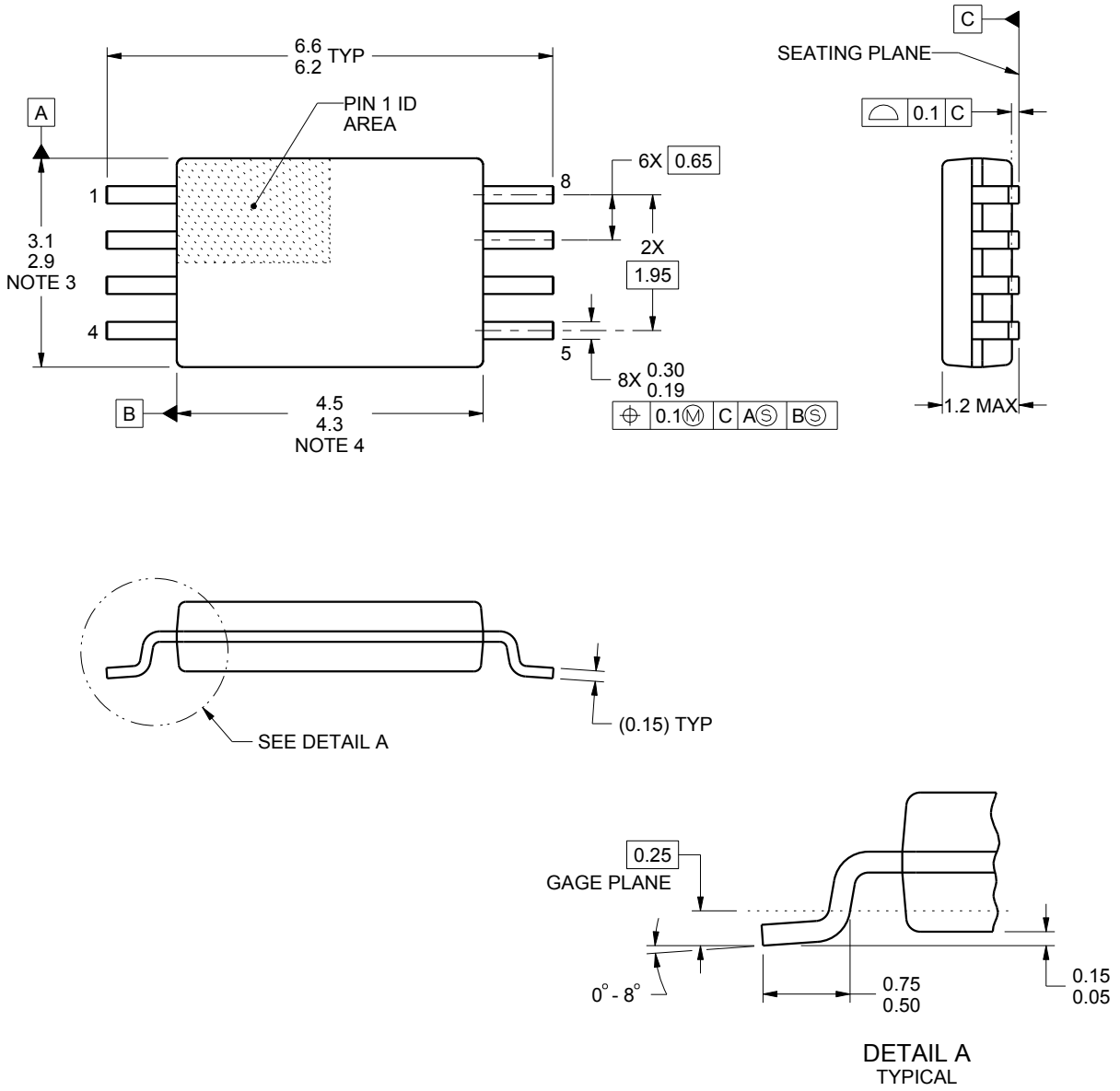


PACKAGE OUTLINE

PW0008A

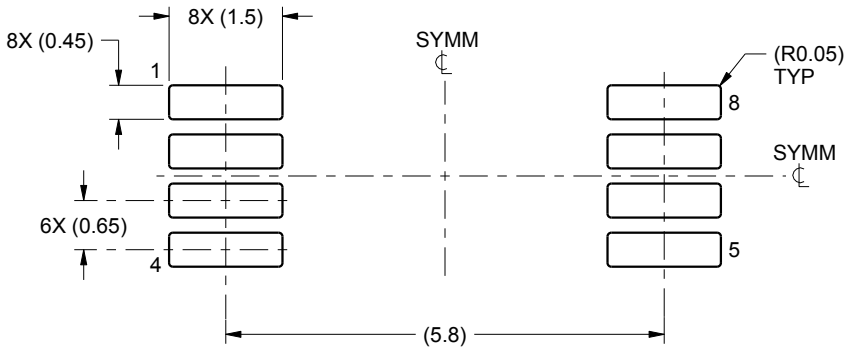
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

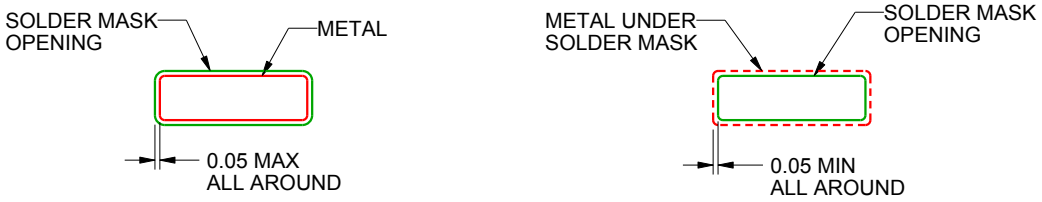


NOTES:

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4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

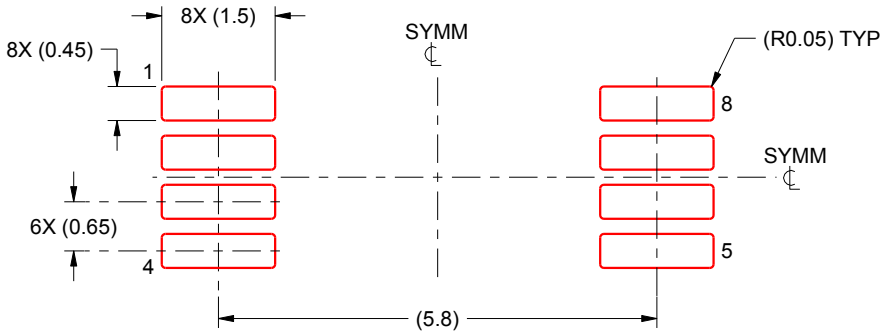


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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