Unitrode Products from Texas Instruments

application INFO available

UCC1809-1/-2
UCC2809-1/-2
UCC3809-1/-2

Economy Primary Side Controller

FEATURES

- User Programmable Soft Start With Active Low Shutdown
- User Programmable Maximum Duty Cycle
- Accessible 5V Reference
- Undervoltage Lockout
- Operation to 1MHz
- 0.4A Source/0.8A Sink FET Driver
- Low 100μA Startup Current

PART NUMBER	TURN ON THRESHOLD	TURN OFF THRESHOLD
UCCX809-1	10V	8V
UCCX809-2	15V	8V

DESCRIPTION

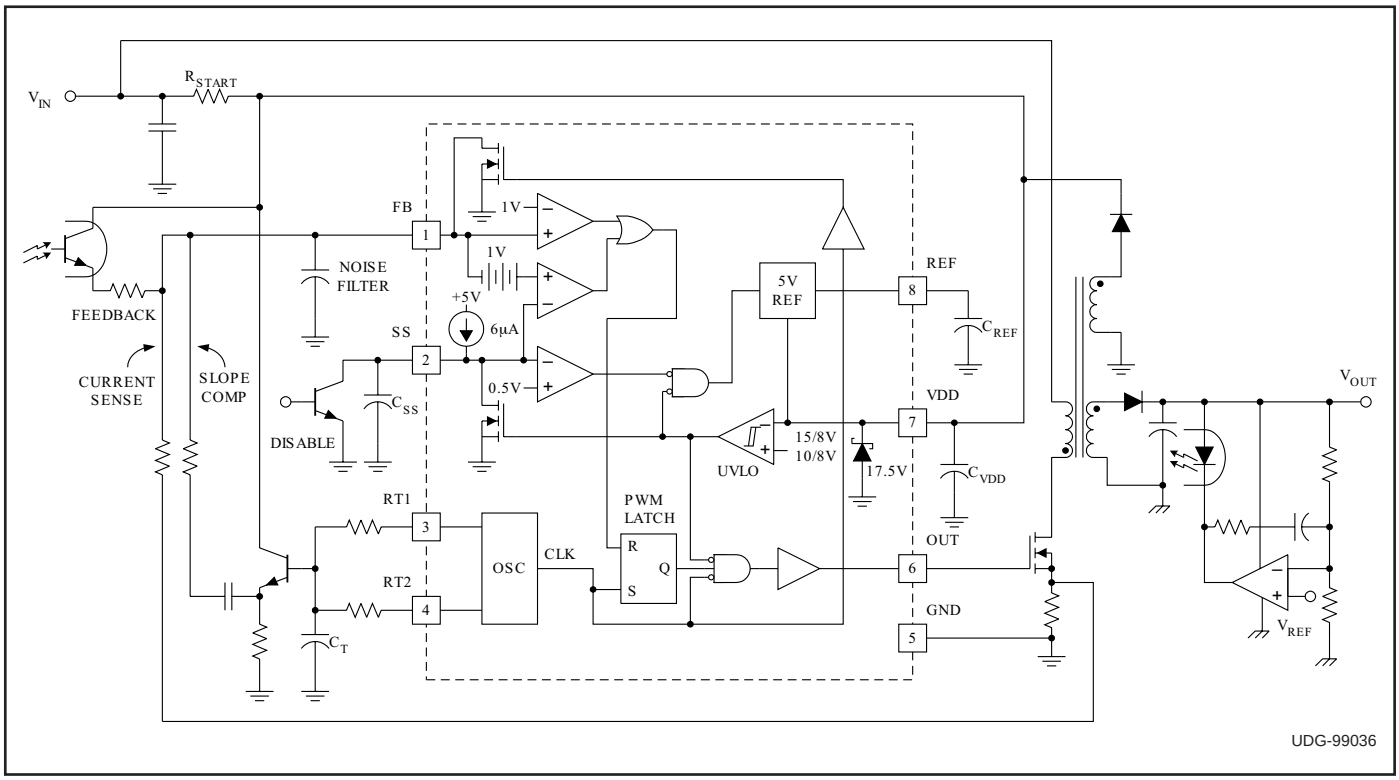
The UCC3809 family of BCDMOS economy low power integrated circuits contains all the control and drive circuitry required for off-line and isolated DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count. Internally implemented circuits include undervoltage lockout featuring startup current less than 100μA, a user accessible voltage reference, logic to ensure latched operation, a PWM comparator, and a totem pole output stage to sink or source peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3809 family also features full cycle soft start.

The family has UVLO thresholds and hysteresis levels for off-line and DC-to-DC systems as shown in the table to the left.

The UCC3809 and the UCC2809 are offered in the 8 pin SOIC (D), PDIP (N), TSSOP (PW), and MSOP (P) packages. The small TSSOP and MSOP packages make the device ideal for applications where board space and height are at a premium.

TYPICAL APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

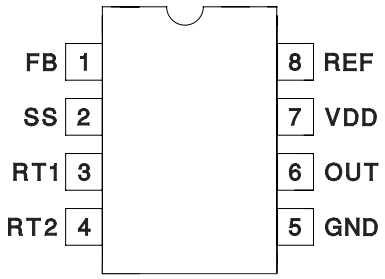
VDD 19V
I_{VDD} 25mA
I_{OUT} (tpw < 1μs and Duty Cycle < 10%) . . . . . –0.4A to 0.8A
RT1, RT2, SS . . . . . –0.3V to REF + 0.3V
I_{REF} . . . . . –15mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

* Values beyond which damage may occur.

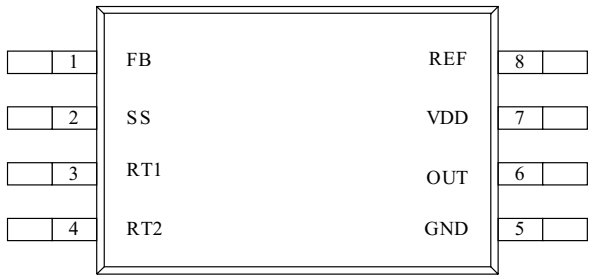
All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

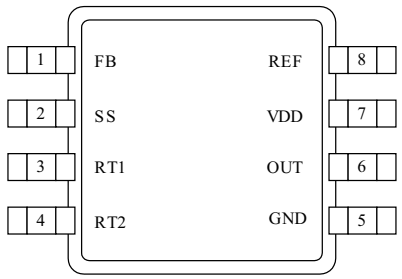
SOIC-8, DIL-8 (Top View)
D, N and J Packages



TSSOP-8 (Top View)
PW Package



MSOP-8 (Top View)
P Package



	Temperature Range	Available Packages
UCC1809-X	–55°C to +125°C	J
UCC2809-X	–40°C to +85°C	N, D, P, PW
UCC3809-X	0°C to +70°C	N, D, P, PW

ORDERING INFORMATION

UCC□ 809□ – □

- UVLO OPTION
- PACKAGE
- TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, C_{VREF} = 0.47 μF, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Section					
VDD Clamp	I_{VDD} = 10mA	16	17.5	19	V
I_{VDD}	No Load		600	900	μA
I_{VDD} Starting	(Note 1)		110		μA
I_{VDD} Standby	UCCx809-1, VDD = Start Threshold - 300mV		110	125	μA
	UCCx809-2, VDD = Start Threshold - 300mV		130	170	μA
Undervoltage Lockout Section					
Start Threshold (UCCx809-1)		9.4		10.4	V
UVLO Hysteresis (UCCx809-1)		1.65			V
Start Threshold (UCCx809-2)		14.0		15.6	V
UVLO Hysteresis (UCCx809-2)		6.2			V
Voltage Reference Section					
Output Voltage	I_{REF} = 0mA	4.75	5	5.25	V
Line Regulation	VDD = 10V to 15V		2		mV
Load Regulation	I_{REF} = 0mA to 5mA		2		mV
Comparator Section					
I_{FB}	Output Off		–100		nA
Comparator Threshold		0.9	0.95	1	V
OUT Propagation Delay (No Load)	V_{FB} = 0.8V to 1.2V at T_R = 10ns		50	100	ns

ELECTRICAL CHARACTERISTICS Unless otherwise specified, C_{VREF} = 0.47 μF, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft Start Section					
I_{SS}	VDD = 16V, V_{SS} = 0V; –40°C to +85°C	–4.9	–7.0	–9.1	μA
	VDD = 16V, V_{SS} = 0V; < –40°C; >+85°C	–4.0	–7.0	–10.0	μA
V_{SS} Low	VDD = 7.5V, I_{SS} = 200μA			0.2	V
Shutdown Threshold		0.44	0.48	0.52	V
Oscillator Section					
Frequency	RT1 = 10k, RT2 = 4.32k, CT = 820pF	90	100	110	kHz
Frequency Change with Voltage	VDD = 10V to 15V		0.1		%/V
C_T Peak Voltage			3.33		V
C_T Valley Voltage			1.67		V
C_T Peak to Peak Voltage		1.54	1.67	1.80	V
Output Section					
Output V_{SAT} Low	I_{OUT} = 80mA (dc)		0.8	1.5	V
Output V_{SAT} High	I_{OUT} = –40mA (dc), VDD – OUT		0.8	1.5	V
Output Low Voltage During UVLO	I_{OUT} = 20mA (dc)			1.5	V
Minimum Duty Cycle	V_{FB} = 2V		0		%
Maximum Duty Cycle			70		%
Rise Time	C_{OUT} = 1nF		35		ns
Fall Time	C_{OUT} = 1nF		18		ns

Note 1. Ensured by design. Not 100% production tested.

PIN DESCRIPTIONS

FB: This pin is the summing node for current sense feedback, voltage sense feedback (by optocoupler) and slope compensation. Slope compensation is derived from the rising voltage at the timing capacitor and can be buffered with an external small signal NPN transistor. External high frequency filter capacitance applied from this node to GND is discharged by an internal 250Ω on resistance NMOS FET during PWM off time and offers effective leading edge blanking set by the RC time constant of the feedback resistance from current sense resistor to FB input and the high frequency filter capacitor capacitance at this node to GND.

GND: Reference ground and power ground for all functions.

OUT: This pin is the high current power driver output. A minimum series gate resistor of 3.9Ω is recommended to limit the gate drive current when operating with high bias voltages.

REF: The internal 5V reference output. This reference is buffered and is available on the REF pin. REF should be bypassed with a 0.47μF ceramic capacitor.

RT1: This pin connects to timing resistor RT1 and controls the positive ramp time of the internal oscillator (Tr = 0.74 • (C_T + 27pF) • RT1). The positive threshold of the internal oscillator is sensed through inactive timing resistor RT2 which connects to pin RT2 and timing capacitor C_T.

RT2: This pin connects to timing resistor RT2 and controls the negative ramp time of the internal oscillator (Tf = 0.74 • (C_T + 27pF) • RT2). The negative threshold of the internal oscillator is sensed through inactive timing resistor RT1 which connects to pin RT1 and timing capacitor C_T.

SS: This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 6μA current source. Under normal soft start SS is discharged to at least 0.4V and then ramps positive to 1V during which time the output driver is held low. As SS charges from 1V to 2V soft start is implemented by an increasing output duty cycle. If SS is taken below 0.5V, the output driver is inhibited and held low. The user accessible 5V voltage reference also goes low and I_{VDD} < 100μA.

VDD: The power input connection for this device. This pin is shunt regulated at 17.5V which is sufficiently below the voltage rating of the DMOS output driver stage. VDD should be bypassed with a 1μF ceramic capacitor.

APPLICATION INFORMATION

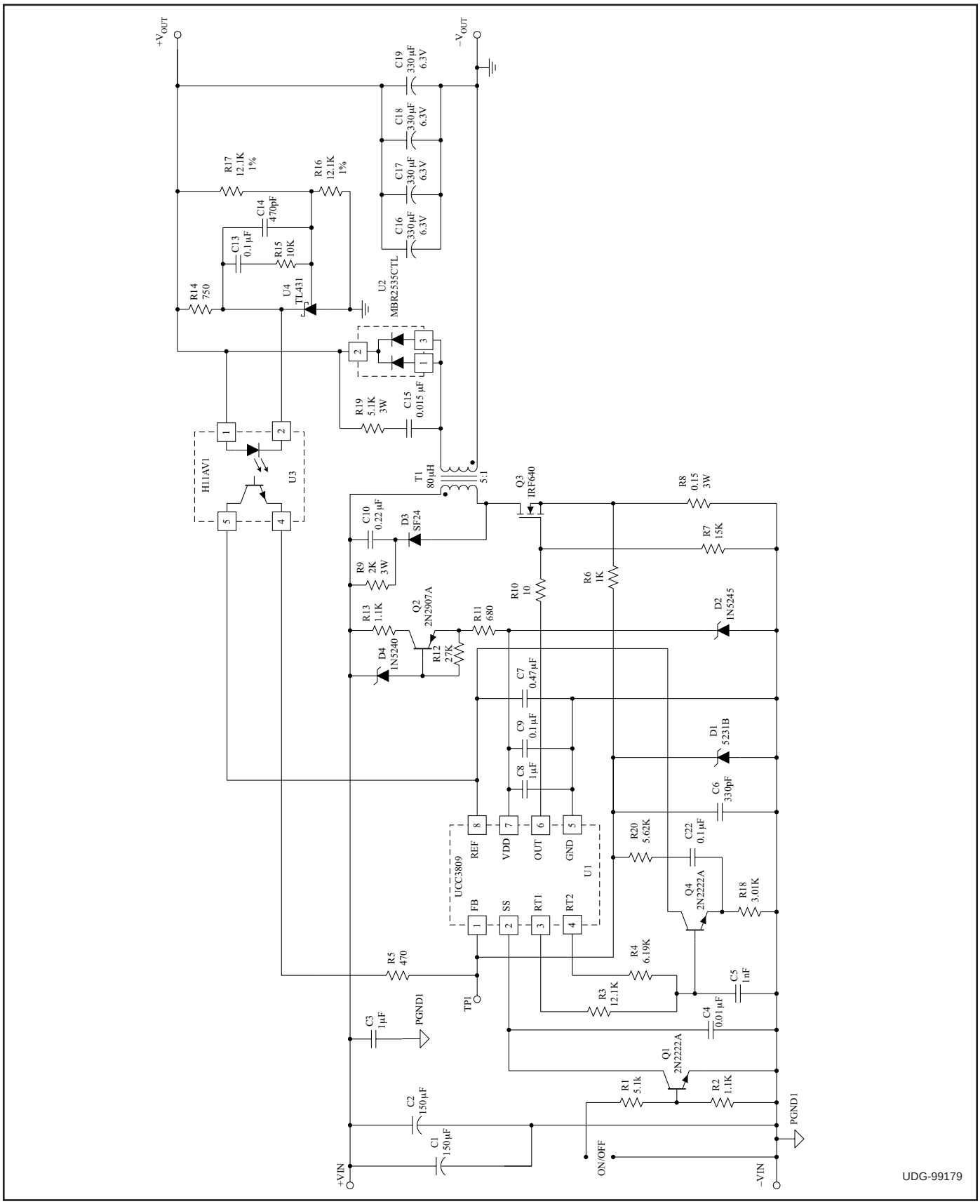


Figure 1. Isolated 50W flyback converter utilizing the UCC3809. The switching frequency is 70kHz, Vin = -32V to -72V, Vout = +5V, Iout = 0A to 10A

APPLICATION INFORMATION (cont.)

The Typical Application Diagram shows an isolated flyback converter utilizing the UCC3809. Note that the capacitors C_{REF} and C_{VDD} are local decoupling capacitors for the reference and IC input voltage, respectively. Both capacitors should be low ESR and ESL ceramic, placed as close to the IC pins as possible, and returned directly to the ground pin of the chip for best stability. REF provides the internal bias to many of the IC functions and C_{REF} should be at least 0.47μF to prevent REF from drooping.

FB Pin

The basic premise of the UCC3809 is that the voltage sense feedback signal originates from an optocoupler that is modulated by an external error amplifier located on the secondary side. This signal is summed with the current sense signal and any slope compensation at the FB pin and compared to a 1V threshold, as shown in the Typical Application Diagram. Crossing this 1V threshold resets the PWM latch and modulates the output driver on-time much like the current sense comparator used in the UC3842. In the absence of a FB signal, the output will follow the programmed maximum on-time of the oscillator.

When adding slope compensation, it is important to use a small capacitor to AC couple the oscillator waveform before summing this signal into the FB pin. By correctly selecting the emitter resistor of the optocoupler, the voltage sense signal can force the FB node to exceed the 1V threshold when the output that is being compared exceeds a desired level. Doing so drives the UCC3809 to zero percent duty cycle.

Oscillator

The following equation sets the oscillator frequency:

$$F_{OSC} = \left[0.74 \bullet \left(CT + 27pF\right) \bullet (RT1 + RT2)\right]^{-1}$$

$$D_{MAX} = 0.74 \bullet RT1 \bullet \left(CT + 27pF\right) \bullet F_{OSC}$$

Referring to Figure 2 and the waveforms in Figure 3, when Q1is on, CT charges via the $R_{DS(on)}$ of Q1 and RT1. During this charging process, the voltage of CT is sensed through RT2. The S input of the oscillator latch, S(OSC), is level sensitive, so crossing the upper threshold (set at 2/3 VREF or 3.33V for a typical 5.0V reference) sets the Q output (CLK signal) of the oscillator latch high. A high CLK signal results in turning off Q1 and turning on Q2. CT now discharges through RT2 and the $R_{DS(on)}$ of Q2. CT discharges from 3.33V to the lower threshold (set at 1/3 VREF or 1.67V for a typical 5.0V reference) sensed through RT1. The R input to the oscillator latch, R(OSC), is also level sensitive and resets the CLK signal low when CT crosses the 1.67V threshold, turning off Q2 and turning on Q1, initiating another charging cycle.

Figure 3 shows the waveforms associated with the oscillator latch and the PWM latch (shown in the Typical Application Diagram). A high CLK signal not only initiates a discharge cycle for CT, it also turns on the internal NMOS FET on the FB pin causing any external capacitance used for leading edge blanking connected to this pin to be discharged to ground. By discharging any external capacitor completely to ground during the external switch's off-time, the noise immunity of the converter is enhanced allowing the user to design in smaller RC components for leading edge blanking. A high CLK signal also sets the level sensitive S input of the PWM latch, S(PWM), high, resulting in a high output, Q(PWM), as shown in Figure 3. This Q(PWM) signal will remain high until a reset signal, R(PWM) is received. A high R(PWM) signal results from the FB signal crossing the 1V threshold, or during soft start or if the SS pin is disabled.

Assuming the UVLO threshold is satisfied, the OUT signal of the IC will be high as long as Q(PWM) is high and S(PWM), also referred to as CLK, is low. The OUT signal will be dominated by the FB signal as long as the FB signal trips the 1V threshold while CLK is low. If the FB signal does not cross the 1V threshold while CLK is low, the OUT signal will be dominated by the maximum duty cycle programmed by the user. Figure 3 illustrates the various waveforms for a design set up for a maximum duty cycle of 70%.

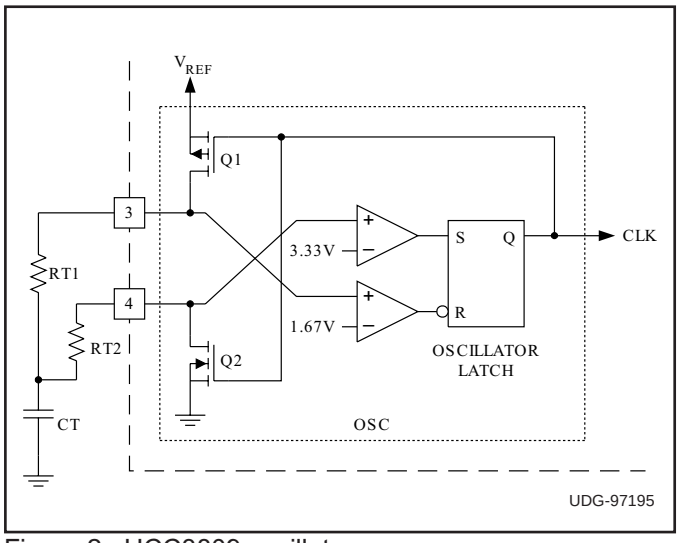


Figure 2. UCC3809 oscillator.

APPLICATION INFORMATION (cont.)

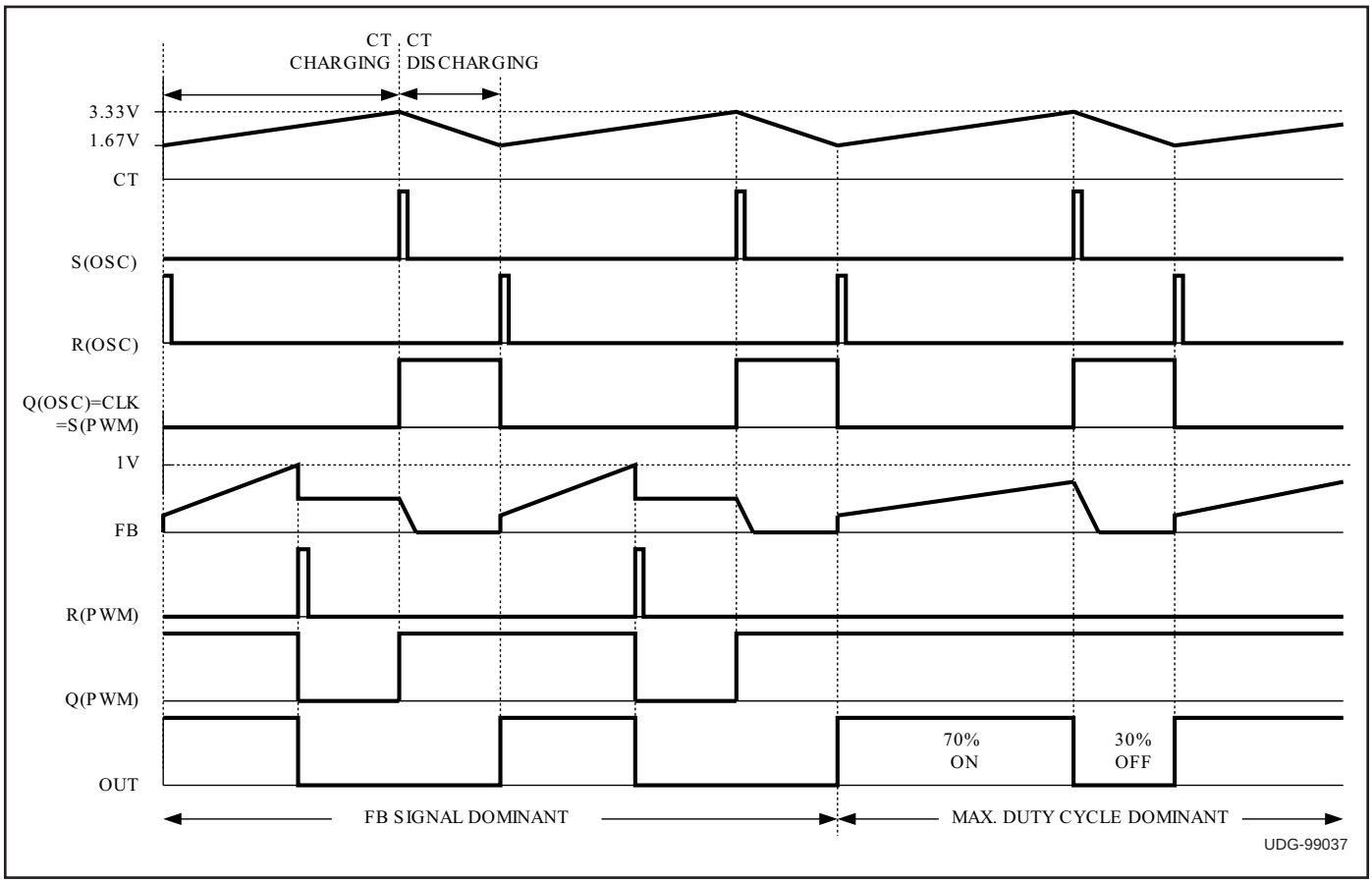


Figure 3. Waveforms associated with the oscillator latch and the PWM latch.

The recommended value for CT is 1nF for frequencies in the 100 kHz or less range and smaller CT for higher frequencies. The minimum recommended values of RT1 and RT2 are 10kΩ and 4.32kΩ, respectively. Using these values maintains a ratio of at least 20:1 between the $R_{DS(on)}$ of the internal FETs and the external timing resistors, resulting in minimal change in frequency over temperature. Because of the oscillator's susceptibility to capacitive coupling, examine the oscillator frequency by looking at the common RT1-RT2-CT node on the circuit board as opposed to looking at pins 3 and 4 directly. For good noise immunity, RT1 and RT2 should be placed as close to pins 3 and 4 of the IC as possible. CT should be returned directly to the ground pin of the IC with minimal stray inductance and capacitance.

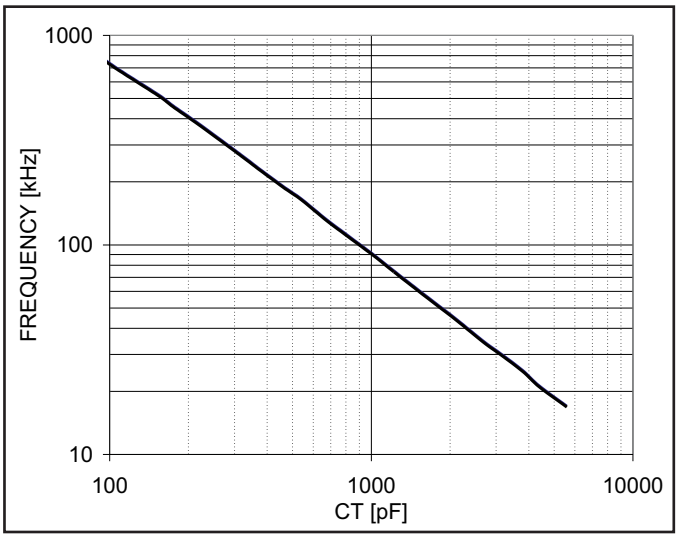


Figure 4. Oscillator frequency vs. C_T (RT1 = 10k, RT2 = 4.32k)

APPLICATION INFORMATION (cont.)

Synchronization

Both of the synchronization schemes shown in Figure 5 can be successfully implemented with the internal oscillator of the UCC3809. Both schemes allow access to the timing ramp needed for slope compensation and have minimal impact on the programmed maximum duty cycle. In the absence of a sync pulse, the PWM controller will run independently at the frequency set by RT1, RT2, and CT. This free running frequency must be approximately 15 to 20% lower than the sync pulse frequency to insure the free running oscillator does not cross the comparator threshold before the desired sync pulse.

Option I uses the synchronization pulse to pull pin 3 low, triggering the internal 1.67V comparator to reset the RS latch and initiate a charging cycle. The valley voltage of the CT waveform is higher when synchronized using this configuration, decreasing the ramp charge and discharge times, thereby increasing the operating frequency; otherwise the overall shape of the CT voltage waveform is unchanged.

Option II uses the synchronization pulse to superimpose the sync voltage onto the peak of the CT waveform. This triggers the internal 3.33V comparator, initiating a discharge cycle. The sync pulse is summed with the free running oscillator waveform at the CT node, resulting in a spike on top of the CT peak voltage.

ADDITIONAL INFORMATION

Please refer to the following Unitrode application topics for additional information.

[1] Application Note U-165, Design Review: Isolated 50W Flyback Converter with the UCC3809 Primary Side Controller by Lisa Dinwoodie.

[2] Design Note DN-89, Comparing the UC3842, UCC3802, and UCC3809 Primary Side PWM Controllers by Lisa Dinwoodie.

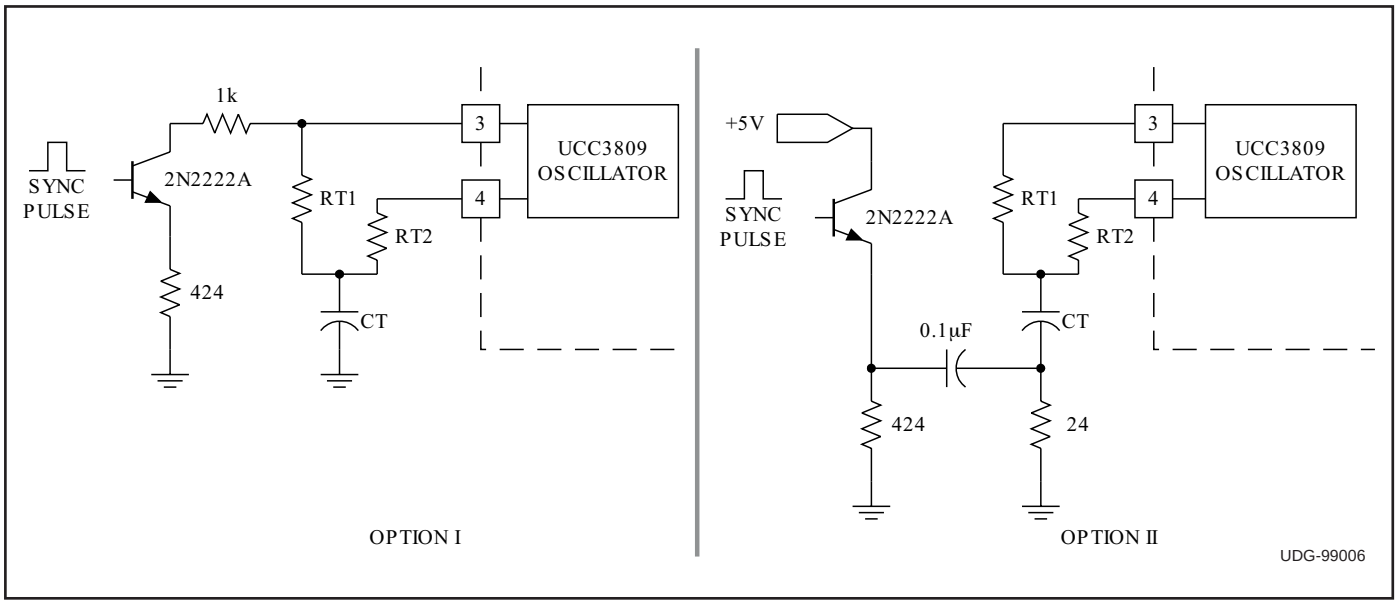


Figure 5. UCC3809 synchronization options.

TYPICAL CHARACTERISTICS CURVES

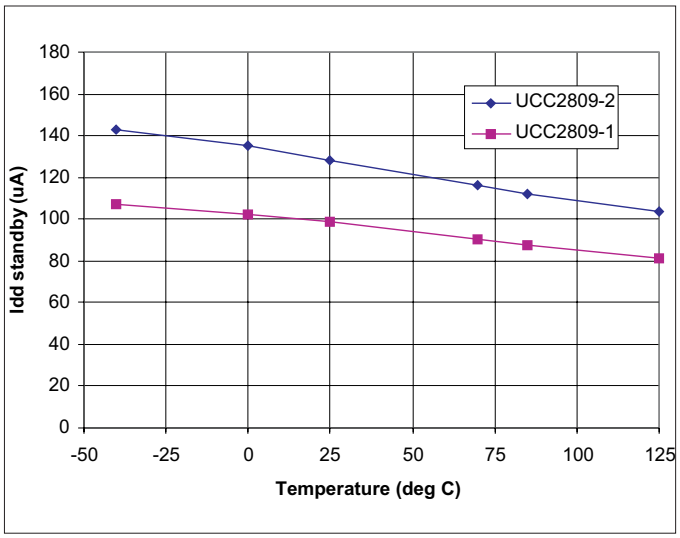


Figure 6. I_{DD} (standby) vs. temperature.

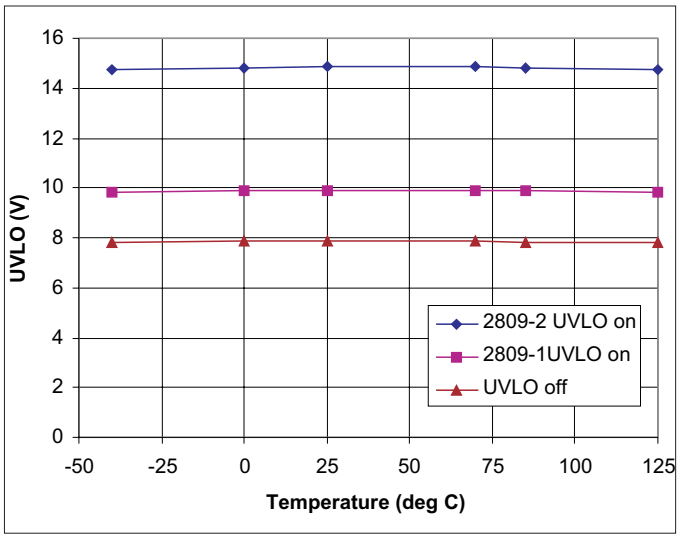


Figure 7. UVLO vs. temperature.

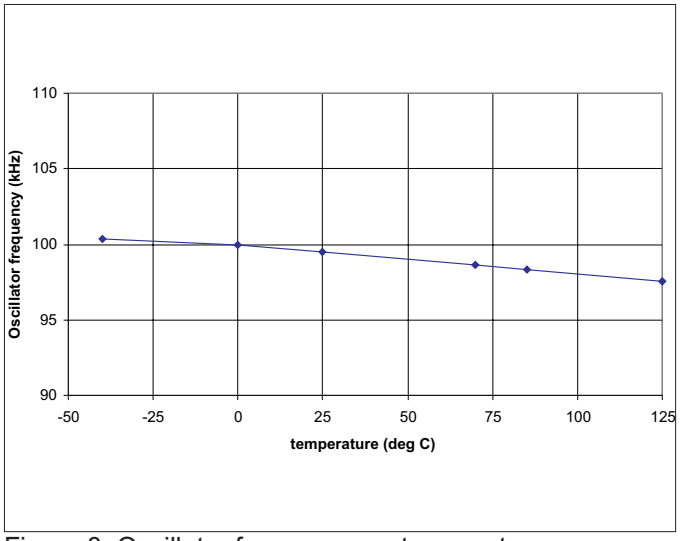


Figure 8. Oscillator frequency vs. temperature.

REVISION HISTORY

REV. B 11/04

Added Ivdd Stand-by Current specifications in the Electrical Characteristics table.

Modified Ivdd Starting specifications in the Electrical Characteristics table.

Added Typical Characteristics Curves for Idd(Standby), UVLO thresholds, and Oscillator Frequency.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2809D-1	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-1 D-1
UCC2809D-1.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-1 D-1
UCC2809D-2	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-2 D-2
UCC2809D-2.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-2 D-2
UCC2809DTR-1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-1 D-1
UCC2809DTR-1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-1 D-1
UCC2809DTR-2	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-2 D-2
UCC2809DTR-2.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-2 D-2
UCC2809P-1	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	28091
UCC2809P-1.A	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	28091
UCC2809P-2	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	28092
UCC2809P-2.A	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	28092
UCC2809PTR-1	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 85	28091
UCC2809PTR-1.A	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	28091
UCC2809PTR-2	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 85	28092
UCC2809PTR-2.A	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	28092
UCC2809PW-1	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28091
UCC2809PW-1.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28091
UCC2809PW-2	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28092
UCC2809PW-2.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28092
UCC2809PWTR-1	NRND	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28091
UCC2809PWTR-1.A	NRND	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28091

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC3809D-1	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-1 D-1
UCC3809D-1.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-1 D-1
UCC3809D-2	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-2 D-2
UCC3809D-2.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-2 D-2
UCC3809DTR-1	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(3809-1, UCC3809) D-1
UCC3809DTR-1.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(3809-1, UCC3809) D-1
UCC3809DTR-1G4	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	(3809-1, UCC3809) D-1
UCC3809DTR-2	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-2 D-2
UCC3809DTR-2.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-2 D-2
UCC3809P-1	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	38091
UCC3809P-1.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	38091
UCC3809P-2	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	38092
UCC3809P-2.A	NRND	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	38092
UCC3809PTR-1	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	0 to 70	38091
UCC3809PTR-1.A	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	0 to 70	38091
UCC3809PTR-2	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-	38092
UCC3809PTR-2.A	NRND	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	0 to 70	38092
UCC3809PW-2	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	38092
UCC3809PW-2.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	38092

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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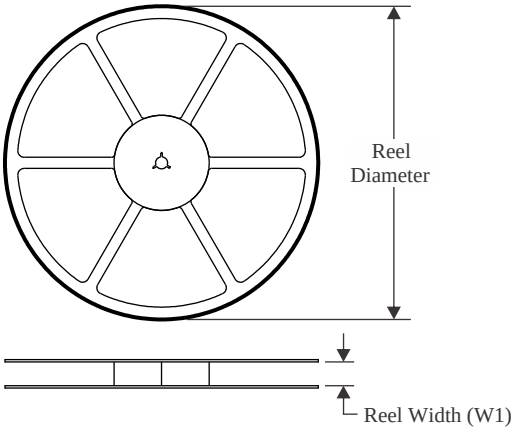
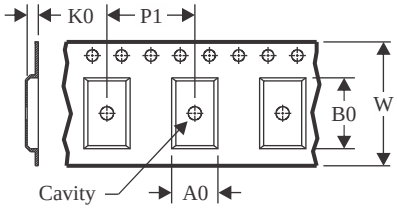
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

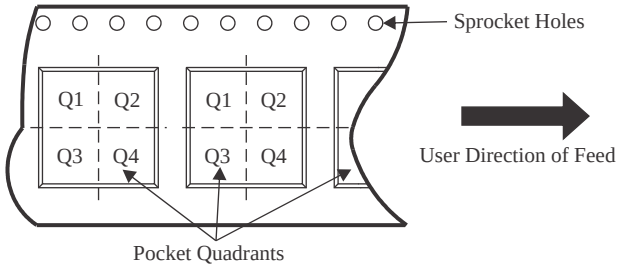


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

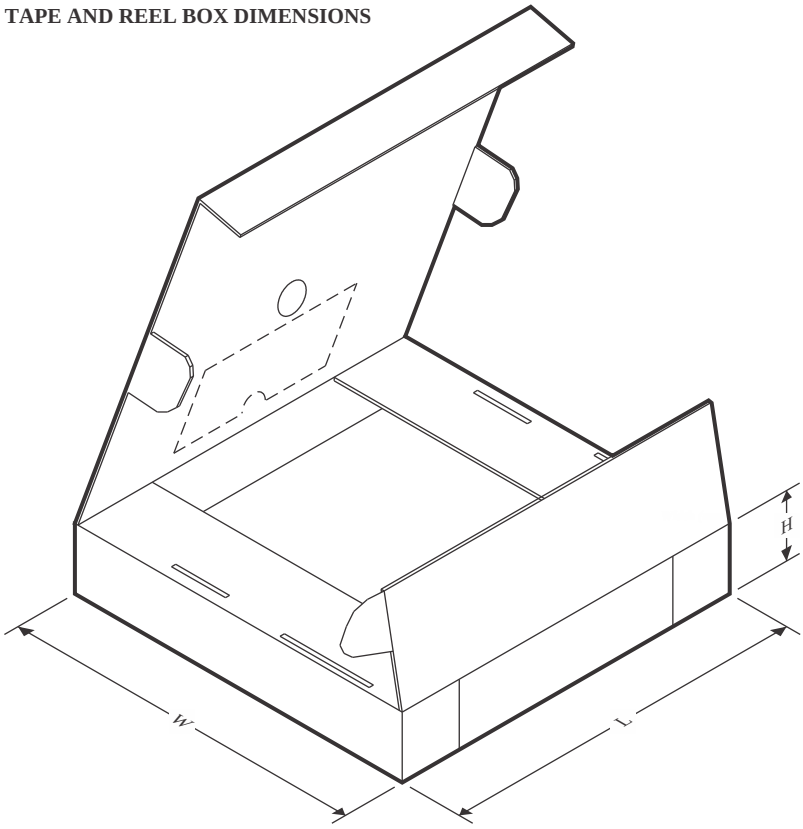
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2809DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2809DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2809PTR-1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC2809PTR-2	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
UCC2809PWTR-1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3809DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3809DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3809PTR-1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
UCC3809PTR-2	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

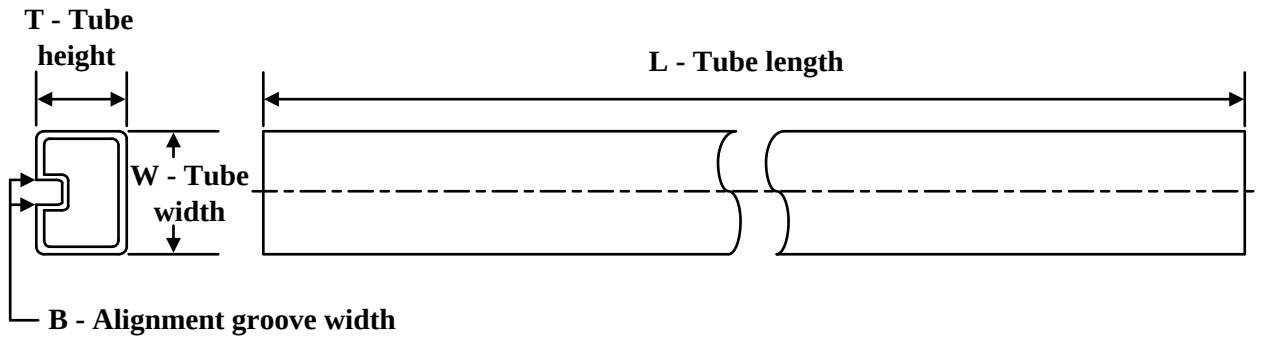
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2809DTR-1	SOIC	D	8	2500	353.0	353.0	32.0
UCC2809DTR-2	SOIC	D	8	2500	353.0	353.0	32.0
UCC2809PTR-1	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC2809PTR-2	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC2809PWTR-1	TSSOP	PW	8	2000	353.0	353.0	32.0
UCC3809DTR-1	SOIC	D	8	2500	353.0	353.0	32.0
UCC3809DTR-2	SOIC	D	8	2500	353.0	353.0	32.0
UCC3809PTR-1	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC3809PTR-2	VSSOP	DGK	8	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

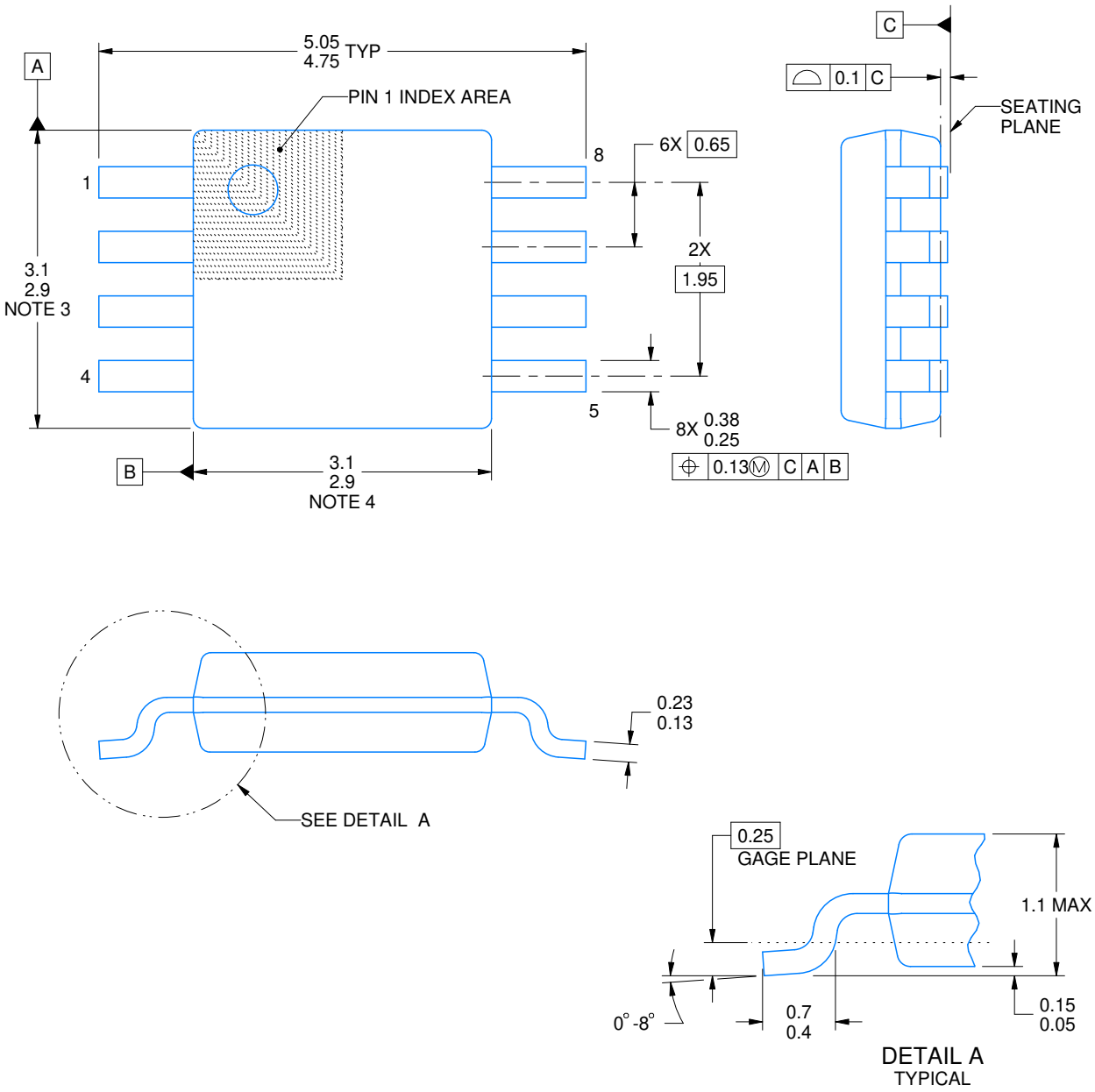
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC2809D-1	D	SOIC	8	75	507	8	3940	4.32
UCC2809D-1.A	D	SOIC	8	75	507	8	3940	4.32
UCC2809D-2	D	SOIC	8	75	507	8	3940	4.32
UCC2809D-2.A	D	SOIC	8	75	507	8	3940	4.32
UCC2809P-1	DGK	VSSOP	8	80	330	6.55	500	2.88
UCC2809P-1.A	DGK	VSSOP	8	80	330	6.55	500	2.88
UCC2809P-2	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC2809P-2	DGK	VSSOP	8	80	330	6.55	500	2.88
UCC2809P-2.A	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
UCC2809P-2.A	DGK	VSSOP	8	80	330	6.55	500	2.88
UCC2809PW-1	PW	TSSOP	8	150	508	8.5	3250	2.8
UCC2809PW-1.A	PW	TSSOP	8	150	508	8.5	3250	2.8
UCC2809PW-2	PW	TSSOP	8	150	508	8.5	3250	2.8
UCC2809PW-2.A	PW	TSSOP	8	150	508	8.5	3250	2.8
UCC3809D-1	D	SOIC	8	75	507	8	3940	4.32
UCC3809D-1.A	D	SOIC	8	75	507	8	3940	4.32
UCC3809D-2	D	SOIC	8	75	507	8	3940	4.32
UCC3809D-2.A	D	SOIC	8	75	507	8	3940	4.32
UCC3809P-1	DGK	VSSOP	8	80	330	6.55	500	2.88
UCC3809P-1.A	DGK	VSSOP	8	80	330	6.55	500	2.88
UCC3809P-2	DGK	VSSOP	8	80	330	6.55	500	2.88
UCC3809P-2.A	DGK	VSSOP	8	80	330	6.55	500	2.88
UCC3809PW-2	PW	TSSOP	8	150	508	8.5	3250	2.8
UCC3809PW-2.A	PW	TSSOP	8	150	508	8.5	3250	2.8

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

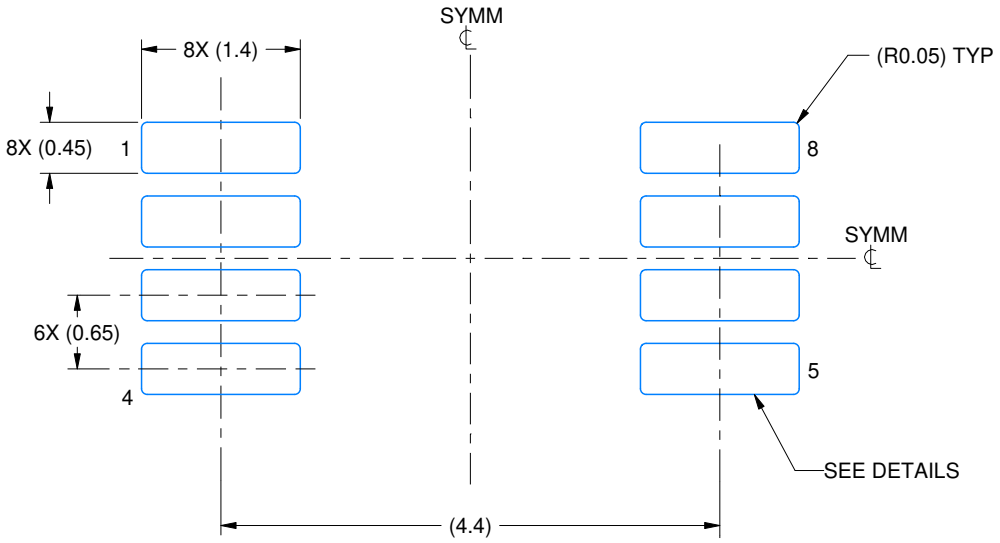


4214862/A 04/2023

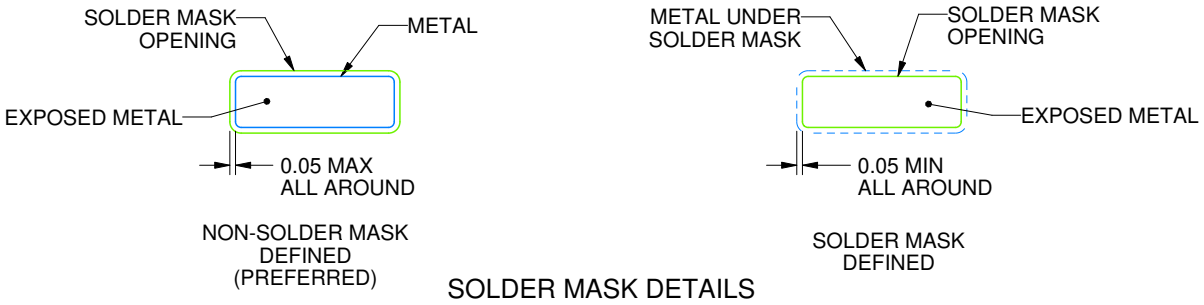
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

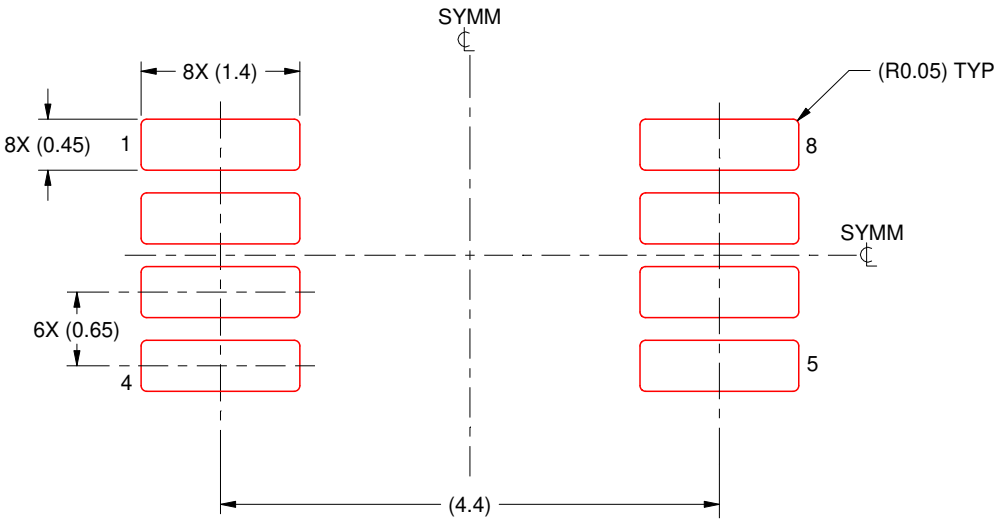


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

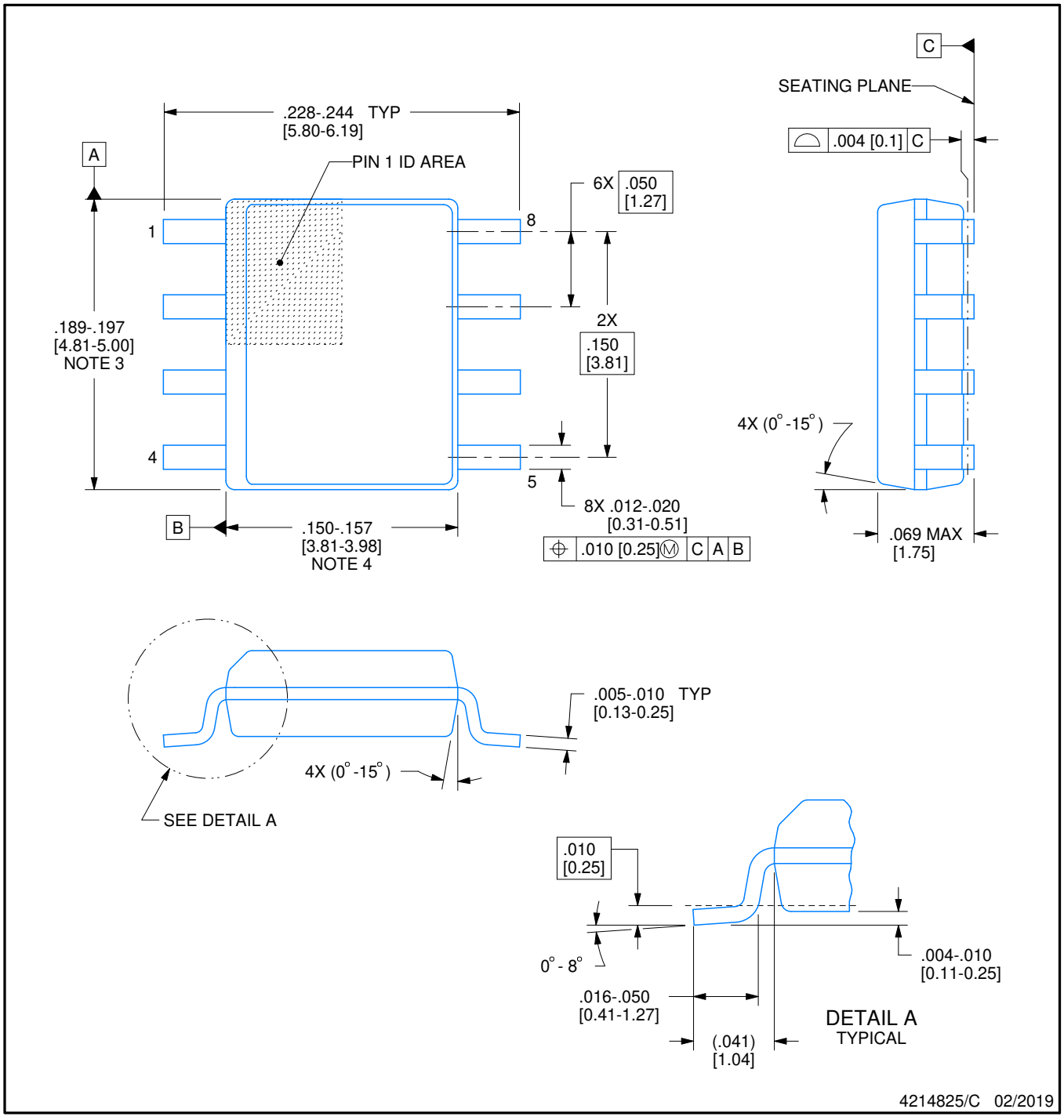


PACKAGE OUTLINE

D0008A

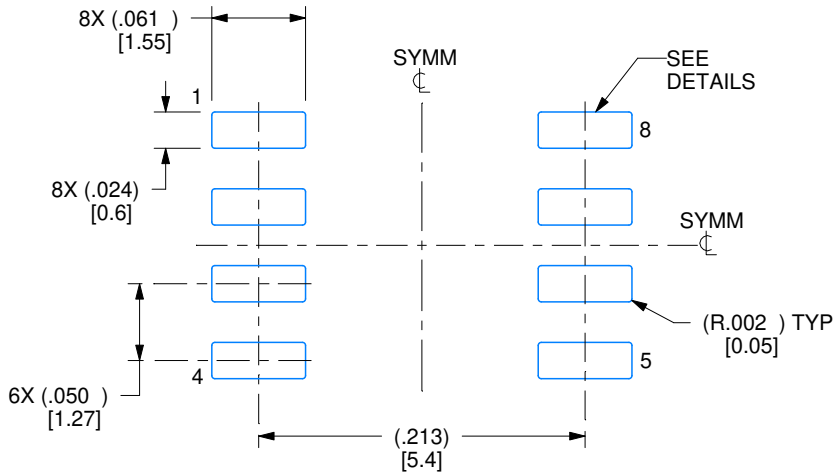
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

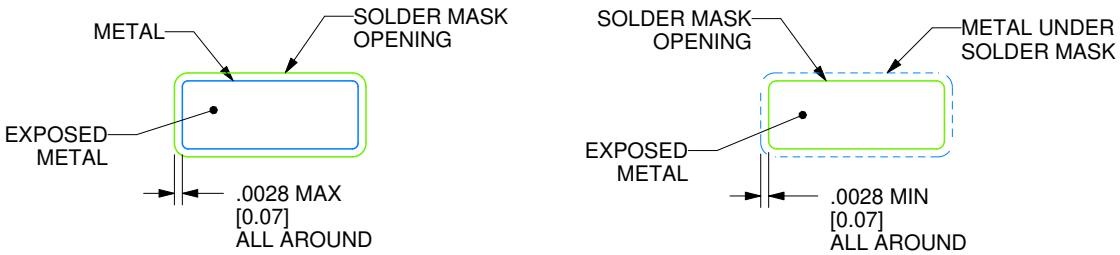


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

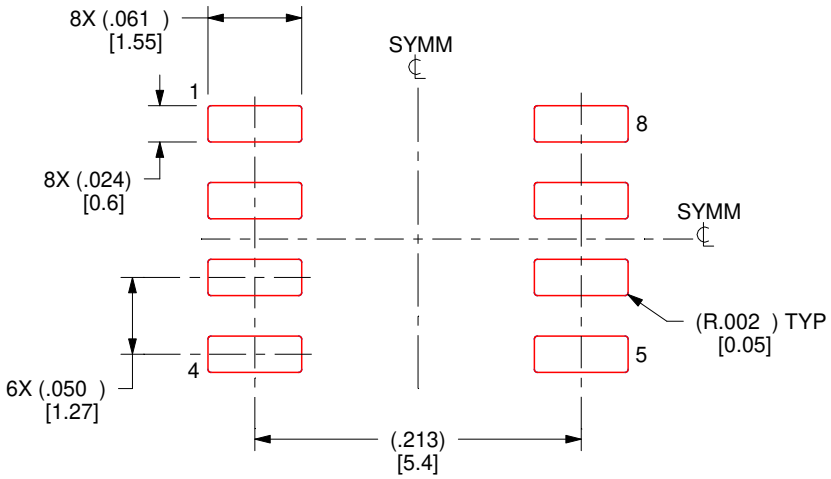
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

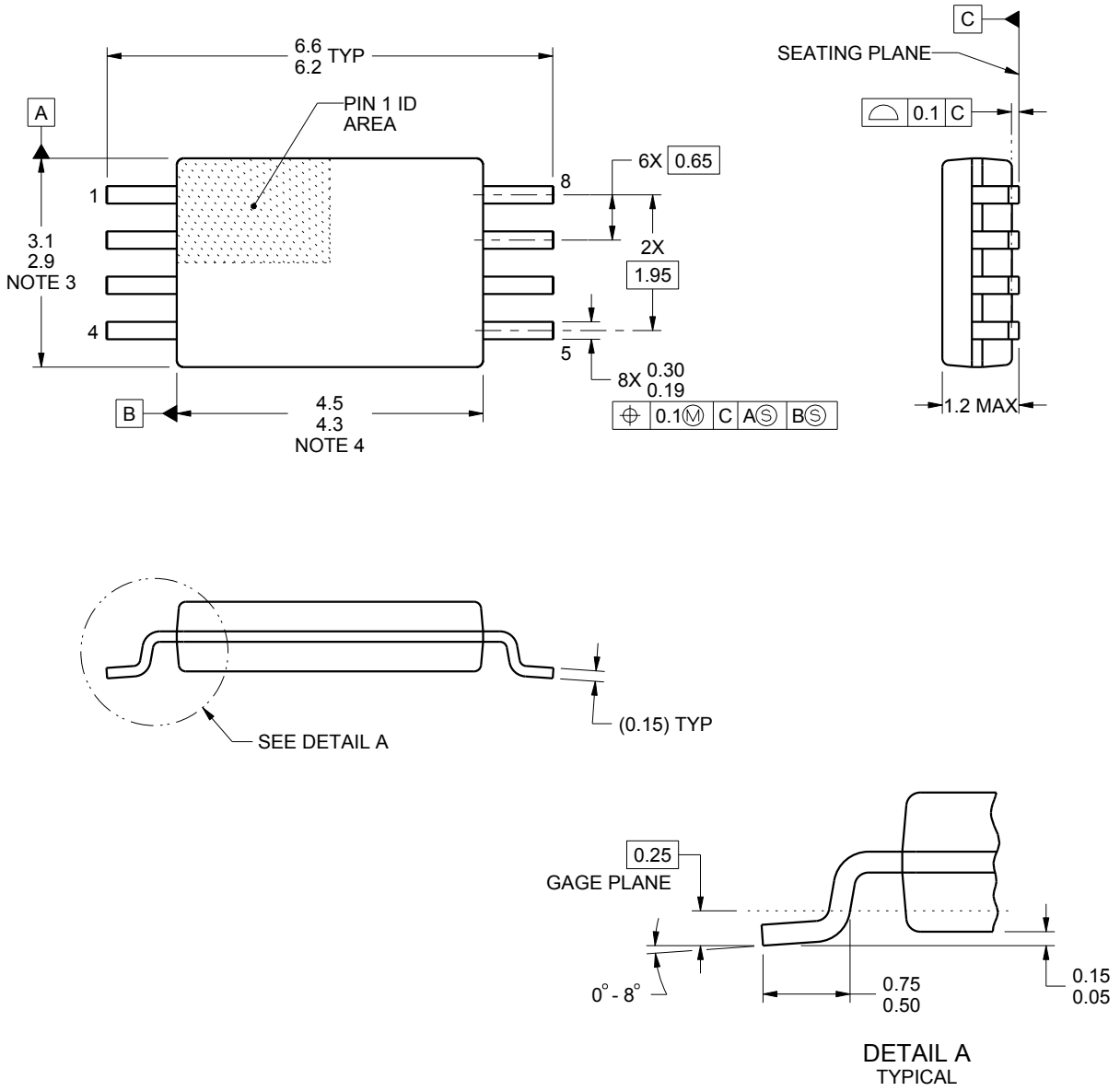


PACKAGE OUTLINE

PW0008A

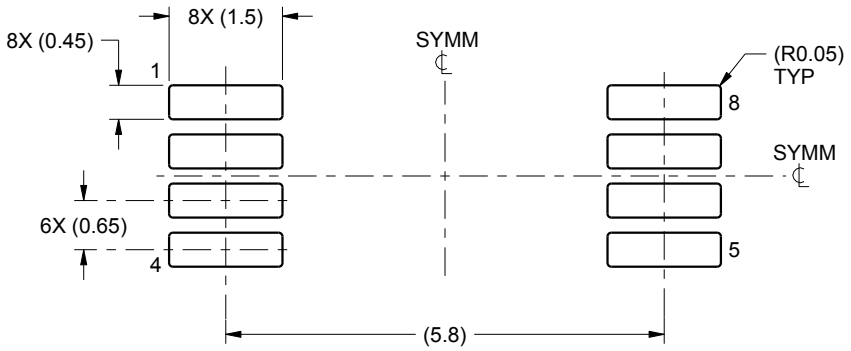
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

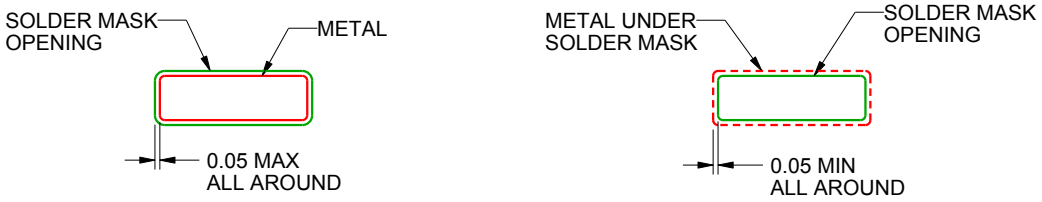


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

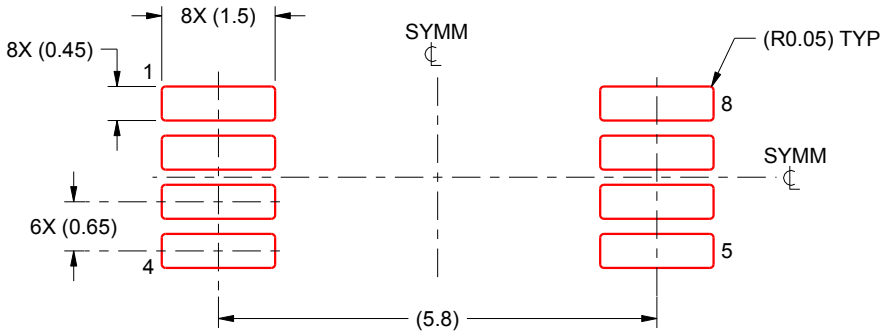


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025