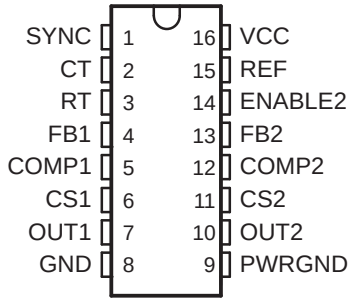
DUAL CHANNEL SYNCHRONIZED CURRENT-MODE PWM

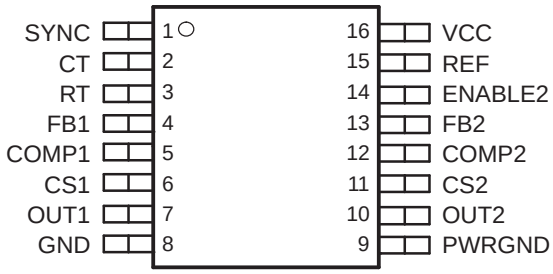
FEATURES

- **Single Oscillator Synchronizes Two PWMs**
- **150-µA Startup Supply Current**
- **2-mA Operating Supply Current**
- **Operation to 1 MHz**
- **Internal Soft-Start**
- **Full-Cycle Fault Restart**
- **Internal Leading-Edge Blanking of the Current Sense Signal**
- **1-A Totem Pole Outputs**
- **75-ns Typical Response from Current Sense to Output**
- **1.5% Tolerance Voltage Reference**

N PACKAGE
(TOP VIEW)



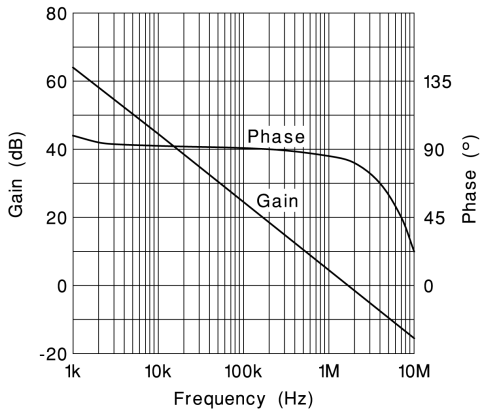
PW PACKAGE
(TOP VIEW)



DESCRIPTION

The UCC3810 is a high-speed BiCMOS controller integrating two synchronized pulse width modulators for use in off-line and dc-to-dc power supplies. The UCC3810 family provides perfect synchronization between two PWMs by usin g the same oscillator. The oscillator's sawtooth waveform can be used for slope compensation if required.

Using a toggle flip-flop to alternate between modulators, the UCC3810 ensures that one PWM does not slave, interfere, or otherwise affect the other PWM. This toggle flip- flop also ensures that each PWM is limited to 50% maximum duty cycle, insuring adequate off-time to reset magnetic elements. This device contains many of the same elements of the UC3842 current mode controller family, combined with the enhancements of the UCC3802. This minimizes power supply parts count. Enhancements include leading edge blanking of the current sense signals, full cycle fault restart, CMOS output drivers, and outputs which remain low even when the supply voltage is removed.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	PACKAGED DEVICES(1)	
	SOP (DW)	PDIP (N)
–40°C to 85°C	UCC2810DW (16)	UCC2810N (16)
0°C to 70°C	UCC3810DW (16)	UCC3810N (16)

(1) All packages are available taped and reeled (indicated by the R suffix on the device type e.g., UCC2810JR)

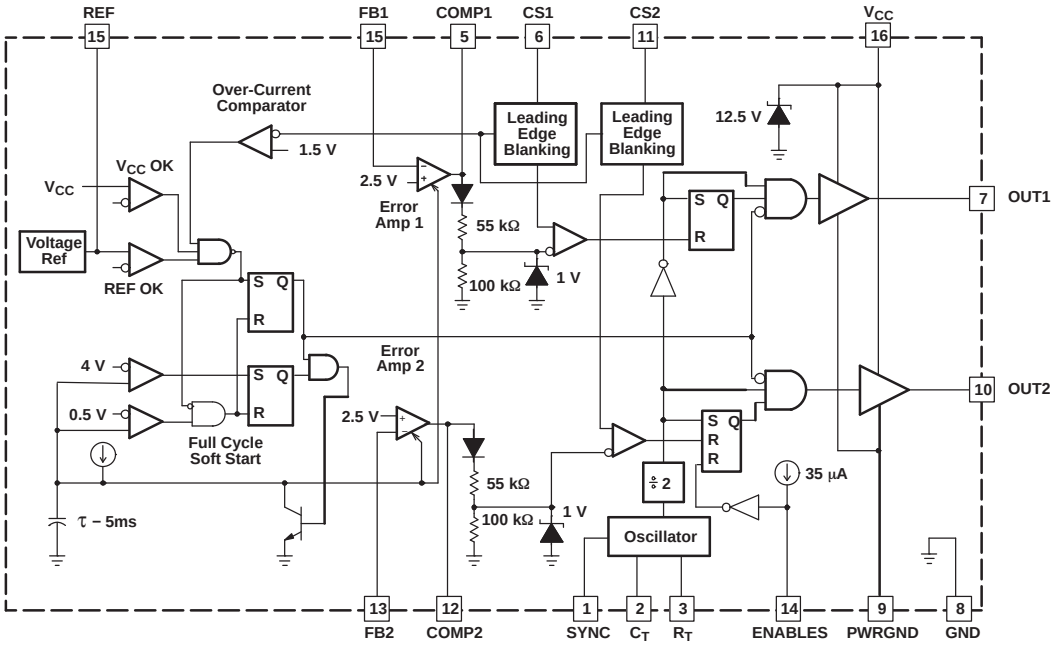
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		UNIT
V_{CC}	Supply voltage(3)	11V
I_{CC}	Supply current	20mA
	Output peak current, OUT1, OUT2, 5% duty cycle	±1A
	Output energy, OUT1, OUT2, capacitive load 20 µJ	20µJ
	Analog inputs, FB1, FB2, CS1, CS2, SYNC	–0.3 to 6.3V
T_J	Operating junction temperature	150°C
T_{stg}	Storage temperature range	–65 to 150°C
	Lead temperature (soldering, 10 sec)	300°C

(1) Currents are positive into, negative out of the specified terminal. All voltages are with respect to GND.
(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) In normal operation, V_{CC} is powered through a current-limiting resistor. Absolute maximum of 11 V applies when driven from a low impedance such that the V_{CC} current does not exceed 20 mA.

BLOCK DIAGRAM



VDG–92062–1

ELECTRICAL CHARACTERISTICS

All parameters are the same for both channels, –40°C ≤ T_A ≤ 85°C for the UCC2810, 0°C ≤ T_A ≤ 70°C for the UCC3810, V_{CC} = 10 V[1] ; R_T = 150 kΩ, C_T = 120 pF; no load; T_A = T_J; (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE							
V_{CC}	Output voltage	T_J = 25°C		4.925	5.000	5.075	V
		T_J = full range, 0 mA ≤ I_{REF} ≤ 5 mA		4.85	5.00	5.10	
	Load regulation	0 mA ≤ I_{REF} ≤ 5 mA			5	30	mV
	Line regulation	UVLO stop threshold voltage, 0.5 V ≤ V_{CC} ≤ V_{SHUNT}			12		
	Output noise voltage[2]	10Hz <f< 10 kHz,	T_J = 25°C		235		µV
	Long term stability[2]	TA = 125°C,	1000 hours		5		mV
$I_{O(SC)}$	Output short circuit current				-8	-25	mA
OSCILLATOR							
f_{OSC}	Oscillator frequency[3]	R_T = 30 kΩ,	C_T = 120 pF	860	980	1100	kHz
		R_T = 150 kΩ,	C_T = 120 pF	190	220	250	
	Temperature stability[2]				2.5%		
	Peak voltage				2.5		V
	Valley voltage				0.05		
	Peak-to-peak amplitude			2.25	2.45	2.65	
	SYNC threshold voltage			0.80	1.65	2.20	
	SYNC input current	SYNC = 5 V			30		µA
ERROR AMPLIFIER							
V_{FB}	FB input voltage	COMP = 2.5 V		2.44	2.50	2.56	V
I_{FB}	FB input bias current					±1	µA
	Open loop voltage gain			60	73		dB
f_{GAIN}	Unity gain bandwidth[2]				2		MHz
I_{SINK}	Sink current, COMP	FB = 2.7 V,	COMP = 1 V	0.3	1.4	3.5	
I_{SRCE}	Source current, COMP	FB = 1.8 V,	COMP = 4 V	-0.2	-0.5	-0.8	mA
	Minimum duty cycle	COMP = 0 V				0%	
	Soft-start rise time, COMP	FB = 1.8 V, Rise from 0.5 V to (REF – 1.5 V)				5	ms
CURRENT SENSE							
	Gain[4]			1.20	1.55	1.80	V/V
	Maximum input signal[5]	COMP = 5 V		0.9	1.0	1.1	V
I_{CS}	Input bias current, CS					±200	nA
	Propagation delay time (CS to OUT)	CS steps from 0 V to 1.2 V, COMP = 2.5 V			75		ns
	Blank time, CS[6]				55		
	Overcurrent threshold voltage, CS			1.35	1.55	1.85	V
	COMP-to-CS offset voltage	CS = 0 V		0.45	0.90	1.35	

(1) For UCC3810, adjust V_{CC} above the start threshold before setting at 10 V.
(2) Ensured by design. Not production tested.

$$f_{OSC} = \frac{4}{R_T \times C_T}$$

(3) Oscillator frequency is twice the output frequency.

$$A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$$

(4) Current sense gain A is defined by: , 0 V ≤ V_{CS} ≤ 0.8 V.
(5) Parameter measured at trip point of latch with FB = 0 V.
(6) CS blank time is measured as the difference between the minimum non-zero on-time and the CS-to-OUT delay.

ELECTRICAL CHARACTERISTICS (continued)

All parameters are the same for both channels, –40°C ≤ T_A ≤ 85°C for the UCC2810, 0°C ≤ T_A ≤ 70°C for the UCC3810, V_{CC} = 10 V ; R_T = 150 kΩ, C_T = 120 pF; no load; T_A = T_J; (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PWM							
	Maximum duty cycle(2)	R_T = 150 kΩ,	C_T = 120 pF	45%	49%	50%	
		R_T = 30 kΩ,	C_T = 120 pF	40%	45%	48%	
	Minimum on-time	CS = 1.2 V,	COMP = 5 V		130		ns
OUTPUT							
V_{OL}	Low-level output voltage	I_{OUT} = 20 mA			0.12	0.42	V
		I_{OUT} = 200 mA			0.48	1.10	
		I_{OUT} = 20 mA,	V_{CC} = 0 V		0.7	1.2	
V_{OH}	High-level output voltage (V_{CC} – OUT)	I_{OUT} = –20 mA			0.15	0.42	
		I_{OUT} = –200 mA			1.2	2.3	
t_R	Rise time, OUT	C_{OUT} = 1 nF			20	50	ns
t_F	Fall time, OUT	C_{OUT} = 1 nF			30	60	
UNDERVOLTAGE LOCKOUT (UVLO)							
	Start threshold voltage			9.6	11.3	13.2	V
	Stop threshold voltage			7.1	8.3	9.5	
	Start-to-stop hysteresis			1.7	3.0	4.7	
	ENABLE2 input bias current	ENABLE2 = 0 V		-20	-35	-55	µA
	ENABLE2 input threshold voltage			0.80	1.53	2.00	V
OVERALL							
	Startup current	V_{CC} < Start threshold voltage			0.15	0.25	mA
	Operating supply current, outputs off	VCC = 10 V,	FB = 2.75 V		2	3	
	Operating supply current, outputs on	VCC = 10 V, CS = 0 V,	FB = 0 V, RT = 150 kΩ		3.2	5.1	
		VCC = 10 V, CS = 0 V,	FB = 0 V, RT = 30 kΩ		8.5	14.5	
	VCC internal zener voltage	I_{CC} = 10 mA		11.0	12.9	14.0	V
	VCC internal zener voltage minus start threshold voltage			0.4	1.2		

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
COMP1	5	O	Low impedance output of the error amplifiers.
COMP2	12	O	
CS1	6	I	Current sense inputs to the PWM comparators. These inputs have leading edge blanking. For most applications, no input filtering is required. Leading edge blanking disconnects the CS inputs from all internal circuits for the first 55 ns of each PWM cycle. When used with very slow diodes or in other applications where the current sense signal is unusually noisy, a small current-sense R-C filter may be required.
CS2	11	I	
CT	2	O	The timing capacitor of the oscillator. Recommended values of CT are between 100 pF and 1 nF. Connect the timing capacitor directly across CT and GND.
ENABLE2	14	I	A logic input which disables PWM 2 when low. This input has no effect on PWM 1. This input is internally pulled high. In most applications it can be left floating. In unusually noisy applications, the input should be bypassed with a 1-nF ceramic capacitor. This input has TTL compatible thresholds.
FB1	4	I	The high impedance inverting inputs of the error amplifiers.
FB2	13	I	
GND	8	–	To separate noise from the critical control circuits, this part has two different ground connections: GND and PWRGND. GND and PWRGND must be electrically connected together. However, use care to avoid coupling noise into GND.
OUT1	7	O	The high-current push-pull outputs of the PWM are intended to drive power MOSFET gates through a small resistor. This resistor acts as both a current limiting resistor and as a damping impedance to minimize ringing and overshoot.
OUT2	10	O	
PWRGND	9	–	To separate noise from the critical control circuits, this part has two different ground connections: GND and PWRGND. GND and PWRGND must be electrically connected together.
REF	15	O	The output of the 5-V reference. Bypass REF to GND with a ceramic capacitor ≥ 0.01-µF for best performance.
RT	3	O	The oscillator charging current is set by the value of the resistor connected from RT to GND. This pin is regulated to 1 V, but the actual charging current is 10 V/RT. Recommended values of RT are between 10 kΩ and 470 kΩ. For a given frequency, higher timing resistors give higher maximum duty cycle and slightly lower overall power consumption.
SYNC	1	I	This logic input can be used to synchronize the oscillator to a free running oscillator in another part. This pin is edge triggered with TTL thresholds, and requires at least a 10-ns-wide pulse. If unused, this pin can be grounded, open circuited, or connected to REF.
VCC	16	I	The power input to the device. This pin supplies current to all functions including the high current output stages and the precision reference. Therefore, it is critical that VCC be directly bypassed to PWRGND with an 0.1-µF ceramic capacitor.

APPLICATION INFORMATION

TIMING RESISTOR

Supply current decreases with increased R_T by the relationship:

$$\Delta I_{CC} = \frac{11V}{R_T}$$

For more information, see the detailed oscillator block diagram.

LEADING EDGE BLANKING AND CURRENT SENSE

Figure 1 shows how an external power stage is connected to the UCC3810. The gate of an external power N-channel MOSFET is connected to OUT through a small current-limiting resistor. For most applications, a 10-Ω resistor is adequate to limit peak current and also practical at damping resonances between the gate driver and the MOSFET input reactance. Long gate lead length increases gate capacitance and mandates a higher series gate resistor to damp the R-L-C tank formed by the lead, the MOSFET input reactance, and the device's driver output resistance.

The UCC3810 features internal leading edge blanking of the current-sense signal on both current sense inputs. The blank time starts when OUT rises and continues for 55 ns. During that 55 ns period, the signal on CS is ignored. For most PWM applications, this means that the CS input can be connected to the current-sense resistor as shown in Figure 1. However, high speed grounding practices and short lead lengths are still required for good performance.

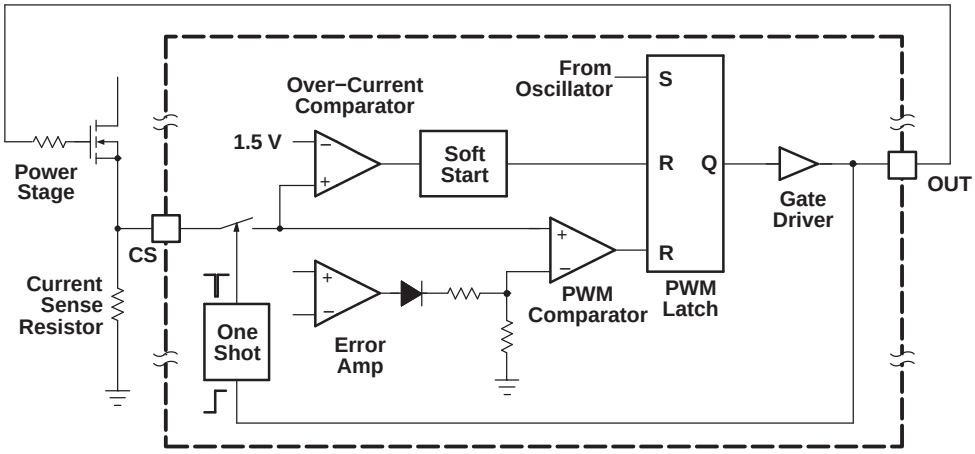


Figure 1. Detailed Block Diagram

OSCILLATOR

The UCC3810 oscillator generates a sawtooth wave at CT. The sawtooth rise time is set by the resistor from RT to GND. Since R_T is biased at 1 V, the current through R_T is 1 V/R_T. The actual charging current is 10 times higher. The fall time is set by an internal transistor on-resistance of approximately 100 Ω. During the fall time, all outputs are off and the maximum duty cycle is reduced to below 50%. Larger timing capacitors increase the discharge time and reduce frequency. However, the percentage maximum duty cycle is only a function of the timing resistor R_T, and the internal 100-Ω discharge resistance.

ERROR AMPLIFIER OUTPUT STAGE

The UCC3810 error amplifiers are operational amplifiers with low-output resistance and high-input resistance. The output stage of one error amplifier is shown in Figure 3. This output stage allows the error amplifier output to swing close to GND and as high as one diode drop below 5 V with little loss in amplifier performance.

APPLICATION INFORMATION (continued)

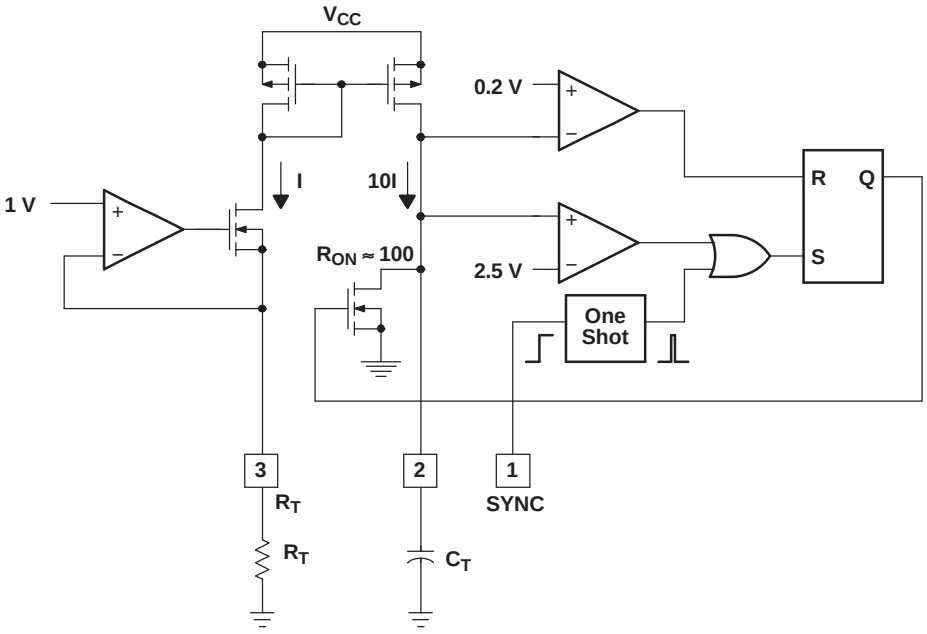


Figure 2. Oscillator

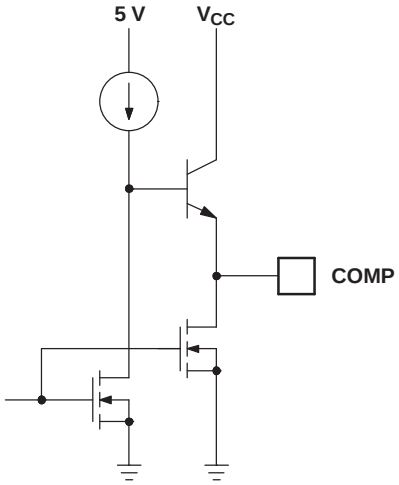


Figure 3. Error Amplifier Output Stage

TYPICAL CHARACTERISTICS

ERROR AMPLIFER GAIN AND PHASE
vs
FREQUENCY

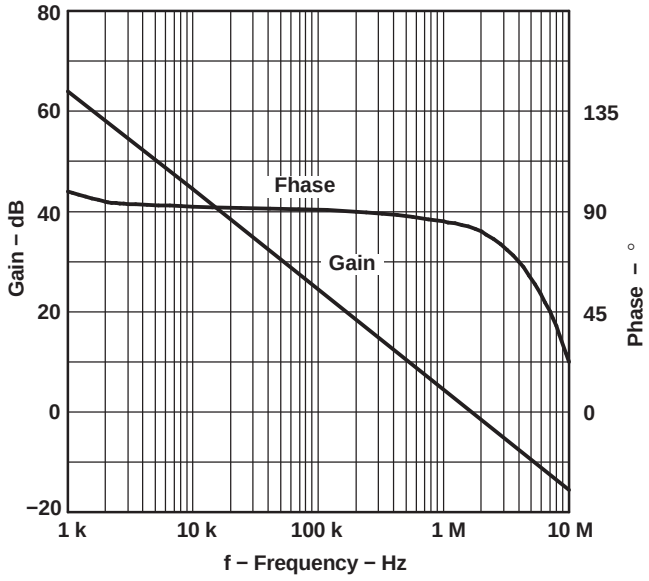


Figure 4.

OSCILLATOR FREQUENCY
vs
TIMING RESISTANCE

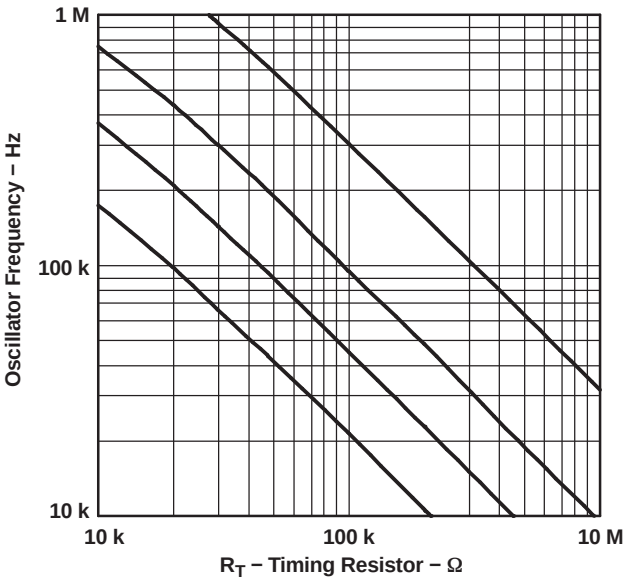


Figure 5.

OSCILLATOR FREQUENCY
vs
TEMPERATURE

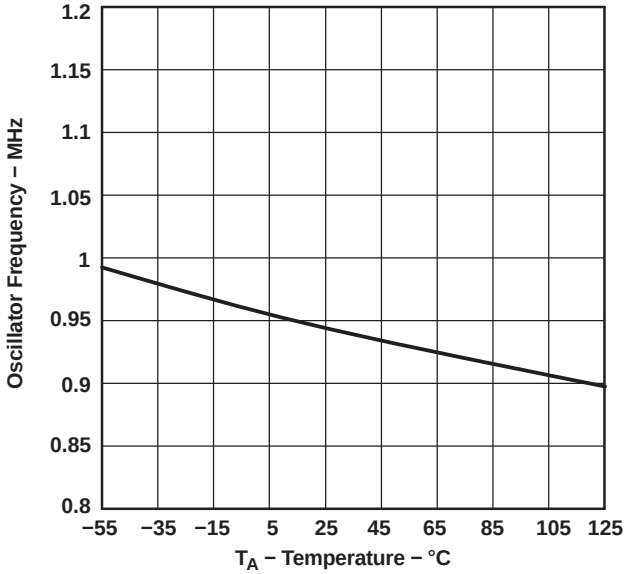


Figure 6.

MAXIMUM DUTY CYCLE
vs
TIMING RESISTANCE

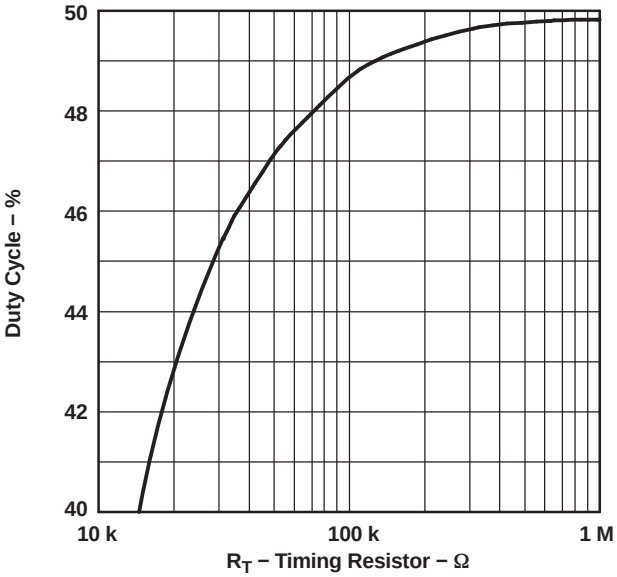


Figure 7.

TYPICAL CHARACTERISTICS (continued)

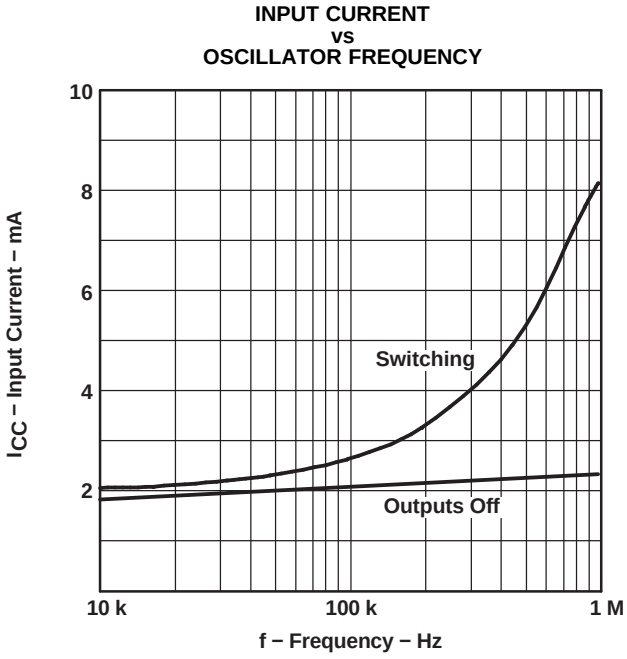


Figure 8.

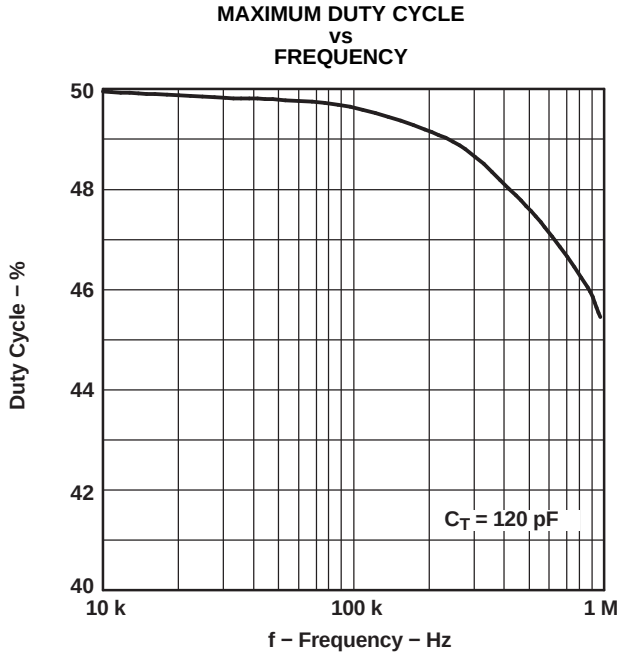


Figure 9.

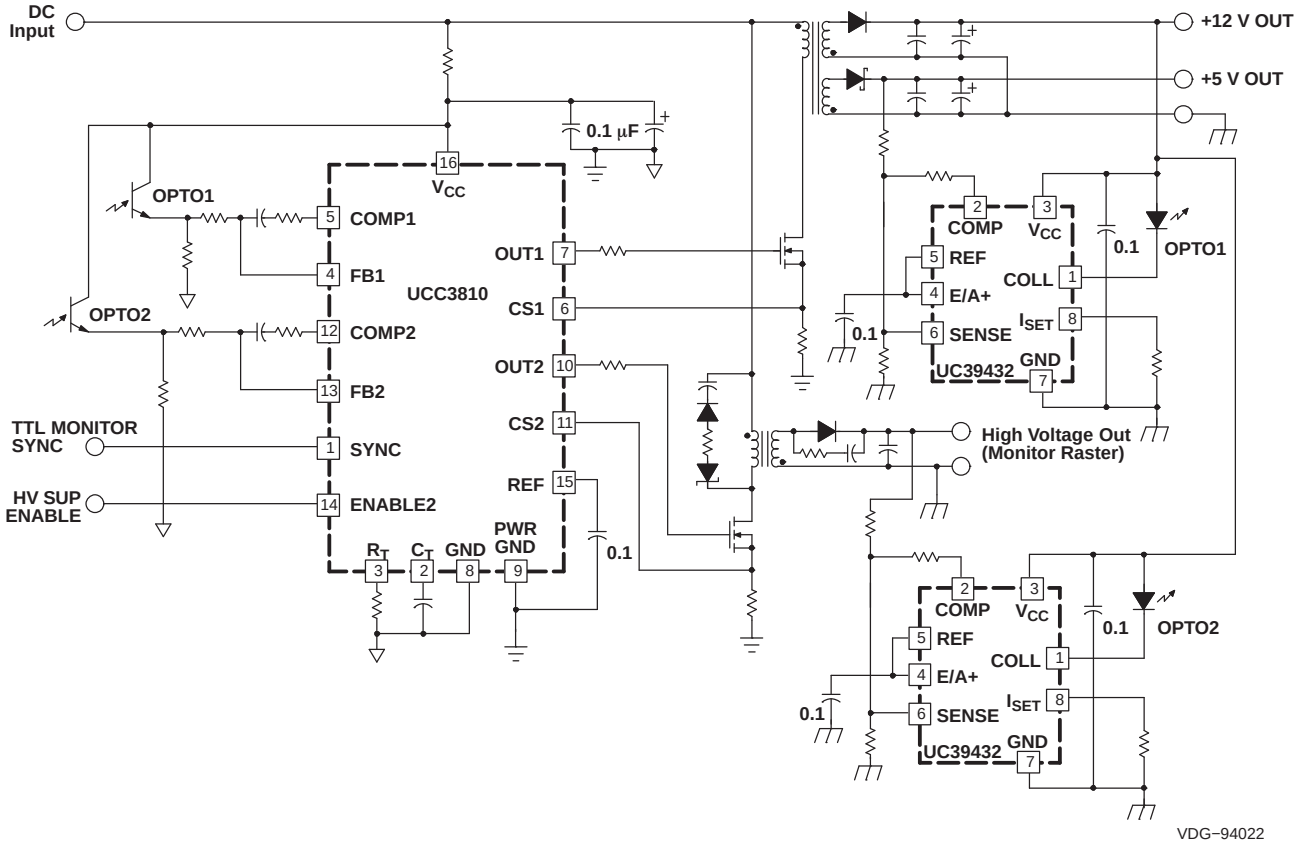


Figure 10. Typical Application

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2810DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2810DW
UCC2810DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2810DW
UCC2810DWG4	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2810DW
UCC2810DWTR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2810DW
UCC2810DWTR.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2810DW
UCC2810DWTRG4	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2810DW
UCC2810N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UCC2810N
UCC2810N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UCC2810N
UCC2810NG4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UCC2810N
UCC3810DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3810DW
UCC3810DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3810DW
UCC3810DWTR	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3810DW
UCC3810DWTR.A	NRND	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3810DW
UCC3810N	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC3810N
UCC3810N.A	NRND	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UCC3810N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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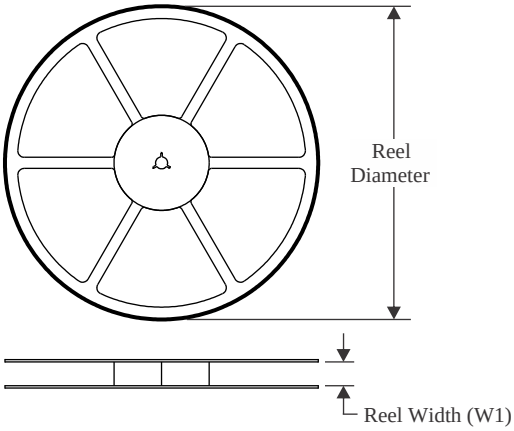
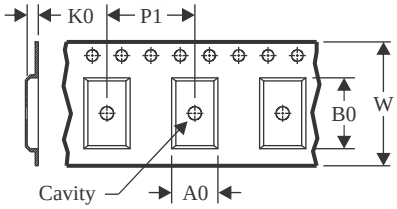
TAPE AND REEL INFORMATION

REEL DIMENSIONS

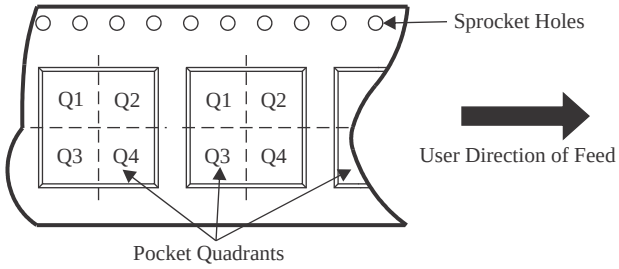


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

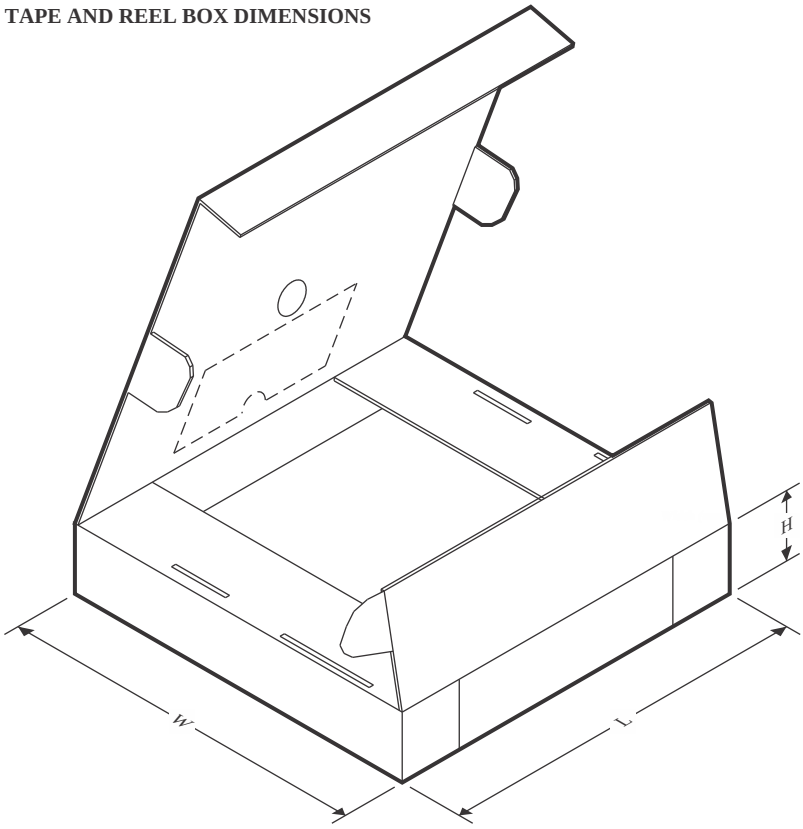
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2810DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UCC3810DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

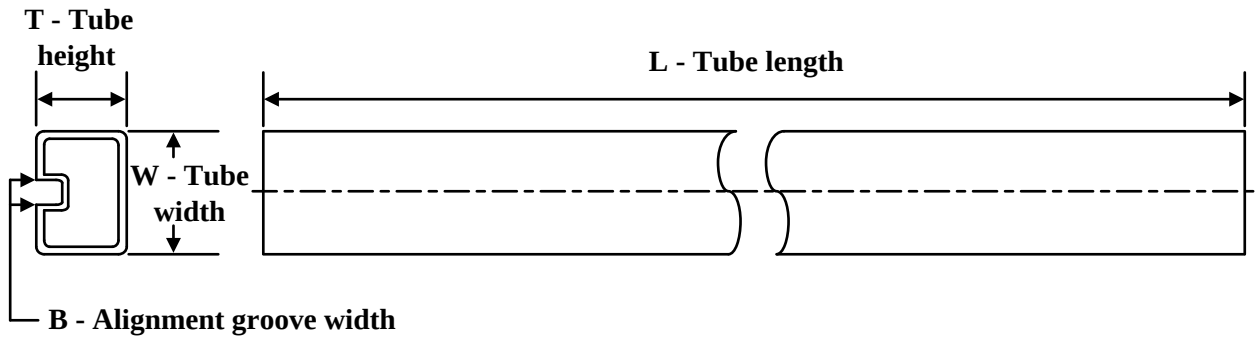
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2810DWTR	SOIC	DW	16	2000	353.0	353.0	32.0
UCC3810DWTR	SOIC	DW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC2810DW	DW	SOIC	16	40	507	12.83	5080	6.6
UCC2810DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UCC2810DWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UCC2810N	N	PDIP	16	25	506	13.97	11230	4.32
UCC2810N.A	N	PDIP	16	25	506	13.97	11230	4.32
UCC2810NG4	N	PDIP	16	25	506	13.97	11230	4.32
UCC3810DW	DW	SOIC	16	40	507	12.83	5080	6.6
UCC3810DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UCC3810N	N	PDIP	16	25	506	13.97	11230	4.32
UCC3810N.A	N	PDIP	16	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

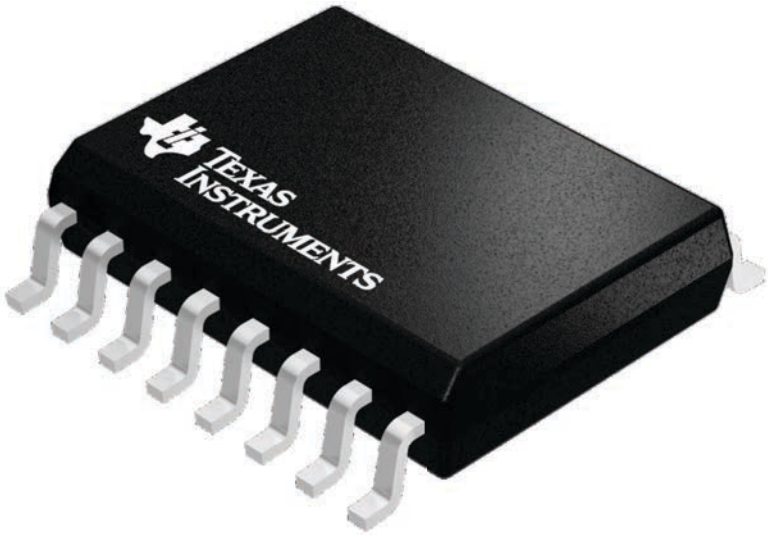
DW 16

SOIC - 2.65 mm max height

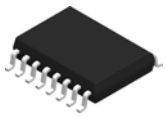
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

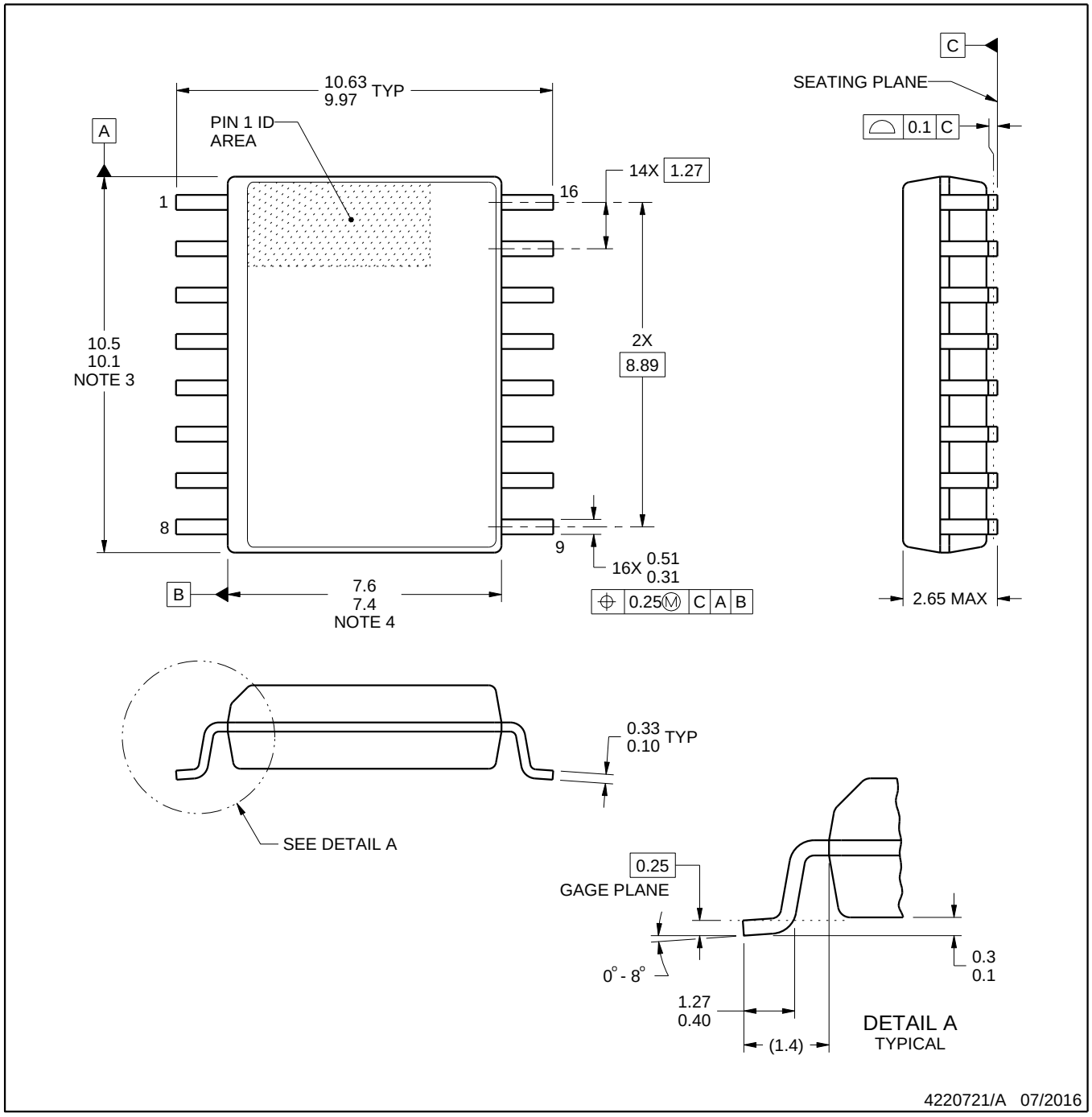


PACKAGE OUTLINE

DW0016A

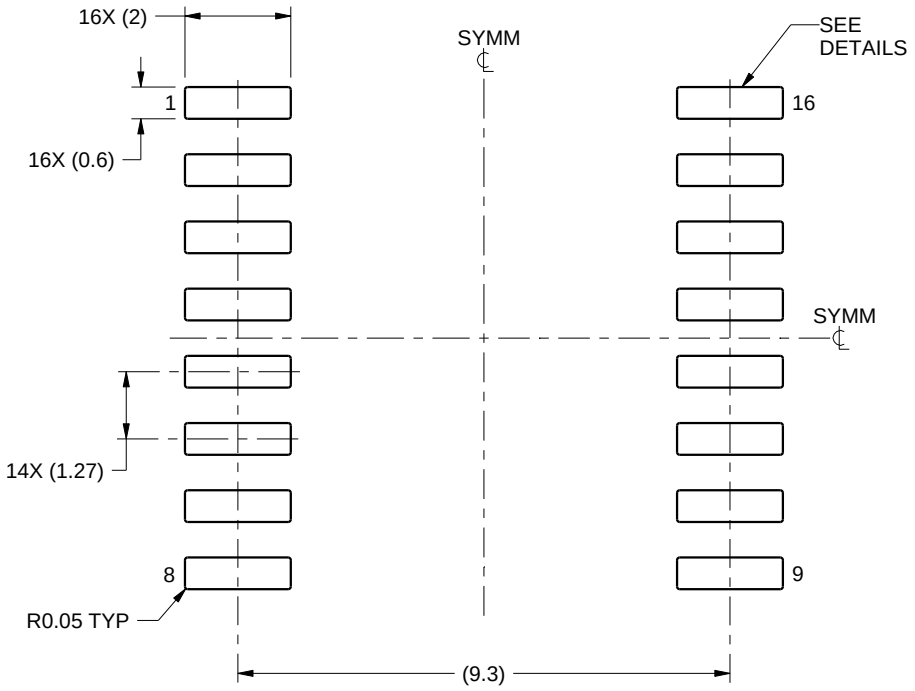
SOIC - 2.65 mm max height

SOIC

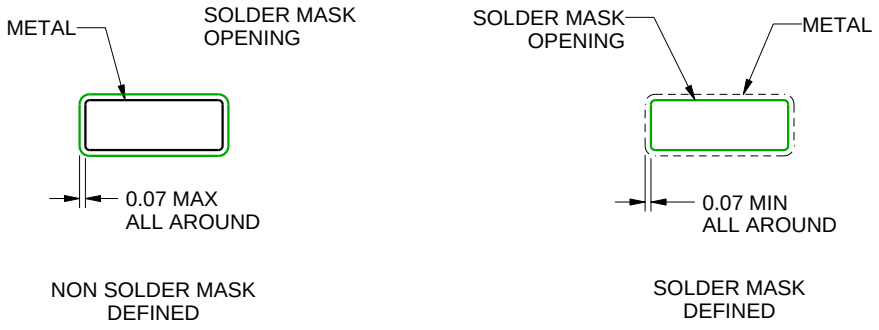


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

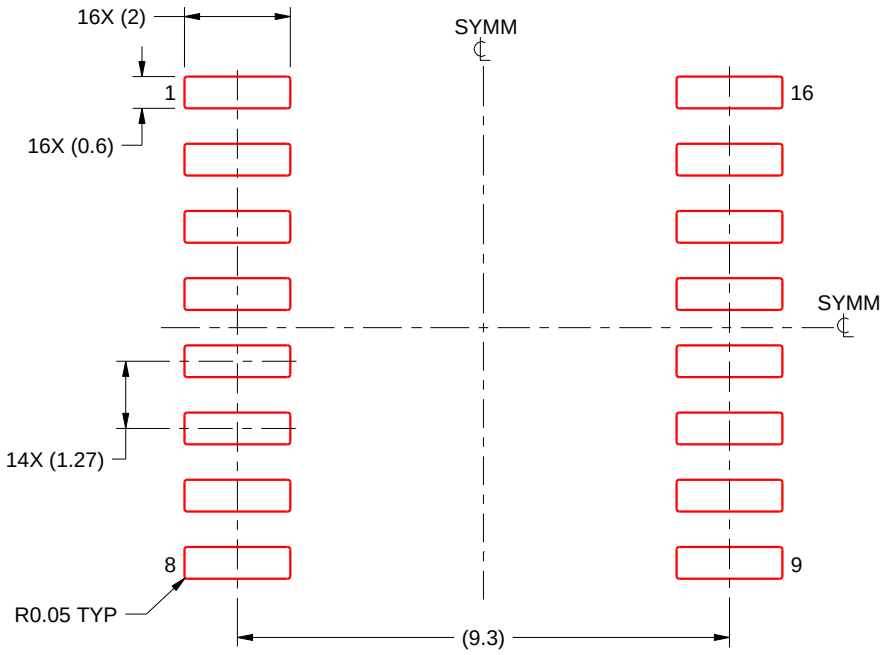


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

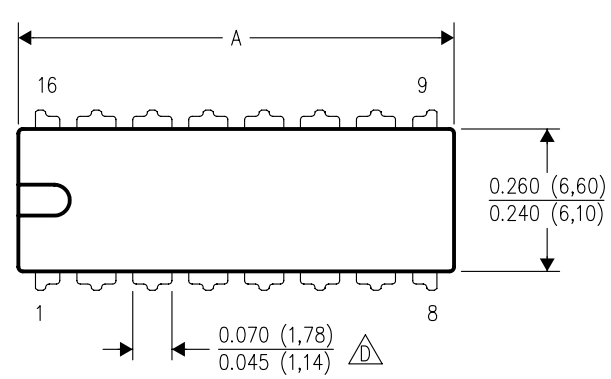
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

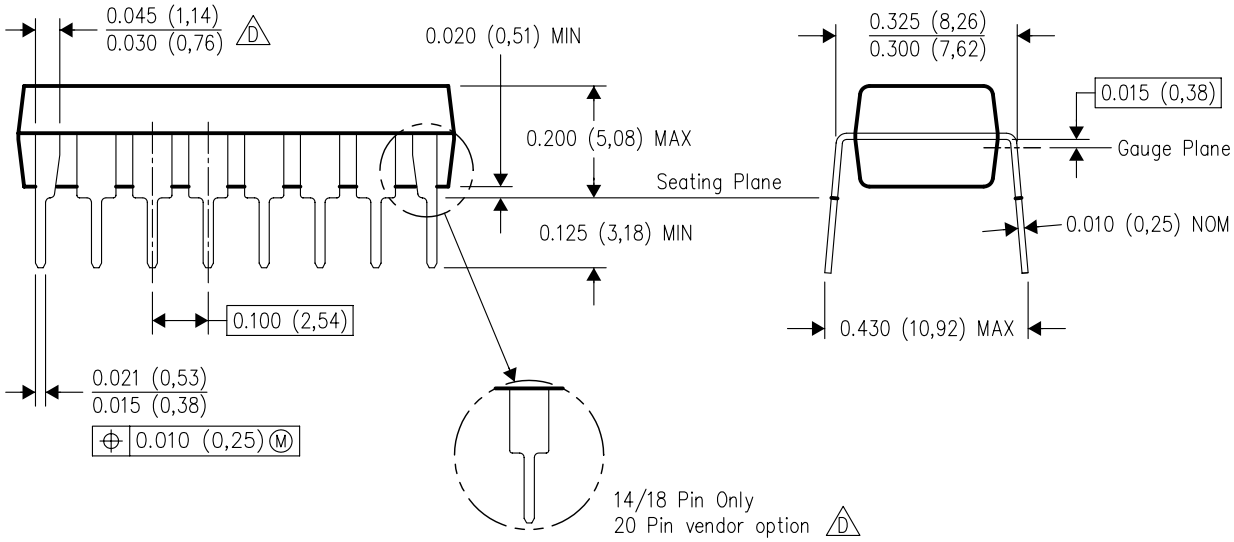
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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