UCD3138064A Highly Integrated Digital Controller for Isolated Power

1 Device Overview

1.1 Features

- 64 kB Program Flash Derivative of UCD3138 Family
  - 2-32 kB Program Flash Memory Banks
  - Supports Execution From 1 Bank, While Programming Another
  - Capability to Update Firmware Without Shutting Down the Power Supply
  - Additional Communication Ports Compared to the UCD3138 (+1 SPI, +1 I2C)
  - Pin-to-Pin Compatible with UCD3138 (SLUSAP2B)
- Digital Control of up to 3 Independent Feedback Loops
  - Dedicated PID Based Hardware
  - 2-pole/2-zero Configurable
  - Non-Linear Control
- Soft Start / Stop with and without Prebias
- Fast Input Voltage Feed Forward Hardware
- Synchronous Rectifier Dead Time Optimization Peripheral to Use with UCD7138 Synchronous Rectifier Driver
- Up to 16 MHz Error A/D Converter (EADC)
  - Configurable Resolution as Small as 1 mV/LSB
  - Up to 8x Oversampling
  - Hardware Based Averaging (Up to 8x)
  - 14 bit Effective DAC With 4 Bits of Dither
  - Adaptive Trigger Positioning
- Up to 8 High Resolution Digital Pulse Width Modulated (DPWM) Outputs
  - 250 ps Pulse Width Resolution
  - 4 ns Frequency and Phase Resolution
  - Adjustable Phase Shift Between Outputs
  - Adjustable Dead-band Between Pairs
  - Cycle-by-Cycle Duty Cycle Matching
  - Up to 2 MHz Switching Frequency
- Configurable Trailing/Leading/Triangular Modulation
- Configurable Feedback Control
  - Voltage, Average Current and Peak Current Mode Control
  - Constant Current, Constant Power
- Configurable FM, Phase Shift Modulation and PWM
- Fast, Automatic and Smooth Mode Switching
  - Frequency Modulation and PWM
  - Phase Shift Modulation and PWM
  - Frequency Modulation and Phase Shift Modulation
- High Efficiency and Light Load Management
  - Burst Mode
  - Ideal Diode Emulation
  - Synchronous Rectifier Soft On/Off
  - Low Device Standby Power
- Primary Side Voltage Sensing
- Flux and Phase Current Balancing
- Current Share (Average & Master/Slave)
- Feature Rich Fault Protection Options
  - 7 Analog / 4 Digital Comparators
  - Cycle-by-Cycle Current Limiting
  - Programmable Blanking Time and Fault Counting
  - External Fault Inputs
- Synchronization of DPWM Waveforms Between Multiple UCD3138064A Devices
- 14 channel, 12 bit, 267 ksps General Purpose ADC with Integrated
  - Programmable Averaging Filters
  - Dual Sample and Hold
- Internal Temperature Sensor
- Fully Programmable High-Performance 31.25 MHz, 32-bit ARM7TDMI-S Processor
  - 64 kB Program Flash (2-32 kB Banks)
  - 2 kB Data Flash with ECC
  - 4 kB Data RAM
  - 8 kB Boot ROM
  - Firmware Boot-Load in the Field via I^2C or UART
- Communication Peripherals
  - 1 - I^2C/PMBus, 1 - I^2C (master mode only)
  - 2 - UARTs
  - 1 - SPI
- UART Auto-baud Rate Adjustment
- Timer Capture with Selectable Input Pins
- Built In Watchdog: BOD and POR
- 64-pin QFN and 48-pin QFN Packages
- Operating Temperature: –40°C to +125°C
- Debug interface
  - Code Composer Studio™ with JTAG Interface
  - Fusion Digital Power™ Designer GUI Support

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.2 Applications

- Power Supplies and Telecom Rectifiers
- Power Factor Correction
- Isolated DC-DC Modules

1.3 Description

The UCD3138064A is a digital power supply controller from Texas Instruments offering superior levels of integration and performance in a single-chip solution. The UCD3138064A, in comparison to Texas Instruments UCD3138 digital power controller (Section 3), offers 64 kB of program Flash memory (vs 32 kB in UCD3138) and additional options for communication such as SPI and a second I^2C port. The availability of 64 kB of program Flash memory in 2-32 kB banks, enables the designers to implement dual images of firmware (e.g. one main image + one back-up image) in the device and the flexibility to execute from either of the banks using appropriate algorithms. It also creates the unique opportunity for the processor to load a new program and subsequently execute that program without interrupting power delivery. This feature allows the end user to add new features to the power supply in the field while eliminating any down-time required to load the new program.

The flexible nature of the UCD3138064A makes it suitable for a wide variety of power conversion applications. In addition, multiple peripherals inside the device have been specifically optimized to enhance the performance of AC/DC and isolated DC/DC applications and reduce the solution component count in the IT and network infrastructure space. The UCD3138064A is a fully programmable solution offering customers complete control of their application, along with ample ability to differentiate their solution. At the same time, TI is committed to simplifying our customers' development effort through offering best in class development tools, including application firmware, Code Composer Studio™ software development environment, and TI's Fusion Power Development GUI which let customers configure and monitor key system parameters.

At the core of the UCD3138064A controller are the Digital Power Peripherals (DPP). Each DPP implements a high-speed digital control loop consisting of a dedicated Error Analog-to-Digital Converter (EADC), a PID-based 2-pole/general-purpose ADC with up to 14 channels2-zero digital compensator and DPWM outputs with 250-ps pulse width resolution. The device also contains a 12-bit, 267-ksps general-purpose ADC with up to 14 channels, timers, interrupt control, PMBus, I^2C, SPI and UART communications ports. The device is based on a 32-bit ARM7TDMI-S RISC microcontroller that performs real-time monitoring, configures peripherals, and manages communications. The ARM microcontroller executes its program out of programmable flash memory as well as on chip RAM and ROM.

In addition to the DPP, specific power management peripherals have been added to enable high efficiency across the entire operating range, high integration for increased power density, reliability, and lowest overall system cost and high flexibility with support for the widest number of control schemes and topologies. Such peripherals include: light load burst mode, synchronous rectification, automatic mode switching, input voltage feed forward, copper trace current sense, ideal diode emulation, constant current constant power control, synchronous rectification soft on and off, peak current mode control, flux balancing, secondary side input voltage sensing, high-resolution current sharing, hardware-configurable soft start with pre bias, as well as several other features. Topology support has been optimized for voltage mode and peak current mode controlled phase shifted full bridge, single and dual phase PFC, bridgeless PFC, hard switched full bridge and half bridge, and LLC half bridge and full bridge.

The UCD3138064A is a functional variant of the UCD3138064A Digital Power Controller that includes significant improvements over the UCD3138064. For a description of the complete changes made in the UCD3138064A, refer to *UCD3138064A Migration Guide*. The major improvements are:

The General Purpose ADC has been improved for better accuracy and performance at extreme cold temperatures (–40°C).

The UART peripheral has been modified to include a hardware based auto-baud rate adjustment feature.

A new Synchronous Rectifier Dead Time Optimization hardware peripheral has been added. Benefits include:

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– Improved efficiency
– Reduced synchronous rectifier voltage stresses
– Shorter development cycle

A Duty Cycle Read Function has been added to improve use in peak current mode.

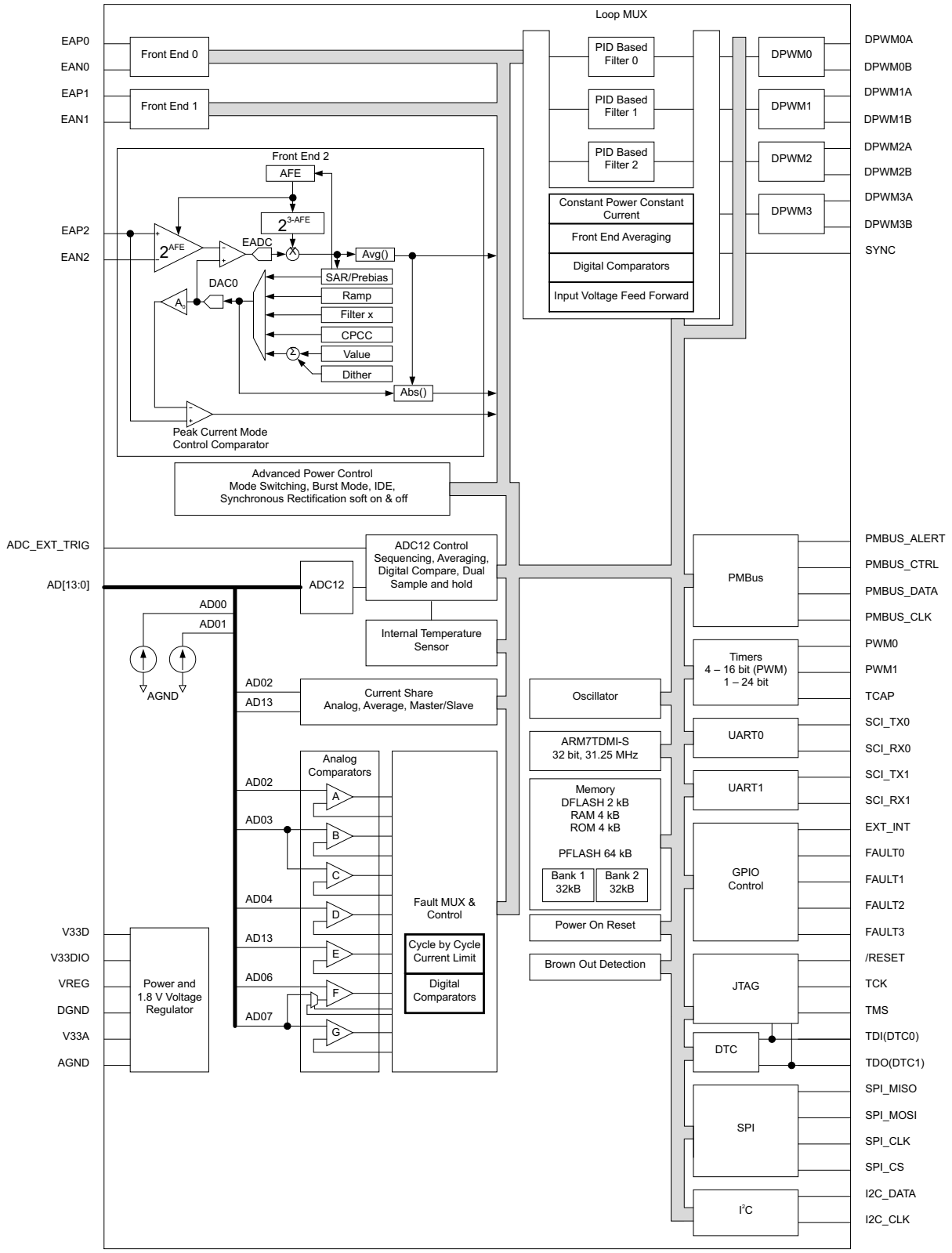
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCD3138064A	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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1.4 Functional Block Diagram



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Figure 1-1. Functional Block Diagram

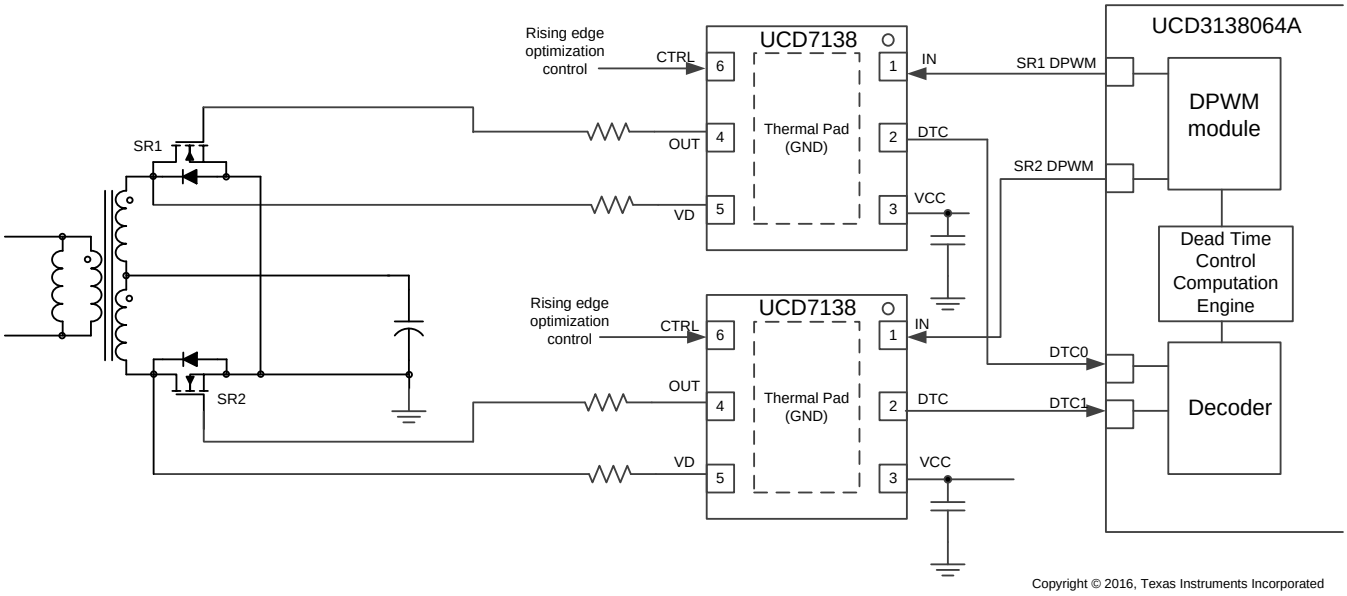


Figure 1-2. Synchronous Rectifier Peripheral use with Synchronous Rectifier Driver

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2015) to Revision A	Page
• Deleted WQFN (40) from the *Device Information* table	3
• Deleted the 3138064, 3138064A RMH (40 Pin) column from the *Device Comparison Table*	7
• Deleted the *Product Selection Matrix* table	7
• Deleted the 40-Pin QFN RMH Package from the *Pin Diagrams* section	8
• Deleted VQFN (RGZ) and WQFN (RMH) packages from the *Thermal Information* table	11
• Added updated V33 slew rate values in the Device Grounding and Layout Guidelines section.	73
• Changed the capacitor value from 0.22 µF to 2.2 µF.	73
• Added BP18 decoupling requirements updated	73
• Added GPIO settings for unused pins	74
• Changed New PCB Layout image	74

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3 Device Options

3.1 Device Comparison Table

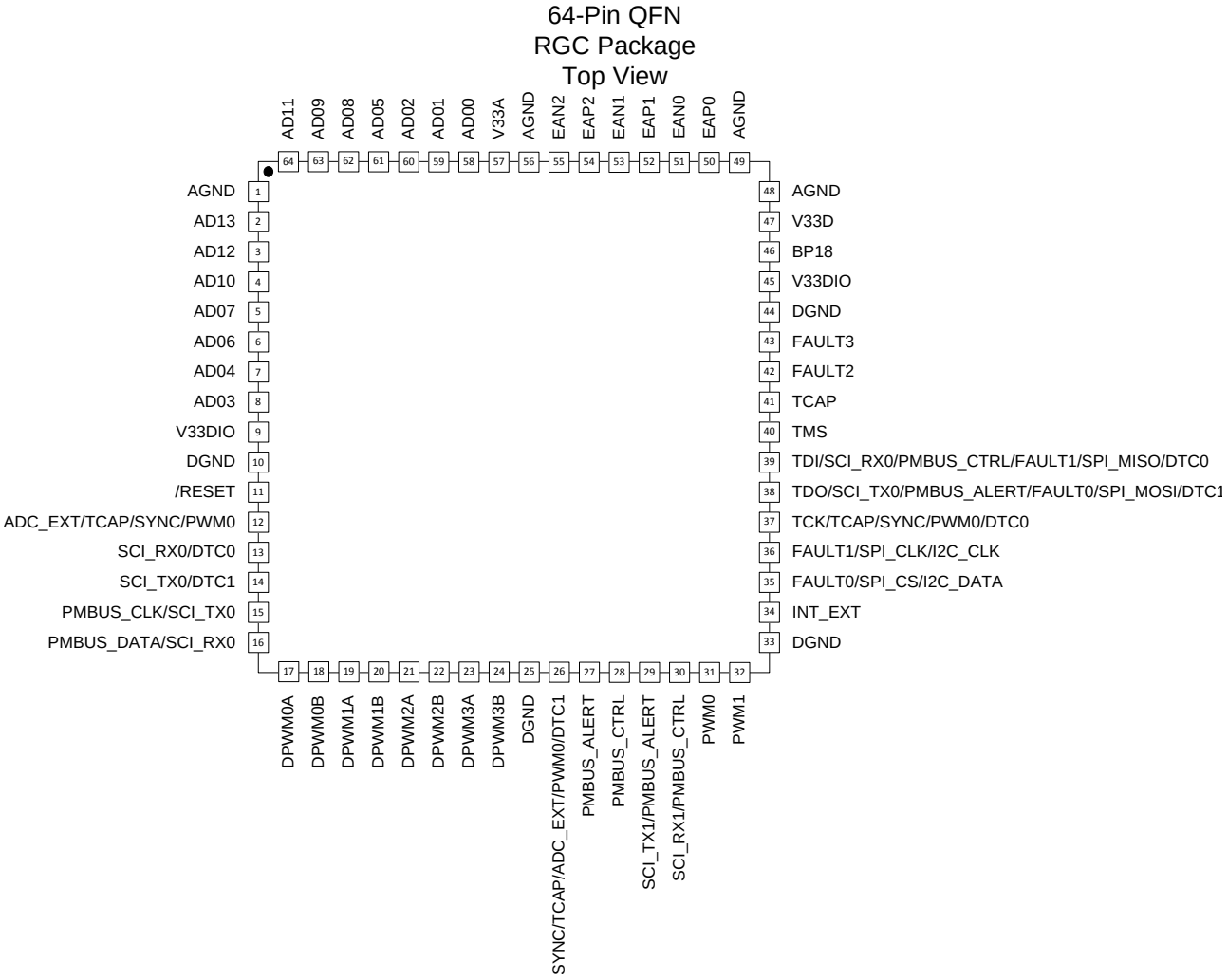
FEATURE	UCD					
	3138 3138A RHA/RMH	3138 3138A RGC	3138064 3138064A RGC	3138064 RGZ	3138128 3138128A PFC	3138A64 3138A64A PFC
Package Offering	40 Pin QFN (6 mm x 6 mm)	64 Pin QFN (9 mm x 9 mm)	64 Pin QFN (9 mm x 9 mm)	48 Pin QFN (7 mm x 7 mm)	80 Pin QFP (14 mm x 14 mm) (Includes leads)	80 Pin QFP (14 mm x 14 mm) (Includes leads)
ARM7TDMI-S Core Processor	31.25 MHz	31.25 MHz	31.25 MHz	31.25 MHz	31.25 MHz	31.25 MHz
High Resolution DPWM Outputs (250ps Resolution)	8	8	8	8	8	8
Number of High Speed Independent Feedback Loops (# Regulated Output Voltages	3	3	3	3	3	3
12-bit, 256kps, General Purpose ADC Channels	7	14	14	9	15	15
Digital Comparators at ADC Outputs	4	4	4	4	4	4
Flash Memory (Program)	32 kB	32 kB	64 kB	64 kB	128 kB	64 kB
Number of Memory 32kB Flash Memory Banks	1	1	2	2	4	Only 1 bank of 64 kB Flash available
Flash Memory (Data)	2 kB	2 kB	2 kB	2 kB	2 kB	2 kB
RAM	4 kB	4 kB	4 kB	4 kB	8 kB	8 kB
Programmable Fault Inputs	1 + 2(1)	4	2 + 2(1)	1 + 2(1)	4	4
High Speed Analog Comparators with Cycle-by-Cycle Current Limiting	6	7	7	6	7	7
UART (SCI)	1(1)	2	2	2	2	2
PMBus/I^2C	1	1	1	1	1	1
Additional I^2C	0	0	1(1)	1(1)	1	1
SPI	0	0	1(1)	1(1)	1	1
Timers	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 1 (24 bit)	4 (16 bit) and 2 (24 bit)	4 (16 bit) and 2 (24 bit)
Timer PWM Outputs	1(1)	2	2	1(1)	4	4
Timer Capture Inputs	2(1)	1 + 3(1)	1 + 3(1)	2(1)	2 + 2(1)	2 + 2(1)
Total Digital GPIOs	18	30	30	24	43	43
External Interrupts	0	1	1	0	1	1
External Crystal Clock Support	no	no	no	no	Yes (pins #61, 62)	Yes (pins #61, 62)
Peak Current Mode Control	EADC2 Only	EADC Only	All EADC channels	All EADC channels	All EADC Channels	All EADC Channels

(1) Represents an alternate pin out that is programmable via firmware.

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4 Pin Configuration and Functions

4.1 Pin Diagrams



Pin Functions

Pin Functions - 64 VQFN

PIN		PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT					CONFIGURABLE AS A GPIO?
NUMBER	NAME		NO. 1	NO. 2	NO. 3	NO. 4	NO. 5	
1	AGND	Analog ground						
2	AD13	12-bit ADC, Ch 13, comparator E, I-share	DAC output					
3	AD12	12-bit ADC, Ch 12						
4	AD10	12-bit ADC, Ch 10						
5	AD07	12-bit ADC, Ch 7, Connected to comparator F and reference to comparator G	DAC output					
6	AD06	12-bit ADC, Ch 6, Connected to comparator F	DAC output					
7	AD04	12-bit ADC, Ch 4, Connected to comparator D	DAC output					
8	AD03	12-bit ADC, Ch 3, Connected to comparator B and C						
9	V33DIO	Digital I/O 3.3V core supply, connected to V33D internally						
10	DGND	Digital ground						
11	$\overline{\text{RESET}}$	Device Reset Input, active low						

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Pin Functions - 64 VQFN (continued)

PIN		PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT					CONFIGURABLE AS A GPIO?
NUMBER	NAME		NO. 1	NO. 2	NO. 3	NO. 4	NO. 5	
12	ADC_EXT	ADC conversion external trigger input	TCAP	SYNC	PWM0			Yes
13	SCI_RX0	SCI RX 0	DTC0					Yes
14	SCI_TX0	SCI TX 0	DTC1					Yes
15	PMBUS_CLK	PMBUS Clock (Open Drain)	SCI TX 0					Yes
16	PMBUS_DATA	PMBus data (Open Drain)	SCI RX 0					Yes
17	DPWM0A	DPWM 0A output						Yes
18	DPWM0B	DPWM 0B output						Yes
19	DPWM1A	DPWM 1A output						Yes
20	DPWM1B	DPWM 1B output						Yes
21	DPWM2A	DPWM 2A output						Yes
22	DPWM2B	DPWM 2B output						Yes
23	DPWM3A	DPWM 3A output						Yes
24	DPWM3B	DPWM 3B output						Yes
25	DGND	Digital ground						
26	SYNC	DPWM Synchronize pin	TCAP	ADC_EXT_TRIG	PWM0	DTC1		Yes
27	PMBUS_ALERT	PMBus Alert (Open Drain)						Yes
28	PMBUS_CTRL	PMBus Control (Open Drain)						Yes
29	SCI_TX1	SCI TX 1	PMBUS_ALERT					Yes
30	SCI_RX1	SCI RX 1	PMBUS_CTRL					Yes
31	PWM0	General purpose PWM 0						Yes
32	PWM1	General purpose PWM 1						Yes
33	DGND	Digital ground						
34	INT_EXT	External Interrupt						Yes
35	FAULT0	External fault input 0	SPI_CS	I2C_DATA				Yes
36	FAULT1	External fault input 1	SPI_CLK	I2C_CLK				Yes
37	TCK(1)	JTAG TCK (for manufacturer test only)	TCAP	SYNC	PWM0	DTC0		Yes
38	TDO(1)	JTAG TDO (for manufacturer test only)	SCI_TX0	PMBUS_ALERT	FAULT0	SPI_MOSI	DTC1	Yes
39	TDI(1)	JTAG TDI (for manufacturer test only)	SCI_RX0	PMBUS_CTRL	FAULT1	SPI_MISO	DTC0	Yes
40	TMS(1)	JTAG TMS (for manufacturer test only)						Yes
41	TCAP	Timer capture input						Yes
42	FAULT2	External fault input 2						Yes
43	FAULT3	External fault input 3						Yes
44	DGND	Digital ground						
45	V33DIO	Digital I/O 3.3 V core supply, connected to V33D internally						
46	BP18	1.8V Bypass						
47	V33D	Digital 3.3V core supply; V33DIO is connected to V33D internally						
48	AGND	Substrate analog ground						
49	AGND	Analog ground						
50	EAP0	Channel #0, differential analog voltage, positive input						
51	EAN0	Channel #0, differential analog voltage, negative input						
52	EAP1	Channel #1, differential analog voltage, positive input						
53	EAN1	Channel #1, differential analog voltage, negative input						
54	EAP2	Channel #2, differential analog voltage, positive input						
55	EAN2	Channel #2, differential analog voltage, negative input						
56	AGND	Analog ground						
57	V33A	Analog 3.3 V supply						
58	AD00	12-bit ADC, Ch 0, Connected to current source						

(1) Fusion Digital Power based debug tools are recommended instead of JTAG.

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Pin Functions - 64 VQFN (continued)

PIN		PRIMARY ASSIGNMENT	ALTERNATE ASSIGNMENT					CONFIGURABLE AS A GPIO?
NUMBER	NAME		NO. 1	NO. 2	NO. 3	NO. 4	NO. 5	
59	AD01	12-bit ADC, Ch 1, Connected to current source						
60	AD02	12-bit ADC, Ch 2, Connected to comparator A, I-share						
61	AD05	12-bit ADC, Ch 5						
62	AD08	12-bit ADC, Ch 8						
63	AD09	12-bit ADC, Ch 9						
64	AD11	12-bit ADC, Ch 11						

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V33D	V33D to DGND	–0.3	3.8	V
V33DIO	V33DIO to DGND	–0.3	3.8	V
V33A	V33A to AGND	–0.3	3.8	V
BP18	BP18 to DGND	–0.3	2.5	V
Ground difference	|DGND – AGND|		0.3	V
All Pins, excluding AGND (2)	Voltage applied to any pin	–0.3	3.8	V
Junction Temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommend Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Referenced to DGND

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V33D	Digital power	3	3.3	3.6	V
V33DIO	Digital I/O power	3	3.3	3.6	V
V33A	Analog power	3	3.3	3.6	V
BP18	1.8-V digital power	1.6	1.8	2	V
T_J	Junction temperature	–40	-	125	°C

5.4 Thermal Information

THERMAL METRIC (1)		UCD3138064A VQFN (RGC) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	19.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

V33A = V33D = V33DIO = 3V to 3.6 V; 1μF from BP18 to DGND, T_J = –40 °C to 125 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
	I33A	Measured on V33A. The device is powered up but all ADC12 and EADC sampling is disabled		6.3		mA
	I33DIO	All GPIO and communication pins are open		0.35		mA
	I33D	ROM program execution		60		mA
	I33D (1)	Flash programming in ROM mode			70	mA
	I33	The device is in ROM mode with all DPWMs enabled and switching at 2 MHz. The DPWMs are all unloaded.			105	mA
ERROR ADC INPUTS EAP, EAN						
	EAP – AGND		–0.15		1.998	V
	EAP – EAN		–0.256		1.848	V
	Typical error range	AFE = 0	–256		248	mV
	EAP – EAN Error voltage digital resolution	AFE = 3	0.8	1	1.20	mV
		AFE = 2	1.7	2	2.30	mV
		AFE = 1	3.55	4	4.45	mV
		AFE = 0	6.90	8	9.10	mV
R_{EA} (1)	Input impedance (See Figure 6-2)	AGND reference	0.5			MΩ
I_{OFFSET}	Input offset current (See Figure 6-2)		–5		5	μA
	EADC Offset	Input voltage = 0 V at AFE = 0	–2		2	LSB
		Input voltage = 0 V at AFE = 1	–2.5		2.5	LSB
		Input voltage = 0 V at AFE = 2	–3		3	LSB
		Input voltage = 0 V at AFE = 3	–4		4	LSB
	Sample Rate				15.625	MHz
	Analog Front End Amplifier Bandwidth (1)			100		MHz
A_0	Gain	See Figure 6-3		1		V/V
	Minimum output voltage				21	mV
EADC DAC						
	DAC range		0		1.6	V
	VREF DAC reference resolution	10-bit, No dithering enabled		1.56		mV
	VREF DAC reference resolution	With 4-bit dithering enabled		97.6		μV
	INL		–2.0		2.0	LSB
	DNL		–2.0		2.0	LSB
	DAC reference voltage		1.58		1.61	V
τ	Settling Time (1)	From 10% to 90%		250		ns
ADC12						
I_{BIAS}	Bias current for PMBus address pins		9.5		10.5	μA
	Measurement range for voltage monitoring		0		2.5	V
	Internal ADC reference voltage	–40 to 125 °C	2.475	2.500	2.53	V
	Change in Internal ADC reference from 25°C reference voltage (1)	–40 to 25 °C		–0.3		mV
		25 to 125 °C		–3.4		

(1) Characterized by design and not production tested.

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Electrical Characteristics *(continued)*

V33A = V33D = V33DIO = 3V to 3.6 V; 1μF from BP18 to DGND, T_J = –40 °C to 125 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ADC12 INL integral nonlinearity, end point (1)	ADC_SAMPLING_SEL = 6 for all ADC12 data, 25 to 125 °C	–3.9	–2/+2	4.5	LSB
	ADC12 INL integral nonlinearity, best fit		–2.4	–1.5/+1.5	2.9	LSB
	ADC12 DNL differential nonlinearity (1)			–0.8/+2.9		LSB
	ADC Zero Scale Error		–7		7	mV
	ADC Full Scale Error		–35		35	mV
	Input bias	2.5 V applied to pin			200	nA
	Input leakage resistance (1)	ADC_SAMPLING_SEL= 6 or 0		1		MΩ
	Input Capacitance (1)			10		pF
	ADC single sample conversion time			3.744		μs
DIGITAL INPUTS/OUTPUTS (2)						
V_{OL}	Low-level output voltage (3)	I_{OH} = 4 mA, V33DIO = 3 V			DGND + 0.25	V
V_{OH}	High-level output voltage (3)	I_{OH} = –4 mA, V33DIO = 3 V	V33DIO – 0.6			V
V_{IH}	High-level input voltage	V33DIO = 3 V	2.1			V
V_{IL}	Low-level input voltage	V33DIO = 3 V			1.1	V
I_{OH}	Output sinking current				4	mA
I_{OL}	Output sourcing current		–4			mA
$V_{OL(PMBus)}$	Low-level output voltage for PMBus pins (PMBUS_CLK, PMBUS_DATA, PMBUS_ALERT, PMBUS_CTRL)	I_{OL} = 20 mA		400		mV
SYSTEM PERFORMANCE						
t_{WD}	Watchdog timeout resolution		13.1	17	22.7	ms
	Processor master clock (MCLK)			31.25		MHz
t_{Delay}	Digital filter delay (4)	(1 clock = 32 ns)			6	MCLKs
	Retention period of flash content (data retention and program)	T_J = 25 °C	100			years
$f_{(PCLK)}$	Internal oscillator frequency	–40 C to +125 C	240	250	260	MHz
		–5 C to +85 C	245	250	255	MHz
$f_{(LFO)}$	Internal low frequency oscillator frequency			10		MHz
	Flash Read			1		MCLKs
I_{SHARE}	Current share current source (See Figure 6-25)		238		259	μA
R_{SHARE}	Current share resistor (See Figure 6-25)		9.75		10.3	kΩ
POWER ON RESET AND BROWN OUT (V33A PIN, SEE Figure 5-4)						
VGH		Voltage Good High		2.6		V
VGL		Voltage Good Low		2.55		V
V_{res} (1)	Voltage at which IReset signal is valid (1)			0.8		V
	Brownout	Internal signal warning of brownout conditions		2.9		V
TEMPERATURE SENSOR (1)						
V_{TEMP}		Voltage range of sensor	1.46		2.44	V

(2) DPWM outputs are low after reset. Other GPIO pins are configured as inputs after reset. During power up or power down, all GPIO pins output low.
(3) The maximum total current, IOHmax and IOLmax for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified. Maximum sink current per pin = –6 mA at V_{OL}; maximum source current per pin = 6 mA at V_{OH}.
(4) Time from close of error ADC sample window to time when digitally calculated control effort (duty cycle) is available. This delay, which has no variation associated with it, must be accounted for when calculating the system dynamic response.

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Electrical Characteristics *(continued)*

V33A = V33D = V33DIO = 3V to 3.6 V; 1μF from BP18 to DGND, T_J = –40 °C to 125 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Voltage resolution	Volts/°C		5.9		mV/ºC
	Temperature resolution	Degree C per bit		0.1034		ºC/LSB
	Accuracy (1) (5)	–40 to 125 °C	–10	±5	10	ºC
	Temperature range	–40 to 125 °C	–40		125	ºC
I_{TEMP}		Current draw of sensor when active		30		μA
V_{AMB}	Ambient temperature	Trimmed 25 °C reading		1.85		V
ANALOG COMPARATOR						
DAC	Reference DAC Range		0.01953		2.5	V
	Reference Voltage		2.478	2.5	2.513	V
	Bits			7		bits
	INL (1)		–0.5		0.21	LSB
	DNL (1)		0.06		0.12	LSB
	Offset (1)		–19.5		19.5	mV
	Reference DAC buffered output load (6)		–0.5		1	mA
	Buffer Offset (–0.5 mA)	0.156V < DAC < 2.363V	–10		10	mV
	Buffer Offset (1.0 mA)	0.059V < DAC < 2.305V	–10		10	mV

(5) Ambient temperature offset value should be used from the TEMPSENCTRL register to meet accuracy.
(6) Available from reference DACs for comparators D, E, F and G.

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5.6 Timing Characteristics

V33A = V33D = V33DIO = 3.3 V; 1 μF from BP18 to DGND, T_J = –40 to 125 °C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
EADC DAC						
τ	Settling Time	From 10 to 90%		250		ns
ADC12						
	ADC single sample conversion time (1)	ADC_SAMPLING_SEL= 6 or 0		3.9		μs
SYSTEM PERFORMANCE						
	Time to disable DPWM output based on active FAULT pin signal	High level on FAULT pin		70		ns
	Retention period of flash content (data retention and program)	T_J = 25 °C	100			years
	Program time to erase one page or block in data flash or program flash			20		ms
	Program time to write one word in data flash or program flash			30		μs
	Sync-in/sync-out pulse width	Sync pin		256		ns
	Flash Write			20		μs
POWER ON RESET AND BROWN OUT (V33D PIN, SEE Figure 5-4						
t_{POR}		Time delay after Power is good or RESET* relinquished		1		ms
t_{EXC1}	The time it takes from the device to exit a reset state and begin executing program flash bank 1 (32 kB). (1)	I_{RESET} goes from a low state to a high state. This is approximately equivalent to toggling the external reset pin from low to high state.		9.5		ms
t_{EXC2}	The time it takes from the device to exit a reset state and begin executing program flash bank 2 (32 kB). (1)	I_{RESET} goes from a low state to a high state. This is approximately equivalent to toggling the external reset pin from low to high state.		19		ms
t_{EXCT}	The time it takes from the device to exit a reset state and begin executing the total program flash (64 kB). (1)	I_{RESET} goes from a low state to a high state. This is approximately equivalent to toggling the external reset pin from low to high state.		19		ms
TEMPERATURE SENSOR (1)						
t_{ON}		Turn on time / settling time of sensor		100		μs
ANALOG COMPARATOR						
	Time to disable DPWM output based on 0 V to 2.5 V step input on the analog comparator. (1)				150	ns

(1) Characterized by design and not production tested.

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5.7 PMBus/SMBus/I²C Timing

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus, and PMBus in Slave or Master mode are shown in Table 5-1, Figure 5-1, and Figure 5-2. The numbers in Table 5-1 shows that the device supports standard (100 kHz), fast (400 kHz), and fast-mode plus (1 MHz) speeds.

Table 5-1. I²C/SMBus/PMBus Timing Characteristics

PARAMETER		TEST CONDITIONS	100 kHz Class		400 kHz Class		1 MHz Class		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Typical values at T_A = 25 °C and VCC = 3.3 V (unless otherwise noted)									
f_{SMB}	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle	10	100	10	400	10	1000	kHz
f_{I2C}	I²C operating frequency	Slave mode, SCL 50% duty cycle	10	100	10	400	10	1000	kHz
$t_{(BUF)}$	Bus free time between start and stop(1)		4.7		1.3		0.5		µs
$t_{(HD:STA)}$	Hold time after (repeated) start(1)		4		0.6		0.26		µs
$t_{(SU:STA)}$	Repeated start setup time(1)		4.7		0.6		0.26		µs
$t_{(SU:STO)}$	Stop setup time(1)		4		0.6		0.26		µs
$t_{(HD:DAT)}$	Data hold time	Receive mode	0		0		0		ns
$t_{(SU:DAT)}$	Data setup time		250		100		50		ns
$t_{(TIMEOUT)}$	Error signal/detect(2)		25	35	25	35	25	35	ms
$t_{(LOW)}$	Clock low period		4.7		1.3		0.5		µs
$t_{(HIGH)}$	Clock high period(3)		4	50	0.6	50	0.26	50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time(4)			25		25		25	ms
t_r	Clock/data fall time	Rise time t_r = (V_{ILmax} – 0.15) to (V_{IHmin} + 0.15)	20 + 0.1 Cb(5)	300	20 + 0.1 Cb(5)	300	20 + 0.1 Cb(5)	120	ns
t_f	Clock/data rise time	Fall time t_f = 0.9 VDD to (V_{ILmax} – 0.15)	20 + 0.1 Cb(5)	1000	20 + 0.1 Cb(5)	300	20 + 0.1 Cb(5)	120	ns
C_b	Total capacitance of one bus line					400			pF

(1) Fast mode, 400 kHz
(2) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(3) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(4) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) C_b (pF)

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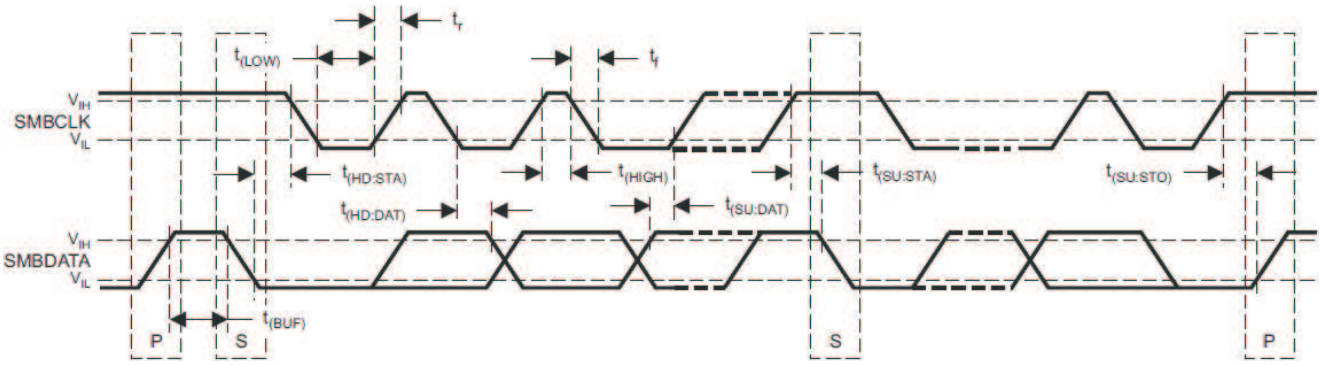


Figure 5-1. I²C/SMBus/PMBus Timing Diagram

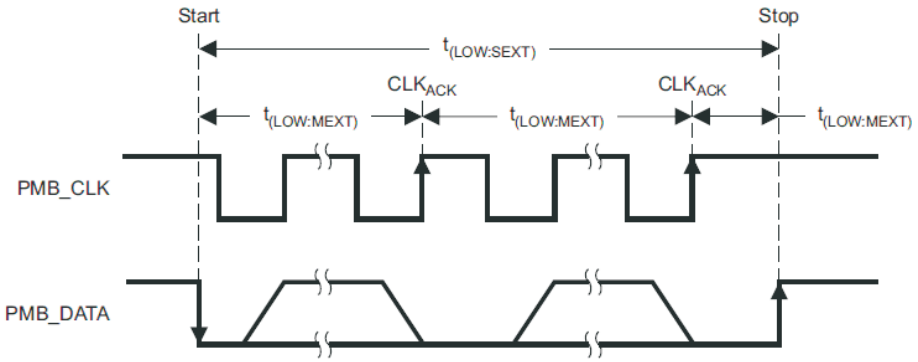


Figure 5-2. Bus Timing in Extended Mode

5.8 Parametric Measurement Information

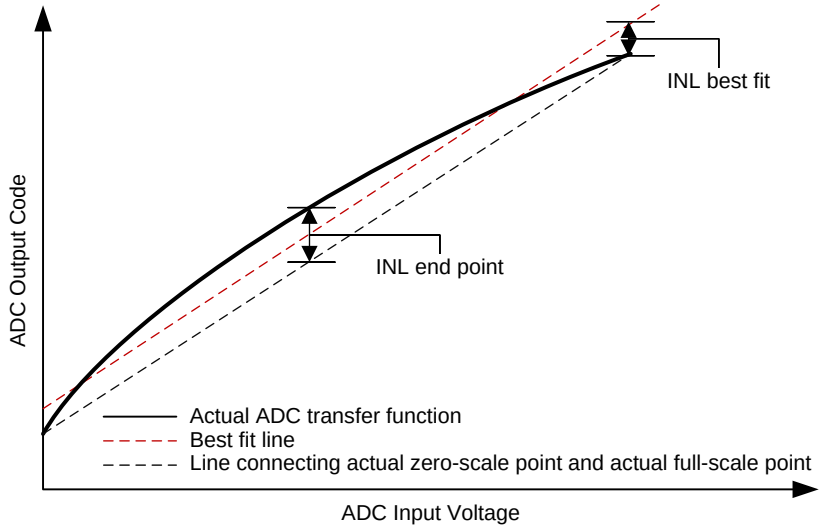


Figure 5-3. Best Fit INL and End Point INL

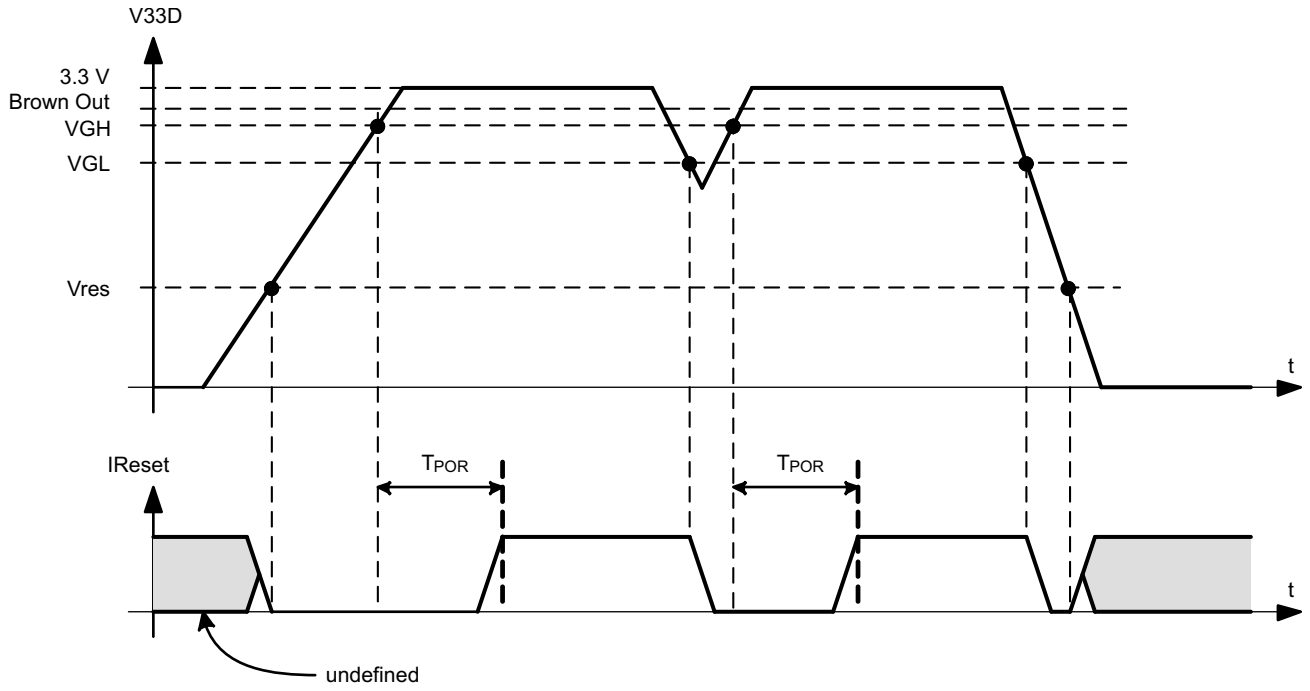


Figure 5-4. Power On Reset (POR) / Brown Out Reset (BOR)

VGH – This is the V33A threshold where the internal power is declared good. The UCD3138064A comes out of reset when above this threshold.

VGL – This is the V33A threshold where the internal power is declared bad. The device goes into reset when below this threshold.

V_{res} – This is the V33A threshold where the internal reset signal is no longer valid. Below this threshold the device is in an indeterminate state.

I_{Reset} – This is the internal reset signal. When low, the device is held in reset. This is equivalent to holding the reset pin on the IC low.

T_{POR} – The time delay from when VGH is exceeded to when the device comes out of reset.

Brown Out – This is the V33A voltage threshold at which the device sets the brown out status bit. In addition an interrupt can be triggered if enabled.

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5.9 Typical Characteristics

(Data is taken from the UCD3138)

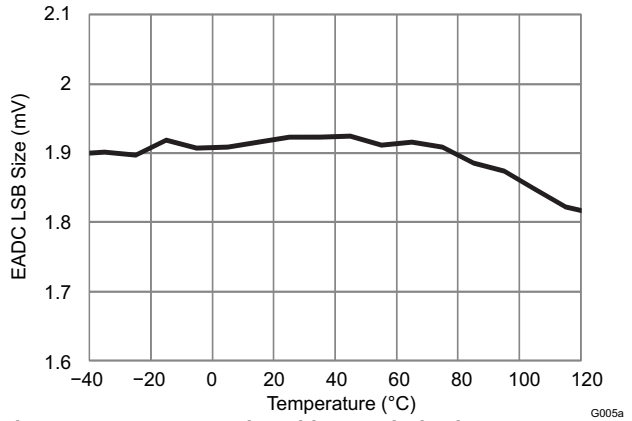


Figure 5-5. EADC LSB Size with 4X Gain (mV) vs Temperature

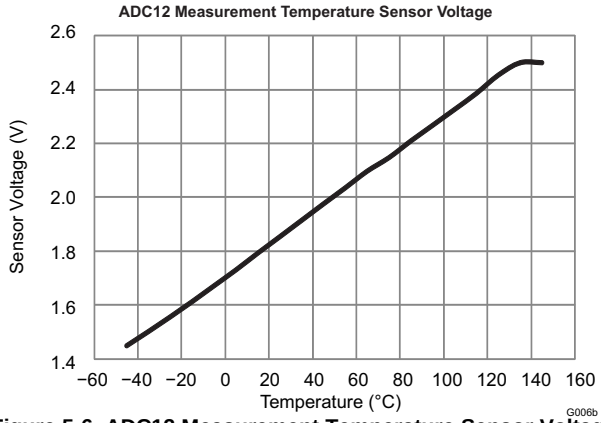


Figure 5-6. ADC12 Measurement Temperature Sensor Voltage vs Temperature

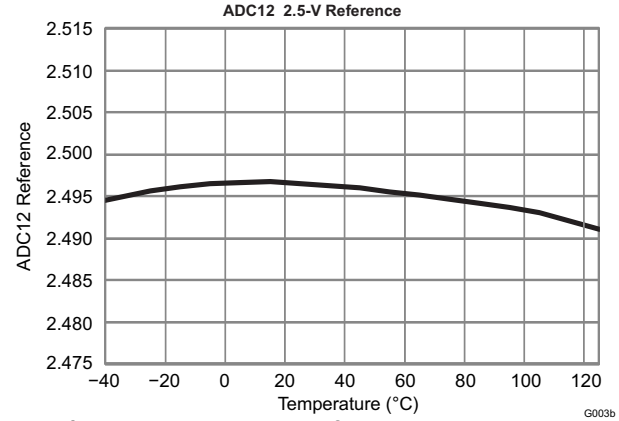


Figure 5-7. ADC12 2.5-V Reference vs Temperature

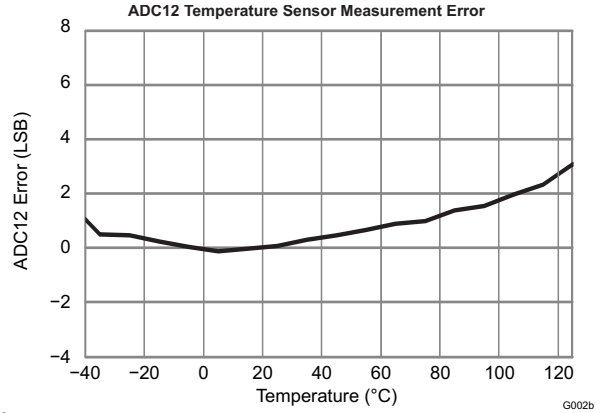


Figure 5-8. ADC12 Temperature Sensor Measurement Error vs Temperature

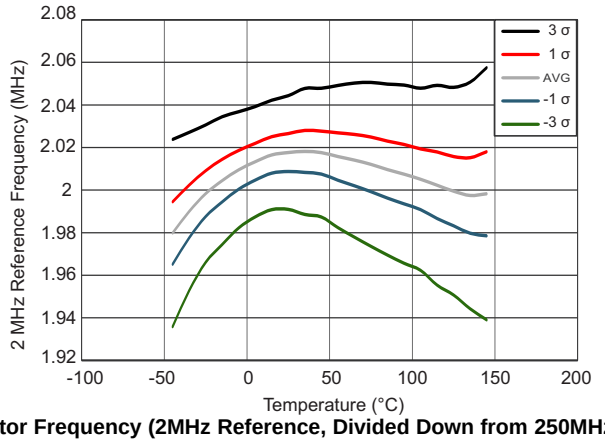


Figure 5-9. Oscillator Frequency (2MHz Reference, Divided Down from 250MHz) vs Temperature

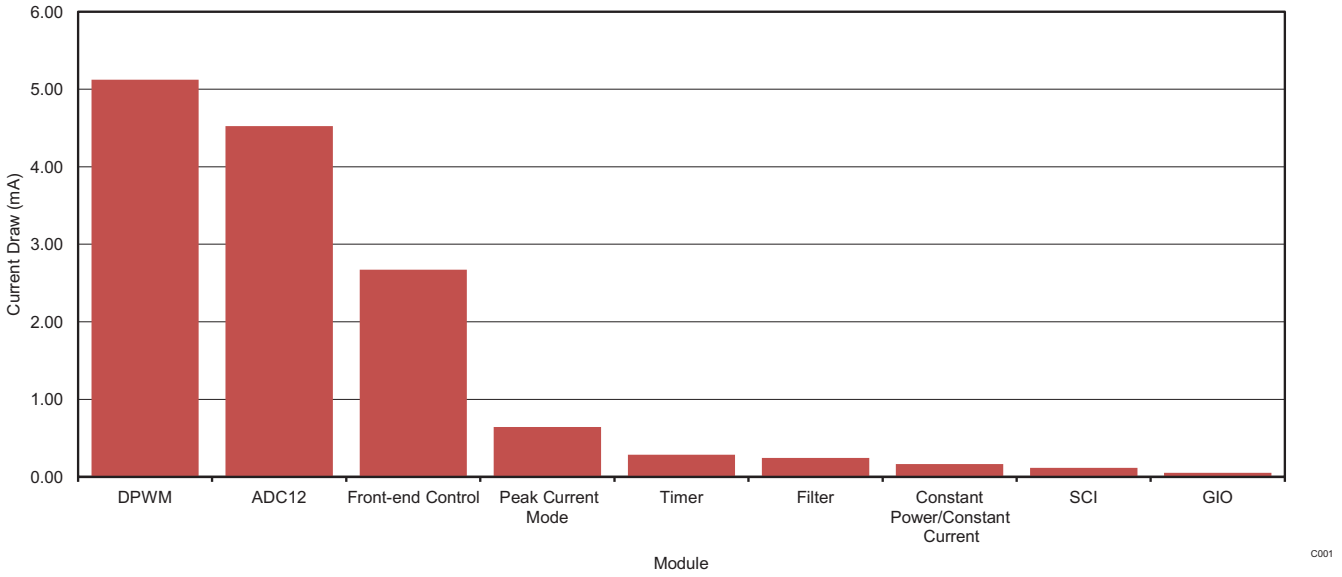


Figure 5-10. Clock Gating Power Savings

The power disable control register provides control bits that can enable or disable the clock to several peripherals such as, PCM, CPCC, digital filters, front ends, DPWMs, UARTs, ADC-12 and more.

By default, all these controls are enabled. If a specific peripheral is not used the clock gate can be disabled in order to block the propagation of the clock signal to that peripheral and therefore reduce the overall current consumption of the device. The power savings chart displays the power savings per module. For example there are 4 DPWM modules, therefore, if all 4 are disabled a total of ~20 mA can be saved.

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6 Detailed Description

6.1 Overview

The UCD3138064A family is a digital power supply controller from Texas Instruments offering superior levels of integration and performance in a single chip solution. The flexible nature of the UCD3138064A family makes it suitable for a wide variety of power conversion applications. Multiple peripherals inside the device have been specifically optimized to enhance the performance of AC/DC and isolated DC/DC applications and reduce the solution component count in the IT and network infrastructure space. The UCD3138064A family is a fully programmable solution offering customers complete control of their application, along with ample ability to differentiate their solution.

6.2 ARM Processor

The ARM7TDMI-S processor is a synthesizable member of the ARM family of general purpose 32-bit microprocessors. The ARM architecture is based on RISC (Reduced Instruction Set Computer) principles where two instruction sets are available: the 32-bit ARM instruction set and the 16-bit Thumb instruction set. The Thumb instructions allow for higher code density equivalent to a 16-bit microprocessor, with the performance of the 32-bit microprocessor.

The three-staged pipelined ARM processor has fetch, decode and execute stage architecture. Major blocks in the ARM processor include a 32-bit ALU, 32 x 8 multiplier, and a barrel shifter.

6.3 Memory

The UCD3138064A (ARM7TDMI-S) is a Von-Neumann architecture, where a single bus provides access to all of the memory modules. All of the memory module addresses are sequentially aligned along the same address range.

Within the UCD3138064A family architecture, there is a 1024x32-bit Boot ROM that contains the initial firmware startup routines for PMBUS communication and non-volatile (FLASH) memory download. This boot ROM is executed after power-up-reset checks if there is a valid FLASH program written. If a valid program is present, the ROM code branches to the main FLASH-program execution. If there is no valid program, the device waits for a program download through the PMBus.

The UCD3138064A family also supports customization of the boot program by allowing an alternative boot routine to be executed from program FLASH. This feature enables assignment of a unique address to each device; therefore, enabling firmware reprogramming even when several devices are connected on the same communication bus.

There are three separate flash memory areas present inside the device. There are 2-32 kB program flash blocks and 1-2 kB data flash area. The 32 kB program areas are organized as 8 k x 32 bit memory blocks and are intended to be for the firmware programs. The blocks are configured with page erase capability for erasing blocks as small as 1 kB per page, or with a mass erase for erasing the entire 32 kB array. The flash endurance is specified at 1000 erase/write cycles and the data retention is good for 100 years. The 2 kB data flash array is organized as a 512 x 32 bit memory (32 byte page size). The data flash is intended for firmware data value storage and data logging. Thus, the Data flash is specified as a high endurance memory of 20 k cycles with embedded error correction code (ECC).

For run time data storage and scratchpad memory, a 8 kB RAM is available. The RAM is organized as a 2 k x 32 bit array. The availability of 64 kB of program Flash memory in 2-32 kB banks, enables designers to implement multiple images of firmware (e.g. one main image + one back-up image) in the device and the flexibility to execute from either of the banks using appropriate algorithms. It also creates the unique opportunity for the processor to load a new program and subsequently execute that program without interrupting power delivery. This feature allows the end user to add new features to the power supply while eliminating any down-time required to load the new program.

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6.4 Feature Description

6.4.1 System Module

The System Module contains the interface logic and configuration registers to control and configure all the memory, peripherals and interrupt mechanisms. The blocks inside the system module are the address decoder, memory management controller, system management unit, central interrupt unit, and clock control unit.

6.4.1.1 Address Decoder (DEC)

The Address Decoder generates the memory selects for the FLASH, ROM and RAM arrays. The memory map addresses are selectable through configurable register settings. These memory selects can be configured from 1 kB to 16 MB. Power on reset uses the default addresses in the memory map for ROM execution, which is then configured by the ROM code to the application setup. During access to the DEC registers, a wait state is asserted to the CPU. DEC registers are only writable in the ARM privilege mode for user mode protection.

6.4.1.2 Memory Management Controller (MMC)

The MMC manages the interface to the peripherals by controlling the interface bus for extending the read and write accesses to each peripheral. The unit generates eight peripheral select lines with 1 kB of address space decoding.

6.4.1.3 System Management (SYS)

The SYS unit contains the software access protection by configuring user privilege levels to memory or peripherals modules. It contains the ability to generate fault or reset conditions on decoding of illegal address or access conditions. A clock control setup for the processor clock (MCLK) speed, is also available.

6.4.1.4 Central Interrupt Module (CIM)

The CIM accepts 32 interrupt requests for meeting firmware timing requirements. The ARM processor supports two interrupt levels: FIQ and IRQ. FIQ is the highest priority interrupt. The CIM provides hardware expansion of interrupts by use of FIQ/IRQ vector registers for providing the offset index in a vector table. This numerical index value indicates the highest precedence channel with a pending interrupt and is used to locate the interrupt vector address from the interrupt vector table. Interrupt channel 0 has the lowest precedence and interrupt channel 31 has the highest precedence. To remove the interrupt request, the firmware should clear the request as the first action in the interrupt service routine. The request channels are maskable, allowing individual channels to be selectively disabled or enabled.

Table 6-1. Interrupt Priority Table

NAME	MODULE COMPONENT OR REGISTER	DESCRIPTION	PRIORITY
BRN_OUT_INT	Brownout	Brownout interrupt	0 (Lowest)
EXT_INT	External Interrupts	Interrupt on external input pin	1
WDRST_INT	Watchdog Control	Interrupt from watchdog exceeded (reset)	2
WDWAKE_INT	Watchdog Control	Wake-up interrupt when watchdog equals half of set watch time	3
SCI_ERR_INT	UART or SCI Control	UART or SCI error Interrupt. Frame, parity or overrun	4
SCI_RX_0_INT	UART or SCI Control	UART0 RX buffer has a byte	5
SCI_TX_0_INT	UART or SCI Control	UART0 TX buffer empty	6
SCI_RX_1_INT	UART or SCI Control	UART1 RX buffer has a byte	7
SCI_TX_1_INT	UART or SCI Control	UART1 TX buffer empty	8
PMBUS_INT		PMBus related interrupt	9
DIG_COMP_SPI_I2C_INT	12-bit ADC Control, SPI, I^2C	Digital comparator, SPI and I^2C interrupt	10

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Table 6-1. Interrupt Priority Table (continued)

NAME	MODULE COMPONENT OR REGISTER	DESCRIPTION	PRIORITY
FE0_INT	Front End 0	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	11
FE1_INT	Front End 1	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	12
FE2_INT	Front End 2	“Prebias complete”, “Ramp Delay Complete”, “Ramp Complete”, “Load Step Detected”, “Over-Voltage Detected”, “EADC saturated”	13
PWM3_INT	16-bit Timer PWM 3	16-bit Timer PWM3 counter overflow or compare interrupt	14
PWM2_INT	16-bit Timer PWM 2	16-bit Timer PWM2 counter Overflow or compare interrupt	15
PWM1_INT	16-bit Timer PWM 1	16-bit Timer PWM1 counter overflow or compare interrupt	16
PWM0_INT	16-bit timer PWM 0	16-bit Timer PWM0 counter overflow or compare interrupt	17
OVF24_INT	24-bit Timer Control	24-bit Timer counter overflow interrupt	18
DTC_FLT_INT	DTC Fault Interrupt	DTC module fault interrupt	19
Reserved for future use			20
CAPTURE_0_INT	24-bit Timer Control	24-bit Timer capture 0 interrupt	21
COMP_0_INT	24-bit Timer Control	24-bit Timer compare 0 interrupt	22
CPCC_RTC_INT	Constant Power Constant Current or Real Time Clock Output	Mode switched in CPCC module Flag needs to be read for details. RTC timer output generates an interrupt.	23
ADC_CONV_INT	12-bit ADC Control	ADC end of conversion interrupt	24
FAULT_INT	Fault Mux Interrupt	Analog comparator interrupts, Over-Voltage detection, Under-Voltage detection, LLM load step detection	25
DPWM3	DPWM3	Same as DPWM1	26
DPWM2	DPWM2	Same as DPWM1	27
DPWM1	DPWM1	1) Every (1-256) switching cycles 2) Fault Detection 3) Mode switching	28
DPWM0	DPWM0	Same as DPWM1	29
EXT_FAULT_INT	External Faults	Fault pin interrupt	30
SYS_SSI_INT	System Software	System software interrupt	31 (highest)

6.4.2 Peripherals

6.4.2.1 Digital Power Peripherals

At the core of the UCD3138x controller are 3 Digital Power Peripherals (DPP). Each DPP can be configured to drive from one to eight DPWM outputs. Each DPP consists of:

- Differential input error ADC (EADC) with sophisticated controls
- Hardware accelerated digital 2-pole/2-zero PID based filter
- Digital PWM module with support for a variety of topologies

These can be connected in many different combinations, with multiple filters and DPWMs. They are capable of supporting functions like input voltage feed forward, current mode control, and constant current/constant power, etc.. The simplest configuration is shown in Figure 6-1:



Figure 6-1. Simple Digital Power Configuration

6.4.2.1.1 Front End

Figure 6-2 shows the block diagram of the front end module. It consists of a differential amplifier, an adjustable gain error amplifier, a high speed flash analog to digital converter (EADC), digital averaging filters and a precision high resolution set point DAC reference. The programmable gain amplifier in concert with the EADC and the adjustable digital gain on the EADC output work together to provide 9 bits of range with 6 bits of resolution on the EADC output. The output of the Front End module is a 9 bit sign extended result with a gain of 1 LSB / mV. Depending on the value of AFE selected, the resolution of this output could be either 1, 2, 4 or 8 LSBs. In addition Front End 0 has the ability to automatically select the AFE value such that the minimum resolution is maintained that still allows the voltage to fit within the range of the measurement. The EADC control logic receives the sample request from the DPWM module for initiating an EADC conversion. EADC control circuitry captures the EADC-9-bit-code and strobes the filter for processing of the representative error. The set point DAC has 10 bits with an additional 4 bits of dithering resulting in an effective resolution of 14 bits. This DAC can be driven from a variety of sources to facilitate things like soft start, nested loops, etc. Some additional features include the ability to change the polarity of the error measurement and an absolute value mode which automatically adds the DAC value to the error.

It is possible to operate the controller in a peak current mode control configuration. In this mode topologies like the phase shifted full bridge converter can be controlled to maintain transformer flux balance. The internal DAC can be ramped at a synchronously controlled slew rate to achieve a programmable slope compensation. This eliminates the sub-harmonic oscillation as well as improves input voltage feed-forward performance. A0 is a unity gain buffer used to isolate the peak current mode comparator. The offset of this buffer is specified in the Electrical Characteristics table.

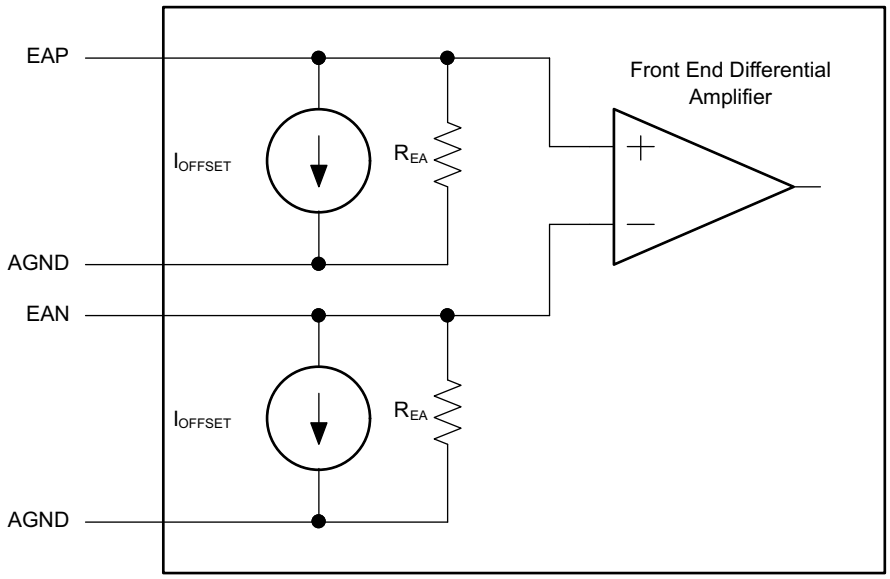


Figure 6-2. Input Stage Of EADC Module

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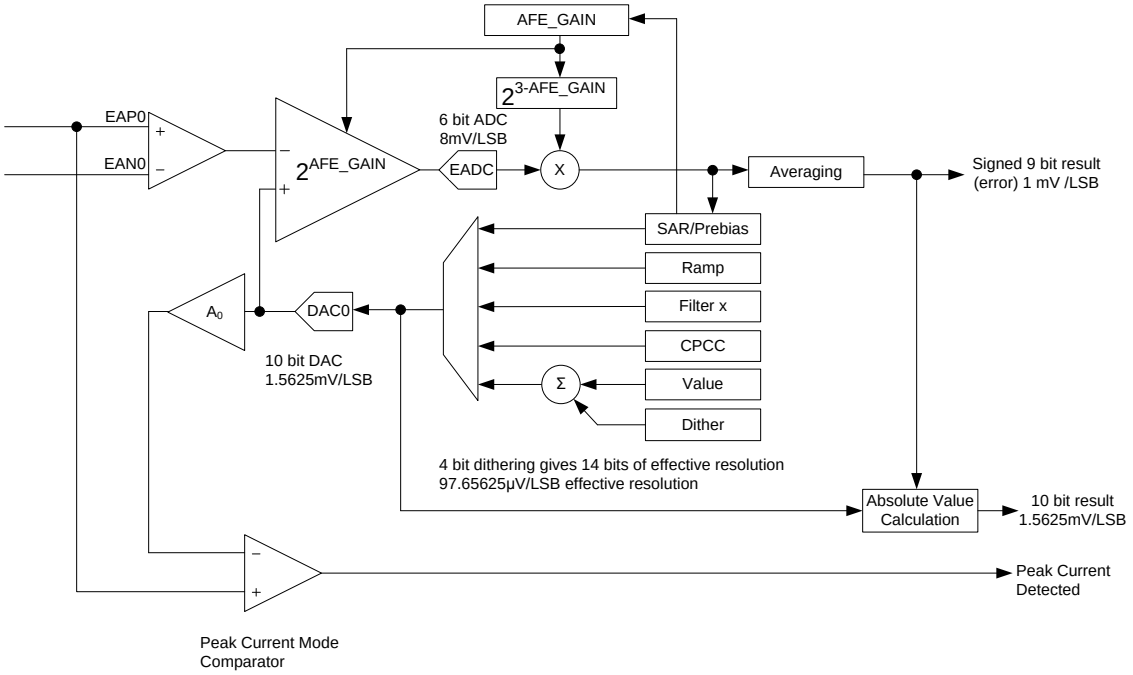


Figure 6-3. Front End Module

6.4.2.1.2 DPWM Module

The DPWM module represents one complete DPWM channel with 2 independent outputs, A and B. Multiple DPWM modules within the UCD3138x system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power supply output voltage rail. It can also be used as a synchronized DPWM—with user selectable phase shift between the DPWM channels to control power supply outputs with multiphase or interleaved DPWM configurations.

The output of the filter feeds the high resolution DPWM module. The DPWM module produces the pulse width modulated outputs for the power stage switches. The filter calculates the necessary duty ratio as a 24-bit number in Q23 fixed point format (23 bit integer with 1 sign bit). This represents a value within the range 0.0 to 1.0. This duty ratio value is used to generate the corresponding DPWM output ON time. The resolution of the DPWM ON time is 250 psec.

Each DPWM module can be synchronized to another module or to an external synchronization signal. An input SYNC signal causes a DPWM ramp timer to reset. The SYNC signal outputs—from each of the four DPWM modules—occur when the ramp timer crosses a programmed threshold. This allows the phase of the DPWM outputs for multiple power stages to be tightly controlled.

The DPWM logic takes the output of the filter and converts it into the correct DPWM output for several power supply topologies. It provides for programmable dead times and cycle adjustments for current balancing between phases. It controls the triggering of the EADC. It can synchronize to other DPWMs or to external sources. It can provide synchronization information to other DPWMs or to external recipients. In addition, it interfaces to several fault handling circuits. Some of the control for these fault handling circuits is in the DPWM registers. Fault handling is covered in the Fault Mux section.

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Each DPWM module supports the following features:

- Dedicated 14 bit time-base with period and frequency control
- Shadow period register for end of period updates.
- Quad-event control registers (A and B, rising and falling) (Events 1-4)
  - Used for on/off DPWM duty ratio updates.
- Phase control relative to other DPWM modules
- Sample trigger placement for output voltage sensing at any point during the DPWM cycle.
- Support for 2 independent edge placement DPWM outputs (same frequency or period setting)
- Dead-time between DPWM A and B outputs
- High Resolution PWM capability – 250 ps
- Pulse cycle adjustment of up to ±8.192 µs (32768 × 250 ps)
- Active high/ active low output polarity selection
- Provides events to trigger both CPU interrupts and start of ADC12 conversions.

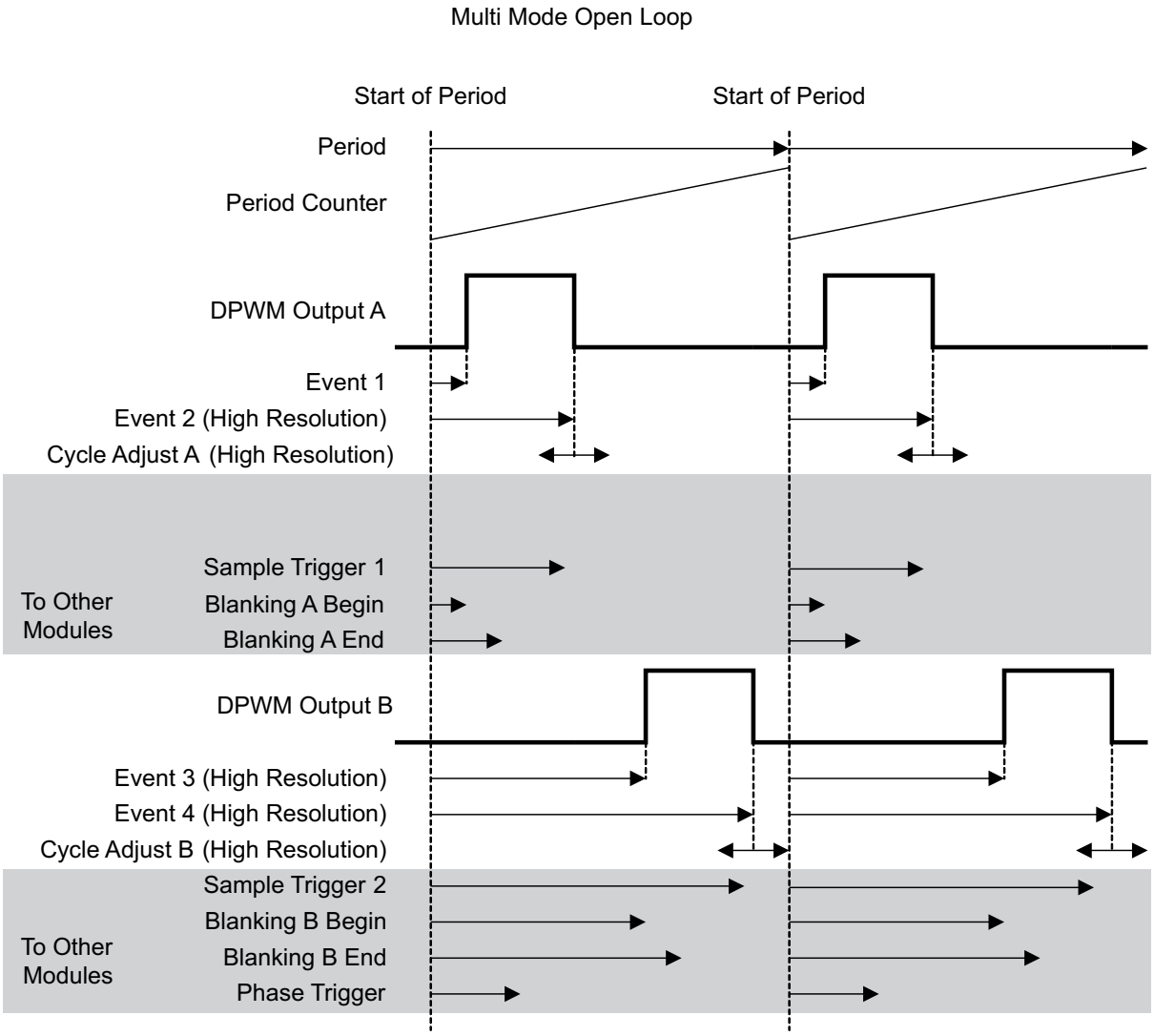
6.4.2.1.3 DPWM Events

Each DPWM can control the following timing events:

1. *Sample Trigger Count*–This register defines where the error voltage is sampled by the EADC in relationship to the DPWM period. The programmed value set in the register should be one fourth of the value calculated based on the DPWM clock. As the DCLK (DCLK = 62.5 MHz max) controlling the circuitry runs at one fourth of the DPWM clock (PCLK = 250MHz max). When this sample trigger count is equal to the DPWM Counter, it initiates a front end calculation by triggering the EADC, resulting in a CLA calculation, and a DPWM update. Over-sampling can be set for 2, 4 or 8 times the sampling rate.
2. *Phase Trigger Count*–count offset for slaving another DPWM (Multi-Phase/Interleaved operation).
3. *Period*–low resolution switching period count. (count of PCLK cycles)
4. *Event 1*–count offset for rising DPWM A event. (PCLK cycles)
5. *Event 2*–DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3*–DPWM count for rising DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
7. *Event 4*–DPWM count for falling DPWM B event. Last 4 bits of the register are for high resolution control. Upper 14 bits are the number of PCLK cycle counts.
8. *Cycle Adjust*–Constant offset for Event 2 and Event 4 adjustments.

Basic comparisons between the programmed registers and the DPWM counter can create the desired edge placements in the DPWM. High resolution edge capability is available on Events 2, 3 and 4.

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Events which change with DPWM mode:

DPWM A Rising Edge = Event 1
DPWM A Falling Edge = Event 2 + Cycle Adjust A
DPWM B Rising Edge = Event 3
DPWM B Falling Edge = Event 4 + Cycle Adjust B
Phase Trigger = Phase Trigger Register value

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

Figure 6-4. Multi Mode Open Loop

Figure 6-4 is for multi-mode, open loop. Open loop means that the DPWM is controlled entirely by its own registers, not by the filter output. In other words, the power supply control loop is not closed.

The Sample Trigger signals are used to trigger the Front End to sample input signals. The Blanking signals are used to blank fault measurements during noisy events, such as FET turn on and turn off. Additional DPWM modes are described below.

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6.4.2.1.4 High Resolution DPWM

Unlike conventional PWM controllers where the frequency of the clock dictates the maximum resolution of PWM edges, the UCD3138x DPWM can generate waveforms with resolutions as small as 250 ps. This is 16 times the resolution of the clock driving the DPWM module.

This is achieved by providing the DPWM mechanism with 16 phase shifted clock signals of 250 MHz each.

6.4.2.1.5 Over Sampling

The DPWM module has the capability to trigger an over sampling event by initiating the EADC to sample the error voltage. The default “00” configuration has the DPWM trigger the EADC once based on the sample trigger register value. The over sampling register has the ability to trigger the sampling 2, 4 or 8 times per PWM period. Thus the time the over sample happens is at the divide by 2, 4, or 8 time set in the sampling register. The “01” setting triggers 2X over sampling, the “10” setting triggers 4X over sampling, and the “11” triggers over sampling at 8X.

6.4.2.1.6 DPWM Interrupt Generation

The DPWM has the capability to generate a CPU interrupt based on the PWM frequency programmed in the period register. The interrupt can be scaled by a divider ratio of up to 255 for developing a slower interrupt service execution loop. This interrupt can be fed to the ADC circuitry for providing an ADC12 trigger for sequence synchronization. Table 6-2 outlines the divide ratios that can be programmed.

6.4.2.1.7 DPWM Interrupt Scaling/Range

Table 6-2. DPWM Interrupt Divide Ratio

INTERRUPT DIVIDE SETTING	INTERRUPT DIVIDE COUNT	INTERRUPT DIVIDE COUNT (HEX)	SWITCHING PERIOD FRAMES (assume 1MHz loop)	NUMBER OF 32 MHZ PROCESSOR CYCLES
1	0	00	1	32
2	1	01	2	64
3	3	03	4	128
4	7	07	8	256
5	15	0F	16	512
6	31	1F	32	1024
7	47	2F	48	1536
8	63	3F	64	2048
9	79	4F	80	2560
10	95	5F	96	3072
11	127	7F	128	4096
12	159	9F	160	5120
13	191	BF	192	6144
14	223	DF	224	7168
15	255	FF	256	8192

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6.4.3 Synchronous Rectifier Dead Time Optimization Peripheral

The UCD3138064A has an advanced dead time control interface where it can accept UCD7138 output signals and optimize SR gate driver signals accordingly. The UCD7138 low-side MOSFET driver is a high-performance driver for secondary-side synchronous rectification (SR) with body diode conduction sensing. The device is suitable for high power high efficiency isolated converter applications where dead-time optimization is desired. The UCD7138 gate driver is a companion device to UCD3138064A highly integrated digital controller for isolated power.

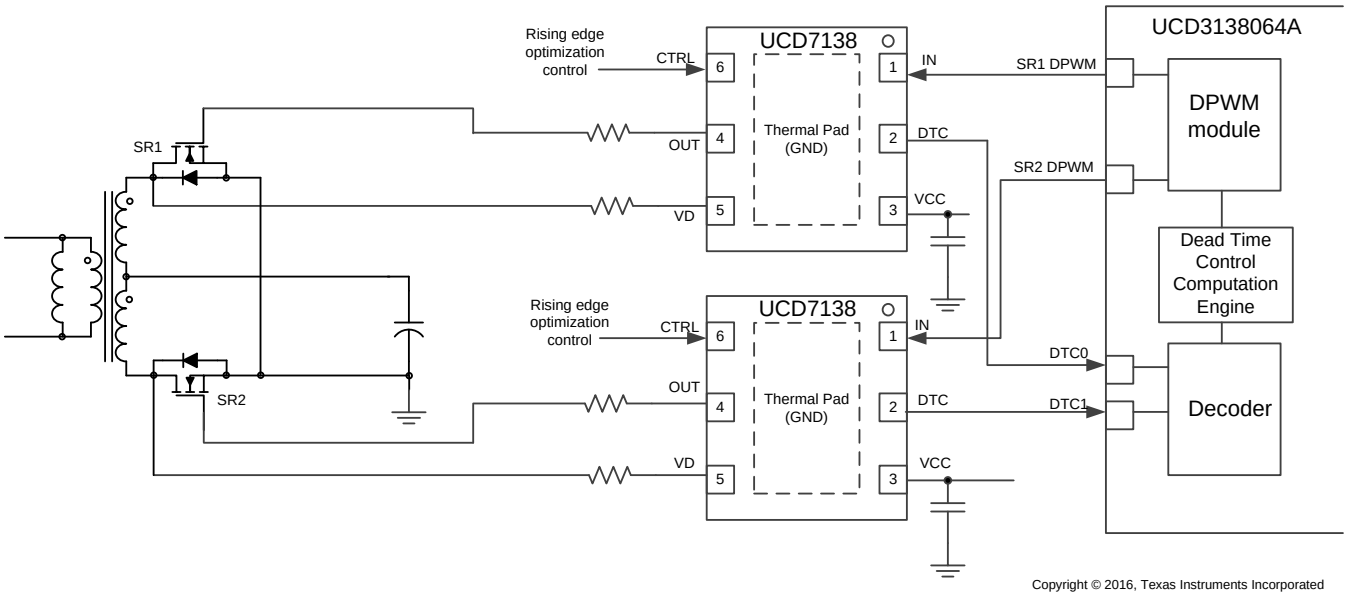


Figure 6-5. Synchronous Rectifier Peripheral use with Synchronous Rectifier Driver

DTC0 and DTC1 are received body diode conduction inputs from UCD7138. SR0_DPWM and SR1_DPWM are the DPWM waveforms for the SRs. The red and green edges are moving edges controlled by both the filter output and the DTC interface. In each cycle, right after the falling edge of the SR DPWM waveform, a body diode conduction time detection window is generated. The detection window is defined by both DETECT_BLANK and DETECT_LEN registers. During this detection window, a 4-ns timer capture counts how long the body diode conducts. Then the DPWM turn off edge of the next cycle is adjusted accordingly.

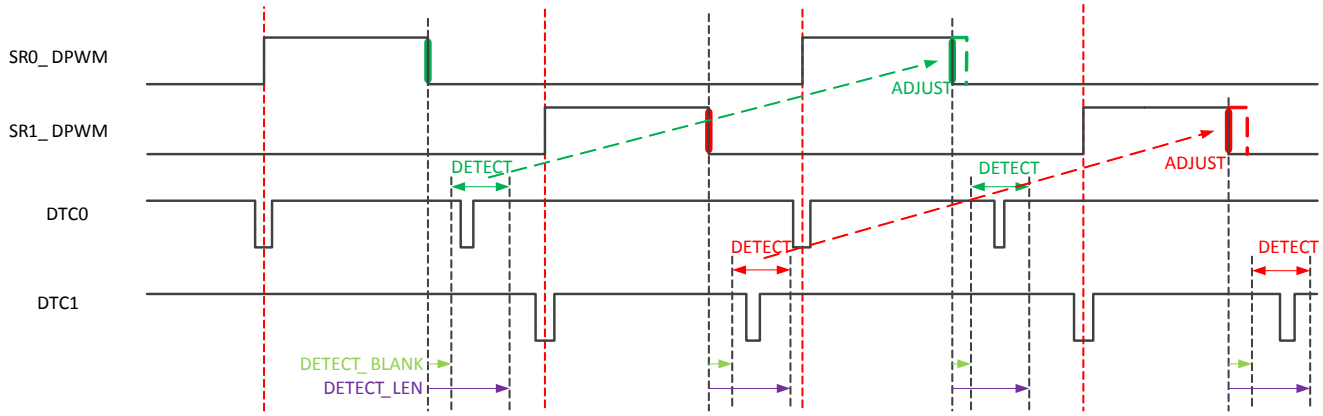


Figure 6-6. Timing Diagram of the DTC Interface

Figure 6-7 shows how the turn-off edge is adjusted based on the DTC measurement of the previous cycle. The A_ADJ and B_ADJ registers in DTCMONITOR are signed accumulators; default value is 0.

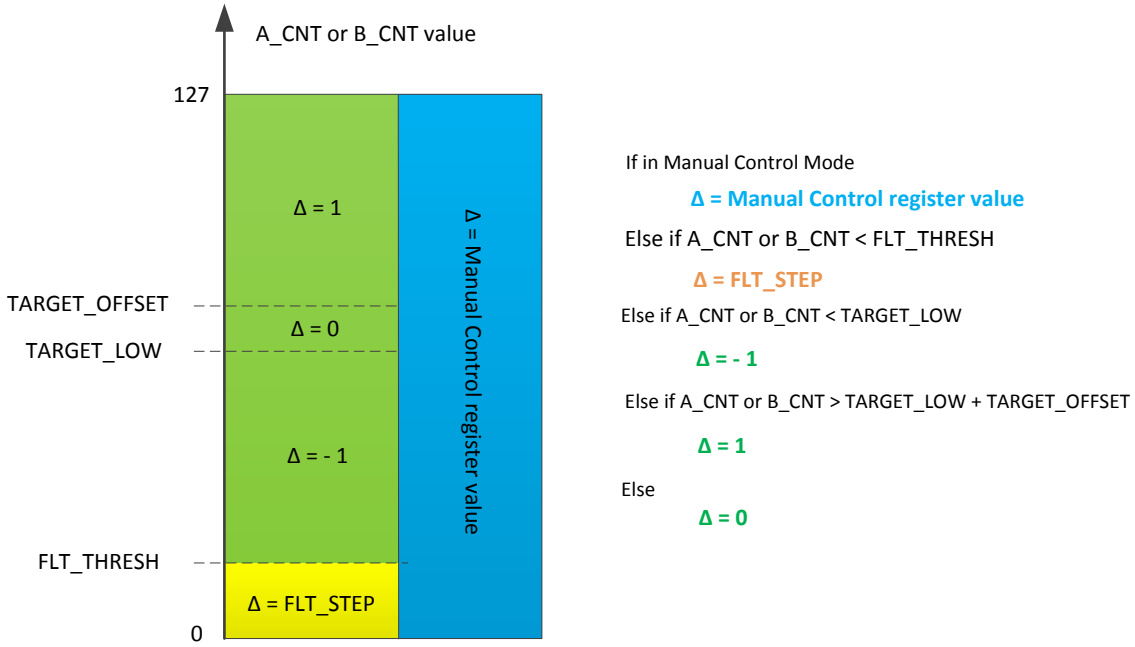


Figure 6-7. DTC Interface Principle

Based on the DTC measured, in the next cycle:

- A_ADJ = A_ADJ + A_Δ
- A_ADJ = A_ADJ + B_Δ

In each cycle, the A_ADJ and B_ADJ accumulator values are dynamically adjust the dead time. The Δ value changes after the measured body diode conduction time. A_ADJ and B_ADJ have been measured and compared to the threshold values in automatic control mode. A_ADJ and B_ADJ can be controlled by firmware while in manual control mode.

Other figures of this peripheral include negative current fault protection, consecutive fault counter, DTC input multiplexor, etc. For details, refer to the programmer's manual.

6.4.4 Automatic Mode Switching

Automatic Mode switching enables the DPWM module to switch between modes automatically, with no firmware intervention. This is useful to increase efficiency and power range. The following paragraphs describe phase-shifted full bridge and LLC examples.

6.4.4.1 Phase Shifted Full Bridge Example

In phase shifted full bridge topologies, efficiency can be increased by using pulse width modulation, rather than phase shift, at light load. This is shown in Figure 6-8 below:

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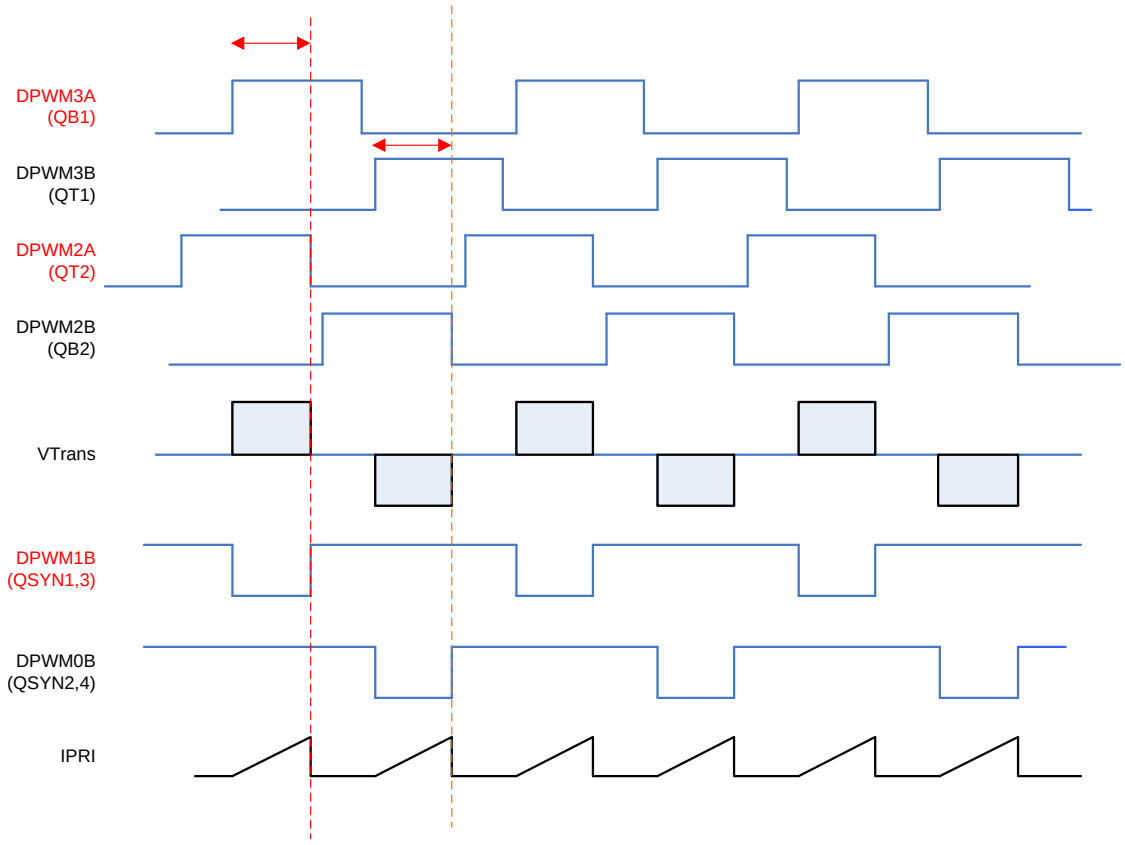


Figure 6-8. Phase-Shifted Full Bridge Waveforms

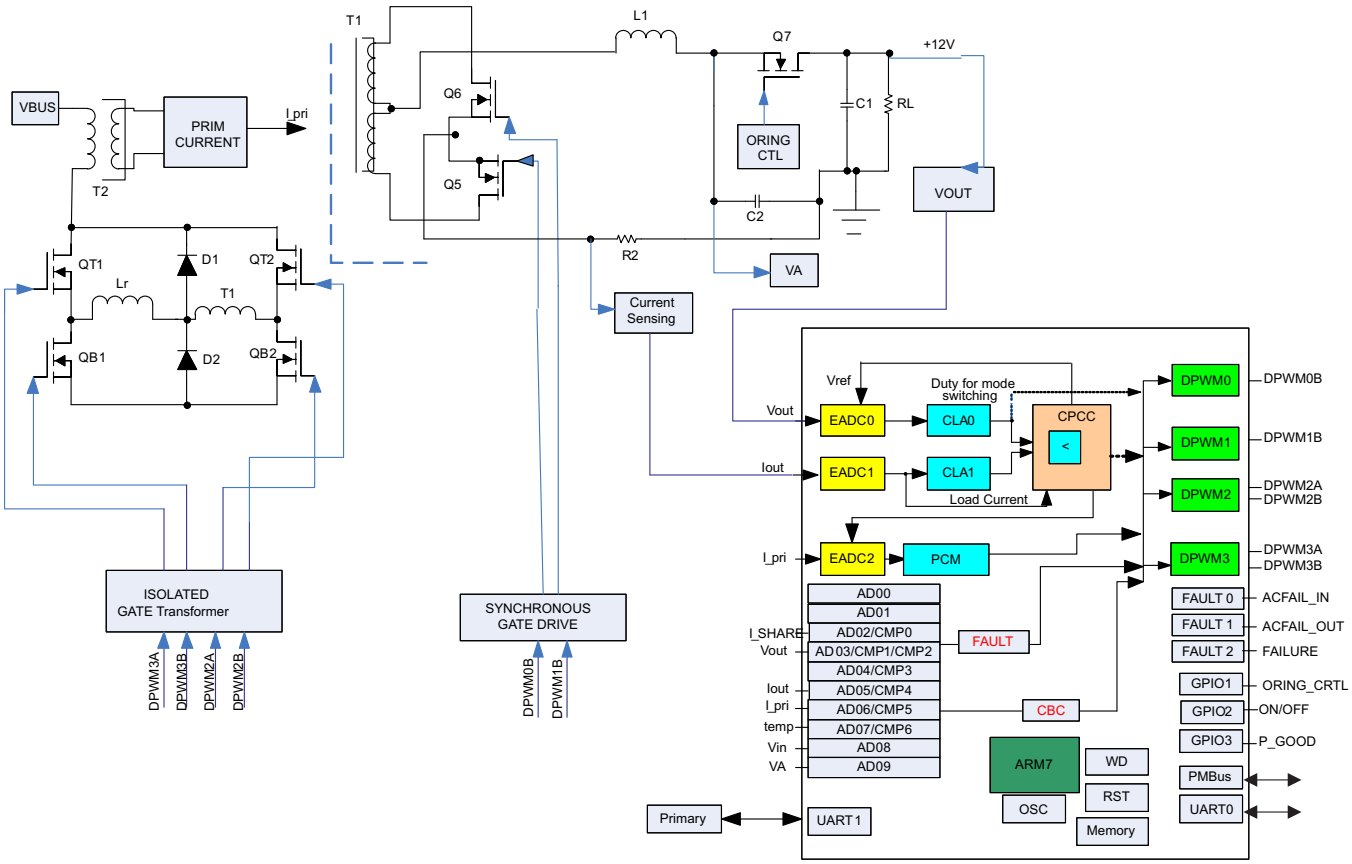


Figure 6-9. Secondary-Referenced Phase-Shifted Full Bridge Control With Synchronous Rectification

6.4.4.2 LLC Example

In LLC, three modes are used. At the highest frequency, a pulse width modulated mode (Multi Mode) is used. As the frequency decreases, resonant mode is used. As the frequency gets still lower, the synchronous MOSFET drive changes so that the on-time is fixed and does not increase. In addition, the LLC control supports cycle-by-cycle current limiting. This protection function operates by a comparator monitoring the maximum current during the DPWMA conduction time. Any time this current exceeds the programmable comparator reference the pulse is immediately terminated. Due to classic instability issues associated with half-bridge topologies it is also possible to force DPWMB to match the truncated pulse width of DPWMA. The waveforms for the LLC are shown in Figure 6-10:

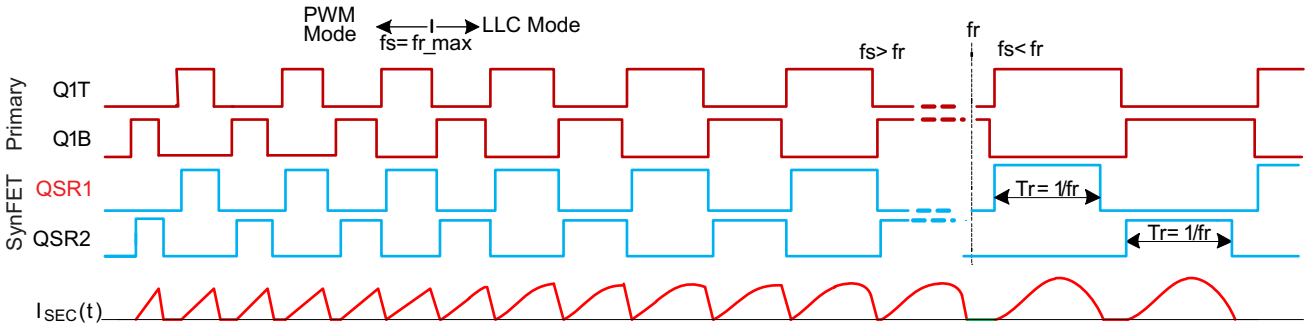


Figure 6-10. LLC Waveforms

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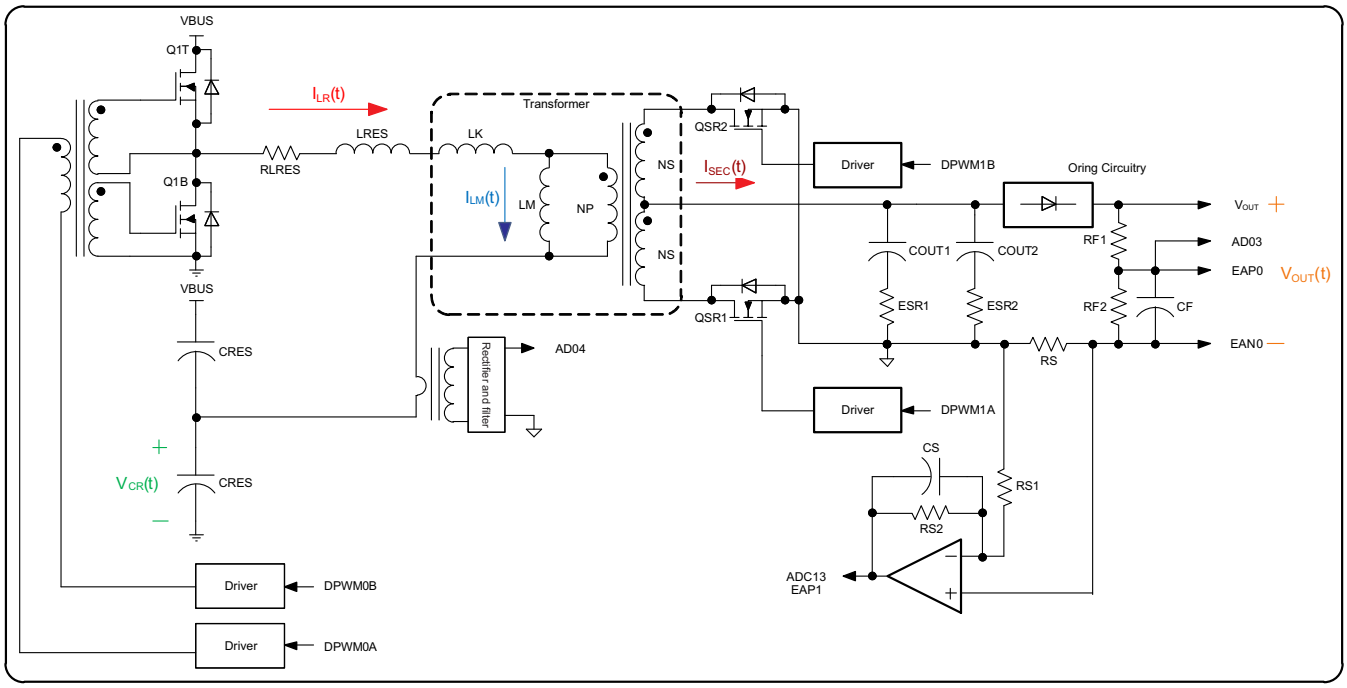


Figure 6-11. Secondary-Referenced Half-Bridge Resonant LLC Control With Synchronous Rectification

6.4.4.3 Mechanism For Automatic Mode Switching

The UCD3138064A allows the customer to enable up to two distinct levels of automatic mode switching. These different modes are used to enhance light load operation, short circuit operation and soft start. Many of the configuration parameters for the DPWM are in DPWM Control Register 1. For automatic mode switching, some of these parameters are duplicated in the Auto Config Mid and Auto Config High registers.

If automatic mode switching is enabled, the filter duty signal is used to select which of these three registers is used. There are 4 registers which are used to select the points at which the mode switching takes place. They are used as shown in Figure 6-12 below.

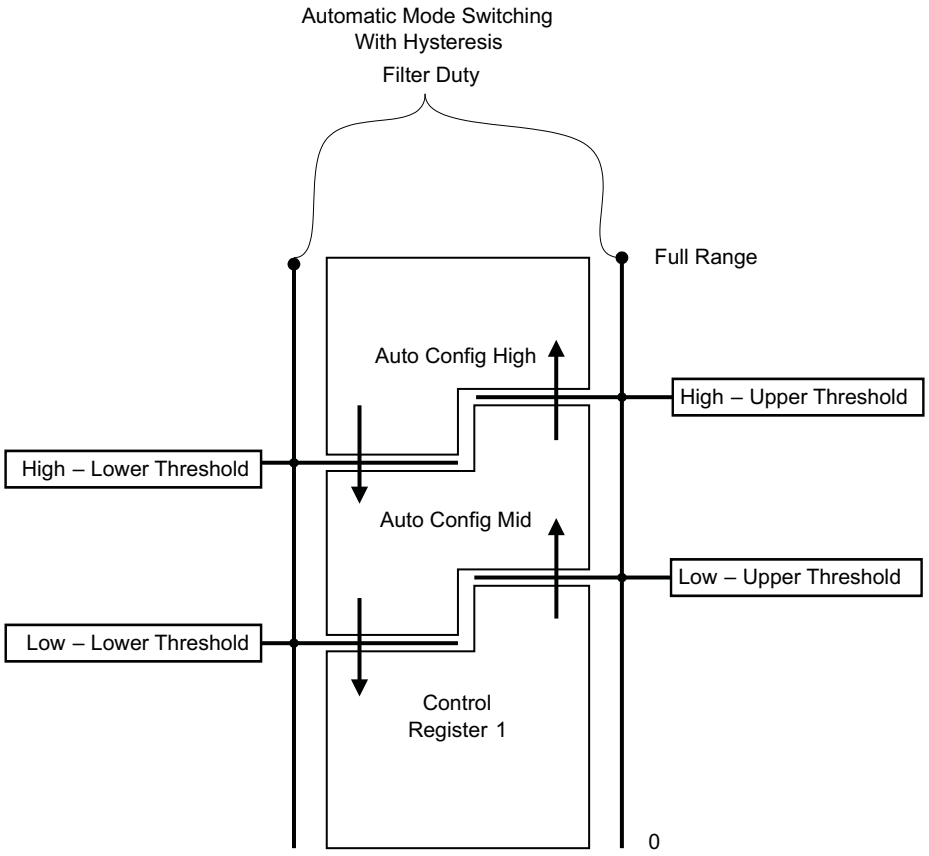


Figure 6-12. Automatic Mode Switching

As shown, the registers are used in pairs for hysteresis. The transition from Control Register 1 to Auto Config Mid only takes place when the Filter Duty goes above the Low Upper threshold. It does not go back to Auto Config Mid until the Low Lower Threshold is passed. This prevents oscillation between modes if the filter duty is close to a mode switching point.

6.4.5 DPWMC, Edge Generation, IntraMux

The UCD3138064A has hardware for generating complex waveforms beyond the simple DPWMA and DPWMB waveforms already discussed – DPWMC, the Edge Generation Module, and the IntraMux.

DPWMC is a signal inside the DPWM logic. It goes high at the Blanking A begin time, and low at the Blanking A end time.

The Edge Gen module takes DPWMA and DPWMB from its own DPWM module, and the next one, and uses them to generate edges for two outputs. For DPWM3, the DPWM0 is considered to be the next DPWM. Each edge (rising and falling for DPWMA and DPWMB) has 8 options which can cause it.

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The options are:

0 = DPWM(n) A Rising edge
1 = DPWM(n) A Falling edge
2 = DPWM(n) B Rising edge
3 = DPWM(n) B Falling edge
4 = DPWM(n+1) A Rising edge
5 = DPWM(n+1) A Falling edge
6 = DPWM(n+1) B Rising edge
7 = DPWM(n+1) B Falling edge

Where “n" is the numerical index of the DPWM module of interest. For example n=1 refers to DPWM1.

The Edge Gen is controlled by the DPWMEDGEGEN register. It also has an enable/disable bit.

The IntraMux is controlled by the Auto Config registers. Intra Mux is short for intra multiplexer. The IntraMux takes signals from multiple DPWMs and from the Edge Gen and combines them logically to generate DPWMA and DPWMB signals This is useful for topologies like phase-shifted full bridge, especially when they are controlled with automatic mode switching. Of course, it can all be disabled, and DPWMA and DPWMB will be driven as described in the sections above. If the Intra Mux is enabled, high resolution must be disabled, and DPWM edge resolution goes down to 4 ns.

Figure 6-13 shows the Edge Gen/Intra Mux:

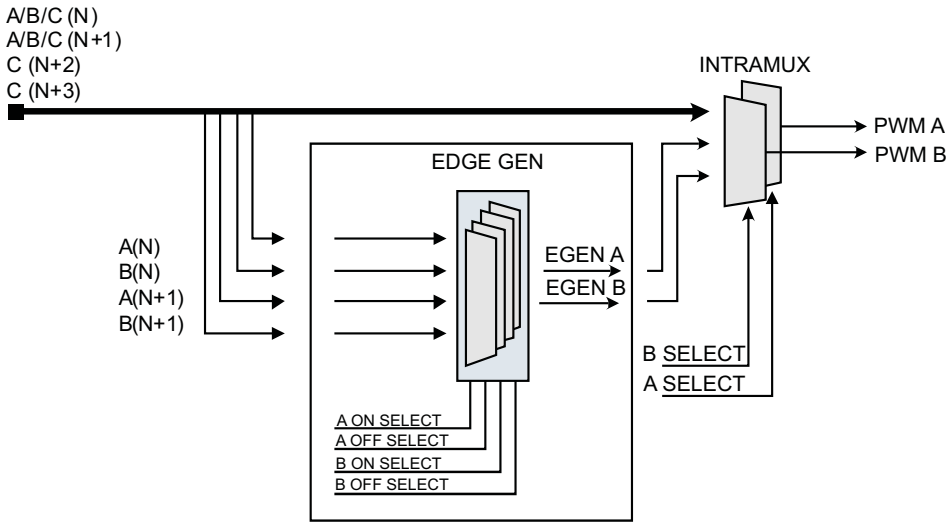


Figure 6-13. Edge Generation / IntraMux

Here is a list of the IntraMux modes for DPWMA:

0 = DPWMA(n) pass through (default)
1 = Edge-gen output, DPWMA(n)
2 = DPWNC(n)
3 = DPWMB(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

and for DPWMB:

0 = DPWMB(n) pass through (default)
1 = Edge-gen output, DPWMB(n)
2 = DPWNC(n)

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3 = DPWMA(n) (Crossover)
4 = DPWMA(n+1)
5 = DPWMB(n+1)
6 = DPWMC(n+1)
7 = DPWMC(n+2)
8 = DPWMC(n+3)

The DPWM number wraps around just like the Edge Gen unit. For DPWM3 the following definitions apply:

DPWM(n)	DPWM3
DPWM(n+1)	DPWM0
DPWM(n+2)	DPWM1
DPWM(n+3)	DPWM2

6.4.6 Filter

The UCD3138064A filter is a PID filter with many enhancements for power supply control. Some of its features include:

- Traditional PID Architecture
- Programmable non-linear limits for automated modification of filter coefficients based on received EADC error
- Multiple coefficient sets fully configurable by firmware
- Full 24-bit precision throughout filter calculations
- Programmable clamps on integrator branch and filter output
- Ability to load values into internal filter registers while system is running
- Ability to stall calculations on any of the individual filter branches
- Ability to turn off calculations on any of the individual filter branches
- Duty cycle, resonant period, or phase shift generation based on filter output.
- Flux balancing
- Voltage feed forward

The first section of the filter is shown in Figure 6-14 :

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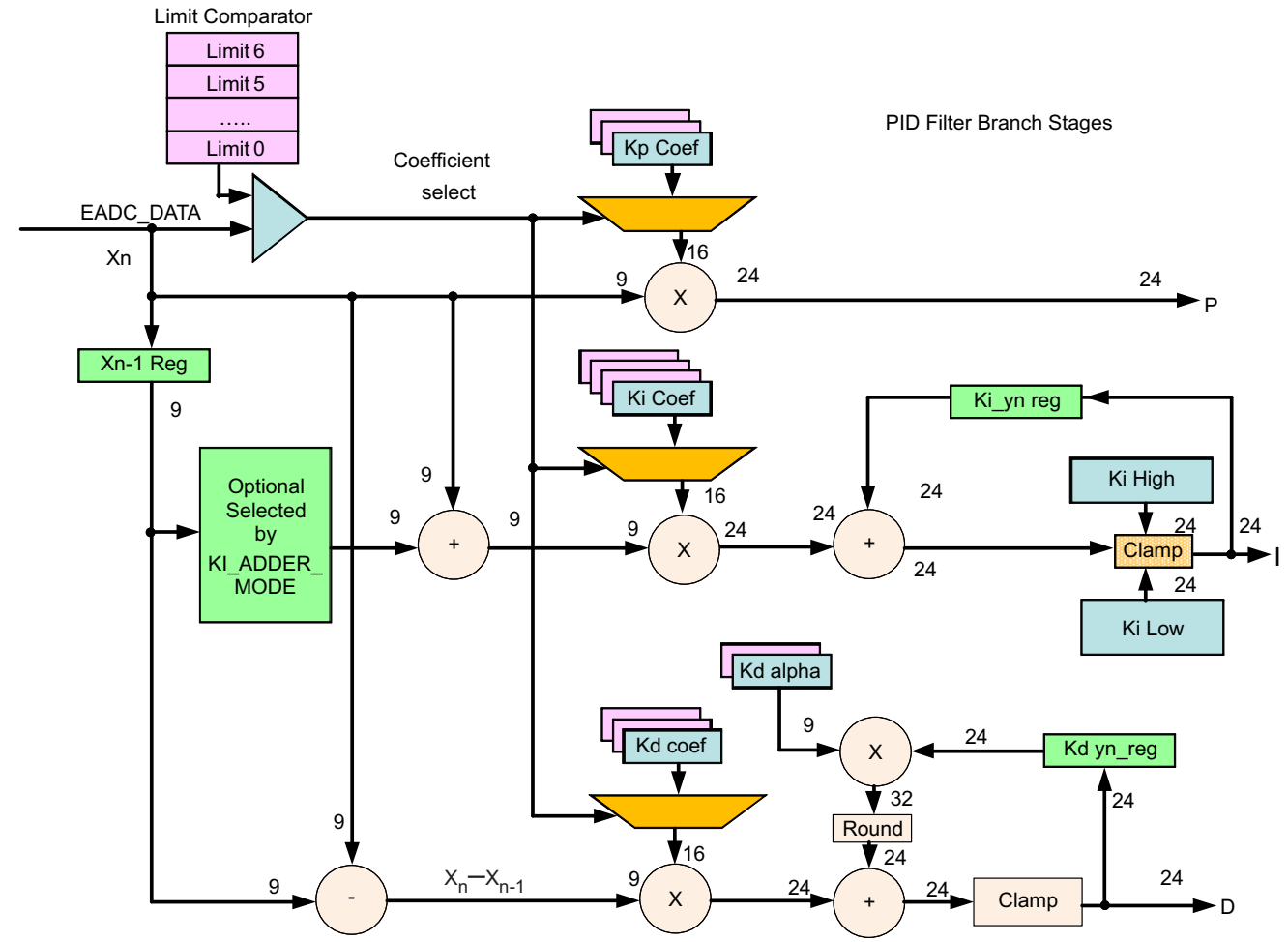


Figure 6-14. First Section of the Filter

The filter input, Xn, generally comes from a front end. Then there are three branches, P, I. and D. Note that the D branch also has a pole, Kd Alpha. Clamps are provided both on the I branch and on the D alpha pole.

The filter also supports a nonlinear mode, where up to 7 different sets of coefficients can be selected depending on the magnitude of the error input Xn. This can be used to increase the filter gain for higher errors to improve transient response.

Tthe output section of the filter (S0.23 means that there is 1 sign bit, 0 integer bits and 23 fractional bits) is shown in Figure 6-15.:

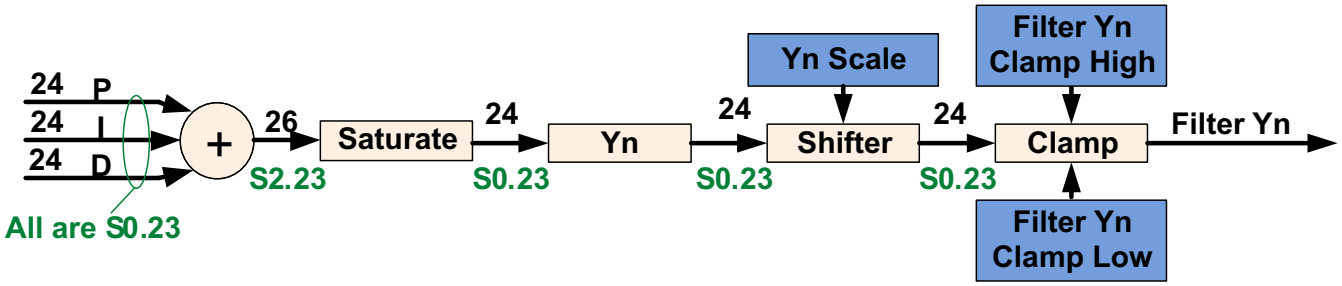


Figure 6-15. Output Section of the Filter

This section combines the P, I, and D sections, and provides for saturation, scaling, and clamping.

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There is a final section for the filter, shown in Figure 6-16 that permits its output to be matched to the DPWM:

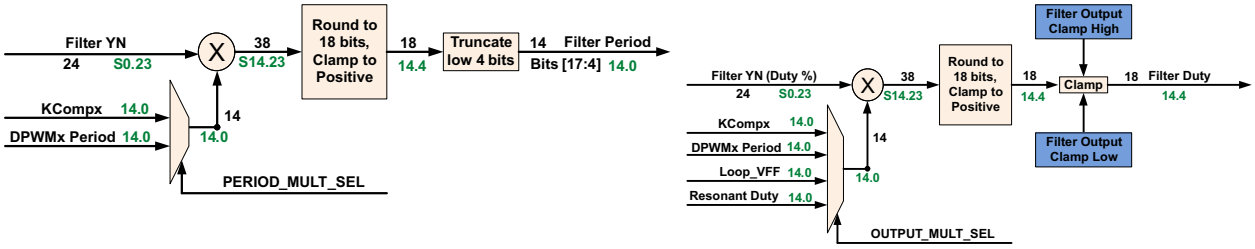


Figure 6-16. Final Section for the Filter

This permits the filter output to be multiplied by a variety of correction factors to match the DPWM Period, to provide for Voltage Feed Forward, or for other purposes. After this, there is another clamp. For resonant mode, the filter can be used to generate both period and duty cycle.

6.4.6.1 Loop Multiplexer

The Loop Mux controls interconnections between the filters, front ends, and DPWMs. Any filter, front end, and DPWM can be combined in a variety of configurations.

It also controls the following connections:

- DPWM to Front End
- Front End DAC control from Filters or Constant Current/Constant Power Module
- Filter Special Coefficients and Feed Forward
- DPWM synchronization
- Filter to DPWM

The following control modules are configured in the Loop Mux:

- Constant Power/Constant Current
- Cycle Adjustment (Current and flux balancing)
- Global Period
- Light Load (Burst Mode)
- Analog Peak Current Mode

6.4.6.2 Fault Multiplexer

In order to allow a flexible way of mapping several fault triggering sources to all the DPWMs channels, the UCD3138x provides an extensive array of multiplexers that are united under the name Fault Mux module.

The Fault Mux Module supports the following types of mapping between all the sources of fault and all the different fault response mechanisms inside each DPWM module.

- Many fault sources may be mapped to a single fault response mechanism. For instance an analog comparator in charge of over voltage protection, a digital comparator in charge of over current protection and an external digital fault pin can be all mapped to a Fault-A signal connected to a single FAULT MODULE and shut down DPWM1-A.
- A single fault source can be mapped to many fault response mechanisms inside many DPWM modules. For instance an analog comparator in charge of over current protection can be mapped to DPWM-0 through DPWM-3 by way of several fault modules.
- Many fault sources can be mapped to many fault modules inside many DPWM modules.

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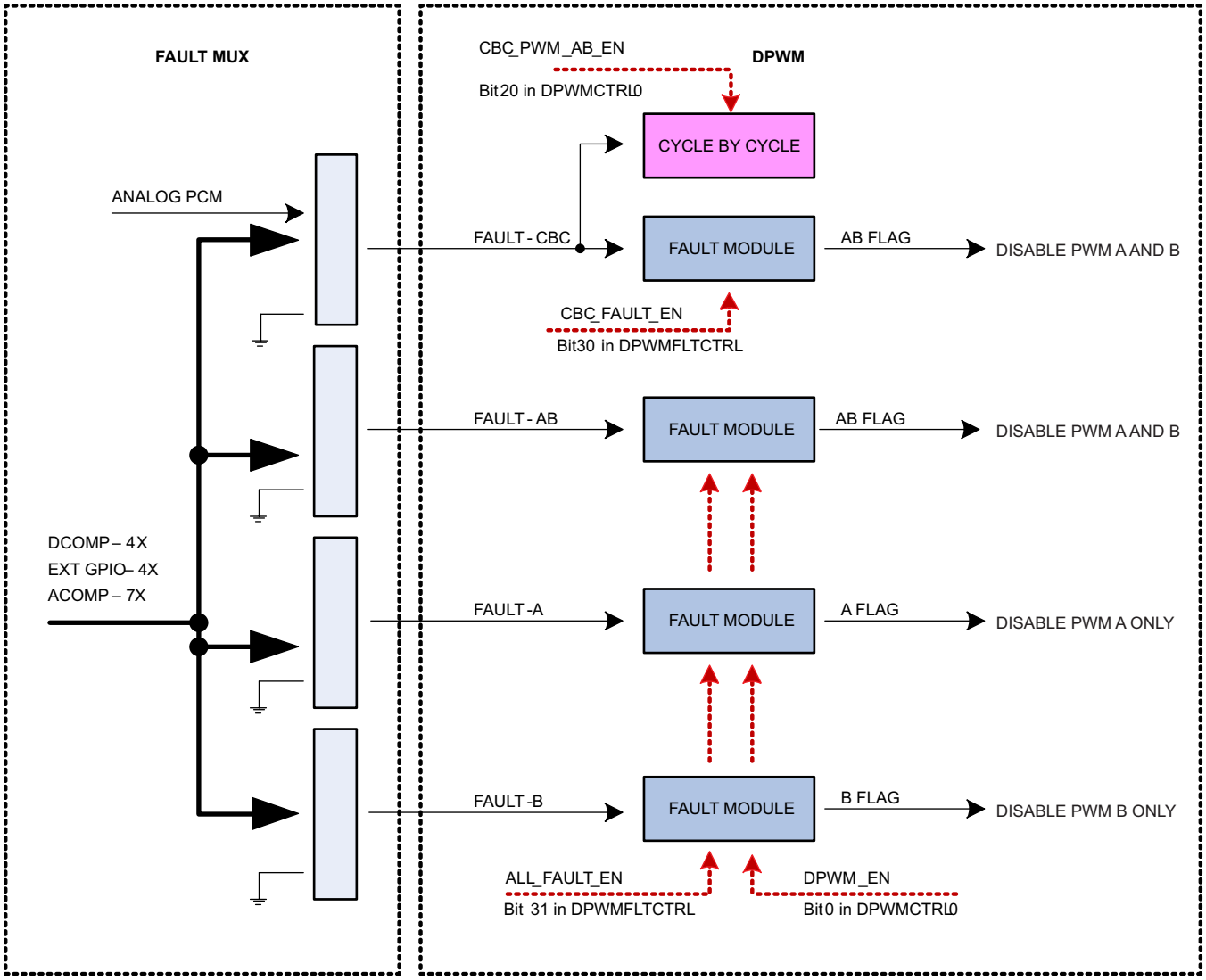


Figure 6-17. Fault Mux Module

The Fault Mux Module provides a multitude of fault protection functions within the UCD3138x high-speed loop (Front End Control, Filter, DPWM and Loop Mux modules). The Fault Mux Module allows highly configurable fault generation based on digital comparators, high-speed analog comparators and external fault pins. Each of the fault inputs to the DPWM modules can be configured to one or any combination of the fault events provided in the Fault Mux Module.

Each one of the DPWM engines has four fault modules. The modules are called CBC fault module, AB fault module, A fault module and B fault module.

The internal circuitry in all the four fault modules is identical, and the difference between the modules is limited to the way the modules are attached to the DPWMs.

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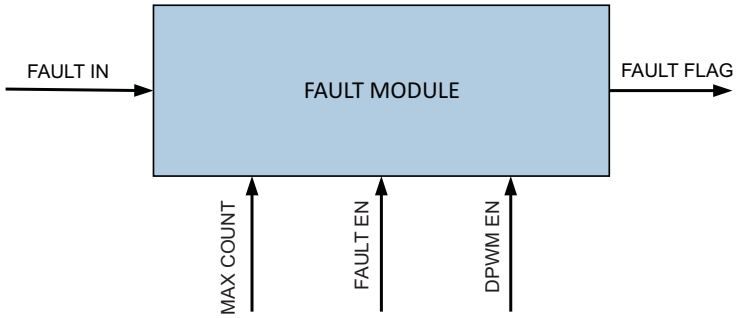


Figure 6-18. Fault Module

All fault modules provide immediate fault detection but only once per DPWM switching cycle. Each one of the fault modules own a separate max_count and the fault flag will be set only if sequential cycle-by-cycle fault count exceeds max_count.

Once the fault flag is set, DPWMs need to be disabled by DPWM_EN going low in order to clear the fault flags. Please note, all four Fault Modules share the same DPWM_EN control, all fault flags (output of Fault Modules) will be cleared simultaneously.

All four Fault Modules share the same global FAULT_EN as well. Therefore a specific Fault Module cannot be enabled/ disabled separately.



Figure 6-19. Cycle-By-Cycle Block

Unlike Fault Modules, only one Cycle by Cycle block is available in each DPWM module.

The Cycle by Cycle block works in conjunction with CBC Fault Module and enables DPWM reaction to signals arriving from the Analog Peak current mode (PCM) module.

The Fault Mux Module supports the following basic functions:

- 4 digital comparators with programmable thresholds and fault generation
- Configuration for 7 high speed analog comparators with programmable thresholds and fault generation
- External GPIO detection control with programmable fault generation
- Configurable DPWM fault generation for DPWM Current Limit Fault, DPWM Over-Voltage Detection Fault, DPWM A External Fault, DPWM B External Fault and DPWM IDE Flag
- Clock Failure Detection for High and Low Frequency Oscillator blocks
- Discontinuous Conduction Mode Detection

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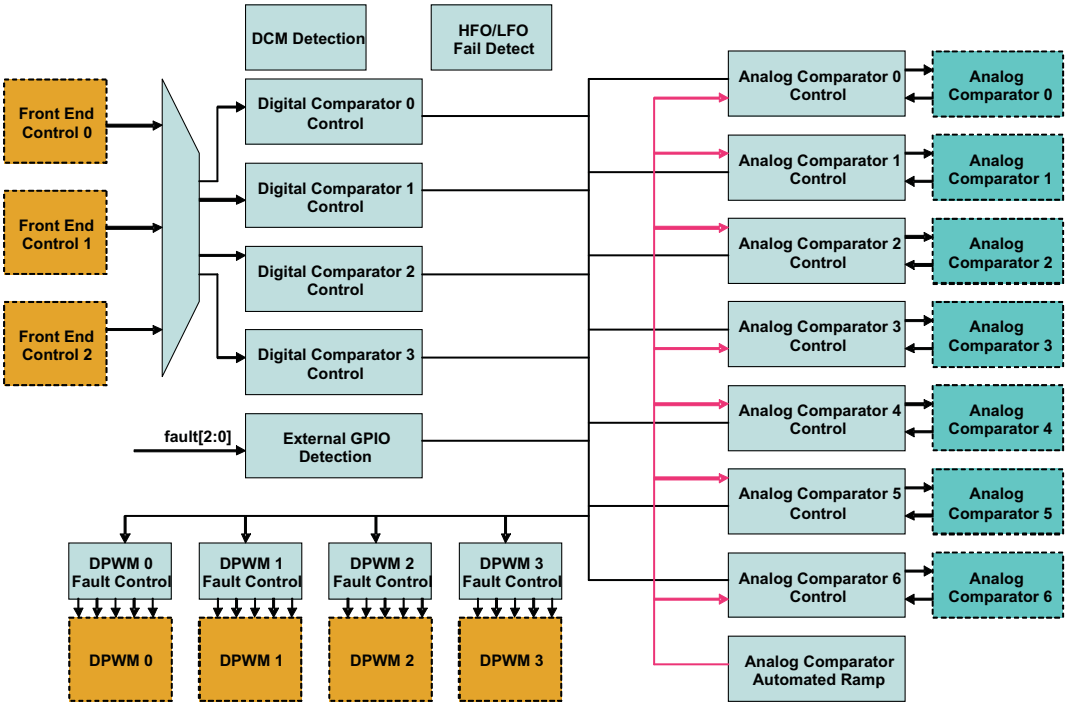


Figure 6-20. Fault Mux Block Diagram

6.4.7 Communication Ports

6.4.7.1 SCI (UART) Serial Communication Interface

A maximum of two independent Serial Communication Interface (SCI) or Universal Asynchronous Receiver/Transmitter (UART) interfaces are included within the device for asynchronous start-stop serial data communication (see the pin out sections for details). Each interface has a 24 bit pre-scaler for supporting programmable baud rates, a programmable data word and stop bit options. Half or full duplex operation is configurable through register bits. A loop back feature can also be setup for firmware verification. Both SCI-TX and SCI-RX pin sets can be used as GPIO pins when the peripheral is not being used.

The UART peripheral includes a hardware based auto baud rate adjustment feature. Power supply controllers typically use temperature compensated RC based oscillators. Despite the temperature compensation, the clock speed will change with temperature. This can lead to a difference in baud rate between two controllers, leading to lost of communication. The UCD3138064A adds logic which can match the receive baud rate by measuring the bit timing of the incoming signal.

In Addition, the UCD3138064A increases the resolution of the baud rate adjustment. The UCD3138064 has 512 ns resolution, while the UCD3138064A adds 3 bits and provides 64 ns resolution on the baud rate. This makes the use ot auto baud possible at higher baud rates.

6.4.7.2 PMBUS/I^2C

The PMBus interface in UCD3138064A supports both master and slave modes. The I^2C interface only supports master mode. Only one of the interfaces has control of the address pin current sources as well as support for the optional Control and Alert lines described in the PMBus specification. Other than these differences, the interfaces are identical.

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The PMBus/I^{2}C interface is designed to minimize the processor overhead required for interface. It can automatically detect and acknowledge addresses. It handles start and stop conditions automatically, and can clock stretch until the processor has time to poll the PMBus status. It will automatically receive and send up to 4 bytes at a time. It can automatically verify and generate a PEC. This means that a write byte command can be received by the processor with only one function call. There is no need for any interrupts at all with this PMBus/I^{2}C interface. If it is polled every few milliseconds, it will work perfectly.

The interface also supports automatic ACK of two independent addresses. If both PMBus/I^{2}C interfaces are used at the same time a total of 4 independent addresses can be automatically detected.

Example: PMBus Address Decode via ADC12 Reading

The user can allocate 2 pins of the 12-bit ADC input channels, AD_00 and AD_01, for PMBus address decoding. At power-up the device applies I_{BIAS} to each address detect pin and the voltage on that pin is captured by the internal 12-bit ADC.

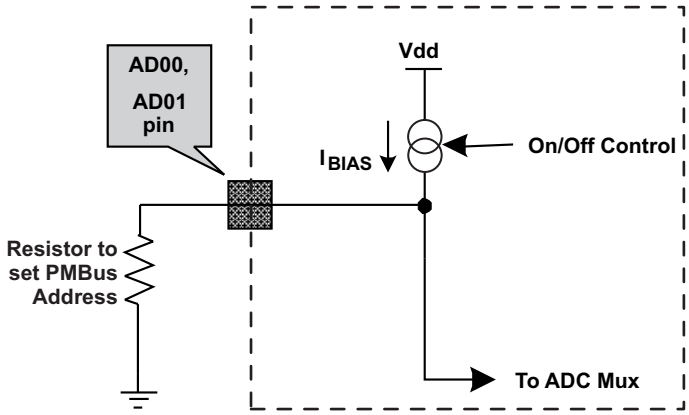


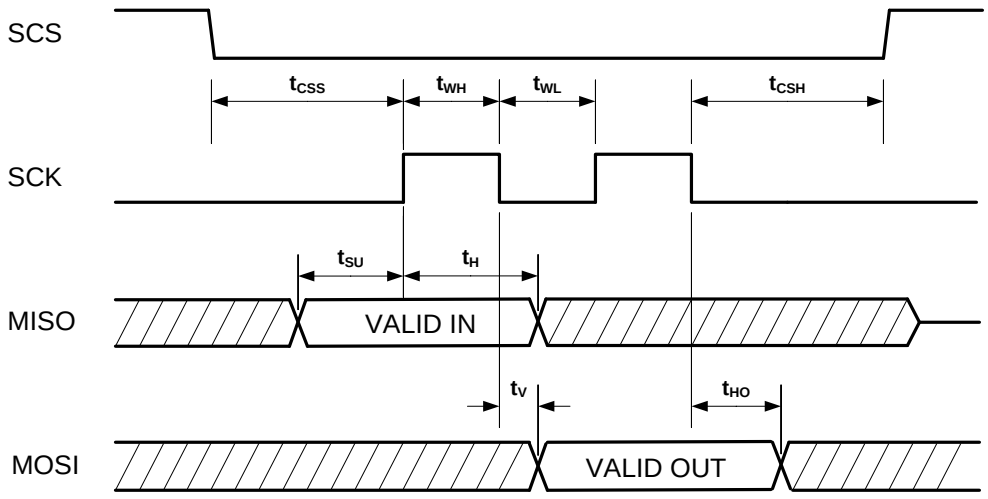
Figure 6-21. PMBUS Address Detection Method

PMBus/I^{2}C address 0x7E is a reserved address and should not be used in a system using the UCD3138x. This address is used for manufacturing test.

6.4.7.3 SPI

The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the UCD3138x and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters. The SPI allows serial communication with other SPI devices through a 3-pin or 4-pin mode interface.

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P_{SCK}	**Period SCK**	**2 ICLK**
t_{WH}	**SCK High Time**	**1/2 P_{SCK}**
t_{WL}	**SCK Low Time**	**1/2 P_{SCK}**
t_{SU}	**Data in setup**	**2 ns (typical)**
t_H	**Data in hold**	**4 ns (typical)**
t_V	**Ouput Valid**	**4 ns (typical)**
t_{HO}	**Ouput Data Hold**	**2 ns (typical)**
t_{CSS}	**Chip Select Setup**	**1 P_{SCK}**
t_{CSH}	**Chip Select Hold**	**1 P_{SCK}**

Figure 6-22. SPI Timing Diagram

6.4.8 Timers

External to the Digital Power Peripherals there are 3 different types of timers in UCD3138x. They are the 24-bit timer, 16-bit timer and the watchdog timer

6.4.8.1 24-Bit Timer

There is one 24 bit timer which runs off the Interface Clock. It can be used to measure the time between two events, and to generate interrupts after a specific interval. Its clock can be divided down by an 8-bit pre-scalar to provide longer intervals. The timer has two compare registers (Data Registers). Both can be used to generate an interrupt after a time interval. . Additionally, the timer has a shadow register (Data Buffer register) which can be used to store CPU updates of the compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

The two capture pins TCAP0 and TCAP1 are inputs for recording a capture event. A capture event can be set either to rising, falling, or both edges of the capture pin signal. Upon this event, the counter value is stored in the corresponding capture data register. Five Interrupts from the 24 bit timer can be set, which are the counter rollover event (overflow), capture events 0 and 1, and the two comparison match events. Each interrupt can be disabled or enabled.

6.4.8.2 16-Bit PWM Timers

There are four 16 bit counter PWM timers which run off the Interface Clock and can further be divided down by a 8-bit pre-scaler to generate slower PWM time periods. Each timer has two compare registers (Data Registers) for generating the PWM set/unset events. Additionally, each timer has a shadow register (Data Buffer register) which can be used to store CPU updates of compare events while still using the timer. The selected shadow register update mode happens after the compare event matches.

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The counter reset can be configured to happen on a counter roll over, a compare equal event, or by a software controlled register. Interrupts from the PWM timer can be set due to the counter rollover event (overflow) or by the two comparison match events. Each comparison match and the overflow interrupts can be disabled or enabled.

Upon an event comparison, the PWM pin can be configured to set, clear, toggle or have no action at the output. The value of PWM pin output can be read for status or simply configured as General Purpose I/O for reading the value of the input at the pin.

6.4.8.3 Watchdog Timer

A watchdog timer is provided on the device for ensuring proper firmware loop execution. The timer is clocked off of a separate low speed oscillator source. If the timer is allowed to expire, a reset condition is issued to the ARM processor. The watchdog is reset by a simple CPU write bit to the watchdog key register by the firmware routine. On device power-up the watchdog is disabled. Yet after it is enabled, the watchdog cannot be disabled by firmware. Only a device reset can put this bit back to the default disabled state. A half timer flag is also provided for status monitoring of the watchdog.

6.4.9 General Purpose ADC12

The ADC12 is a 12 bit, high speed analog to digital converter, equipped with the following options:

- Typical conversion speed of 267 ksps
- Conversions can consist from 1 to 16 ADC channel conversions in any desired sequence
- Post conversion averaging capability, ranging from 4X, 8X, 16X or 32X samples
- Configurable triggering for ADC conversions from the following sources: firmware, DPWM rising edge, ADC_EXT_TRIG pin or Analog Comparator results
- Interrupt capability to embedded processor at completion of ADC conversion
- Six digital comparators on the first 6 channels of the conversion sequence using either raw ADC data or averaged ADC data
- Two 10 µA current sources for excitation of PMBus addressing resistors
- Dual sample and hold for accurate power measurement
- Internal temperature sensor for temperature protection and monitoring

The control module (Figure 6-23) contains the control and conversion logic for auto-sequencing a series of conversions. The sequencing is fully configurable for any combination of 16 possible ADC channels through an analog multiplexer embedded in the ADC12 block. Once converted, the selected channel value is stored in the result register associated with the sequence number. Input channels can be sampled in any desired order or programmed to repeat conversions on the same channel multiple times during a conversion sequence. Selected channel conversions are also stored in the result registers in order of conversion, where the result 0 register is the first conversion of a 16-channel sequence and result 15 register is the last conversion of a 16-channel sequence. The number of channels converted in a sequence can vary from 1 to 16.

Unlike EADC0 through EADC2, which are primarily designed for closing high speed compensation loops, the ADC12 is not usually used for loop compensation purposes. The EADC converters have a substantially faster conversion rate, thus making them more attractive for closed loop control. The ADC12 features make it best suited for monitoring and detection of currents, voltages, temperatures and faults. Please see Section 5.9 for the temperature variation associated with this function.

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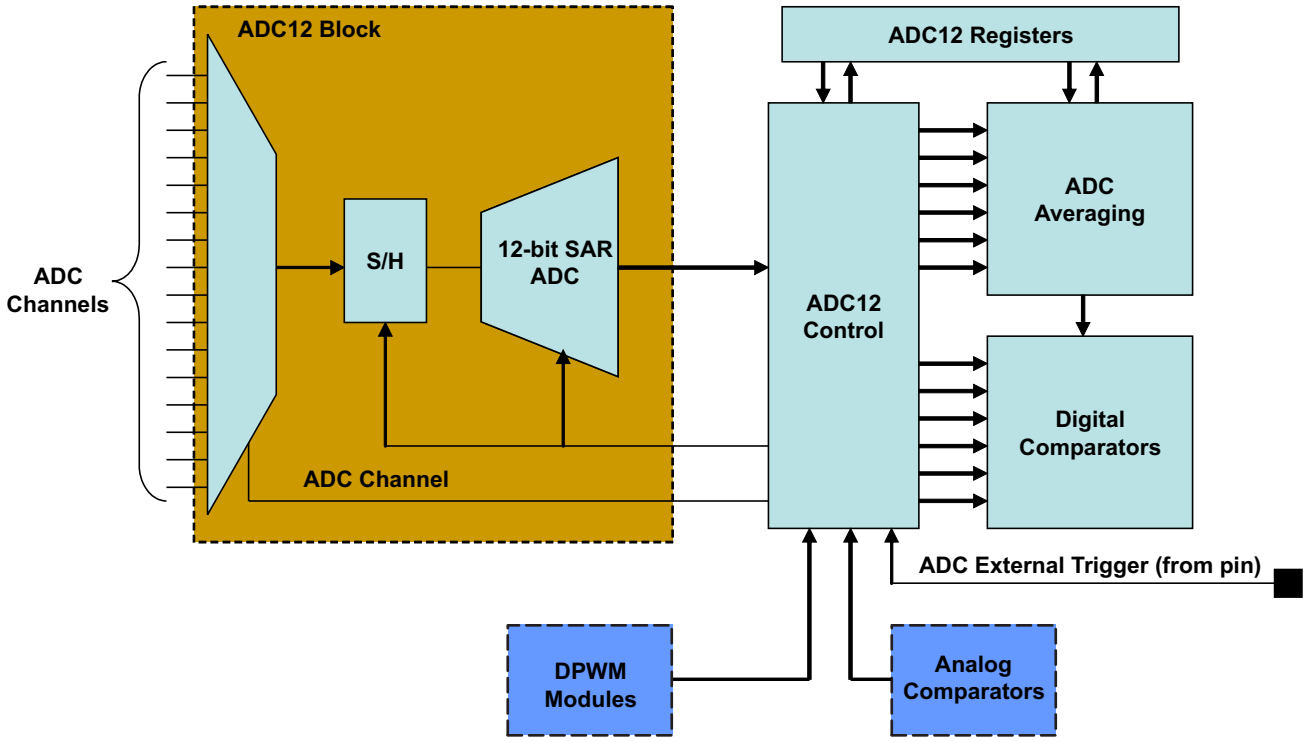


Figure 6-23. ADC12 Control Block Diagram

6.4.10 Miscellaneous Analog

The Miscellaneous Analog Control (MAC) Registers are a catch-all of registers that control and monitor a wide variety of functions. These functions include device supervisory features such as Brown-Out and power saving configuration, general purpose input/output configuration and interfacing, internal temperature sensor control and current sharing control.

The MAC module also provides trim signals to the oscillator and AFE blocks. These controls are usually used at the time of trimming at manufacturing; therefore this document will not cover these trim controls.

6.4.11 Brownout

Brownout function is used to determine if the device supply voltage is lower than a threshold voltage, a condition that may be considered unsafe for proper operation of the device.

The brownout threshold is higher than the reset threshold voltage; therefore, when the supply voltage is lower than brownout threshold, it still does not necessarily trigger a device reset.

The brownout interrupt flag can be polled or alternatively can trigger an interrupt to service such case by an interrupt service routine. Please see Figure 5-4.

6.4.12 Global I/O

Up to 32 pins in UCD3138x can be configured in the Global I/O register to serve as a general purpose input or output pins (GPIO). This includes all digital input or output pins except for the RESET pin.

The pins that cannot be configured as GPIO pins are the supply pins, ground pins, ADC-12 analog input pins, EADC analog input pins and the RESET pin. Additional digital pins not listed in this register can be configured through their local configuration registers.

There are two ways to configure and use the digital pins as GPIO pins:

1. Through the centralized Global I/O control registers.
2. Through the distributed control registers in the specific peripheral that shares it pins with the standard

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GPIO functionality.

The Global I/O registers offer full control of:

1. Configuring each pin as a GPIO.
2. Setting each pin as input or output.
3. Reading the pin's logic state, if it is configured as an input pin.
4. Setting the logic state of the pin, if it is configured as an output pin.
5. Connecting pin/pins to high rail through internal push/pull drivers or external pull up resistors.

The Global I/O registers include Global I/O EN register, Global I/O OE Register, Global I/O Open Drain Control Register, Global I/O Value Register and Global I/O Read Register.

The following is showing the format of Global I/O EN Register (GLBIOEN) as an example:

BIT NUMBER	31:0
Bit Name	GLOBAL_IO_EN
Access	R/W
Default	0000_0000_0000_0000_0000_0000_0000_0000

Bits 29-0: GLOBAL_IO_EN – This register enables the global control of digital I/O pins
0 = Control of IO is done by the functional block assigned to the IO (Default)
1 = Control of IO is done by Global IO registers.

BIT	PIN_NAME	PIN NUMBER
		UCD3138x
31	PWM2	11
30	PWM3	12
29	FAULT3	55
28	ADC_EXT_TRIG	14
27	TCK	45
26	TDO	46
25	TMS	48
24	TDI	47
23	SCI_TX1	37
22	SCI_TX0	35
21	SCI_RX1	38
20	SCI_RX0	36
19	TCAP0	49
18	PWM1	40
17	PWM0	39
16	TCAP1	13
15	I2C_DATA	20
14	PMBUS_CTRL	18
13	PMBUS_ALERT	17
12	EXT_INT	42
11	FAULT2	54
10	FAULT1	44
9	FAULT0	43
8	SYNC	34
7	DPWM3B	29
6	DPWM3A	28
5	DPWM2B	27
4	DPWM2A	26
3	DPWM1B	25

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BIT	PIN_NAME	PIN NUMBER
		UCD3138x
2	DPWM1A	24
1	DPWM0B	23
0	DPWM0A	22

6.4.13 Temperature Sensor Control

Temperature sensor control register provides internal temperature sensor enabling and trimming capabilities. The internal temperature sensor is disabled by default.

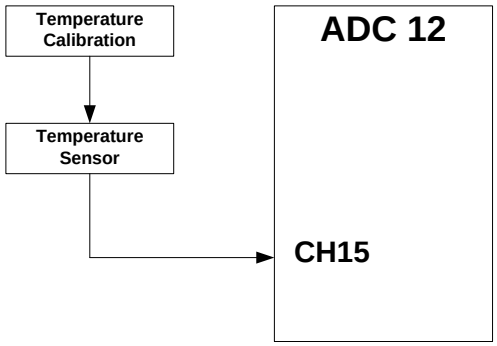


Figure 6-24. Internal Temp Sensor

Temperature sensor is calibrated at room temperature (25 °C) via a calibration register value.

The temperature sensor is measured using ADC12 (via Ch15). The temperature is then calculated using a mathematical formula involving the calibration register (this effectively adds a delta to the ADC measurement).

The temperature sensor can be enabled or disabled.

6.4.14 I/O Mux Control

I/O Mux Control register may be used in order to choose a single specific functionality that is desired to be assigned to a physical device pin for your application. See the UCD3138x programmer's manual for details on the available configurations.

6.4.15 Current Sharing Control

UCD3138x provides three separate modes of current sharing operation.

- Analog bus current sharing
- PWM bus current sharing
- Master/Slave current sharing
- AD02 has a special ESD protection mechanism that prevents the pin from pulling down the current-share bus if power is missing from the UCD3138x

The simplified current sharing circuitry is shown in the drawing below. The digital pulse connected to SW3 transforms SW3 into a pulse-width-modulated current source. Details on the frequency and resolution of this feature are in the digital power fusion peripherals manual.

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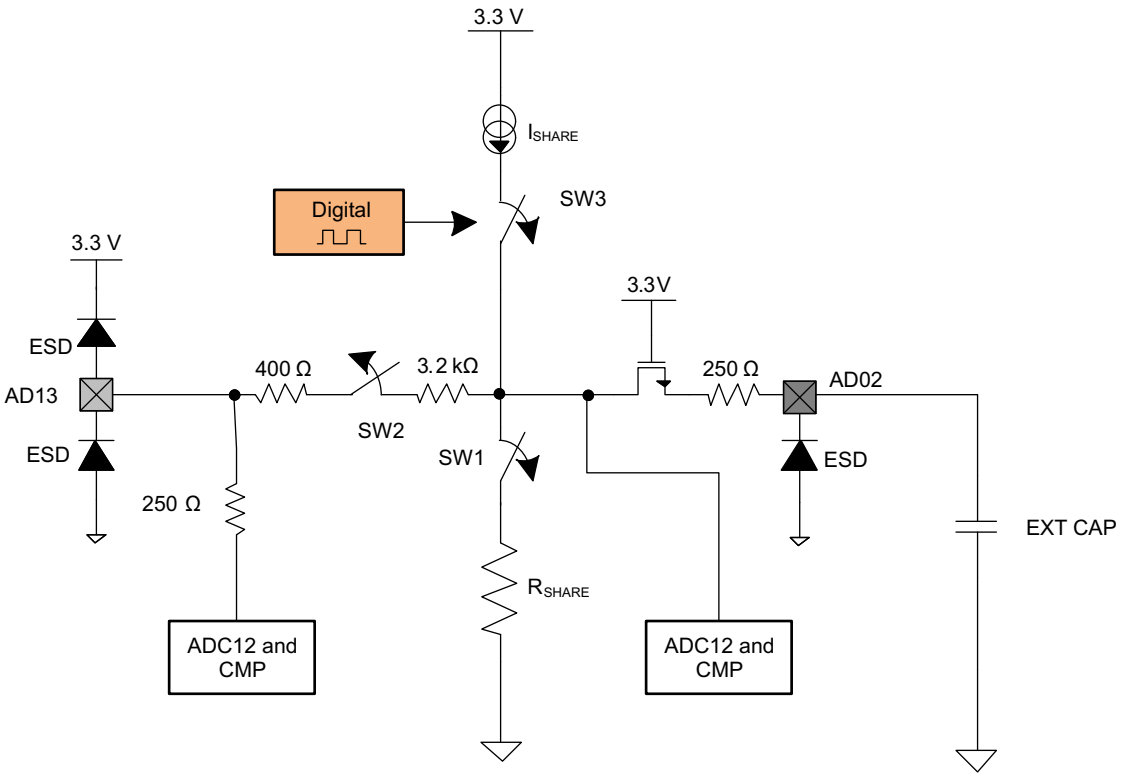


Figure 6-25. Simplified Current Sharing Circuitry

CURRENT SHARING MODE	FOR TEST ONLY, ALWAYS KEEP 00	CS_MODE	EN_SW1	EN_SW2	DPWM
Off or Slave Mode (3-state)	00	00 (default)	0	0	0
PWM Bus	00	01	1	0	ACTIVE
Off or Slave Mode (3-state)	00	10	0	0	0
Analog Bus or Master	00	11	0	1	0

The period and the duty of 8-bit PWM current source and the state of the SW1 and SW2 switches can be controlled through the current sharing control register (CSCTRL).

6.4.16 Temperature Reference

The temperature reference register (TEMPREF) provides the ADC12 count when ADC12 measures the internal temperature sensor (channel 15) during the factory trim and calibration.

This information can be used by different periodic temperature compensation routines implemented in the firmware. But it should not be overwritten by firmware, otherwise this factory written value will be lost until the device is reset.

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6.5 Device Functional Modes

6.5.1 DPWM Modes Of Operation

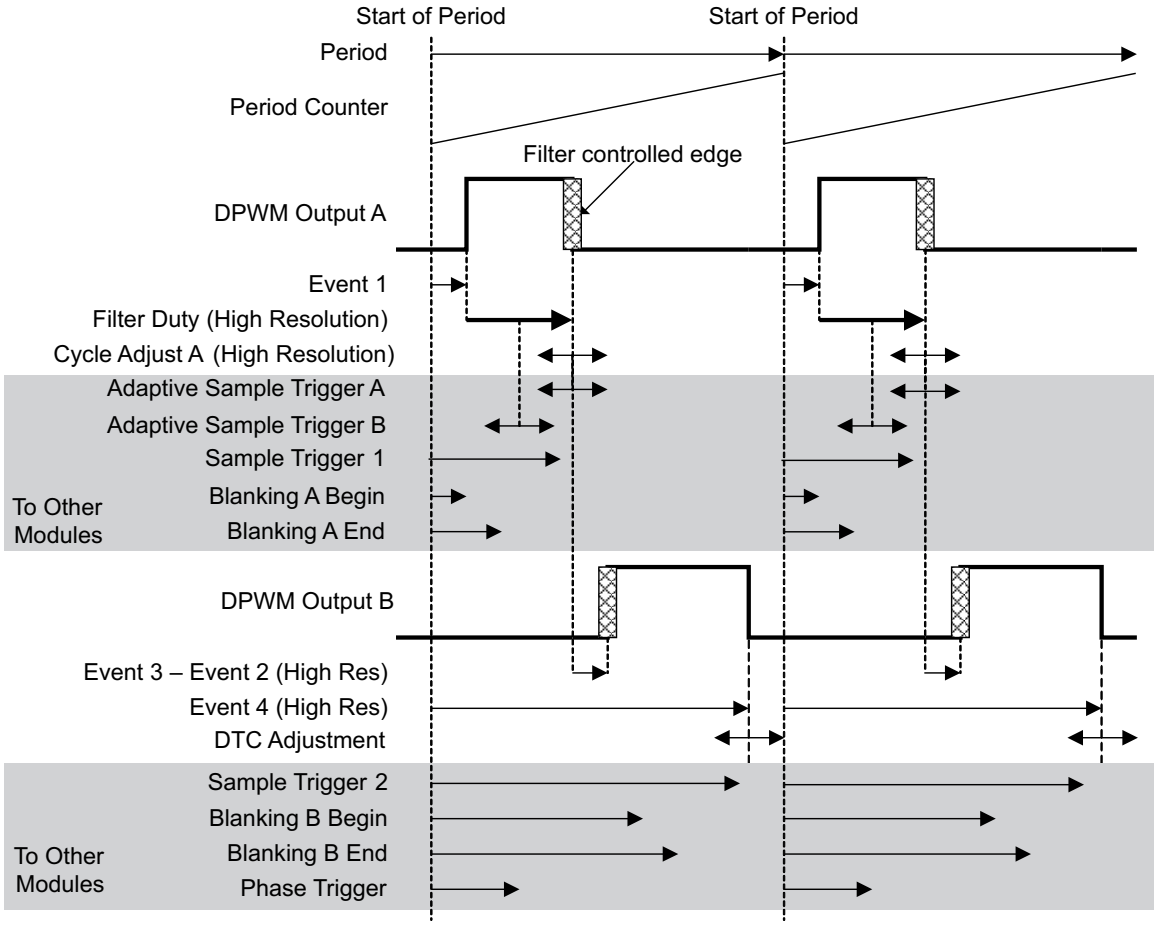
The DPWM is a complex logic system which is highly configurable to support several different power supply topologies. The discussion below will focus primarily on waveforms, timing and register settings, rather than on logic design.

The DPWM is centered on a period counter, which counts up from 0 to PRD, and then is reset and starts over again.

The DPWM logic causes transitions in many digital signals when the period counter hits the target value for that signal.

6.5.1.1 Normal Mode

In Normal mode, the Filter output determines the pulse width on DPWM A. DPWM B fits into the rest of the switching period, with a dead time separating it from the DPWM A on-time. It is useful for buck topologies, among others. Figure 6-26 is a drawing of the Normal Mode waveforms:



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1

DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A

Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or

Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register

DPWM B Rising Edge = Event 1 + Filter Duty + Cycle Adjust A + (Event 3 – Event 2)

DPWM B Falling Edge = Event 4 + DTC Adjustment

Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

Figure 6-26. Normal Mode - Closed Loop

Cycle adjust A can be used to adjust pulse widths on individual phases of a multi-phase system. This can be used for functions like current balancing. The Adaptive Sample Triggers can be used to sample in the middle of the on-time (for an average output), or at the end of the on-time (to minimize phase delay) The Adaptive Sample Register provides an offset from the center of the on-time. This can compensate for external delays, such as MOSFET and gate driver turn on times.

Blanking A-Begin and Blanking A-End can be used to blank out noise from the MOSFET turn on at the beginning of the period (DPWMA rising edge). Blanking B could be used at the turn off time of DPWMB. The other edges are dynamic, so blanking is more difficult.

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Cycle Adjust B has no effect in Normal Mode.

6.5.1.2 Phase Shifting

In most modes, it is possible to synchronize multiple DPWM modules using the phase shift signal. The phase shift signal has two possible sources. It can come from the Phase Trigger Register. This provides a fixed value, which is useful for an application like interleaved PFC.

The phase shift value can also come from the filter output. In this case, the changes in the filter output causes changes in the phase relationship of two DPWM modules. This is useful for phase shifted full bridge topologies.

Figure 6-27 shows the mechanism of phase shift:

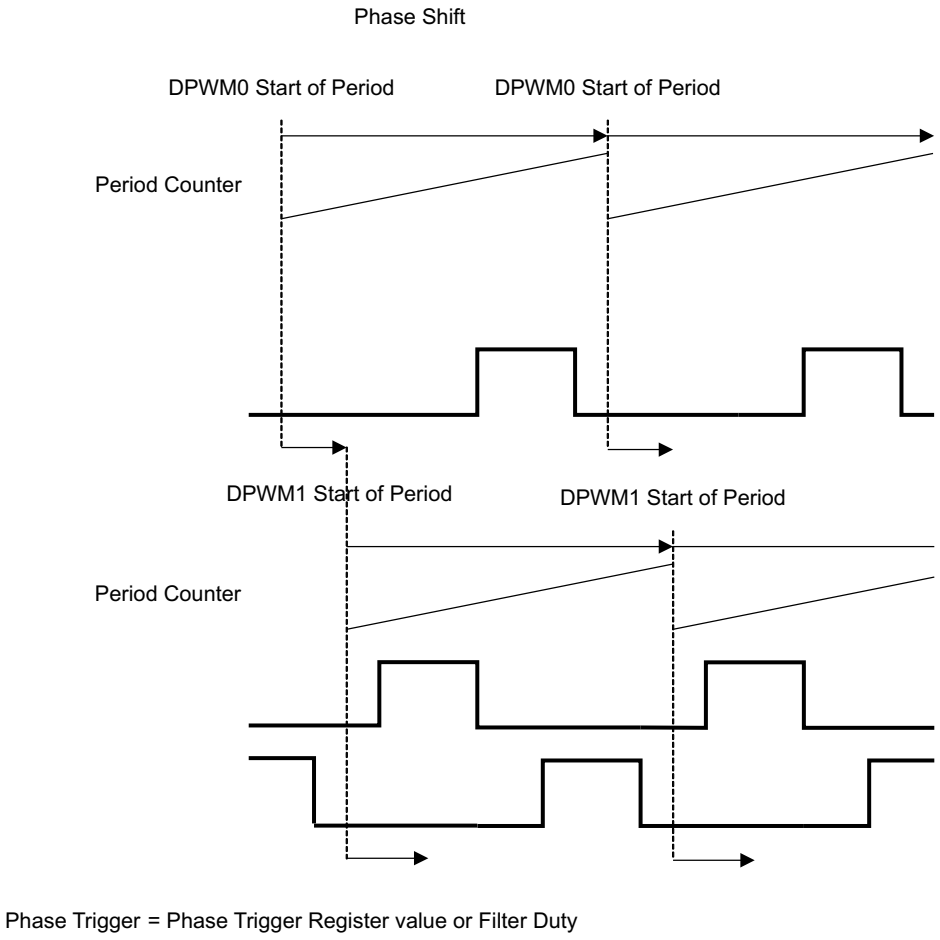
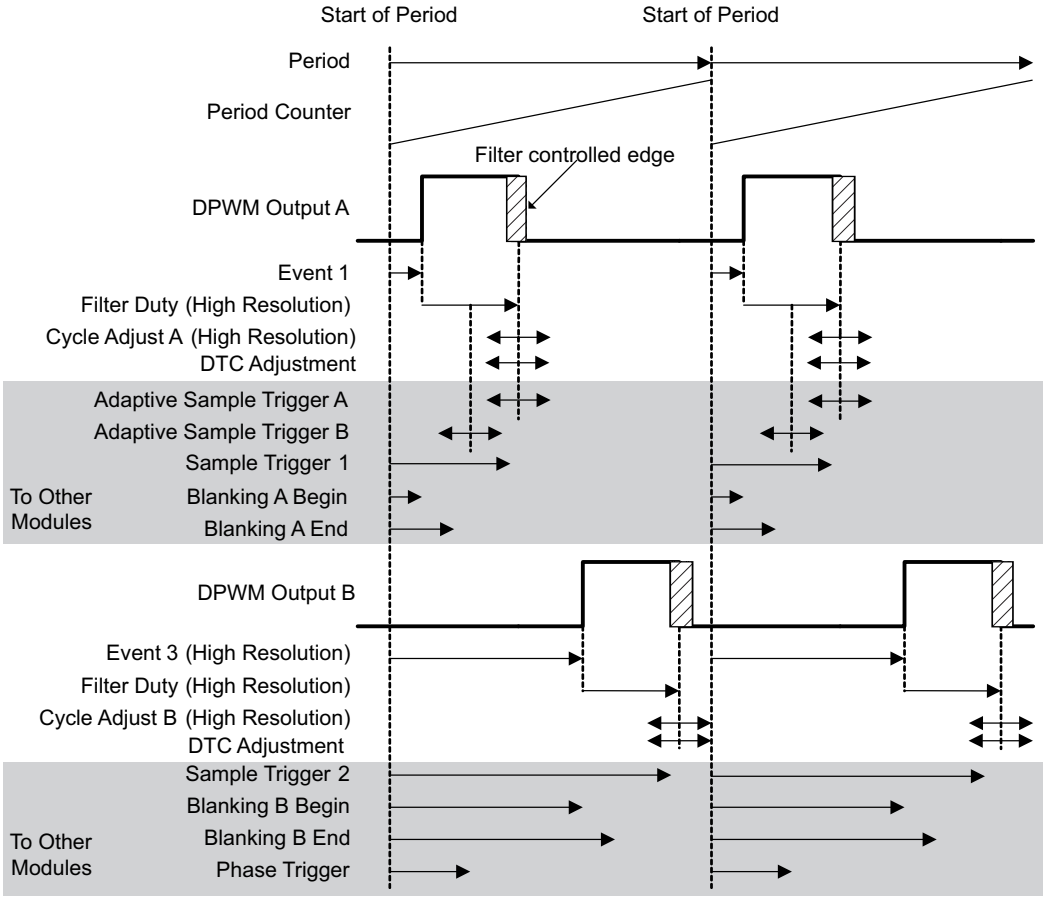


Figure 6-27. Phase Shifting

6.5.1.3 DPWM Multiple Output Mode

Multi mode is used for systems where each phase has only one driver signal. It enables each DPWM peripheral to drive two phases with the same pulse width, but with a time offset between the phases, and with different cycle adjusts for each phase.

The Multi-Mode diagram is shown in Figure 6-28.



Events which change with DPWM mode:

DPWM A Rising Edge = Event 1

DPWM A Falling Edge = Event 1 + Filter Duty + Cycle Adjust A + DTC Adjustment

Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or

Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register

DPWM B Rising Edge = Event 3

DPWM B Falling Edge = Event 3 + Filter Duty + Cycle Adjust B + DTC Adjustment

Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

Figure 6-28. DPWM Multi-Mode Closed Loop

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Event 2 and Event 4 are not relevant in Multi mode.

DPWMB can cross over the period boundary safely, and still have the proper pulse width, so full 100% pulse width operation is possible. DPWMA cannot cross over the period boundary.

Since the rising edge on DPWM B is also fixed, Blanking B-Begin and Blanking B-End can be used for blanking this rising edge.

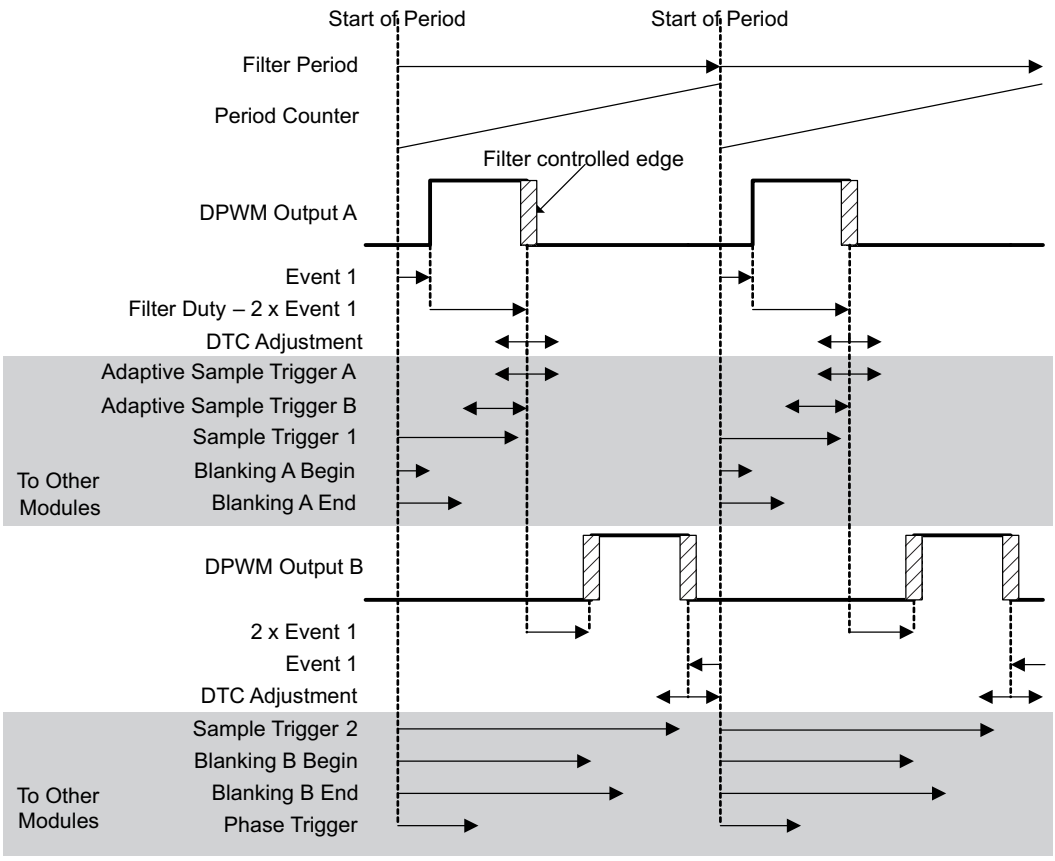
And, of course, Cycle Adjust B is usable on DPWM B.

6.5.1.4 DPWM Resonant Mode

This mode provides a symmetrical waveform where DPWMA and DPWMB have the same pulse width. As the switching frequency changes, the dead times between the pulses remain the same.

The equations for this mode are designed for a smooth transition from PWM mode to resonant mode, as described in Section 6.4.4.2. A diagram of this mode is shown in Figure 6-29:

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Events which change with DPWM mode:

DPWM A Rising Edge = Event 1

DPWM A Falling Edge = Filter Duty – Event 1 + DTC Adjustment

Adaptive Sample Trigger A = Event 1 + Filter Duty + Adaptive Sample Register or

Adaptive Sample Trigger B = Event 1 + Filter Duty/2 + Adaptive Sample Register

DPWM B Rising Edge = Filter Duty + Event 1

DPWM B Falling Edge = Filter Period – Event 1 + DTC Adjustment

Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

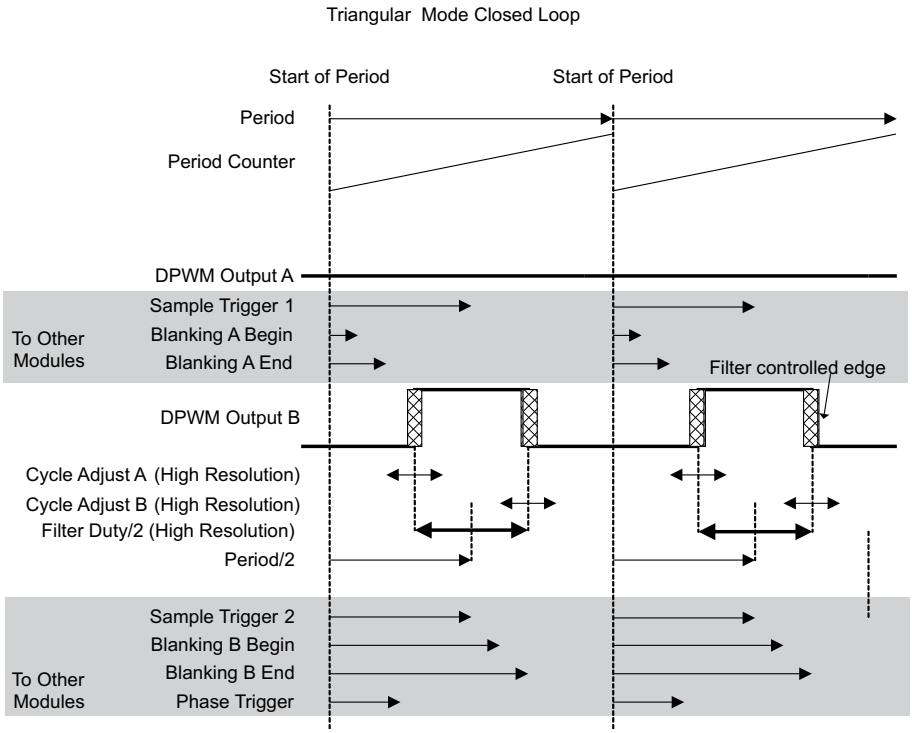
Figure 6-29. DPWM Resonant Symmetrical Mode

The Filter has two outputs, Filter Duty and Filter Period. In this case, the Filter is configured so that the Filter Period is twice the Filter Duty. So if there were no dead times, each DPWM pin would be on for half of the period. For dead time handling, the average of the two dead times is subtracted from the Filter Duty for both DPWM pins. Therefore, both pins will have the same on-time, and the dead times will be fixed regardless of the period. The only edge which is fixed relative to the start of the period is the rising edge of DPWM A. This is the only edge for which the blanking signals can be used easily.

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6.5.2 Triangular Mode

Triangular mode provides a stable phase shift in interleaved PFC and similar topologies. In this case, the PWM pulse is centered in the middle of the period, rather than starting at one end or the other. In Triangular Mode, only DPWM-B is available. A diagram for Triangular Mode is shown in Figure 6-30:



Events which change with DPWM mode:

DPWM A Rising Edge = None

DPWM A Falling Edge = None

Adaptive Sample Trigger None

DPWM B Rising Edge = Period/2 – Filter Duty/2 + Cycle Adjust A

DPWM B Falling Edge = Period/2 + Filter Duty/2 + Cycle Adjust B

Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

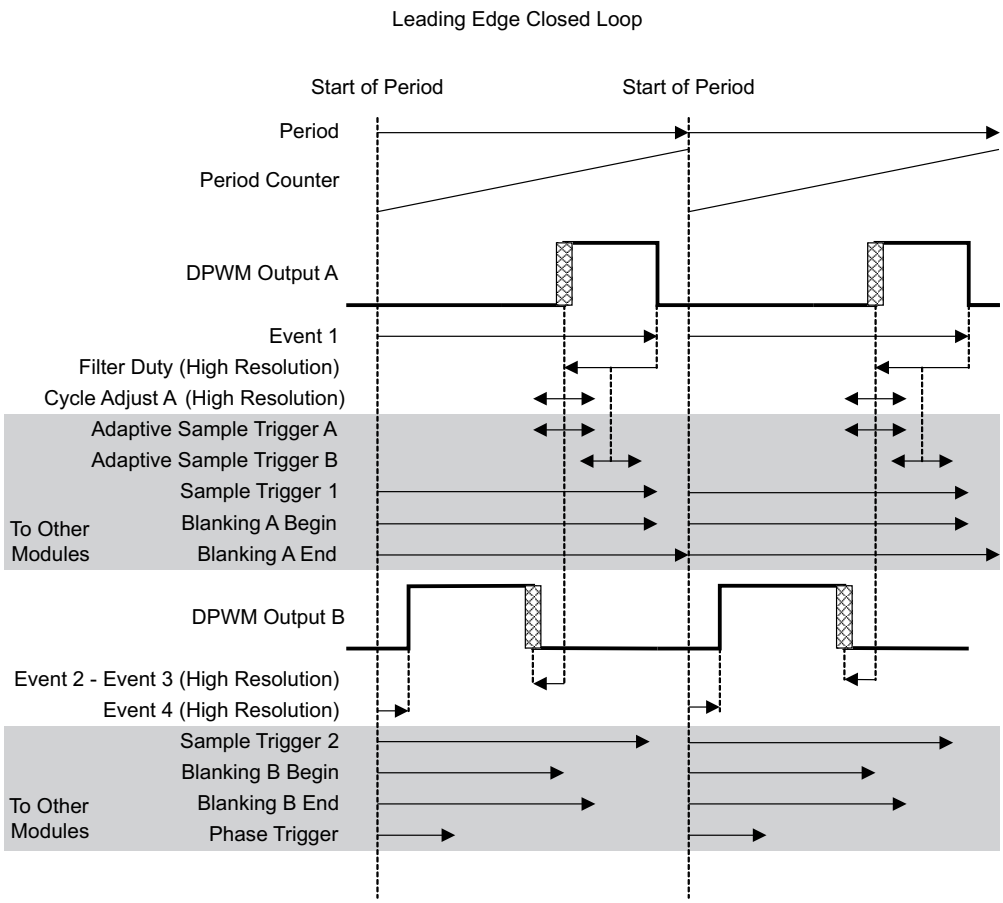
Figure 6-30. Triangular Mode

All edges are dynamic in triangular mode, so fixed blanking is not that useful. The adaptive sample trigger is not needed. It is very easy to put a fixed sample trigger exactly in the center of the FET on-time, because the center of the on-time does not move in this mode.

6.5.3 Leading Edge Mode

Leading edge mode is similar to Normal mode, reversed in time. The DPWM A falling edge is fixed, and the rising edge moves to the left, or backwards in time, as the filter output increases. The DPWM B falling edge stays ahead of the DPWMA rising edge by a fixed dead time. A diagram of the Leading Edge Mode is shown in Figure 6-31:

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Events which change with DPWM mode:

DPWM A Falling Edge = Event 1

DPWM A Rising Edge = Event 1 – Filter Duty + Cycle Adjust A

Adaptive Sample Trigger A = Event 1 – Filter Duty + Adaptive Sample Register or

Adaptive Sample Trigger B = Event 1 – Filter Duty/2 + Adaptive Sample Register

DPWM B Rising Edge = Event 4

DPWM B Falling Edge = Event 1 – Filter Duty + Cycle Adjust A – (Event 2 – Event 3)

Phase Trigger = Phase Trigger Register value or Filter Duty

Events always set by their registers, regardless of mode:

Sample Trigger 1, Sample Trigger 2, Blanking A Begin, Blanking A End, Blanking B Begin, Blanking B End

Figure 6-31. Leading Edge Mode

As in the Normal mode, the two edges in the middle of the period are dynamic, so the fixed blanking intervals are mainly useful for the edges at the beginning and end of the period.

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6.6 Memory

6.6.1 Register Maps

6.6.1.1 CPU Memory Map and Interrupts

When the device comes out of power-on-reset, the data memories are mapped to the processor as follows:

6.6.1.1.1 Memory Map (After Reset Operation)

Address	Size (Bytes)	Module
0x0000_0000 – 0x0003_FFFF In 32 repeated blocks of 8 k each	32 X 8 k	Boot ROM
0x0004_0000 – 0x0004_7FFF	32 k	Program Flash 1
0x0004_8000 – 0x0004_FFFF	32 k	Program Flash 2
0x0006_8800 – 0x0006_8FFF	2 k	Data Flash
0x0006_9000 – 0x0006_9FFF	4 k	Data RAM

6.6.1.1.2 Memory Map (Normal Operation)

Just before the boot ROM program gives control to flash program, the ROM configures the memory as follows:

Address	Size (Bytes)	Module
0x0000_0000 – 0x0000_7FFF	32 k	Program Flash 1 (or 2)
0x0000_8000 – 0x0000_FFFF	32 k	Program Flash 2 (or 1)
0x0002_0000 – 0x0002_1FFF	8 k	Boot ROM
0x0006_8800 – 0x0006_8FFF	2 k	Data Flash
0x0006_9000 – 0x0006_9FFF	4 k	Data RAM

6.6.1.1.3 Memory Map (System and Peripherals Blocks)

Address	Size	Module
0x0012_0000 - 0x0012_00FF	256	Loop Mux
0x0013_0000 - 0x0013_00FF	256	Fault Mux
0x0014_0000 - 0x0014_00FF	256	ADC
0x0015_0000 - 0x0015_00FF	256	DPWM 3
0x0016_0000 - 0x0016_00FF	256	Filter 2
0x0017_0000 - 0x0017_00FF	256	DPWM 2
0x0018_0000 - 0x0018_00FF	256	Front End/Ramp Interface 2
0x0019_0000 - 0x0019_00FF	256	Filter 1
0x001A_0000 - 0x001A_00FF	256	DPWM 1
0x001B_0000 – 0x001B_00FF	256	Front End/Ramp Interface 1
0x001C_0000 - 0x001C_00FF	256	Filter 0
0x001D_0000 - 0x001D_00FF	256	DPWM 0
0x001E_0000 - 0x001E_00FF	256	Front End/Ramp Interface 0
0xFFF7_EC00 - 0xFFF7_ECFF	256	UART 0
0xFFF7_ED00 - 0xFFF7_EDFF	256	UART 1
0xFFF7_F000 - 0xFFF7_F0FF	256	Miscellaneous Analog Control
0xFFF7_F600 - 0xFFF7_F6FF	256	PMBus Interface
0xFFF7_FA00 - 0xFFF7_FAFF	256	GIO
0xFFF7_FD00 - 0xFFF7_FDFF	256	Timer
0xFFFF_FD00 - 0xFFFF_FDFF	256	MMC
0xFFFF_FE00 - 0xFFFF_FEFF	256	DEC

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Address	Size	Module
0xFFFF_FF20 - 0xFFFF_FF37	23	CIM
0xFFFF_FF40 - 0xFFFF_FF50	16	PSA
0xFFFF_FFD0 - 0xFFFF_FFEC	28	SYS

The registers and bit definitions inside the System and Peripheral blocks are detailed in the programmer's guide for each peripheral.

6.6.1.2 Boot ROM

The UCD3138064A incorporates a 8 kB boot ROM. This boot ROM includes support for:

- Program download through the PMBus
- Device initialization
- Examining and modifying registers and memory
- Verifying and executing program flash automatically
- Jumping to a customer defined boot program
- Checksum evaluation to facilitate program execution from either Program Flash 1 or Program Flash 2

The Boot ROM is entered automatically on device reset. It initializes the device and then performs checksums on the program flash. If the first 2 kB of either program FLASH has a valid checksum, the program branches to location 0 in the appropriate Program FLASH module. This permits the use of a custom boot program. If the first checksum fails, it performs some additional checksum calculations to determine where the valid program is located. This permits full automated program memory checking, when there is no need for a custom boot program. The complete decision tree is located in Figure 6-32. "Branch to Program Flash 1" means Flash 1 is at address 0x0000, and Flash 2 is at address 0x8000. "Branch to Program Flash 2" means Flash 2 is at address 0x0000, and Flash 1 is at address 0x8000.

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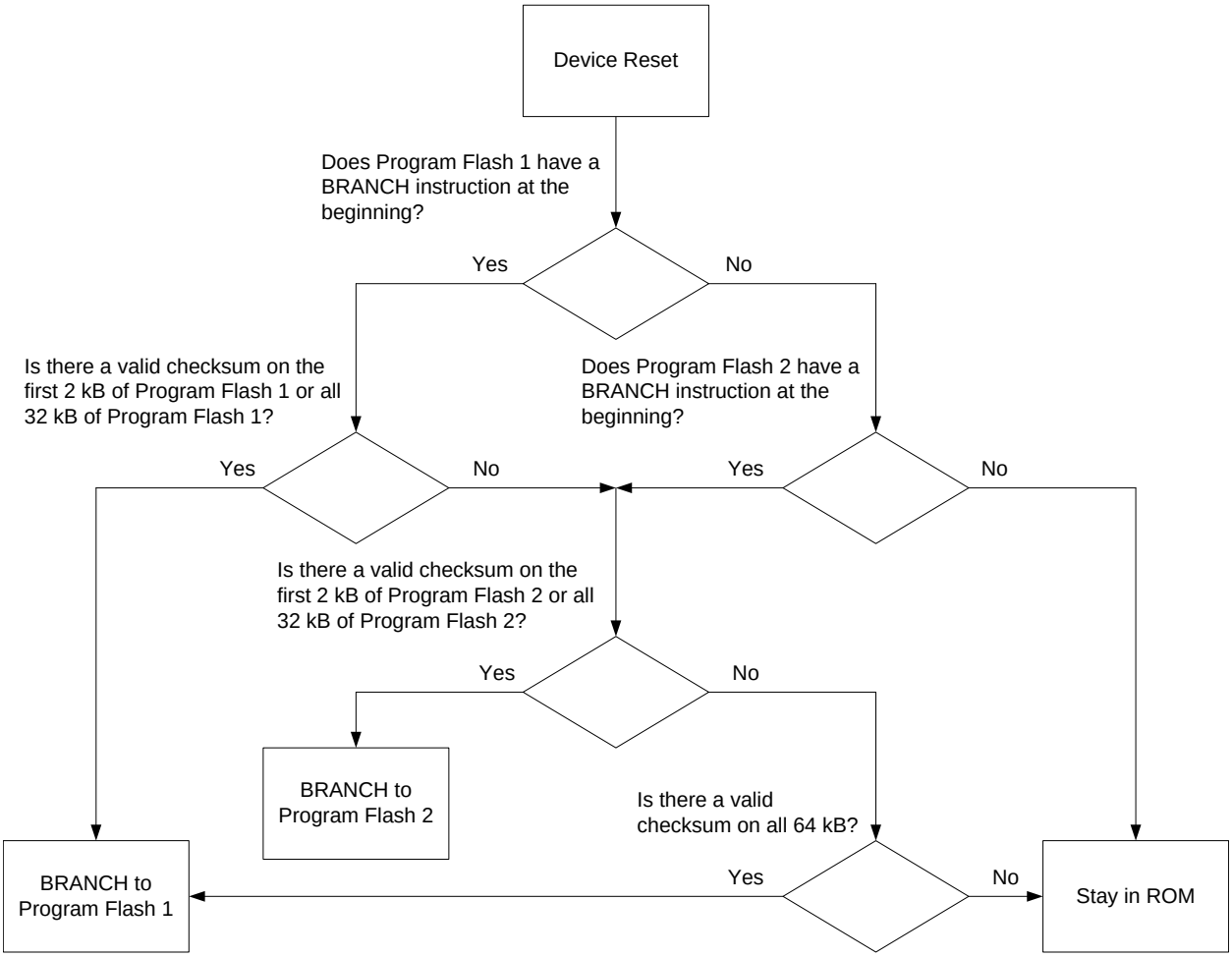


Figure 6-32. Check Sum Evaluation Flowchart

If neither checksum is valid, the Boot ROM stays in control, and accepts commands via the PMBus interface. These functions can be used to read and write to all memory locations in the UCD3138064A. Typically they are used to download a program to Program Flash, and to command its execution.

6.6.1.3 Customer Boot Program

As described above, it is possible to generate a user boot program using 2 kB or more of the Program Flash. This can support things which the Boot ROM does not support, including:

- Program download via UART – useful especially for applications where the UCD3138064A is isolated from the host (e.g., PFC)
- Encrypted download – useful for code security in field updates.
- PMBus download at different addresses

6.6.1.4 Flash Management

The UCD3138064A offers a variety of features providing for easy prototyping and easy flash programming. At the same time, high levels of security are possible for production code, even with field updates. Standard firmware will be provided for storing multiple copies of system parameters in data flash. This minimizes the risk of losing information if data-flash programming is interrupted.

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6.6.1.5 Synchronous Rectifier MOSFET Ramp and IDE Calculation

The UCD3138064A has built in logic for optimizing the performance of the synchronous rectifier MOSFETs. This comes in two forms:

- Synchronous Rectifier MOSFET ramp
- Ideal Diode Emulation (IDE) calculation

When starting up a power supply, It is not uncommon for there to already be a voltage present on the output – this is called pre-bias. It can be very difficult to calculate the ideal synchronous rectifier MOSFET on-time for this case. If it is not calculated correctly, it may pull down the pre-bias voltage, causing the power supply to sink current. To avoid this, the synchronous rectifier MOSFETs are not turned on until after the power supply has ramped up to the nominal output voltage. The synchronous rectifier MOSFETs are then turned on slowly in order to avoid an output voltage glitch. The synchronous rectifier MOSFET ramp logic can be used to turn them on at a rate well below the bandwidth of the filter.

In discontinuous mode, the ideal on-time for the synchronous rectifier MOSFETs is a function of V_{in}, V_{out}, and the primary side duty cycle (D). The IDE logic in the UCD3138064A takes V_{in} and V_{out} data from the firmware and combines it with D data from the filter hardware. It uses this information to calculate the ideal on-time for the synchronous rectifier MOSFETs.

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7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The UCD3138x has an extensive set of fully-programmable, high-performance peripherals that make it suitable for a wide range of power supply applications. In order to make the part easier to use, TI has prepared an extensive set of materials to demonstrate the features of the device for several key applications. In each case the following items are available:

1. Full featured EVM hardware that demonstrates classic power supply functionality.
2. An EVM user guide that contains schematics, bill-of-materials, layout guidance and test data showcasing the performance and features of the device and the hardware.
3. A firmware programmers manual that provides a step-by-step walk through of the code.

Table 7-1. Application Information

APPLICATION	EVM DESCRIPTION
Phase shifted full bridge	This EVM demonstrates a PSFB DC-DC power converter with digital control using the UCD3138x device. Control is implemented by using PCMC with slope compensation. This simplifies the hardware design by eliminating the need for a series blocking capacitors and providing the inherent input voltage feed-forward that comes from PCMC. The controller is located on a daughter card and requires firmware in order to operate. This firmware, along with the entire source code, is made available through TI. A free, custom function GUI is available to help the user experiment with the different hardware and software enabled features. The EVM accepts a DC input from 350 VDC to 400 VDC, and outputs a nominal 12 VDC with full load output power of 360 W, or full output current of 30 A.
LLC resonant converter	This EVM demonstrates an LLC resonant half-bridge DC-DC power converter with digital control using the UCD3138x device. The controller is located on a daughter card and requires firmware in order to operate. This firmware, along with the entire source code, is made available through TI. A free, custom function GUI is available to help the user experiment with the different hardware and software enabled features. The EVM accepts a DC input from 350 VDC to 400 VDC, and outputs a nominal 12 VDC with full load output power of 340 W, or full output current of 29 A.

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7.2 Typical Application

This section summarizes the PSFB EVM DC-DC power converter.

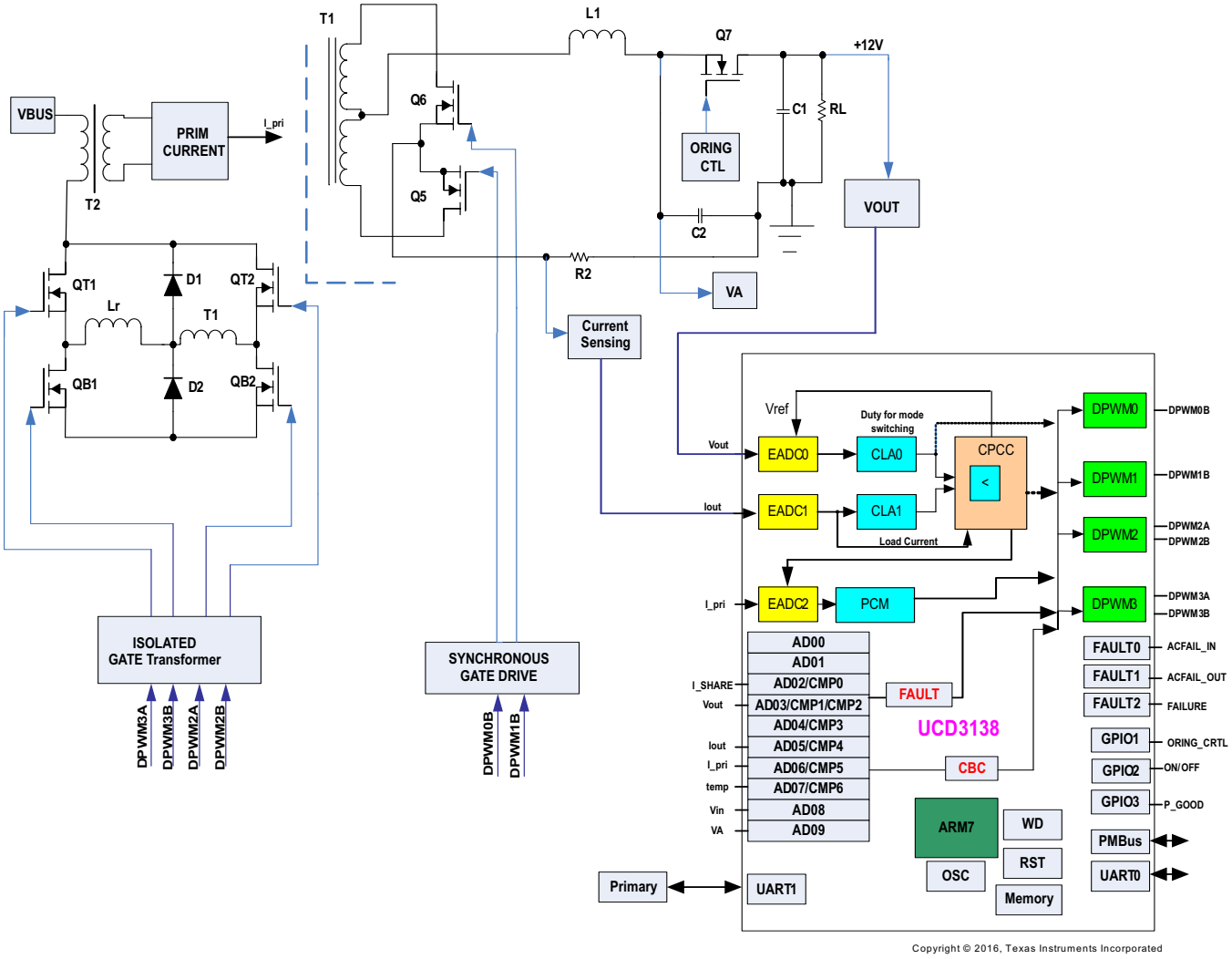


Figure 7-1. Phase-Shifted Full-Bridge

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7.2.1 Design Requirements

Table 7-2. Input Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ALL SPECIFICATIONS at Vin=400V and 25°C AMBIENT UNLESS OTHERWISE NOTED.						
V_{in}	Input voltage range	Normal Operating	350	385	420	V
V_{inmax}	Max input voltage	Continuous			420	V
I_{in}	Input current	Vin=350V, Full Load		1.15		A
I_{stby}	Input no load current	Output current is 0A		30		mA
V_{on}	Under voltage lockout	V_{in} Decreasing (input voltage is detected on secondary side)		340		V
V_{hys}		V_{in} Increasing		360		V

Table 7-3. Output Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ALL SPECIFICATIONS at Vin=400V and 25°C AMBIENT UNLESS OTHERWISE NOTED.						
V_O	Output voltage setpoint	No load on outputs		12		V
Reg_{line}	Line regulation	All outputs; 360 ≤ V_{in} ≤ 420; I_O = I_{Omax}			0.5%	
Reg_{load}	Load regulation	All outputs; 0 ≤ I_O ≤ I_{Omax}; V_{in} = 400 V			1%	
V_n	Ripple and noise(1)	5Hz to 20 MHz		100		mVpp
I_O	Output current		0		30	A
η	Efficiency at phase-shift mode	Vo = 12 V, Io = 15 A		93%		
η	Efficiency at PWM ZVS mode	Vo = 12 V, Io = 15 A		93%		
η	Efficiency at hard switching mode	Vo = 12 V, Io = 15 A		90%		
V_{adj}	Output adjust range		11.4		12.6	V
V_{tr}	Transient response overshoot/undershoot	50% Load Step at 1AμS, min load at 2A		±0.36		V
$t_{settling}$	Transient response settling time			100		μS
t_{start}	Output rise time	10% to 90% of Vout		50		mS
	Overshoot	At Startup			2%	
fs	Switching frequency	Over V_{in} and I_O ranges		150		kHz
I_{share}	Current sharing accuracy	50% - full load		±5%		
φ	Loop phase margin	10% - Full load		45		degree
G	Loop gain margin	10% - Full load		10		dB

(1) Ripple and noise are measured with 10μF Tantalum capacitor and 0.1μF ceramic capacitor across output.

7.2.2 Detailed Design Procedure

7.2.2.1 PCMC (Peak Current Mode Control) PSFB (Phase Shifted Full Bridge) Hardware Configuration Overview

The hardware configuration of the UCD3138x PCMC PSFB converter contains two critical elements that are highlighted in the subsequent sections.

- DPWM initialization - This section will highlight the key register settings and considerations necessary for the UCD3138x to generate the correct MOSFET waveforms for this topology. This maintains the proper phase relationship between the MOSFETs and synchronous rectifiers as well as the proper set up required to function correctly with PCMC.
- PCMC initialization - This section will discuss the register settings and hardware considerations necessary to modulate the DPWM pins with PCMC and internal slope compensation.

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7.2.2.2 DPWM Initialization for PSFB

The UCD3138x DPWM peripheral provides flexibility for a wide range of topologies. The PSFB configuration utilizes the Intra-Mux and Edge Generation Modules of the DPWM. For a diagram showing these modules, see the UCD3138x Digital Power Peripherals Manual.

A schematic of the power stage of the PSFB is shown in Figure 7-2:

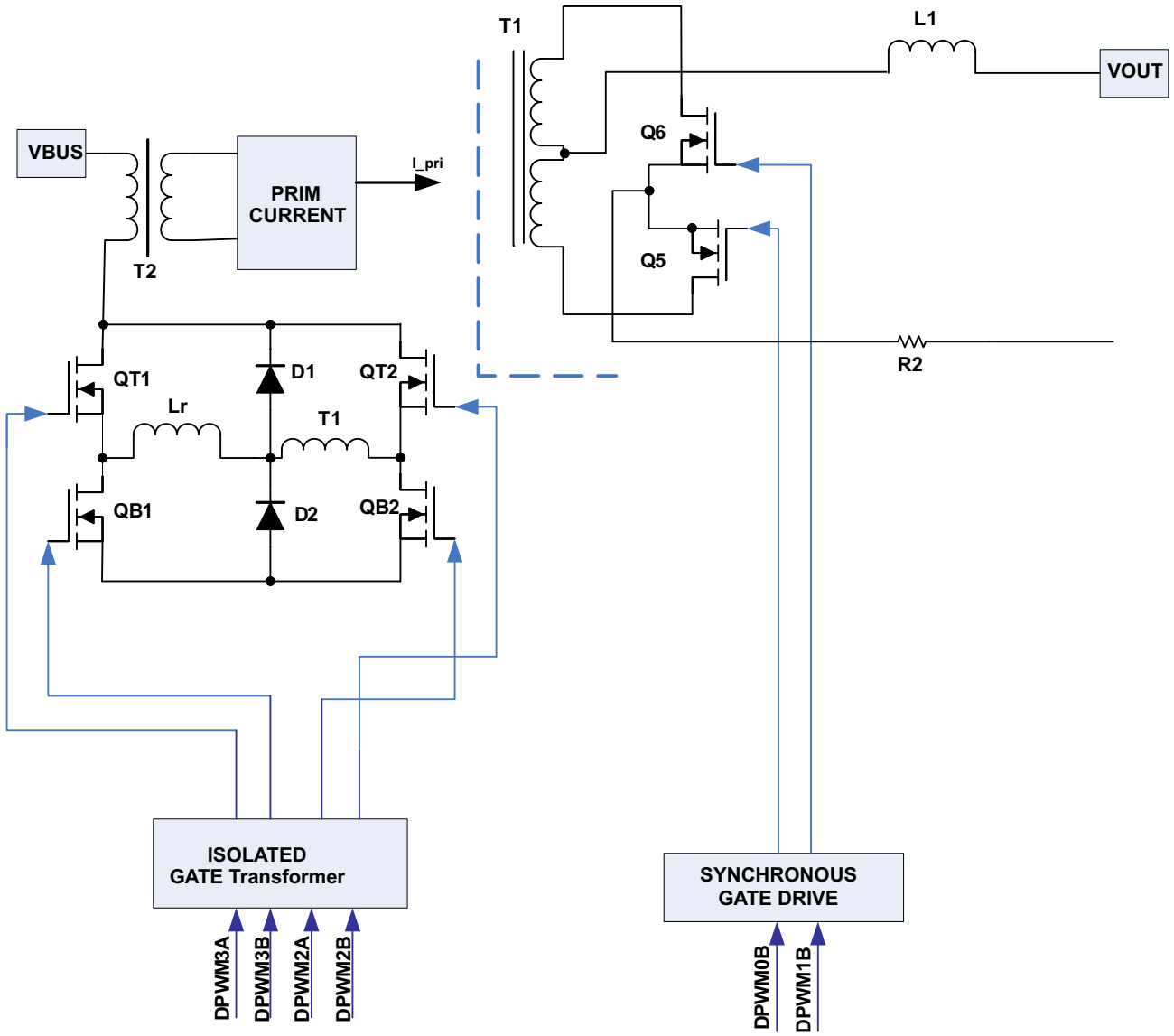


Figure 7-2. Schematic – PSFB Power Stage

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Here is an overview of the key PSFB signals:

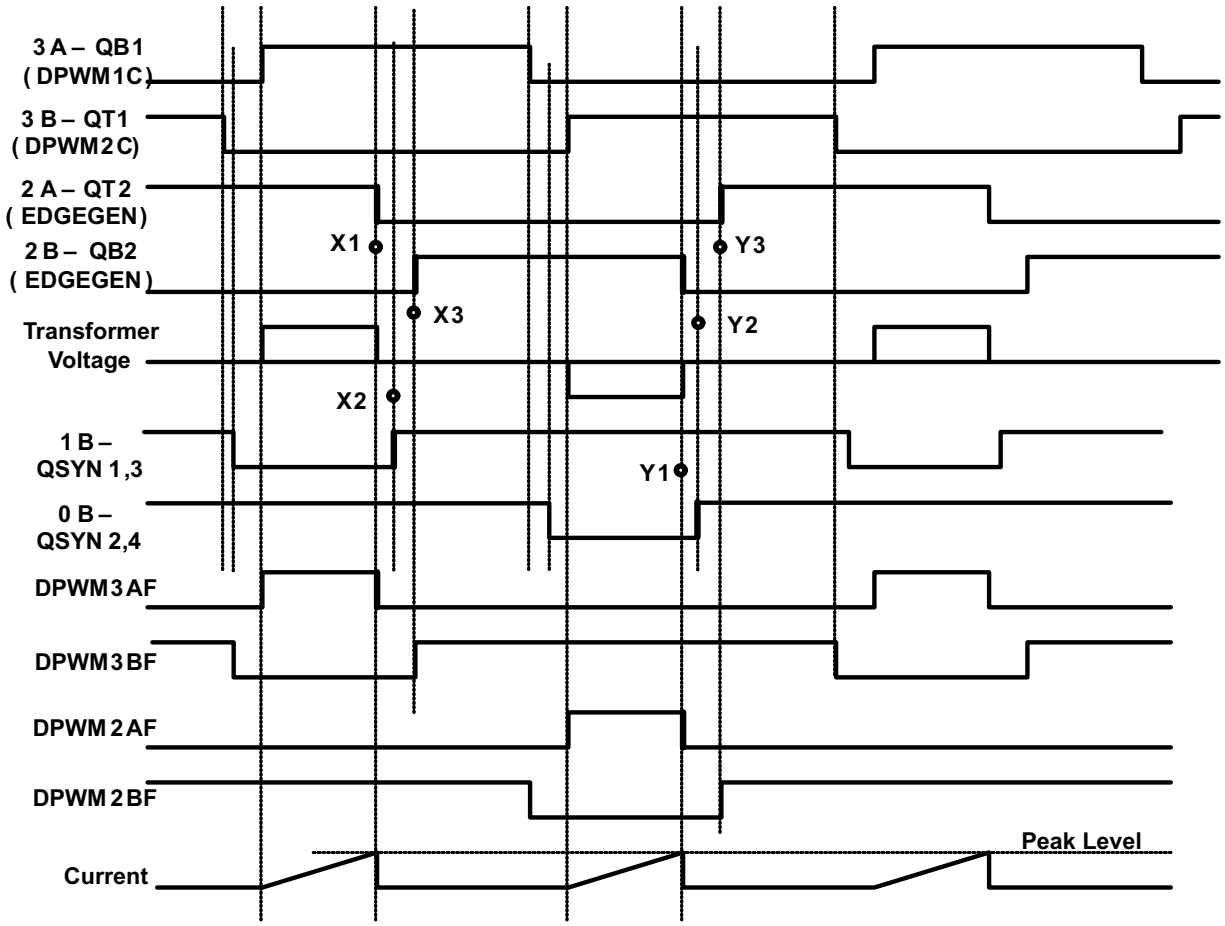


Figure 7-3. Key PSFB Signals

7.2.2.2.1 DPWM Synchronization

DPWM1 is synchronized to DPWM0, DPWM2 is synchronized to DPWM1, and DPWM3 is synchronized to DPWM2, ½ period out of phase using these commands:

```
Dpwm1Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; //configured to slave
Dpwm2Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; // configured to slave
Dpwm3Regs.DPWMCTRL0.bit.MSYNC_SLAVE_EN = 1; // configured to slave

Dpwm0Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
Dpwm1Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;
Dpwm2Regs.DPWMPHASETRIG.all = PWM_SLAVESYNC;

LoopMuxRegs.DPWMMUX.bit.DPWM1_SYNC_SEL    // Slave to dpwm-0
= 0;                                      // Slave to dpwm-1
LoopMuxRegs.DPWMMUX.bit.DPWM2_SYNC_SEL    // Slave to dpwm-2
= 1;
LoopMuxRegs.DPWMMUX.bit.DPWM3_SYNC_SEL
= 2;
```

If the event registers on the DPWMs are the same, the two pairs of signals will be symmetrical. All code examples are taken from the PSFB EVM code, unless otherwise stated.

7.2.2.3 Fixed Signals to Bridge

The two top signals in the above drawing have fixed timing. The DPWM1CF and DPWM2CF signals are used for these pins. DPWMCxF refers to the signal coming out of the fault module of DPWMx, as shown in Figure 7-4.

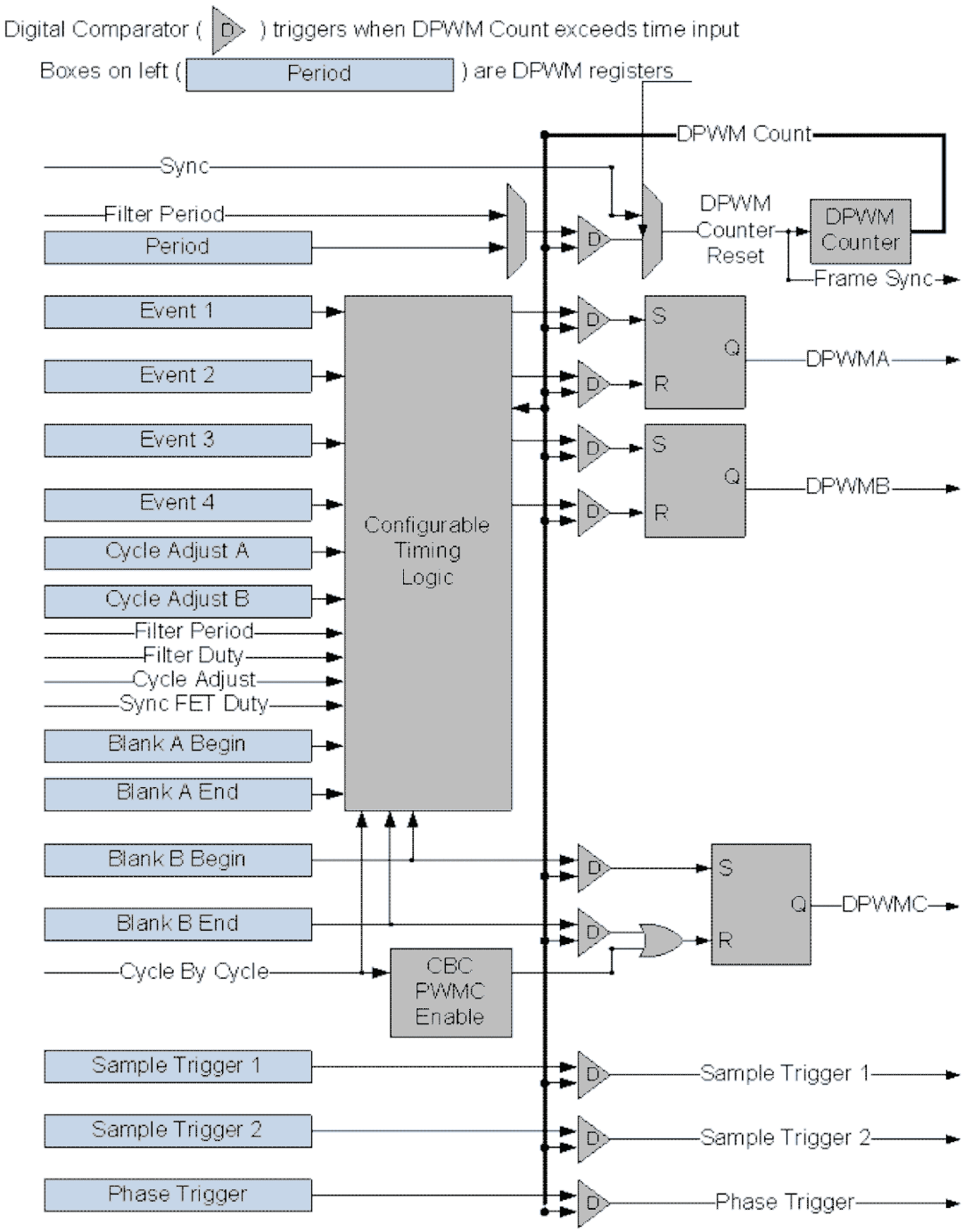


Figure 7-4. Fixed Signals to Bridge

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These signals are actually routed to pins DPWM3A and 3B using the Intra Mux with these statements:

```
Dpwm3Regs.DPWMCTRL0.bit.PWM_A_INTRA_MUX = 7; // Send DPWM1C
Dpwm3Regs.DPWMCTRL0.bit.PWM_B_INTRA_MUX = 8; // Send DPWM2C
```

Since these signals are really being used as events in the timer, the #defines are called EV5 and EV6. Here are the statements which initialize them:

```
// Setup waveform for DPWM-C (re-using blanking B regs)
Dpwm2Regs.DPWMBLKBBEG.all = PWM2_EV5 + (4 *16);
Dpwm2Regs.DPWMBLKBEND.all = PWM2_EV6;
```

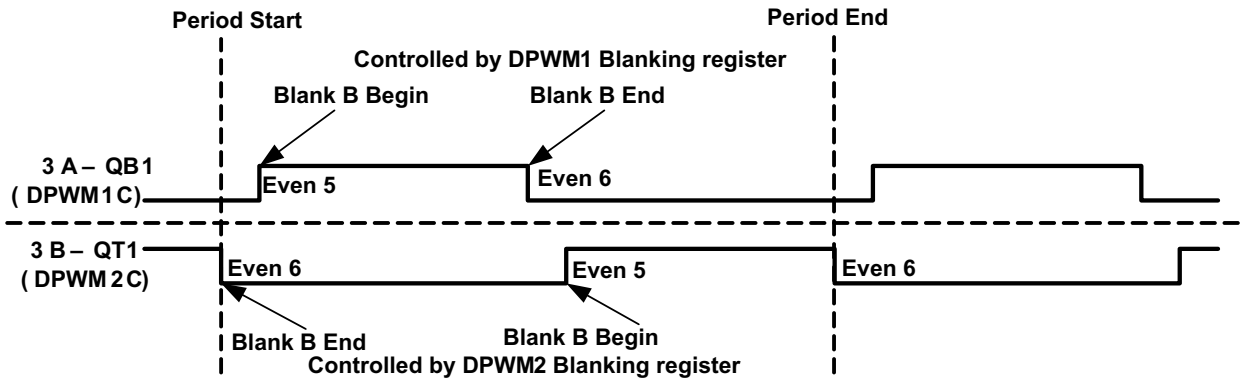


Figure 7-5. Blank B Timing Information

The statements for DPWM1 are the same. Remember that DPWMC reuses the Blank B registers for timing information.

7.2.2.4 Dynamic Signals to Bridge

DPWM0 and 1 are set at normal mode. PCMC triggering signal (fault) chops DPWM0A and 1A cycle by cycle. The corresponding DPWM0B and 1B are used for synchronous rectifier MOSFET control. The same PCMC triggering signal is applied to DPWM2 and DPWM3. Both of these are set to normal mode as well. DPWM2 and 3 are chopped and their edges are used to generate the next two dynamic signals to the bridge. They are generated using the Edge Generator Module in DPWM2. The Edge Generator sources are DPWM2 and DPWM3. The edges used are:

DPWM2A turned on by a rising edge on DPWM2BF
DPWM2A turned off by a falling edge on DPWM3AF
DPWM2B turned on by a rising edge on DPWM3BF
DPWM2B turned off by a falling edge on DPWM2AF

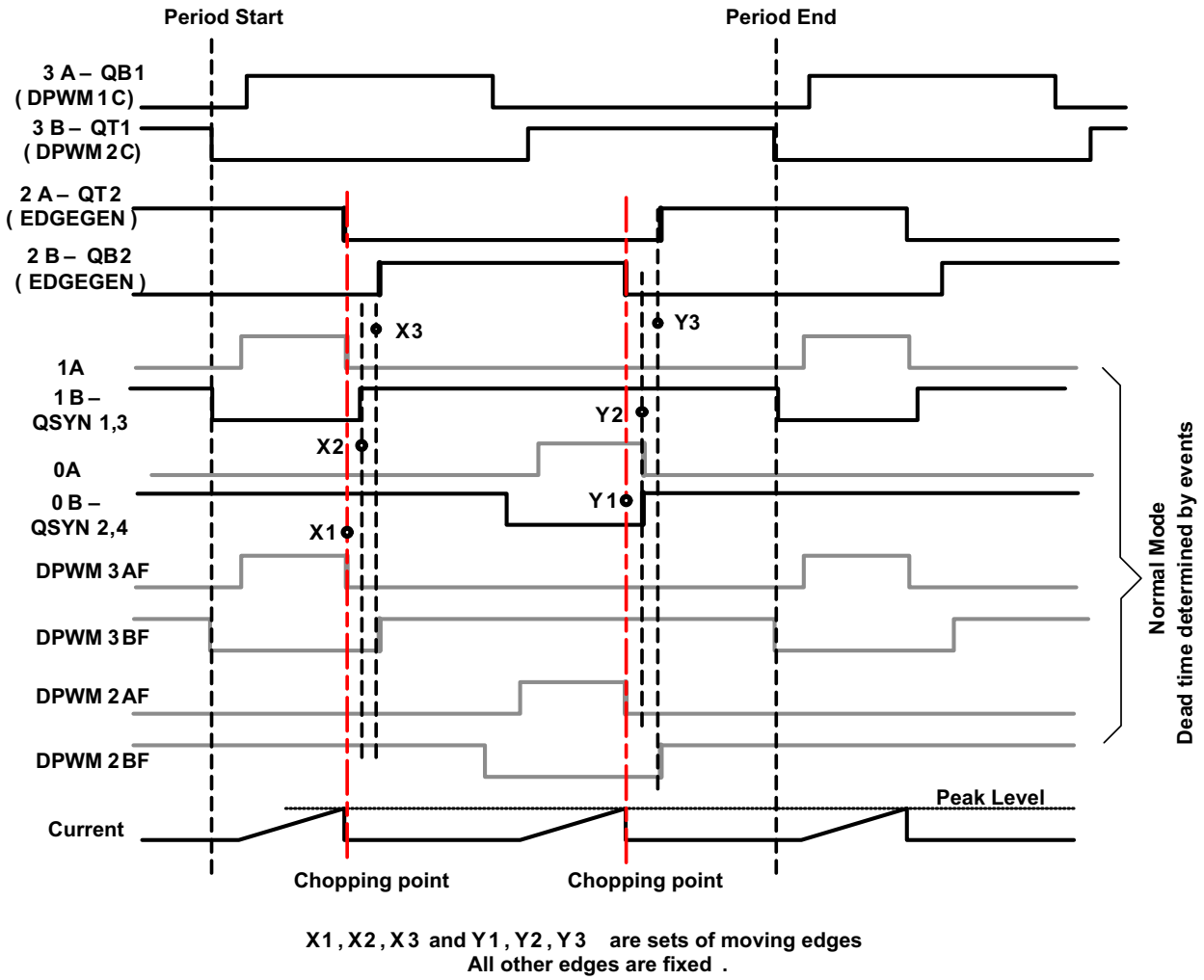


Figure 7-6. Dynamic Signals to Bridge

The Edge Generator is configured with these statements:

```
Dpwm2Regs.DPWMEDGEGEN.bit.A_ON_EDGE = 2;
Dpwm2Regs.DPWMEDGEGEN.bit.A_OFF_EDGE = 5;
Dpwm2Regs.DPWMEDGEGEN.bit.B_ON_EDGE = 6;
Dpwm2Regs.DPWMEDGEGEN.bit.B_OFF_EDGE = 1;

Dpwm2Regs.DPWMCTRL0.bit.PWM_A_INTRA_MUX = 1; // EDGEGEN-A out the A output
Dpwm2Regs.DPWMCTRL0.bit.PWM_B_INTRA_MUX = 1; // EDGEGEN-B out the B output

Dpwm2Regs.DPWMEDGEGEN.bit.EDGE_EN = 1;
```

The EDGE_EN bits are set for all 4 DPWMs. This is done to ensure that all signals have the same timing delay through the DPWM.

The final 6 gate signals are shown in Figure 7-7.

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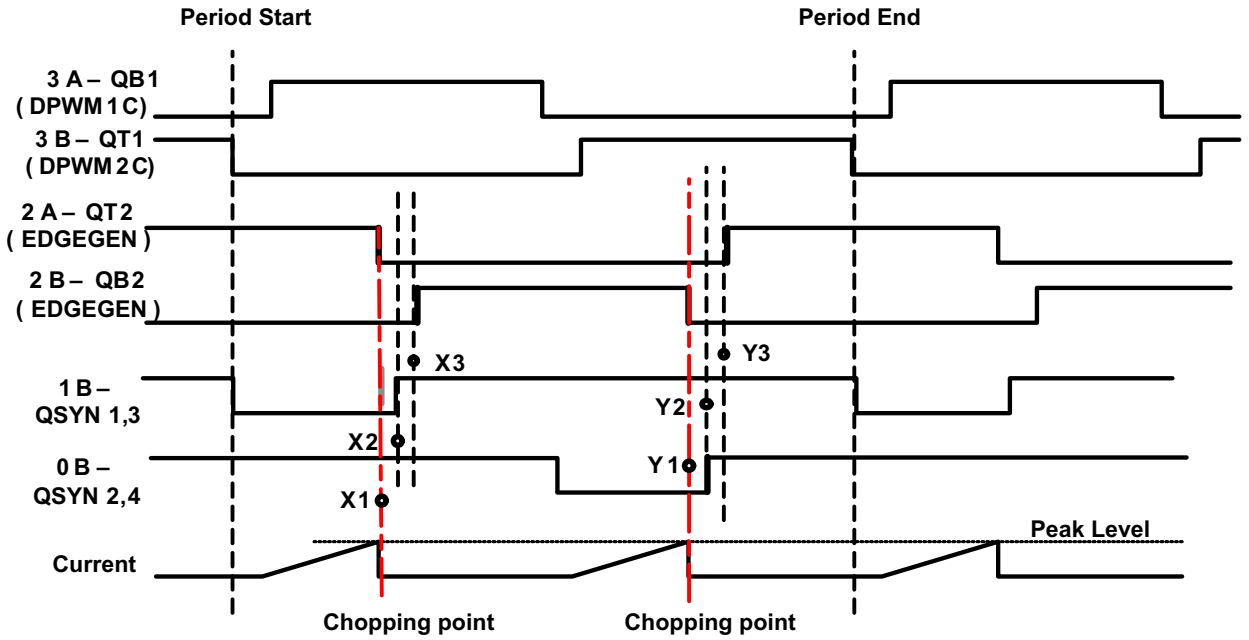


Figure 7-7. Final 6 Gate Signals

Note how the falling edge of DPWM2AF aligns with the X1 edge, and how the rising edge of DPWM2BF aligns with the X3 edge. The falling edges on DPWM2AF and DPWM3AF are caused by the peak detection logic. This is fed through the Cycle By Cycle logic. The Cycle By Cycle logic also has a special feature to control the rising edges of DPWM2BF (X1 and X3) and DPWM3BF (Y1 and Y3). It uses the value of Event3 – Event2 to control the time between the edges. The same feature is used with DPWM0 and DPWM1 to control the X2 and Y2 signals. Using the other 2 DPWMs permits these signals to have a different dead time.

The same setup can be used for voltage mode control. In this case, the Filter output sets the timing of the falling edge on DPWMxAF.

All DPWMs are configured in Normal mode, with CBC enabled. If external slope compensation is used, DPWM1A and DPWM1B are used to reset the external compensator at the beginning of each half cycle. If no PCMC event occurs, the values of Events 2 and 3 determine the locations of the edges, just as in open loop mode.

7.2.2.5 System Initialization for PCM

PCM (Peak Current Mode) is a specialized configuration for the UCD3138x which involves several peripherals. This section describes how it works across the peripherals.

7.2.2.5.1 Use of Front Ends and Filters in PSFB

All three front ends are used in PSFB. The same signals are used in the same places for both PCMC and voltage mode. The same hardware can be used for both control modes, with the mode determined by which firmware is loaded into the device. FE0 and FE1 are used with their associated filters, but Filter 2 is not used at all.

FE0 – Vout – voltage loop
FE1 – Iout – current loop
FE2 – Ipri – PCM

In PCMC mode, FE2 is used for PCMC, and the voltage loop is normally used to provide the start point for the compensation ramp. If the CPCC firmware detects a need for constant current mode, it switches to the current loop for the start point.

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7.2.2.5.2 Peak Current Detection

Peak current detection involves all the major modules of the DPPs, the Front End, Filter, Loop Mux, Fault Mux and the DPWMs. A drawing of the major elements is shown in Figure 7-8.

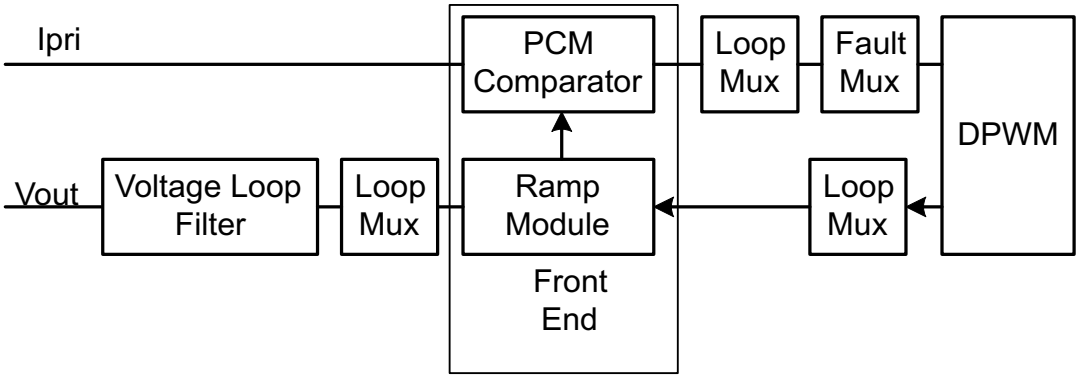


Figure 7-8. Peak Current Detection Function

All signals without arrows flow from left to right. The voltage loop is used to select a peak current level. This level is fed to the Ramp module to generate a compensation ramp. The compensation ramp is compared to the primary current by the PCMC comparator in the Front End. When the ramp value is greater than the primary current, the APCMC signal is sent to the DPWM, causing the events described in the previous sections.

The DPWM frame start and output pin signals can be used to trigger the Ramp Module. In this case, unlike in the case of other ramp module functions, each DPWM frame triggers the start of the ramp. The ramp steps every 32 ns.

The Filter is configured normally, there is no real difference for PCMC. The PCM_FILTER_SEL bits in the LoopMux.PCMCTRL register are used to select which filter is connected to the ramp module:

```
LoopMuxRegs.PCMCTRL.bit.PCM_FILTER_SEL =0; //select filter0
```

With Firmware Constant Power/Constant current, Filter 1 and Front End 1 are used as a current control loop, with the EADCDAC set to high current. If the voltage loop value becomes higher than the current loop value, then Filter 1 is used to control the PCM ramp start value:

```
LoopMuxRegs.PCMCTRL.bit.PCM_FILTER_SEL =1;
        //select filter1 for slope compensation source
```

In the ramp module, there are 2 bitfields in the RAMPCTRL register which must be configured. The PCM_START_SEL must be set to a 1 to enable the Filter to be used as a ramp start source. The RAMP_EN bit must be set, of course.

The DAC_STEP register sets the slope of the compensation ramp. The DAC value is in volts, of course, so it is necessary to calculate the slope after the current to voltage conversion. Here is the formula for converting from millivolts per microsecond to DACSTEP.

m = compensation slope in millivolts per microsecond

$ACSTEP = 335.5 \times M$

In C, this can be written:

```
#define COMPENSATION_SLOPE 150 //compensation slope in millivolts per microsecond
#define DACSTEP_COMP_VALUE ((int) (COMPENSATION_SLOPE*335.5) )
        //value in DACSTEP for desired compensation slope

        FeCtrl0Regs.DACSTEP.all = DACSTEP_COMP_VALUE;
```


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It may also be necessary to set a ramp ending value in the RAMPDACEND register.

In addition, it is necessary to set the D2S_COMP_EN bit in the EADCCTRL register. This is for enabling the differential to single ended comparator function. The front end diagram leaves it out for simplicity, but the connection between the DAC and the EADC amplifier is actually differential. The PCMC comparator, however, is single ended. So a conversion is necessary as shown in Figure 7-9.

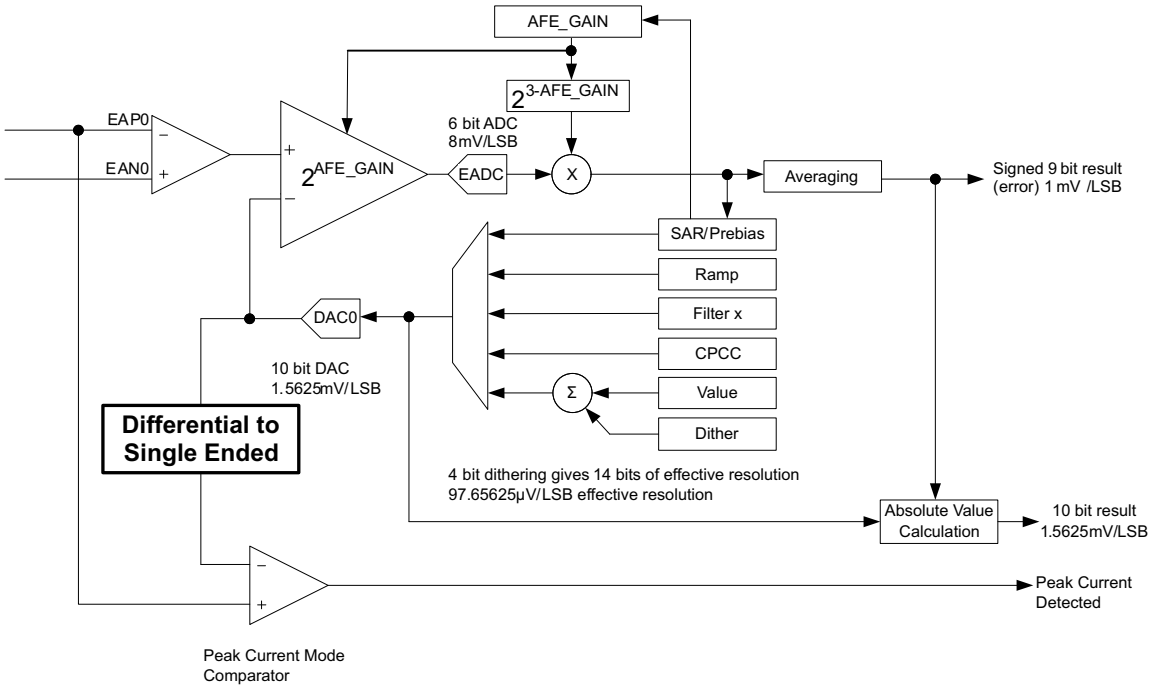


Figure 7-9. Differential to Single-Ended Comparator Function

The EADC_MODE bit in EADCCTRL should be set to a 5 for peak current mode.

The peak current detection signal next goes to the Loop Mux. The Fault Mux has only 1 APCM input, but there are 3 front ends. So the PCM_FE_SEL bits in APCMCTRL must be used to select which front end is used:

LoopMuxRegs.APCMCTRL.bit.PCM_FE_SEL = 2; // use FE2 for PCM */

The PCM_EN bit must also be set.

LoopMuxRegs.APCMCTRL.bit.PCM_EN = 1; // Enable PCM

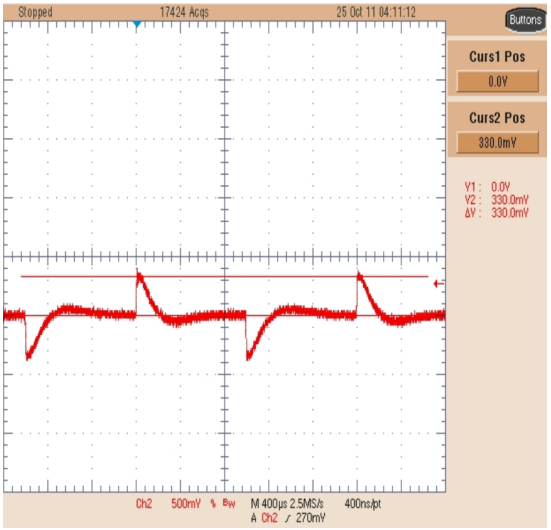
Next the Fault Mux is used to enable the APCM bit to the CLIM/CBC signal to the DPWM. There are 4 DPWMxCLIM registers, one for each DPWM. The ANALOG_PCM_EN bit must be set in each one to connect the PCM detection signal to the CLIM/CBC signal on each DPWM. For the latest configuration information on all of these bits, consult the appropriate EVM firmware. To avoid errors, it is best to configure your hardware design using the same DPWMs, filters, and front ends for the same functions as the EVM.

DPWM timing is used to trigger the start of the ramp. This is selected by the FECTRLxMUX registers in the Loop Mux. DPWMx_FRAME_SYNC_EN bits, when set, cause the ramp to be triggered at the start of the DPWM period.

7.2.2.5.3 Peak Current Mode (PCM)

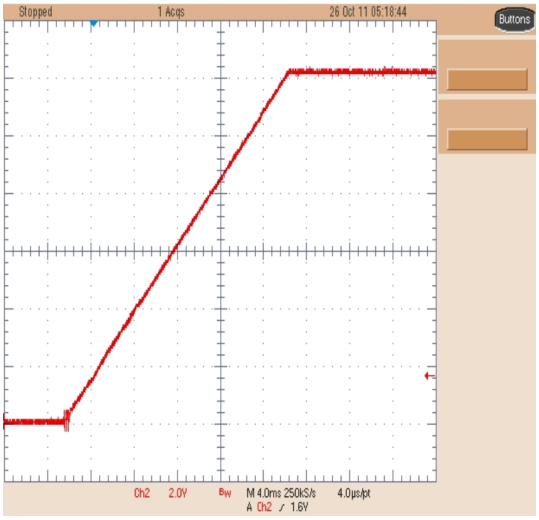
There is one peak current mode control module in the device however any front end can be configured to use this module.

7.2.3 Application Curves



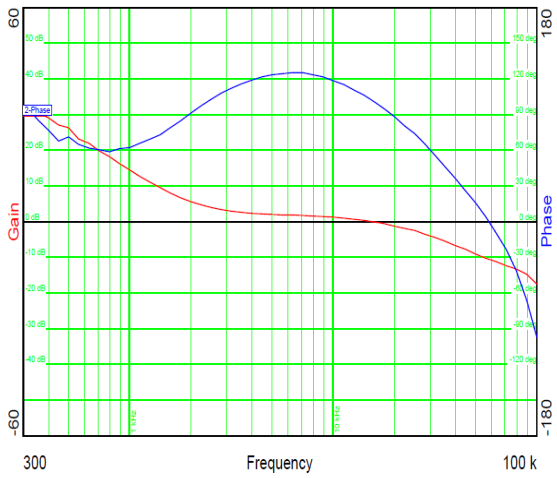
1A-16A-1A Vin =385V

Figure 7-10. Load Transient



30A Load syncFETs off

Figure 7-11. V_{OUT} Soft Start



Kp =14000
Ki =300

Kd =2000

Alpha = –2

Figure 7-12. Bode Plot

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7.2.4 Power Supply Recommendations

- Both 3.3 VD and 3.3 VA should have a local capacitor of at least 4.7-µF in parallel with a 10-nF capacitor placed as close as possible to the device pins.
- BP18 should have a 1-µF capacitor to ground.

7.2.5 Layout

7.2.5.1 Device Grounding and Layout Guidelines

- Single ground is recommended: SGND. A multilayer such as 4 layers board is recommended so that one solid SGND is dedicated for return current path, referred to the layout example.
- Apply multiple different capacitors for different frequency range on decoupling circuits. Each capacitor has different ESL, and ESR, and they have different frequency response.
- Avoid long traces close to radiation components, and place them into an internal layer, and it is preferred to have grounding shield, and in the end, add a termination circuit.
- Analog circuit such as ADC sensing lines needs a return current path into the analog circuitry; digital circuit such as GPIO, PMBus and PWM has a return current path into the digital circuitry; although with a single plane, still try to avoid to mix analog current and digital current.
- Don't use a ferrite bead or larger than 3-Ω resistor to connect between V33A and V33D.
- Both 3.3VD and 3.3VA should have local decoupling capacitors close to the device power pins, add vias to connect decoupling caps directly to SGND.
- Avoid negative current/negative voltage on all pins, so Schottky diodes may need to clamp the voltage; avoid the voltage spike on all pins more than 3.8 V or less than –0.3 V, add Schottky diodes on the pins which could have voltage spikes during surge test; be aware that a Schottky has relatively higher leakage current, which can affect the voltage sensing at high temperature.
- If V33 slew rate is less than 2.5 V/ms the RESET pin should have a 2.21-kΩ resistor between the reset pin and V33D and a 2.2-µF capacitor from RESET to ground. For more details please refer to the UCD3138 Family - Practical Design Guideline This capacitor must be located close to the device RESET pin.
- The 2.2-µF capacitor between V33D and BP18 can be removed due to internal enhancement design.
- Configure unused GPIO pins to be inputs or connect them to the ground (DGND or SGND); when an external pull-up resistor is used for GPIO, the pull-up resistor needs to be 1kOhm or higher.

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7.2.5.2 Layout Example

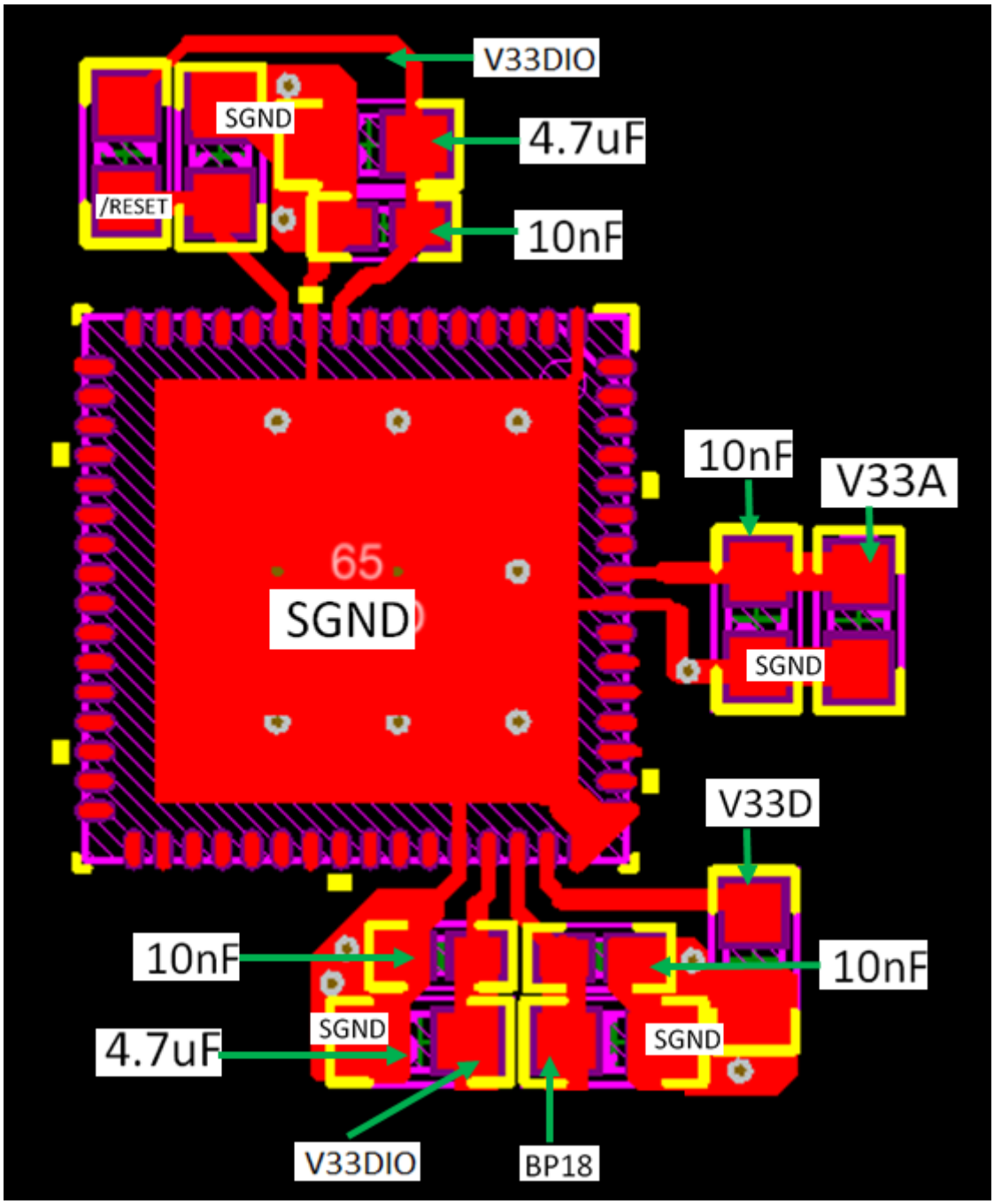


Figure 7-13.
PCB Layout Example

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8 Device and Documentation Support

8.1 Device Support

The application firmware for the UCD3138064A is developed on Texas Instruments Code Composer Studio (CCS) integrated development environment (v3.3 recommended).

Device programming, real time debug and monitoring/configuration of key device parameters for certain power topologies are all available through Texas Instruments' FUSION_DIGITAL_POWER_DESIGNER Graphical User Interface (http://www.ti.com/tool/fusion_digital_power_designer). The FUSION_DIGITAL_POWER_DESIGNER software application uses the PMBus protocol to communicate with the device over a serial bus using an interface adaptor known as the USB-TO-GPIO, available as an EVM from Texas Instruments (http://www.ti.com/tool/usb-to-gpio). PMBUS-based real-time debug capability is available through the 'Memory Debugger' tool within the Device GUI module of the FUSION_DIGITAL_POWER_DESIGNER GUI, which represents a powerful alternative over traditional JTAG-based approaches'.

The software application can also be used to program the devices, with a version of the tool known as FUSION_MFR_GUI optimized for manufacturing environments (http://www.ti.com/tool/fusion_mfr_gui). The FUSION_MFR_GUI tool supports multiple devices on a board, and includes built-in logging and reporting capabilities.

In terms of reference documentation, the following programmer's manuals are available offering detailed information regarding the application and usage of UCD3138064A digital controller:

1. UCD3138064A Programmer's Manual
2. UCD3138064A Digital Power Peripheral Programmer's Manual Key topics covered in this manual include:
   - Digital Pulse Width Modulator (DPWM)
     - Modes of Operation (Normal/Multi/Phase-shift/Resonant etc)
     - Automatic Mode Switching
     - DPWMC, Edge Generation & Intra-Mux
   - Front End
     - Analog Front End
     - Error ADC or EADC
     - Front End DAC
     - Ramp Module
     - Successive Approximation Register Module
   - Filter
     - Filter Math
   - Loop Mux
     - Analog Peak Current Mode
     - Constant Current/Constant Power (CCCP)
     - Automatic Cycle Adjustment
   - Fault Mux
     - Analog Comparators
     - Digital Comparators
     - Fault Pin functions
     - DPWM Fault Action
     - Ideal Diode Emulation (IDE), DCM Detection
     - Oscillator Failure Detection
   - Register Map for all of the above peripherals in UCD3138064A
3. UCD3138064A Monitoring and Communications Programmer's Manual Key topics covered in this manual include:
   - ADC12
     - Control, Conversion, Sequencing & Averaging

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  - Digital Comparators
  - Temperature Sensor
  - PMBUS Addressing
  - Dual Sample & Hold
- Miscellaneous Analog Controls (Current Sharing, Brown-Out, Clock-Gating)
- PMBUS Interface
- General Purpose Input Output (GPIO)
- Timer Modules
- PMBus
- Register Map for all of the above peripherals in UCD3138064A

4. UCD3138064A ARM and Digital System Programmer's Manual Key topics covered in this manual include:
   - Boot ROM & Boot Flash
     - BootROM Function
     - Memory Read/Write Functions
     - Checksum Functions
     - Flash Functions
     - Avoiding Program Flash Lock-Up
   - ARM7 Architecture
     - Modes of Operation
     - Hardware/Software Interrupts
     - Instruction Set
     - Dual State Inter-working (Thumb 16-bit Mode/ARM 32-bit Mode)
   - Memory & System Module
     - Address Decoder, DEC (Memory Mapping)
     - Memory Controller (MMC)
     - Central Interrupt Module
   - Register Map for all of the above peripherals in UCD3138064A
5. FUSION_DIGITAL_POWER_DESIGNER for UCD31xx Isolated Power Applications – User Guide

In addition to the tools and documentation described above, for the most up to date information regarding evaluation modules, reference application firmware and application notes/design tips, visit http://www.ti.com/product/ucd3138064.

8.2 Documentation Support

8.2.1 Related Documentation

1. UCD3138064A Programmer's Manual (SLUUAD8)
2. UCD3138 Digital Power Peripherals Programmer's Manual (SLUU995)
3. UCD3138 Monitoring & Communications Programmer's Manual (SLUU996)
4. UCD3138 ARM and Digital System Programmer's Manual (SLUU994)
5. FUSION_DIGITAL_POWER_DESIGNER for Isolated Power Applications (SLUA676)
6. Code Composer Studio Development Tools v3.3 – Getting Started Guide, (SPRU509H)
7. ARM7TDMI-S Technical Reference Manual
8. System Management Bus (SMBus) Specification
9. PMBus™ Power System Management Prototcol Specification

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8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.5 Trademarks

E2E is a trademark of Texas Instruments.
PMBus is a trademark of SMIF, Inc..
All other trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD3138064ARGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138064A
UCD3138064ARGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138064A
UCD3138064ARGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138064A
UCD3138064ARGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138064A
UCD3138064ARGCTG4	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138064A
UCD3138064ARGCTG4.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCD3138064A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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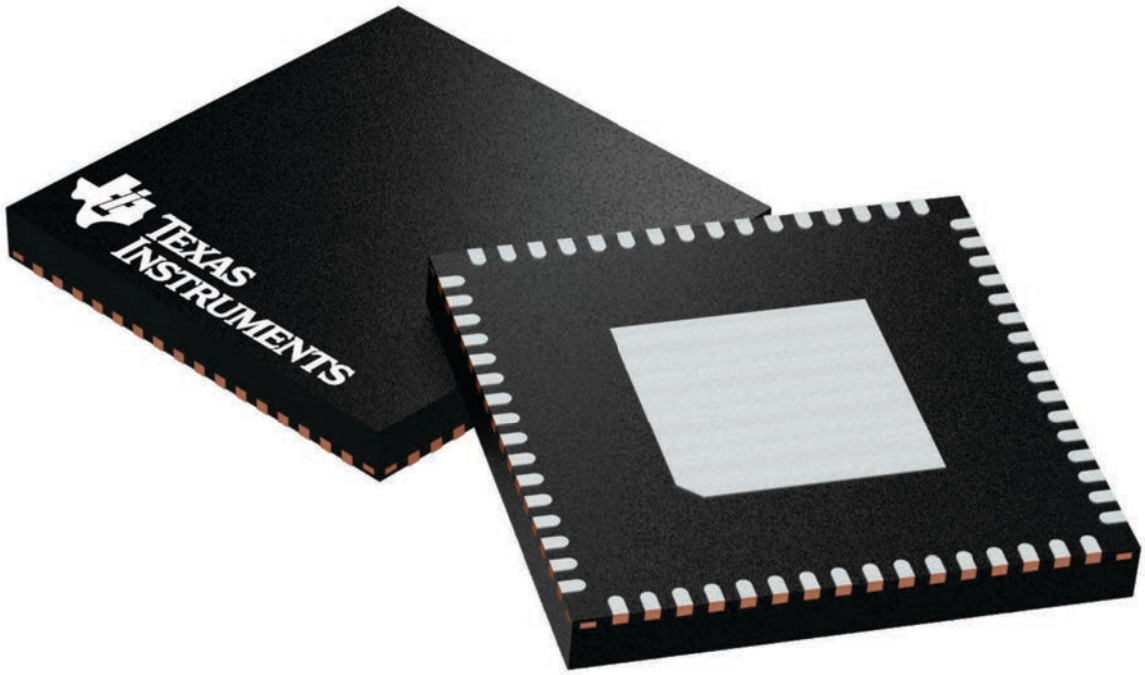
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

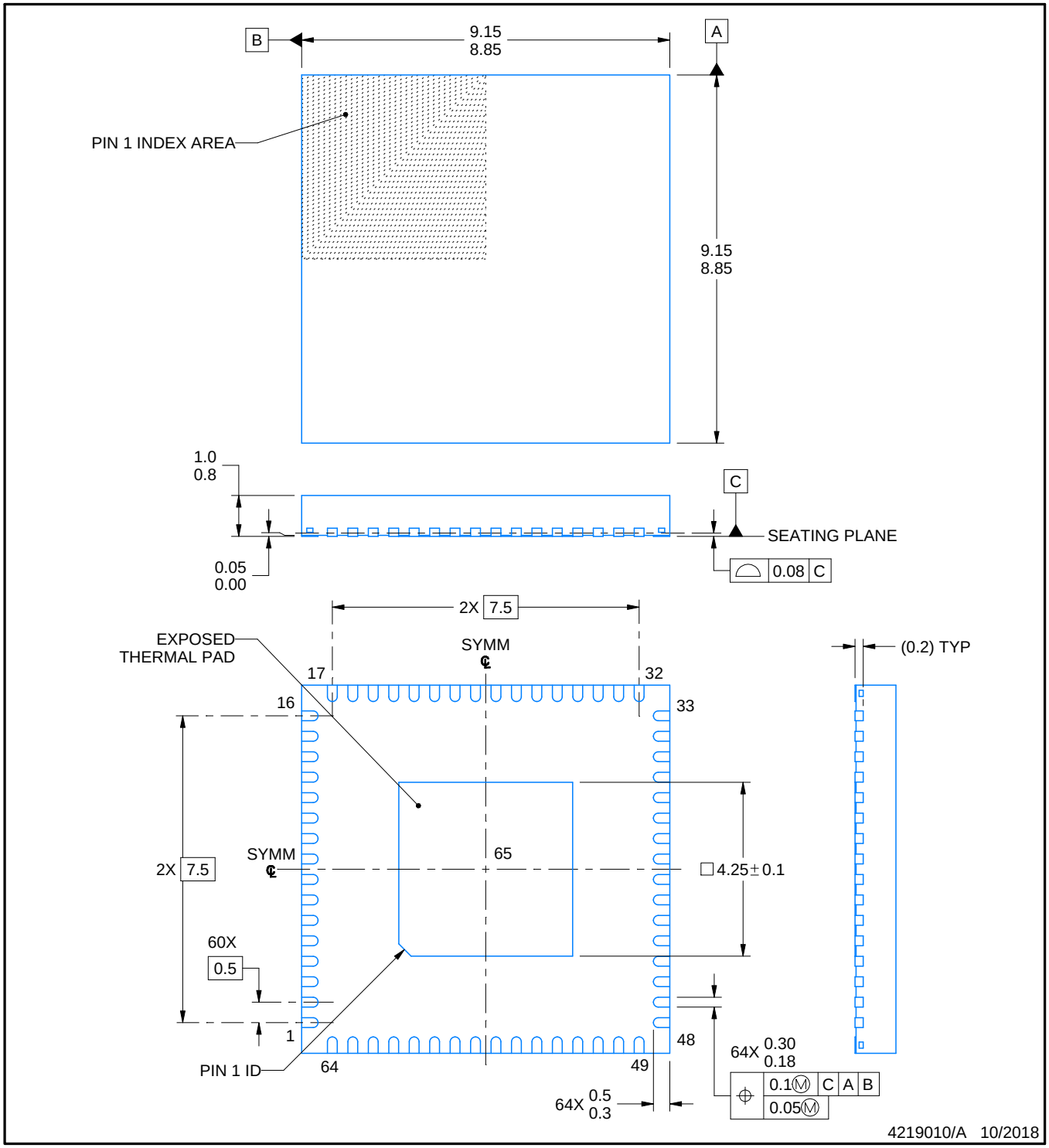
4224597/A

PACKAGE OUTLINE

RGC0064B

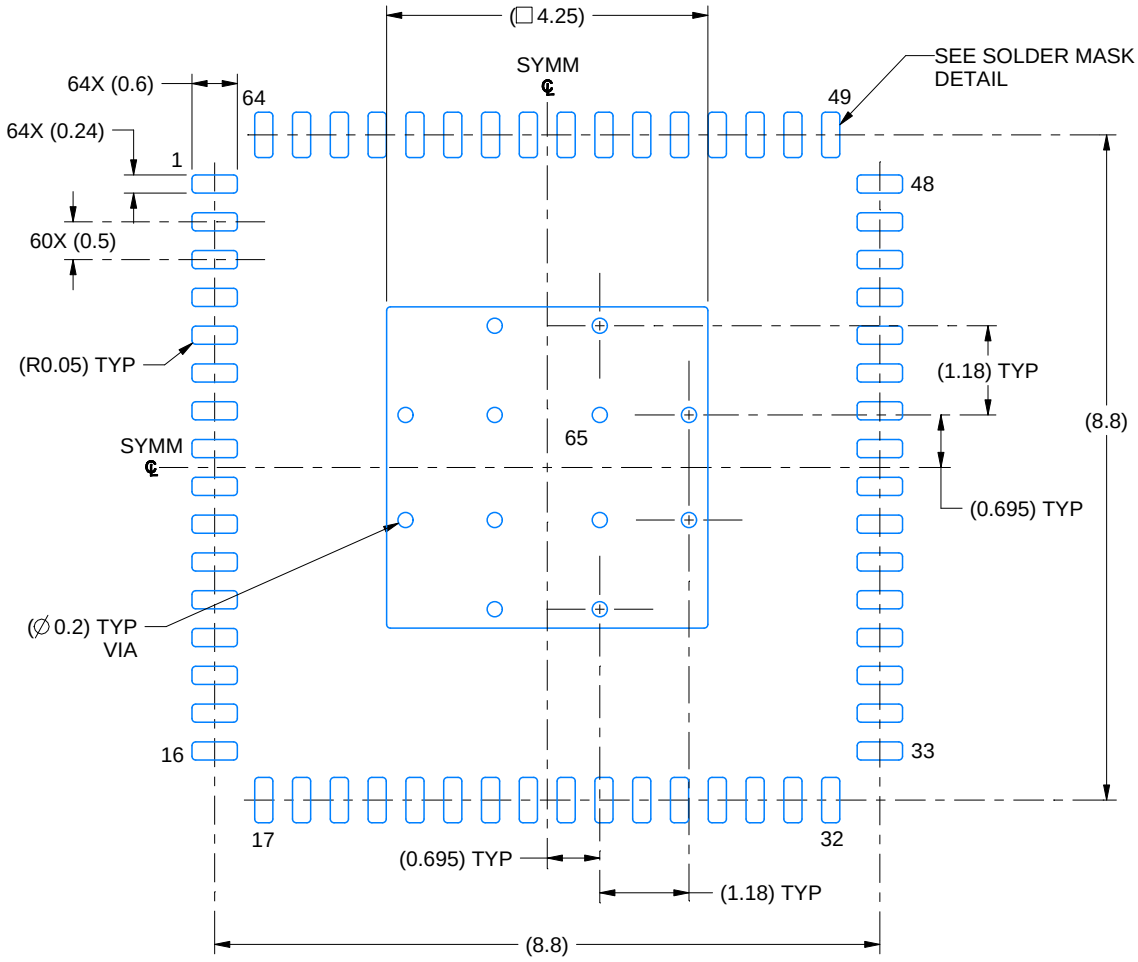
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

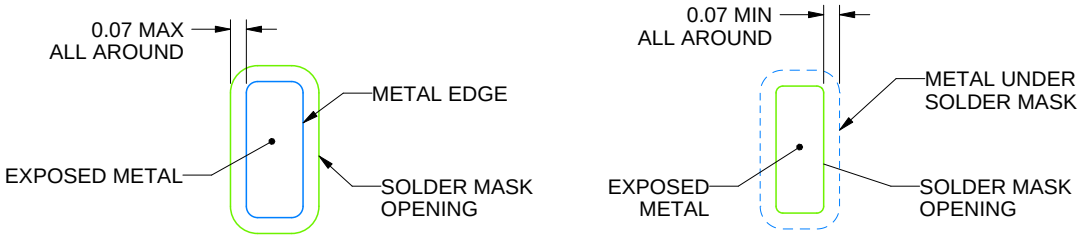


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

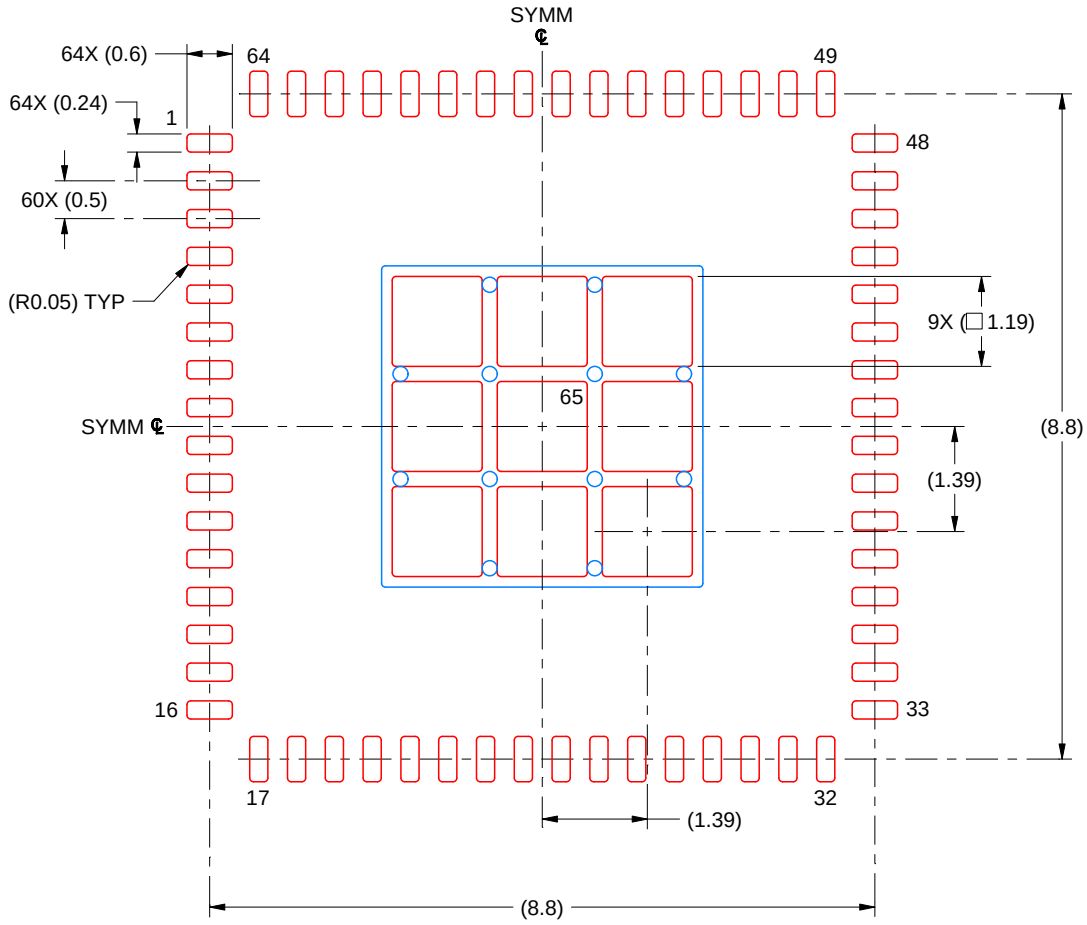


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025