UCD90120 12-Channel Sequencer and System Health Monitor

FEATURES

- **Monitor and Sequence 12 Voltage Rails**
  - **All Rails Sampled Every 200µs**
  - **12-bit ADC With 2.5V, 0.5% Internal V_{REF}**
  - **Sequence Based on Time, Rail and Pin Dependencies**
  - **Six Hardware Comparators for Power Supply Fault Response in < 80µs**
  - **Four Programmable Under-Voltage and Over-Voltage Thresholds per Monitor**
  - **Programmable Fault Response Including Retries, Shutdown Slaves and Resequence**
- **Non-Volatile Error Logging**
  - **Stores Up To 18 Faults**
  - **Log Peak Values For All Monitor Inputs**
- **Closed Loop Margining for 10 Rails**
  - **Margin Output Adjusts Rail Voltage to Match User-Defined Margin Thresholds**
  - **Unused Margin Outputs can be Used as GPIOs or General-Purpose PWM Outputs**
- **Watchdog Timer and System Reset**
  - **Programmable WDT Reset and Start Times**
  - **Configurable System Reset Pulse Widths**
- **Flexible Digital I/O Configuration**
  - **Boolean Logic Builder for GPO Config**
  - **GPIOs can be Used as Enables, Resets, Power Good and Other On-Board Functions**
- **Wide Range Single Supply (3.3V to 12V)**
  - **Internal Temperature Sensor**
  - **64-Pin QFN Package**
- **JTAG and I²C/SMBus/PMBus Interfaces**
- **Fusion Digital Power™ GUI for Configuring and Monitoring Device Operation**

APPLICATIONS

- **Industrial / ATE**
- **Telecommunications and Networking Equipment**
- **Servers and Storage Systems**
- **Any System Requiring Sequencing and Monitoring of Multiple Power Rails**

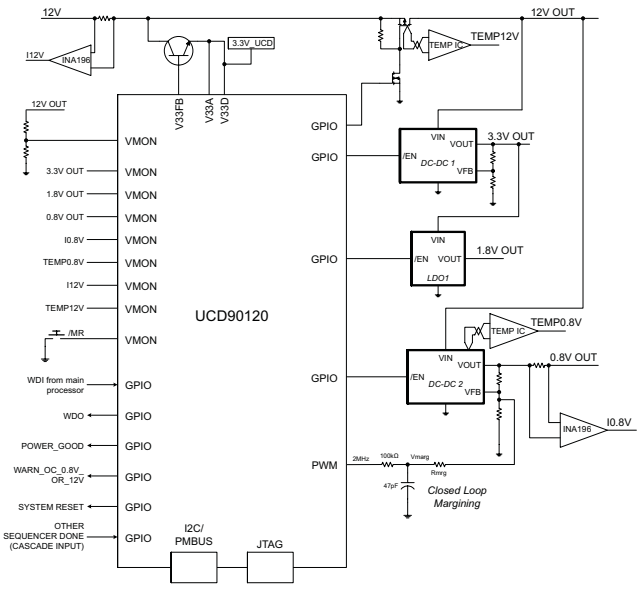
DESCRIPTION

The UCD90120 Power Supply Sequencer and System Health Monitor monitors and sequences up to 12 independent voltage rails. The device integrates a 12-bit ADC with a 2.5V internal reference for monitoring up to 13 power supply voltage, current, or temperature inputs.

26 GPIO pins can be used for power supply enables, power-on reset signals, external interrupts, cascading multiple UCD90120 devices, or other system functions. 12 of these pins can be used as PWM outputs for power supply margining or general-purpose PWM functions including clock generation for switch-mode power supplies.

The TI Fusion Digital Power Designer is provided for device configuration. This PC-based Graphical User Interface (GUI) offers an intuitive interface for configuring, storing, and monitoring all system operating parameters.

The UCD90120 has an I²C/PMBus/SMBus communication interface for pre-production and in-system configuring and monitoring and a JTAG Port for production programming.



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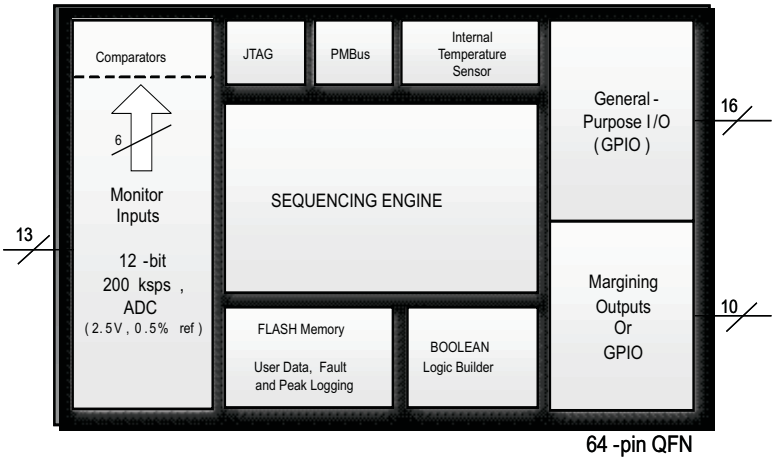
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

ORDERABLE PART NUMBER	PACKAGE	Supply
UCD90120RGCR	64-pin QFN	Reel of 2000
UCD90120RGCT	64-pin QFN	Reel of 250

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Voltage applied at V33D to DV_{SS}		–0.3 V to 3.8	V
Voltage applied at V33A to AV_{SS}		–0.3 V to 3.8	V
Voltage applied to any pin (2)		–0.3 V to 3.8	V
Storage temperature (T_{STG})		–40 to 150	°C
ESD Rating	Human body model (HBM)	2.5	kV
	Charged device model (CDM)	750	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{33D}, V_{33DIO}, V_{33A}	Supply voltage during operation (V_{33D}, V_{33DIO}, V_{33A})	3.0	3.3	3.6	V
T_A	Operating free-air temperature range	–40		110	°C
T_J	Junction temperature			125	°C

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current	V_{V33A} = 3.3V		8	15	mA
I_{V33DIO}		V_{V33DIO} = 3.3V		2	10	mA
I_{V33D}		V_{V33D} = 3.3V		40	45	mA
I_{V33D}		V_{V33D} = 3.3V storing configuration parameters in flash memory		50	55	mA
INTERNAL REGULATOR CONTROLLER INPUTS/OUTPUTS						
V_{V33}	3.3V Linear Regulator	Emitter of NPN transistor	3.25	3.3	3.35	V
V_{V33FB}	3.3V linear Reg Feedback			4	4.6	V
I_{V33FB}	Series pass base drive	V_{VIN} = 12V		10		mA
Beta	Series NPN pass device		40			
EXTERNALLY SUPPLIED 3.3V POWER						
V_{V33D}, V_{V33DIO}	Digital 3.3V power	$T_{ambient}$ = 25°C	3.00		3.60	V
V_{V33A}	Analog 3.3V power	$T_{ambient}$ = 25°C	3.00		3.60	V

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ANALOG INPUTS (MON1–MON13)						
V_{MON}	Input voltage range	MON1–MON9	0.0		2.5	V
		MON10–MON13	0.2		2.5	V
INL	ADC integral nonlinearity		–2.5		2.5	mV
I_{lkg}	Input leakage current	3V applied to pin			100	nA
I_{OFFSET}	Input offset current	1kΩ source impedance	–5		5	µA
R_{IN}	Input impedance	MON1–MON9, Ground reference	8			MΩ
		MON10–MON13, Ground reference	0.5	1.5	3.0	MΩ
C_{IN}	Input capacitance				10	pF
$T_{CONVERT}$	ADC sample period	14 voltages sampled, 3.89 µsec/sample		200		µsec
V_{REF}	ADC 2.5V internal	0°C to 125°C	–0.5%		0.5%	
	reference accuracy	–40°C to 125°C	–1.0%		1.0%	
ANALOG INPUT (PMBUS_ADDRx, INTERNAL TEMP SENSE)						
I_{BIAS}	Bias current for PMBus Addr pins		9		11	µA
V_{ADDR_OPEN}	Voltage – open pin	AddrSens0,1 open	2.26			V
V_{ADDR_SHORT}	Voltage – shorted pin	AddrSens0,1 short to ground			0.124	V
$Temp_{Internal}$	Internal temperature sense accuracy	Over range from 0°C to 100°C	–5		5	°C
DIGITAL INPUTS AND OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA(1), V_{33DIO} = 3.0 V			Dgnd + 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6 mA(2), V_{33DIO} = 3.0 V	V_{33DIO} – 0.6V			V
V_{IH}	High-level input voltage	V_{33DIO} = 3.0 V	2.1		3.6	V
V_{IL}	Low-level input voltage	V_{33DIO} = 3.5 V			1.4	V
SYSTEM PERFORMANCE						
V_{DD}Slew	Minimum V_{DD} slew rate	V_{DD} slew rate between 2.3 and 2.9V	0.25			V/ms
V_{RESET}	Supply voltage at which device comes out of reset	For power on reset (POR)			2.4	V
t_{RESET}	Low pulse length needed at nReset pin	To reset device during normal operation	2			µS
f(PCLK)	Internal oscillator frequency	T_A = 125°C, T_A = 25°C		250		MHz
$T_{retention}$	Retention of configuration parameters	T_J = 25°C	100			Years
Write_Cycles	Number of nonvolatile erase/write cycles	T_J = 25°C	20			K cycles

(1) The maximum total current, IOHmax and IOLmax, for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, IOHmax and IOLmax, for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified.

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PMBus/SMBus/I²C

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus and PMBus is shown below.

I²C/SMBus/PMBus TIMING REQUIREMENTS

T_A = –40°C to 85°C, 3.0V < V_{DD} < 3.6V; Typical values at T_A = 25°C and V_{CC} = 2.5V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSMB	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		1000	kHz
FI2C	I²C operating frequency	Slave mode, SCL 50% duty cycle	10		1000	kHz
t(BUF)	Bus free time between start and stop		4.7			µs
t(HD:STA)	Hold time after (repeated) start		0.26			µs
t(SU:STA)	Repeated start setup time		0.26			µs
t(SU:STO)	Stop setup time		0.26			µs
t(HD:DAT)	Data hold time	Receive Mode	0			ns
t(SU:DAT)	Data setup time		50			ns
t(TIMEOUT)	Error signal/detect	See (1)			35	ms
t(LOW)	Clock low period		0.5			µs
t(HIGH)	Clock high period	See (2)	0.26		50	µs
t(LOW:SEXT)	Cumulative clock low slave extend time	See (3)			25	ms
t_{FALL}	Clock/data fall time	See (4)			120	ns
t_{RISE}	Clock/data rise time	See (5)			120	ns

(1) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) Rise time t_r = (VIL_{MAX} – 0.15) to (VIH_{MIN} + 0.15)
(5) Fall time t_f = 0.9VDD to (VIL_{MAX} – 0.15)

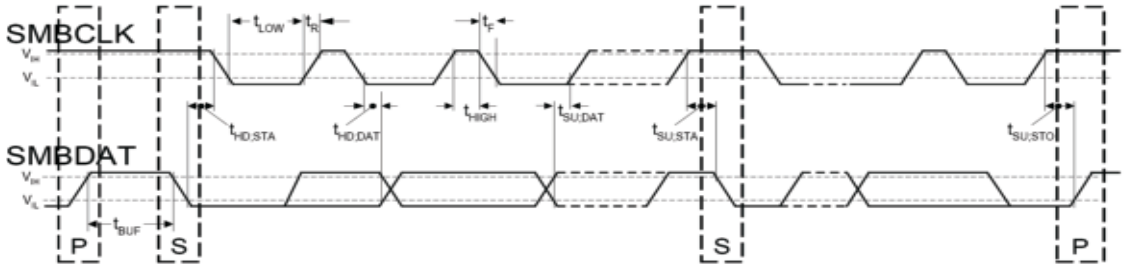


Figure 1. I²C/SMBus Timing Diagram

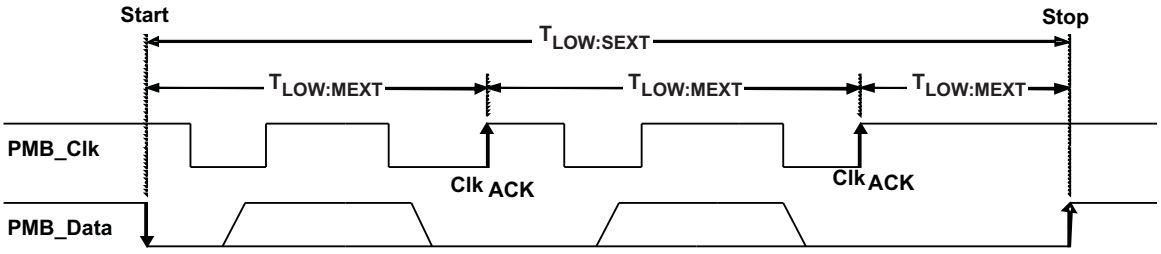
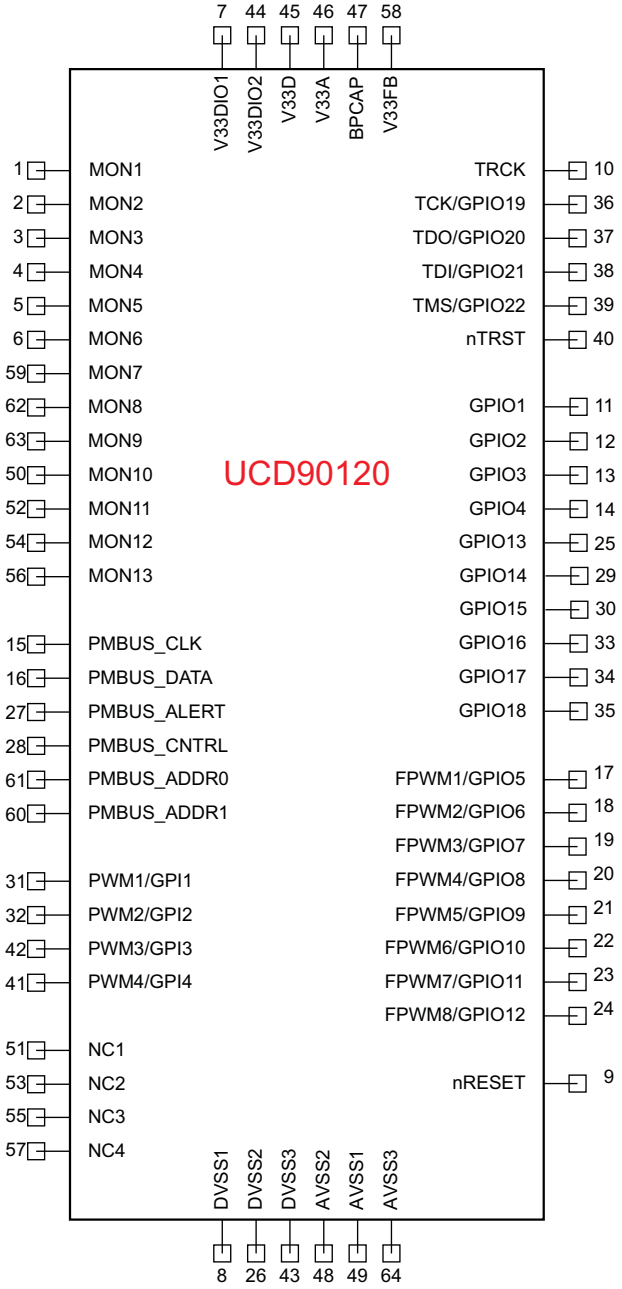


Figure 2. Bus Timing in Extended Mode

DEVICE INFORMATION

UCD90120 PIN ASSIGNMENT



PIN FUNCTIONS

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
ANALOG MONITOR INPUTS			
MON1	1	I	Analog Input (0 V–2.5 V)
MON2	2	I	Analog Input (0 V–2.5 V)
MON3	3	I	Analog Input (0 V–2.5 V)
MON4	4	I	Analog Input (0 V–2.5 V)
MON5	5	I	Analog Input (0 V–2.5 V)
MON6	6	I	Analog Input (0 V–2.5 V)

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PIN FUNCTIONS (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
MON7	59	I	Analog Input (0 V–2.5 V)
MON8	62	I	Analog Input (0 V–2.5 V)
MON9	63	I	Analog Input (0 V–2.5 V)
MON10	50	I	Analog Input (0.2 V – 2.5 V)
MON11	52	I	Analog Input (0.2 V – 2.5 V)
MON12	54	I	Analog Input (0.2 V – 2.5 V)
MON13	56	I	Analog Input (0.2 V – 2.5 V)
GPIO			
GPIO1	11	I/O	General purpose discrete I/O
GPIO2	12	I/O	General purpose discrete I/O
GPIO3	13	I/O	General purpose discrete I/O
GPIO4	14	I/O	General purpose discrete I/O
GPIO13	25	I/O	General purpose discrete I/O
GPIO14	29	I/O	General purpose discrete I/O
GPIO15	30	I/O	General purpose discrete I/O
GPIO16	33	I/O	General purpose discrete I/O
GPIO17	34	I/O	General purpose discrete I/O
GPIO18	35	I/O	General purpose discrete I/O
PWM OUTPUTS			
FPWM1/GPIO5	17	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM2/GPIO6	18	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM3/GPIO7	19	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM4/GPIO8	20	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM5/GPIO9	21	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM6/GPIO10	22	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM7/GPIO11	23	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM8/GPIO12	24	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
PWM1/GPI1	31	I/PWM	Fixed 10 kHz PWM output or GPI
PWM2/GPI2	32	I/PWM	Fixed 1 kHz PWM output or GPI
PWM3/GPI3	42	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PWM4/GPI4	41	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PMBus COMM INTERFACE			
PMBUS_CLK	15	I/O	PMBus Clock (Must have pull-up to 3.3 V)
PMBUS_DATA	16	I/O	PMBus Data (Must have pull-up to 3.3 V)
PMBALERT#	27	O	PMBus Alert, Active Low, Open Drain Output (Must have pull-up to 3.3V)
PMBUS_CNTRL	28	I	PMBus Control
PMBUS_ADDR0	61	I	PMBus analog address input. Least significant address bit.
PMBUS_ADDR1	60	I	PMBus analog address input. Most significant address bit.
JTAG			
TRCK	10	O	Test return clock
TCK/GPIO19	36	I/O	Test clock or GPIO
TDO/GPIO20	37	I/O	Test data out or GPIO
TDI/GPIO21	38	I/O	Test data in (tie to V_{dd} with 10k resistor) or GPIO
TMS/GPIO22	39	I/O	Test mode select (tie to V_{dd} with 10k resistor) or GPIO
nTRST	40	I	Test reset – tie to ground with 10k resistor
INPUT POWER AND GROUNDS			
nRESET	9		Active low device reset input. Hold low for at least 2 μs to reset the device

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PIN FUNCTIONS (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
V33FB	58		3.3V Linear Regulator Feedback connection
V33A	46		Analog 3.3 V supply
V33D	45		Digital Core 3.3V supply
V33DIO1	7		Digital I/O 3.3V supply
V33DIO2	44		Digital I/O 3.3V supply
BPCap	47		1.8V Bypass Capacitor – tie 0.1μF cap to analog ground
AVSS1	49		Analog Ground
AVSS2	48		Analog Ground
AVSS3	64		Analog Ground
DVSS1	8		Digital Ground
DVSS2	26		Digital Ground
DVSS3	43		Digital Ground
QFP Ground Pad	NA		PowerPAD – Tie to ground plane

FUNCTIONAL DESCRIPTION

TI FUSION GUI

The Texas Instruments *Fusion Digital Power Designer* is provided for device configuration. This PC-based Graphical User Interface (GUI) offers an intuitive I^2C/PMBus interface to the device. It allows the design engineer to configure the system operating parameters for the application without directly using PMBus commands, store the configuration to on-chip non-volatile memory, and observe system status (voltage, temperature, etc). Fusion is referenced throughout the datasheet and many sections include screenshots.

THEORY OF OPERATION

Modern electronic systems often use numerous microcontrollers, DSPs, FPGAs, and ASICs. Each device can have multiple supply voltages to power the core processor, analog-to-digital converter or I/O. These devices are typically sensitive to the order and timing of how the voltages are sequenced on and off. The UCD90120 can sequence supply voltages to prevent malfunctions, intermittent operation or device damage caused by improper power-up or power-down. Appropriate handling of under- and over-voltage faults, over-current faults and over-temperature faults can extend system life and improve long term reliability. The UCD90120 stores power supply faults to on-chip non-volatile flash memory for aid in system failure analysis.

System reliability can be improved through four-corner testing during system verification. During four-corner testing, the system is operated at the minimum and maximum expected ambient temperature and with each power supply set to the minimum and maximum output voltage, commonly referred to as margining. The UCD90120 can be used to implement accurate closed-loop margining of up to 10 power supplies.

The UCD90120 12-rail sequencer can be used in a PMBus- or pin-based control environment. The TI Fusion GUI provides a powerful but simple interface for configuring sequencing solutions for systems with between one and 12 power supplies using 13 analog voltage monitor inputs, 4 GPIs and 22 highly configurable GPIOs. A rail can include voltage, temperature, current, a power supply enable and a margining output. At least one must be included in a rail definition. Once the user has defined how the power supply rails should operate in a particular system, analog input pins and GPIOs can be selected to monitor and enable each supply (Figure 3).

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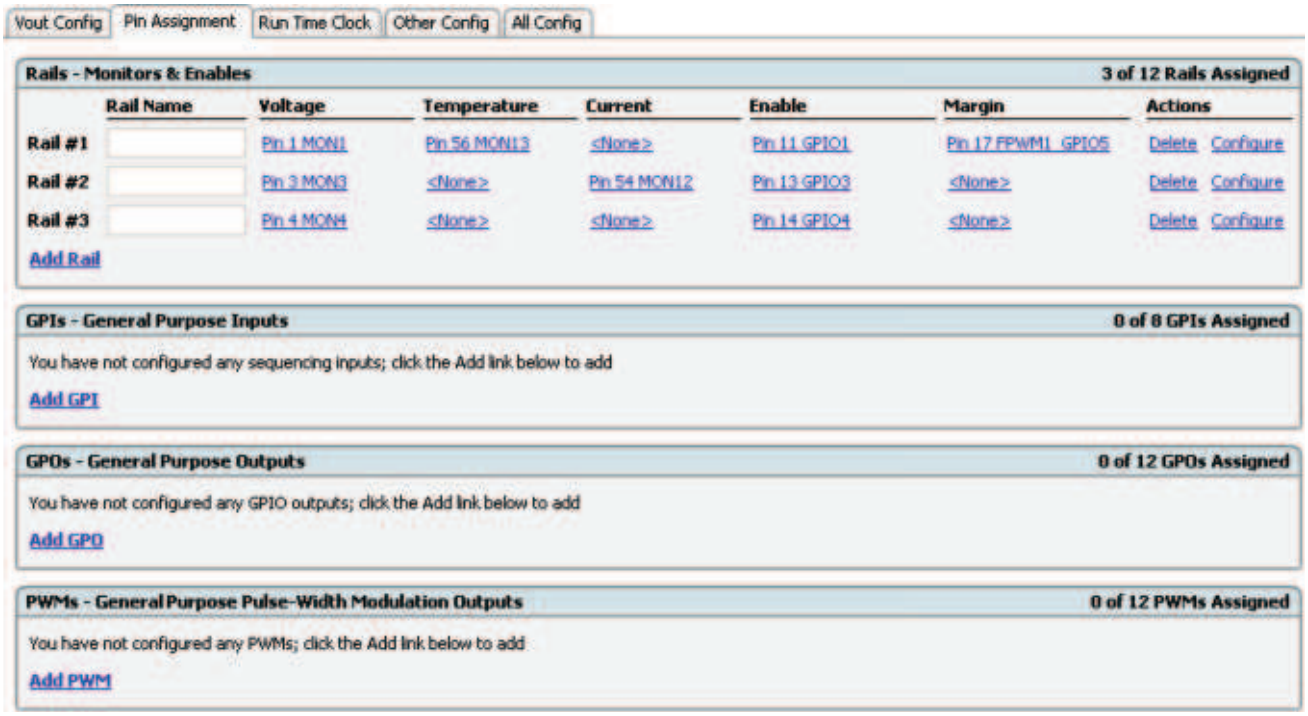


Figure 3. Fusion Pin Assignment Tab

After the pins have been configured, other key monitoring and sequencing criteria are selected for each rail from the Vout Config tab (Figure 4):

- Nominal operating voltage (Vout)
- Under-voltage (UV) and over-voltage (OV) warning and fault limits
- Margin Low and Margin High values
- Power Good On and Power Good Off limits
- PMBus or pin-based sequencing control (On/Off Config)
- Rails that have to achieve Power Good or Input pins that must be at a defined logic state before a Rail is enabled (Rail and Input Pin Dependencies)
- Turn On and Turn Off Delay timing
- Maximum time allowed for a rail to reach POWER_GOOD_ON or POWER_GOOD_OFF after being enabled or disabled
- Other Rails to turn off in case of a fault on a Rail (Fault Shutdown Slaves)

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Figure 4. Fusion Vout Config Tab

The **Synchronize margins/limits/PG** to Vout checkbox is an easy way to change the nominal operating voltage of a Rail and also update all of the other limits associated with that rail according to the percentages shown to the right of each entry.

The plot in the upper left section of Figure 4 shows a simulation of the overall sequence-on and sequence-off configuration, including the nominal voltage, the Turn On and Turn Off Delay times, the Power Good On and Power Good Off voltages and any timing dependencies between the rails.

After a rail voltage has reached its POWER_GOOD_ON voltage and is considered to be in regulation, it is compared against two UV and two OV thresholds in order to determine if a warning or fault limit has been exceeded. If a fault is detected, the UCD90120 responds based on a variety of flexible, user-configured options. Faults can cause rails to restart, shut down immediately, sequence-off using Turn Off Delay times or shut down a group of rails and sequence them back on. Different types of faults can result in different responses.

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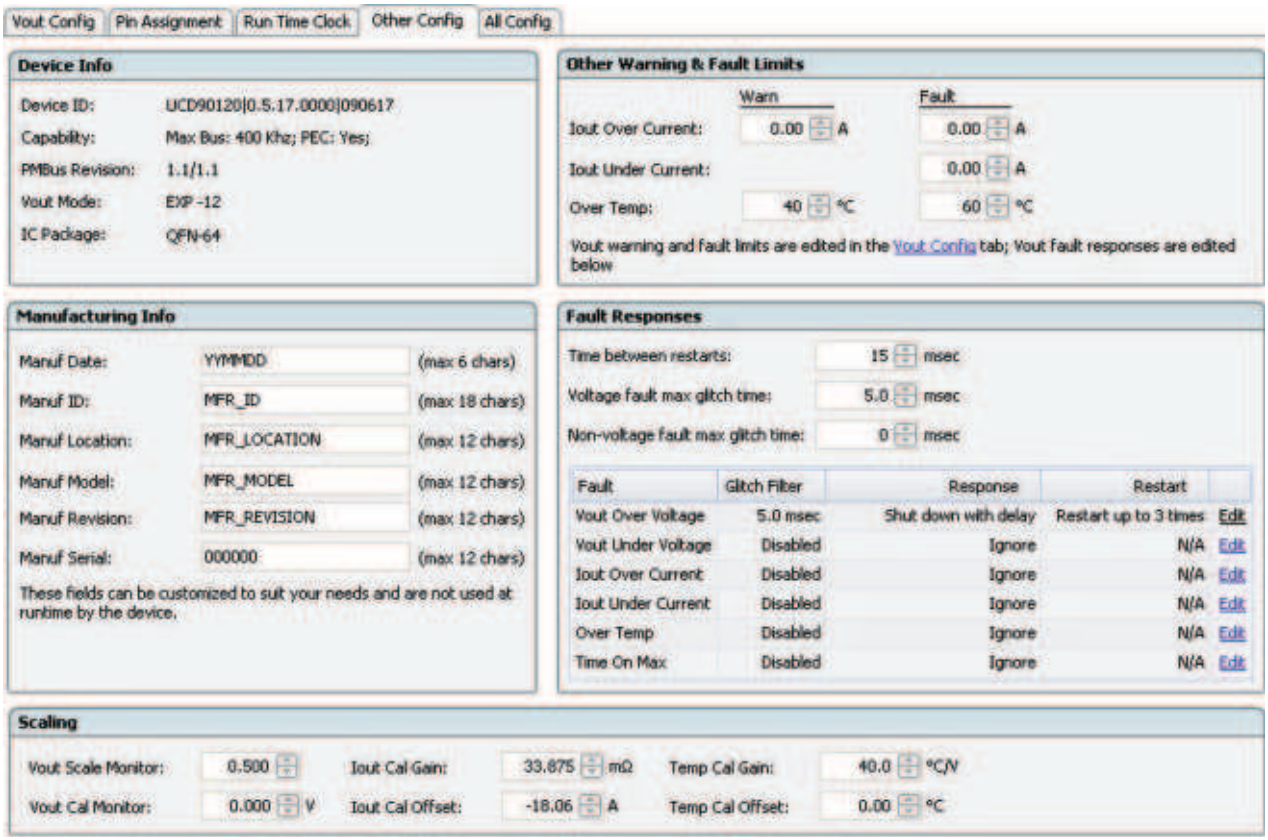


Figure 5. Fusion Other Config Tab for Fault Responses

Fault responses, along with a number of other parameters including user-specific Manufacturing Info and external scaling and offset values, are selected in the Fusion **Other Config** tab. Once the configuration satisfies the user requirements, it can be written to device SRAM if Fusion is connected to a UCD90120 using I^2C/PMBus. SRAM contents can then be stored to data flash memory so that the configuration remains in the device after a reset or power cycle.

The Fusion Monitor page has a number of options, including a Device Dashboard and a System Dashboard, for viewing and controlling device and system status in real time.

Figure 6. Fusion Monitor Page with Device Dashboard and System Dashboard

The UCD90120 also has status registers for each Rail and the capability to log faults to flash memory for use in system troubleshooting. This is very helpful in the case of a power supply or system failure. The status registers (Figure 7) and the fault log (Figure 8) are available in Fusion. Please refer to the UCD90120 PMBus Command Reference and the PMBus_Specification_Part_II_Rev_1-1_20070205 for detailed descriptions of each status register and supported PMBus commands.

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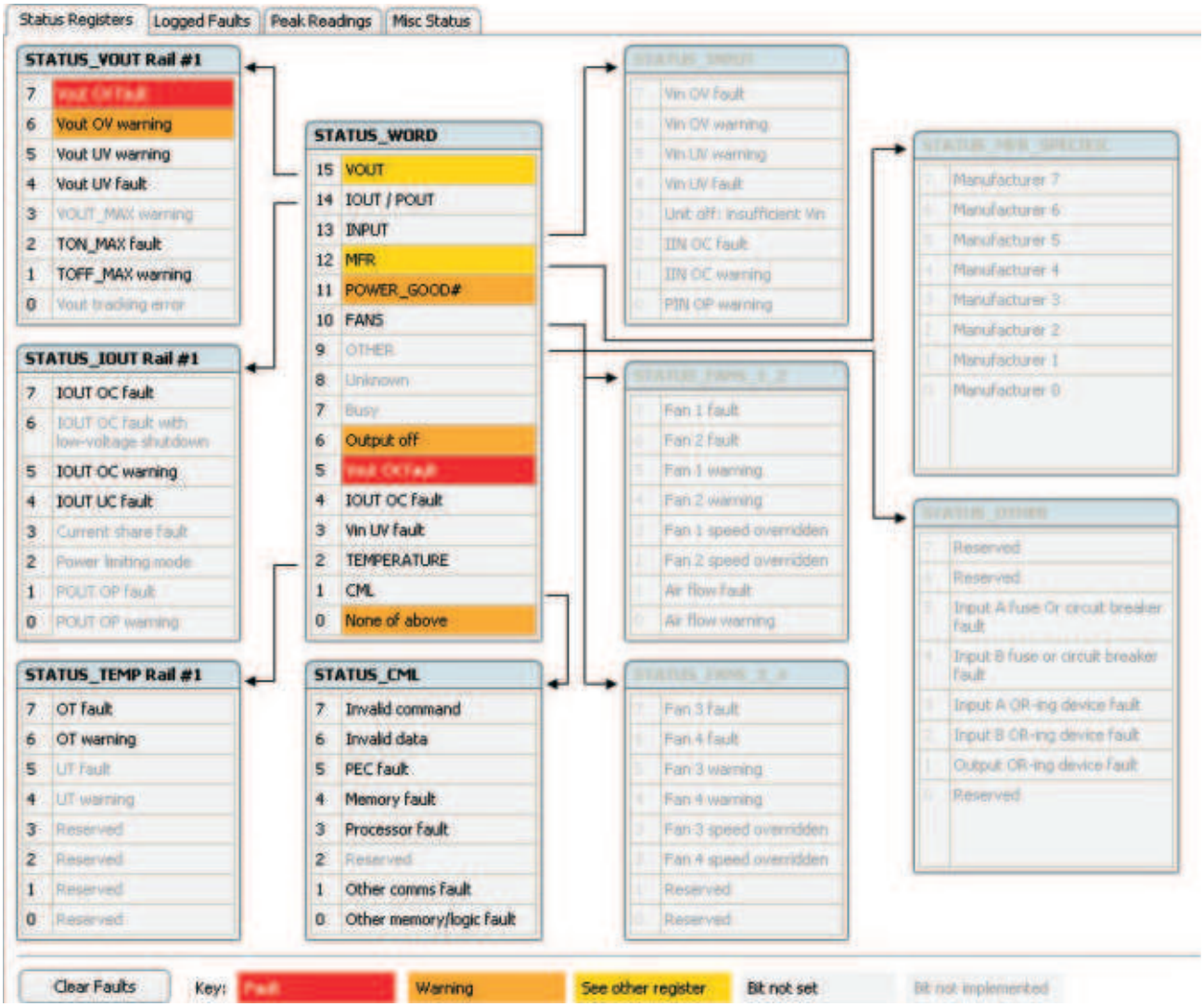


Figure 7. Fusion Rail Status Register

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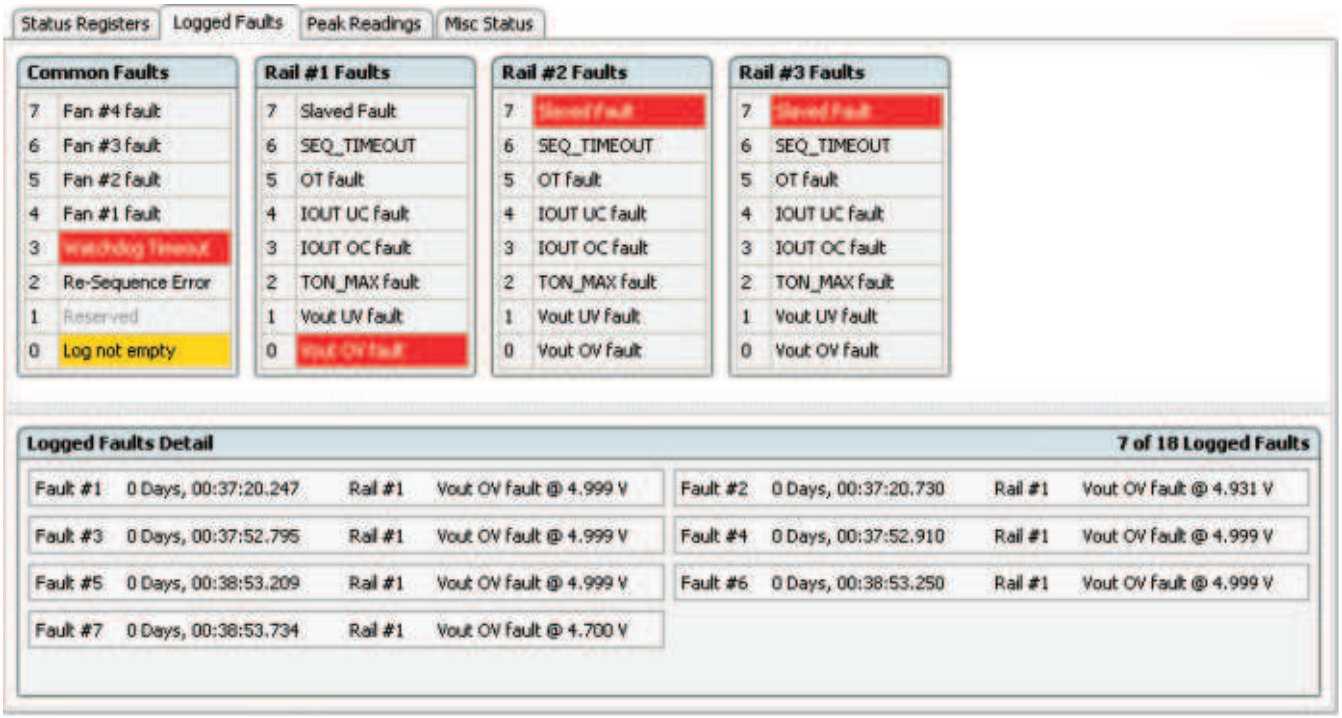


Figure 8. Fusion Flash error Log (Logged Faults)

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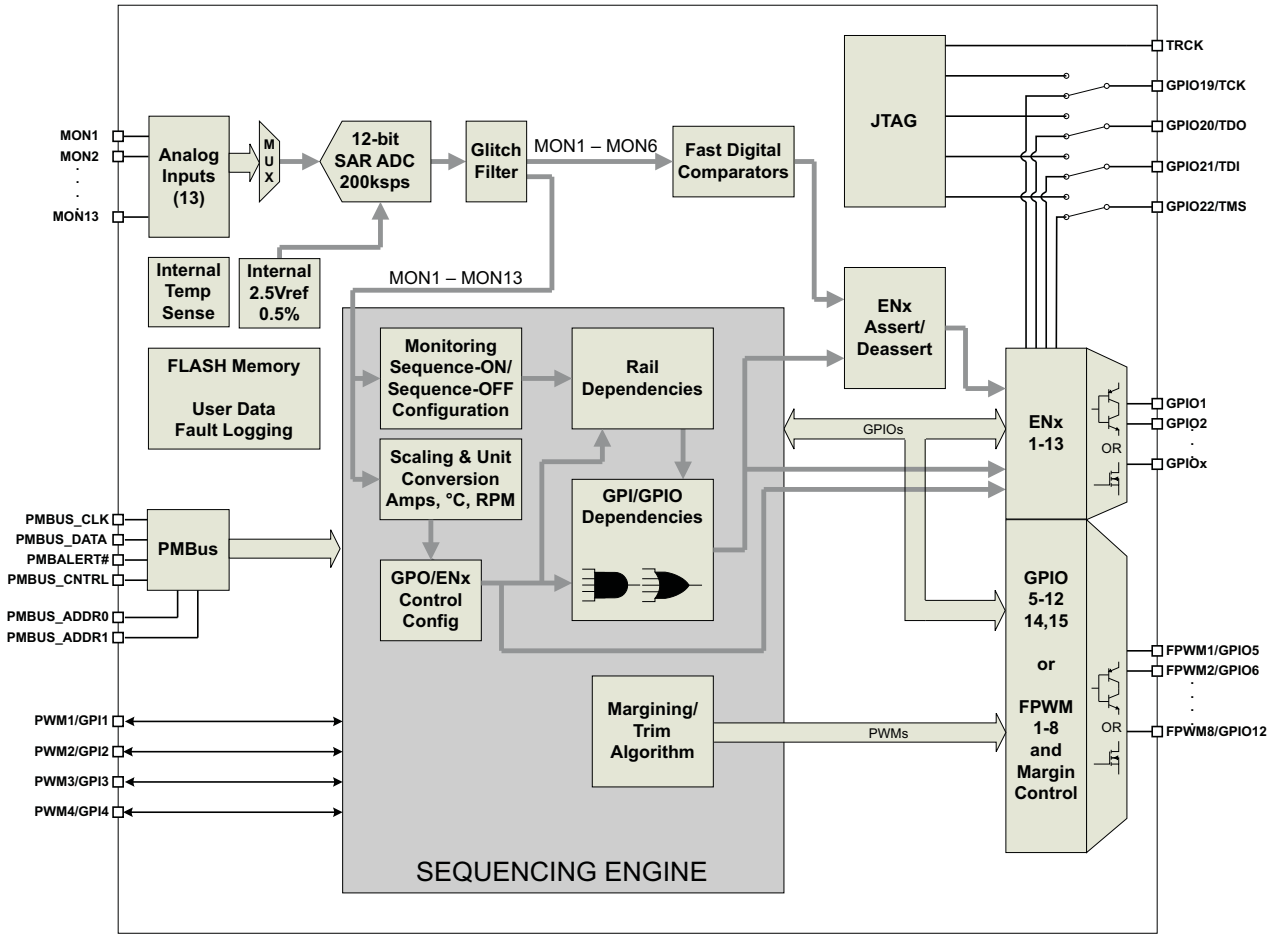


Figure 9. Detailed Block Diagram

POWER SUPPLY SEQUENCING

The UCD90120 can control the turn-on and turn-off sequencing of up to 12 voltage rails by using a GPIO to set a power supply enable pin high or low. In PMBus-based designs, the system PMBus master can initiate a sequence-on event by asserting the PMBUS_CNTRL pin or by sending the OPERATION command over the I^2C serial bus. In pin-based designs, the PMBUS_CNTRL pin can also be used to sequence-on and sequence-off.

The Auto Enable setting ignores the OPERATION command and the PMBUS_CNTRL pin. Sequence-on is started at power up after any dependencies and time delays are met for each rail. A rail is considered to be on or within regulation when the measured voltage for that rail crosses the Power Good On (POWER_GOOD_ON(1)) limit. The rail is still in regulation until the voltage drops below Power Good Off (POWER_GOOD_OFF).

(1) In this document configuration parameters such as Power Good On are referred to using Fusion GUI names. The PMBus Command Reference name is shown in parentheses (POWER_GOOD_ON) the first time the parameter appears.

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Turn-on Sequencing

The following sequence-on options are supported for each rail:

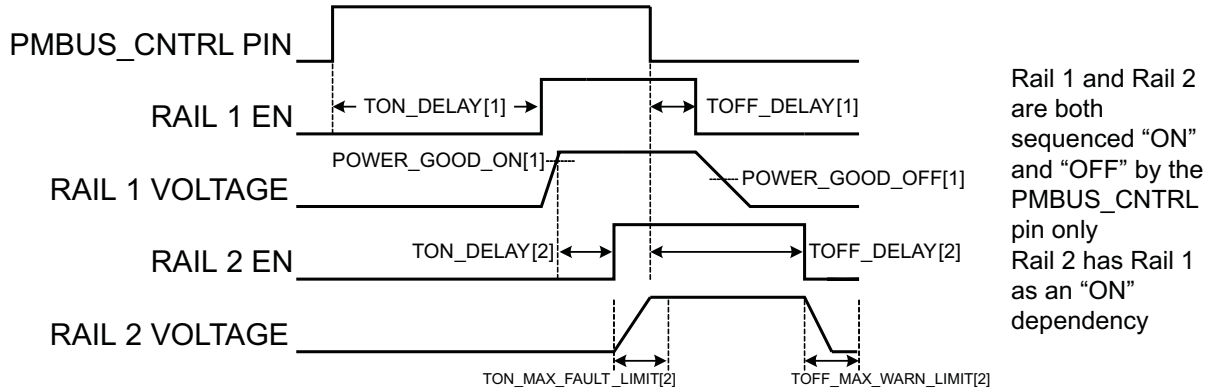


Figure 10. Sequence-on and Sequence-off Timing

- Monitor only – do not sequence-on
- Fixed delay time after a PMBus OPERATION command to turn on
- Fixed delay time after assertion of the PMBUS_CNTRL pin
- Fixed time after one or a group of parent rails achieves regulation
- Fixed time after a designated GPI has reached a user-specified state
- Any combination of the previous options

The maximum TON_DELAY time is 3276ms.

Turn-off Sequencing

The following sequence-off options are supported for each rail:

- Monitor only – do not sequence-off
- Fixed delay time after a PMBus OPERATION command to turn off
- Fixed delay time after deassertion of the PMBUS_CNTRL pin
- Fixed delay time in response to an Under Voltage, Over Voltage, Under Current, Over Current, Under Temperature, Over Temperature or Max Turn On fault on the rail
- Fixed delay time in response to a fault on a different rail when set as a Fault Shutdown Slave to the faulted rail
- Fixed delay time in response to a GPIO reaching a user-specified state

The maximum TOFF_DELAY time is 3276ms.

Sequencing Configuration Options

In addition to the turn-on and turn-off sequencing options described above, the time between when a rail is enabled and when the monitored rail voltage must reach its Power Good On setting can be configured using Max Turn On (TON_MAX_FAULT_LIMIT). Max Turn On can be set in 1ms increments. A value of 0ms means that there is No Limit and the device can try to turn on the output voltage indefinitely.

Rails can be configured to turn off immediately or to sequence-off according to user-defined delay times. A sequenced shutdown is configured by selecting appropriate Turn Off Delay (TOFF_DELAY) times for each rail. The Turn Off Delay times begin when the PMBUS_CNTRL pin is deasserted, when the PMBus OPERATION command is used to give a Soft Stop command, or when a fault occurs on a rail that has other rails set as Fault Shutdown Slaves.

Shut-downs on one rail can initiate shut-downs of other rails or controllers. In systems with multiple UCD90120’s, it is possible for each controller to be both a master and a slave to another controller.

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VOLTAGE MONITORING

Up to 13 voltages can be monitored using the analog input pins. The input voltage range is 0V–2.5V for MON pins 1-6, 59, 62 and 63. Pins 50, 52, 54 and 56 can measure down to 0.2V. Any voltage between 0V and 0.2V on these pins will read as 0.2V. External resistors can be used to attenuate voltages higher than 2.5V.

The ADC operates continuously, requiring 3.89µs to convert a single analog input and 54.5µs to convert all 14 of the analog inputs, including the on-board temperature sensor. Each rail is sampled by the sequencing and monitoring algorithm every 200µs. The maximum source impedance of any sampled voltage should be less than 4kΩ. The source impedance limit is particularly important when a resistor divider network is used to lower the voltage applied to the analog input pins.

MON pins selected for Rail 1 through Rail 6 have optional digital hardware comparators, which can be used to achieve faster fault responses. Each hardware comparator has two thresholds (one UV and one OV) as opposed to four software thresholds. The hardware comparators respond to UV or OV conditions in about 80µs and can be used to disable rails or assert GPOs. The only fault response available for the hardware comparators is to shutdown immediately.

An internal 2.5V reference is used by the ADC. The ADC reference has a tolerance of ±0.5% between 0°C and 125°C and a tolerance of ±1% between –40°C and 125°C. An external voltage divider is required for monitoring voltages higher than 2.5V. The nominal rail voltage and the external scale factor can be entered into the Fusion GUI and are used to report the actual voltage being monitored instead of the ADC input voltage. The nominal voltage is used to set the range and precision of the reported voltage according to Table 1.

Table 1. Voltage Range and Resolution

VOLTAGE RANGE (Volts)		RESOLUTION (millivolts)
0	127.99805	1.95313
0	63.99902	0.97656
0	31.99951	0.48828
0	15.99976	0.24414
0	7.99988	0.12207
0	3.99994	0.06104
0	1.99997	0.03052
0	0.99998	0.01526

Although the monitor results can be reported with a resolution of about 15µV, the real conversion resolution of 610µV is fixed by the 2.5V reference and the 12-bit ADC.

The MON pins can directly measure voltages but each input can be defined as a voltage, current or temperature. A single rail can include all three measurement types, each monitored on separate MON pins. If a rail has both voltage and current assigned to it, then power can be calculated and reported for the rail. Digital filtering applied to each MON input depends on the type of signal. Voltage inputs have no filtering. Current inputs have a low-pass filter with a time constant of about 1 second. Temperature inputs have a low-pass filter with a time constant of about 12.4 seconds.

CURRENT MONITORING

Current can be monitored using the analog inputs. External circuitry must be used in order to first convert the current to a voltage within the range of the UCD90120 MONx input being used.

If a monitor input is configured as a current, the measurements are smoothed by a sliding average digital filter with a time constant of approximately 1 second. The filter reduces the probability of false fault detections, and introduces a small delay to the current reading. If a rail is defined with a voltage monitor and a current monitor, then monitoring for under-current warnings begins once the rail voltage reaches POWER_GOOD_ON. If the rail does not have a voltage monitor, then current monitoring will begin after TON_DELAY.

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The device supports multiple PMBus commands related to current, including READ_IOUT which reads external currents from the MON pins; IOUT_OC_FAULT_LIMIT which sets the over current fault limit; IOUT_OC_WARN_LIMIT which sets the over current warning limit; and IOUT_UC_FAULT_LIMIT which sets the under current fault limit. The UCD90120 PMBus Command Reference contains a detailed description of how current fault responses are implemented using PMBus commands.

IOUT_CAL_GAIN is a PMBus command that allows the scale factor of an external current sensor and any amplifiers or attenuators between the current sensor and the MON pin to be entered by the user in milliohms. IOUT_CAL_OFFSET is the current that results in 0V at the MON pin. The combination of these PMBus commands allows current to be reported in Amps.

TEMPERATURE MONITORING AND INTERNAL TEMPERATURE SENSOR

Temperature can be monitored using the analog inputs. External circuitry must be used in order to first convert the temperature to a voltage within the range of the UCD90120 MONx input being used.

If an input is configured as a temperature, the measurements are smoothed by a sliding average digital filter with a time constant of approximately 12.4 seconds. The filter reduces the probability of false fault detections, and introduces a small delay to the temperature reading. The internal device temperature is measured using a silicon diode sensor with an accuracy of ±5°C and is also monitored using the ADC. Temperature monitoring begins immediately after reset and initialization.

The device supports multiple PMBus commands related to temperature, including READ_TEMPERATURE_1 which reads the internal temperature; READ_TEMPERATURE_2 which reads external temperatures; and OT_FAULT_LIMIT which sets the over temperature fault limit. The UCD90120 PMBus Command Reference contains a detailed description of how temperature fault responses are implemented using PMBus commands.

TEMPERATURE_CAL_GAIN is a PMBus command that allows the scale factor of an external temperature sensor and any amplifiers or attenuators between the temperature sensor and the MON pin to be entered by the user in °C/V. TEMPERATURE_CAL_OFFSET is the temperature that results in 0V at the MON pin. The combination of these PMBus commands allows temperature to be reported in degrees Celsius.

FAULT RESPONSES AND ALARM PROCESSING

Monitored rails have a software window comparator with two programmable warning levels (UV and OV) and two programmable fault levels (UV and OV). When any monitored voltage goes outside of the warning or fault windows, or when a current, temperature or any other recognized faults occurs, the PMBALERT# pin is asserted immediately and the appropriate bits are set in the PMBus status registers (Figure 9). Detailed descriptions of the status registers are provided in the *UCD90120 PMBus Command Reference*and the *PMBus_Specification_Part_II_Rev_1-1_20070205.*

A programmable glitch filter can be enabled or disabled for each MON input. A glitch filter for an input defined as a voltage can be set between 0 and 51ms with 200μs resolution. A glitch filter for an input defined as a current or temperature can be between 0 and 25.5 seconds with 100ms resolution. The longer time constants are due to the fixed low-pass digital filters associated with current and temperature inputs.

Fault response decisions are based on results from the 12-bit ADC. The device cycles through the ADC results and compares them against the programmed limits. The time to respond to an individual event is determined by when the event occurs within the ADC conversion cycle and the selected fault response.

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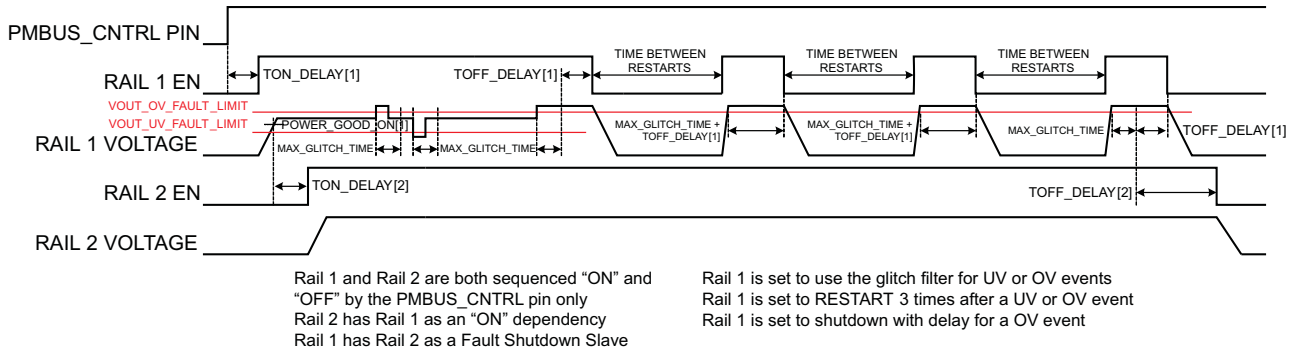


Figure 11. Sequencing and Fault Response Timing

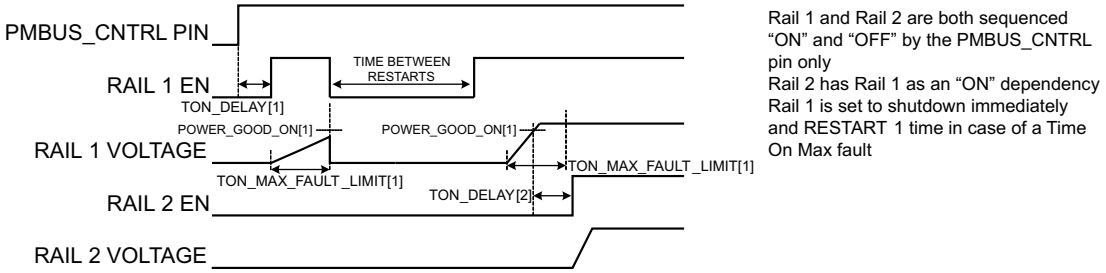


Figure 12. Max Turn On Fault

The configurable fault limits are:

Max Turn On fault– Flagged if a rail that is enabled does not reach the POWER_GOOD_ON limit within the configured time

Under voltage warning– Flagged if a voltage rail drops below the specified UV warning limit after reaching the POWER_GOOD_ON setting

Under voltage fault – Flagged if a rail drops below the specified UV fault limit after reaching the POWER_GOOD_ON setting

Over voltage warning – Flagged if a rail exceeds the specified OV warning limit at any time during startup or operation

Over voltage fault– Flagged if a rail exceeds the specified OV fault limit at any time during startup or operation

Max Turn Off fault– Flagged if a rail that is commanded to shut down does not reach 12.5% of the nominal rail voltage within the configured time.

Faults are more serious than warnings. The PMBALERT# pin is always asserted immediately if a warning or fault occurs. If a warning occurs, the following takes place:

Warning actions

- Immediately assert the PMBALERT# pin
- Status bit gets flagged
- Assert a GPIO pin (optional)
- Warnings are not logged to flash

A number of fault response options can be chosen from:

Fault responses

- *Continue Without Interruption:* Flag the fault and take no action

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Shut Down Immediately: Shut down the faulted rail immediately and Restart according to the rail configuration

— *Shut Down using TOFF_DELAY:* If a fault occurs on a rail, exhaust whatever retries are configured. If the rail does not come back, schedule the shutdown of this rail and all fault shutdown slaves. All selected rails, including the faulty rail, are sequenced-off according to their T_OFF_DELAY times. If Do Not Restart is selected, then sequence off all selected rails when the fault is detected.

Restart

— *Do Not Restart:* Do not attempt to Restart a faulted rail after it has been shut down

— *Restart Up To N Times:* Attempt to Restart a faulted rail up to 14 times after it has been shut down. The time between restarts is measured between when the rail enable pin is deasserted (after any glitch filtering and Turn Off Delay times, if configured to observe them) and then reasserted. It can be set between 0 and 1275ms in 5ms increments.

— *Restart Continuously:* Same as Restart Up To N Times except that the device continues to Restart until the fault goes away, it is commanded off by the specified combination of PMBus OPERATION command and PMBUS_CNTRL pin status, or power is removed from the device.

— *Shut Down Rails and Sequence On:* Shut down selected rails immediately or after Continue Operation time is reached and then sequence-on those rails using Turn On Delay times

SHUT DOWN ALL RAILS AND SEQUENCE ON

In response to a fault, the UCD90120 can be configured to turn off a set of rails and then sequence them back on. To sequence all rails in the system, then all rails must be selected as Fault Shutdown Slaves of the faulted rail. If the faulted rail is set to Stop Immediately or Stop With Delay, then the rails designated as Fault Shutdown Slaves behave the same way. Shut Down All Rails and Sequence On will not be performed until retries are exhausted for a given fault.

While waiting for the rails to turn off, an error is reported if any of the rails reaches its TOFF_MAX_WARN_LIMIT. There is a configurable option to continue with the re-sequencing operation if this occurs. After the faulted rail and Fault Shutdown Slaves sequence off, the UCD90120 will wait for a programmable delay time between 0 and 1275ms in increments of 5ms and then sequence on the faulted rail and Fault Shutdown Slaves according to the start-up sequence configuration. This will be repeated until the faulted rail and Fault Shutdown Slaves successfully achieve regulation or for a user-selected 1, 2, 3 or 4 times. If the re-sequence operation is successful, the re-sequence counter will be reset if all of the rails that were re-sequenced maintain normal operation for one second.

Once Shut Down All Rails and Sequence On begins, any faults on the Fault Shutdown Slave rails will be ignored. If there are two or more simultaneous faults with different Fault Shutdown Slaves the more conservative action is taken. For example, if a set of rails is already on its second re-sequence, and the device is configured to re-sequence three times, and another set of rails enters the re-sequence state, that second set of rails will only be re-sequenced once. Another example – if one set of rails is waiting on all of its rails to shutdown so that it can resequence, and another set of rails enters the re-sequence state, the device will now wait for all rails from both sets to shutdown before re-sequencing.

GPIOs

The UCD90120 has 22 GPIO pins that can function as either inputs or outputs. Each GPIO has configurable output mode options including open-drain or push-pull outputs that can be actively driven to 3.3V or ground. There are an additional four pins that can be used as either inputs or PWM outputs but not as GPOs. Table 2 lists possible uses for the GPIO pins and the maximum number of each type for each use. GPIO pins can be dependents in sequencing and alarm processing. They can also be used for system level functions such as external interrupts, power goods, resets, or cascading of multiple devices. GPOs can be sequenced up or down by configuring a rail without a MON pin but with a GPIO set as an Enable.

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Table 2. GPIO Pin Configuration Options

PIN NAME	PIN#	RAIL EN (12 MAX)	GPI (8 MAX)	GPO (12 MAX)	PWM OUT (12 MAX)	MARGIN PWM (12 MAX)
FPWM1/GPIO5	17	X	X	X	X	X
FPWM2/GPIO6	18	X	X	X	X	X
FPWM3/GPIO7	19	X	X	X	X	X
FPWM4/GPIO8	20	X	X	X	X	X
FPWM5/GPIO9	21	X	X	X	X	X
FPWM6/GPIO10	22	X	X	X	X	X
FPWM7/GPIO11	23	X	X	X	X	X
FPWM8/GPIO12	24	X	X	X	X	X
GPI1/PWM1	31		X		X	X
GPI2/PWM2	32		X		X	X
GPI3/PWM3	42		X		X	X
GPI4/PWM4	41		X		X	X
GPIO1	11	X	X	X		
GPIO2	12	X	X	X		
GPIO3	13	X	X	X		
GPIO4	14	X	X	X		
GPIO13	25	X	X	X		
GPIO14	29	X	X	X		
GPIO15	30	X	X	X		
GPIO16	33	X	X	X		
GPIO17	34	X	X	X		
GPIO18	35	X	X	X		
TCK/GPIO19	36	X	X	X		
TDO/GPIO20	37	X	X	X		
TDI/GPIO21	38	X	X	X		
TMS/GPIO22	39	X	X	X		

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GPI Special Functions

Figure 13 lists and describes five special input functions that GPIs can be used for. There can be no more than one pin assigned to each of these functions.

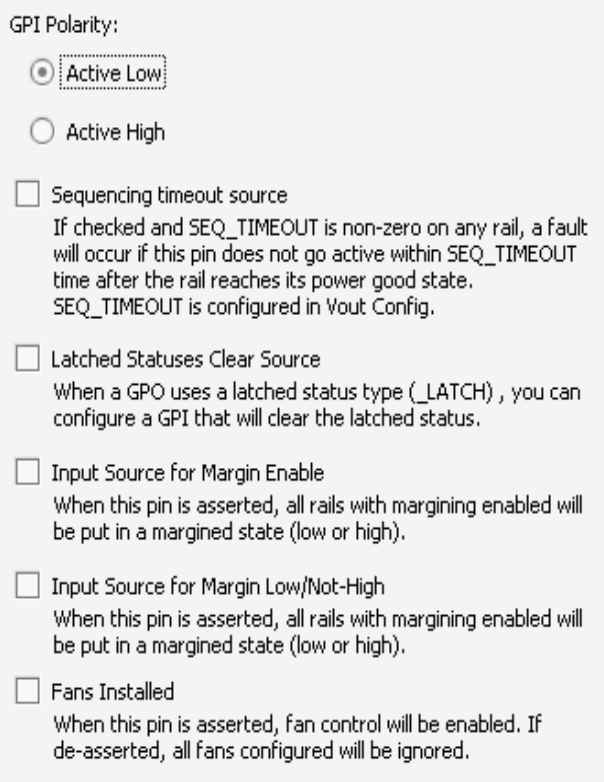


Figure 13. GPI Configuration – Special Input Functions

PWM Outputs

Pins 17-24 can be configured as FPWMs. The frequency range is 15.259 kHz to 125 MHz. FPWMs can be configured as Closed Loop Margining outputs or general purpose PWMs.

Any FPWM pin not used as a PWM output can be configured as a GPIO. One FPWM in a pair can be used as a PWM output and the other pin can be used as a GPO. The FPWM pins are actively driven low from reset when used as GPOs.

The frequency settings for the FPWMs apply to pairs of pins:

- FPWM1 and FPWM2 – same frequency
- FPWM3 and FPWM4 – same frequency
- FPWM5 and FPWM6 – same frequency
- FPWM7 and FPWM8 – same frequency

Pins 31, 32, 41 and 42 can be used as GPIs or PWM outputs.

If configured as PWM outputs, then limitations apply:

- PWM1 has a fixed frequency of 10 kHz
- PWM2 has a fixed frequency of 1 kHz
- PWM3 and PWM4 frequencies can be 0.93 Hz to 7.8125 MHz.

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Power Supply Enables

Each GPIO can be configured as a Rail Enable pin with either active low or active high polarity. Output mode options include open-drain or push-pull outputs that can be actively driven to 3.3V or ground. During reset, the GPIO pins will be high impedance except for the FPWM/GPIO pins 17-24, which will be driven low. External pulldown or pullup resistors can be tied to the Enable pins to hold the power supplies off during reset. The UCD90120 can support a maximum of 12 Enable pins.

Cascading Multiple Devices

A GPIO pin can be used to coordinate multiple controllers by using it as a Power Good output from one device and connecting it to the PMBUS_CNTRL input pin of another. This imposes a master/slave relationship between multiple devices. During startup, the slave controllers will initiate their start sequences after the master has completed its start sequence and all rails have reached regulation voltages. During shutdown, as soon as the master starts to sequence-off it will send the shut-down signal to its slaves.

A shutdown on one or more of the master rails can initiate shutdowns of the slave devices. The master shutdowns can be initiated intentionally or by a fault condition. This method works to coordinate multiple controllers, but it does not enforce interdependency between rails within a single controller.

The PMBus specification implies that the Power Good signal is active when ALL the rails in a controller are regulating at their programmed voltage. The UCD90120 allows GPIOs to be configured to respond to a desired subset of Power Goods.

GPO Dependencies

GPIOs can be configured as outputs that are based on Boolean combinations of up to four AND's all OR'd together (Figure 14). Inputs to the logic blocks can include GPIs and rail status flags. One rail status type is selectable as an input for each AND gate in a Boolean block. For a selected rail status, the status flags of all active rails can be included as inputs to the AND gate. "_LATCH" rails status types stay asserted until cleared by a MFR PMBus command or by a specially configured GPI pin. The different rail status types are shown in Figure 16. Refer to the *UCD90120 PMBus Command Reference* for complete definitions of rail status types.

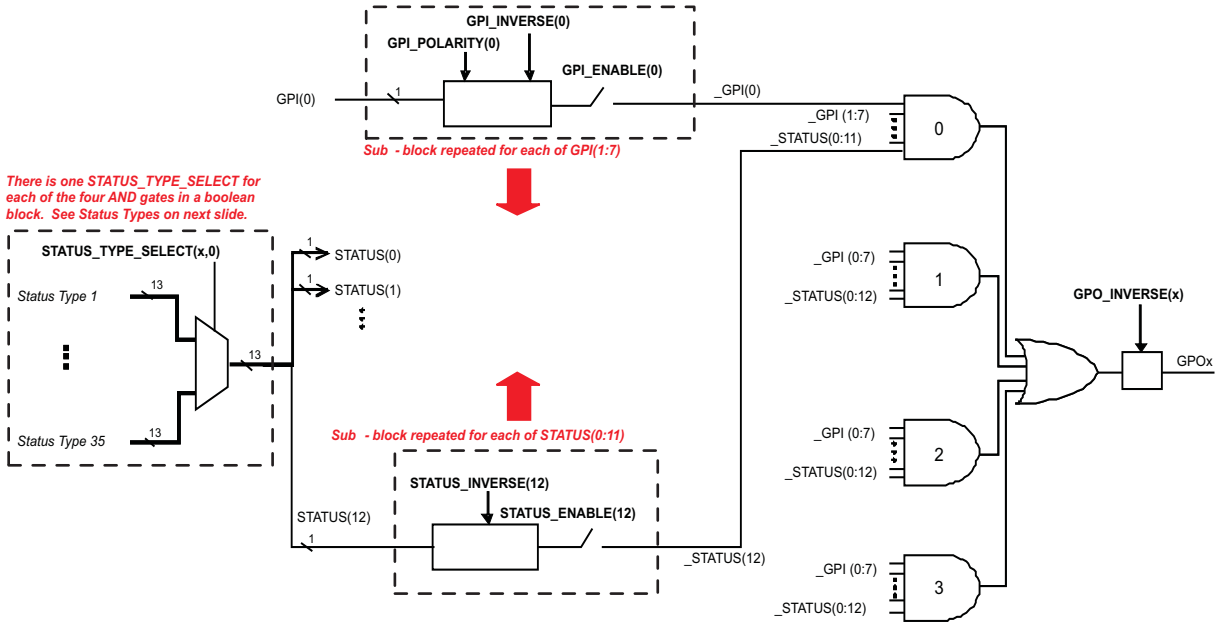


Figure 14. Boolean Logic Combinations

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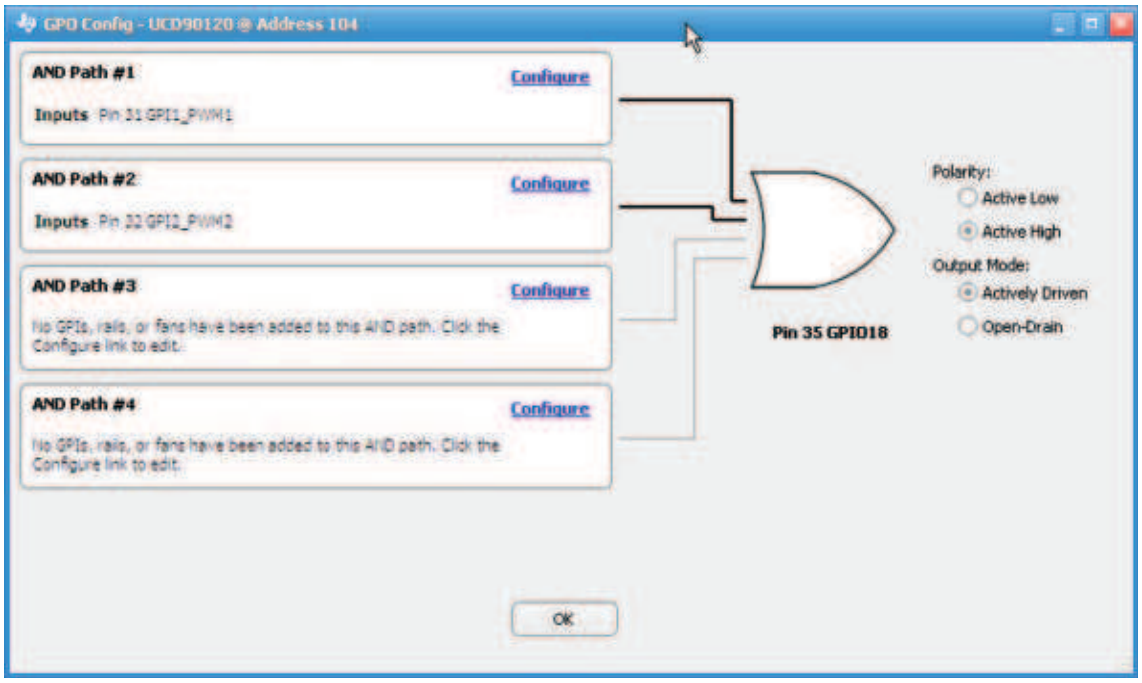


Figure 15. Fusion Boolean Logic Builder

1.	POWER_GOOD(0:12)
2.	VOUT_OV_FAULT(0:12)
3.	VOUT_OV_FAULT_LATCH(0:12)
4.	VOUT_OV_WARN(0:12)
5.	VOUT_OV_WARN_LATCH(0:12)
6.	VOUT_UV_WARN(0:12)
7.	VOUT_UV_WARN_LATCH(0:12)
8.	VOUT_UV_FAULT(0:12)
9.	VOUT_UV_FAULT_LATCH(0:12)
10.	VOUT_TON_FAULT(0:12)
11.	VOUT_TON_FAULT_LATCH(0:12)
12.	VOUT_TOFF_WARN(0:12)
13.	VOUT_TOFF_WARN_LATCH(0:12)
14.	IOUT_OC_FAULT(0:12)
15.	IOUT_OC_FAULT_LATCH(0:12)
16.	IOUT_OC_WARN(0:12)
17.	IOUT_OC_WARN_LATCH(0:12)
18.	IOUT_UC_FAULT(0:12)
19.	IOUT_UC_FAULT_LATCH(0:12)
20.	TEMP_OT_FAULT(0:12)
21.	TEMP_OT_FAULT_LATCH(0:12)
22.	TEMP_OT_WARN(0:12)
23.	TEMP_OT_WARN_LATCH(0:12)
24.	INPUT_VIN_OV_FAULT(0:12)
25.	INPUT_VIN_OV_FAULT_LATCH(0:12)
26.	INPUT_VIN_OV_WARN(0:12)
27.	INPUT_VIN_OV_WARN_LATCH(0:12)
28.	INPUT_VIN_UV_WARN(0:12)
29.	INPUT_VIN_UV_WARN_LATCH(0:12)
30.	INPUT_VIN_UV_FAULT(0:12)
31.	INPUT_VIN_UV_FAULT_LATCH(0:12)
32.	MFR_SEQ_TIMEOUT(0:12)
33.	MFR_SEQ_TIMEOUT_LATCH(0:12)

Figure 16. Rail status types

MARGINING

Margining is used in product validation testing to verify that the complete system works properly over all conditions including minimum and maximum power supply voltages, load range, ambient temperature range and other relevant parameter variations. Margining can be controlled over PMBus using the OPERATION command or by configuring two GPIO pins as Margin EN and Margin UP/DOWN inputs. The MARGIN_CONFIG command in the UCD90120 PMBus Command Reference describes different available margining options including ignoring faults while margining and using closed-loop margining to trim the power supply output voltage one time at power up.

Open-loop margining is done by connecting a power supply feedback node to ground through one resistor and to

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V_{CC} or the power supply input voltage through another resistor. The power supply regulation loop responds to the change in feedback node voltage by increasing or decreasing the power supply output voltage to return the feedback voltage to the original value. The voltage change is determined by the fixed resistor values and the voltage at V_{CC} and ground. Two GPIO pins must be configured as outputs for connecting resistors from the feedback node of each power supply to V_{CC} or ground.

Closed-loop margining uses a PWM or FPWM output for each power supply that is being margined. An external RC network converts the FPWM pulse train into a DC margining voltage. The margining voltage is connected to the appropriate power supply feedback node through a resistor. The power supply output voltage is monitored and the margining voltage is controlled by adjusting the PWM duty cycle until the power supply output voltage reaches the Margin Low and Margin High voltages set by the user.

SYSTEM RESET SIGNAL

The UCD90120 can generate a programmable System Reset pulse as part of Sequence On. The pulse is created by programming a GPIO to remain deasserted until the voltage of a particular rail or combination of rails reach their respective POWER_GOOD_ON levels plus a programmable delay time. The System Reset pulse width can be programmed as shown in Table 3.

Table 3. System Reset Pulse Width

Pulse Width
0 ms
1 ms
2 ms
4 ms
8 ms
16 ms
32 ms
64 ms
128 ms
256 ms
512 ms
1.02 sec
2.05 sec
4.10 sec
8.19 sec
16.38 sec
32.8 sec

WATCH DOG TIMER

A GPI and GPO can be configured as a Watch Dog Timer (WDT). The WDT can be independent of power supply sequencing or tied to a GPIO configured to provide a System Reset signal. The WDT can be reset by toggling a Watchdog Input (WDI) pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C.

The WDT can be active immediately at power up or set to wait while the system initializes. Table 4 lists the programmable wait times before the initial timeout sequence begins.

Table 4. WDT Initial Wait Time

WDT INITIAL WAIT TIME
0 ms
100 ms
200 ms
400 ms

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Table 4. WDT Initial Wait Time (continued)

WDT INITIAL WAIT TIME
800 ms
1.6 sec
3.2 sec
6.4 sec
12.8 sec
25.6 sec
51.2 sec
102 sec
205 sec
410 sec
819 sec
1638 sec

The watchdog timeout is programmable from 0 to 2.55s with a 10ms step size. If the WDT times out, the UCD90120 can assert a GPIO pin configured as WDO that is separate from a GPIO defined as System Reset pin or it can generate a System Reset pulse. After a timeout, the WDT is restarted by toggling the WDI pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C.

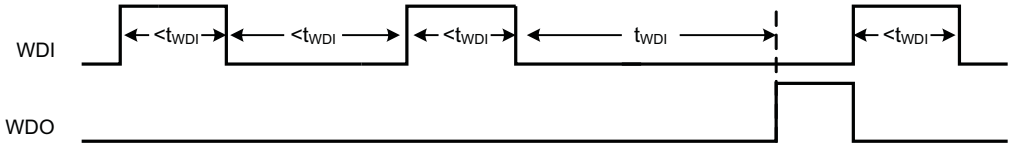


Figure 17. Timing of GPIOs Configured for Watch-Dog Timer Operation

DATA AND ERROR LOGGING TO FLASH MEMORY

The UCD90120 can log faults and the number of device resets to flash memory. Peak voltage, current and temperature measurements are also stored for each rail. To reduce stress on the flash memory, a 30-second timer is started if a measured value exceeds the previously logged value. Only the highest value from the 30-second interval is written from RAM to flash.

Multiple faults can be stored in flash memory and can be accessed over PMBus to help debug power supply bugs or failures. Each logged fault includes:

- Rail number
- Fault type
- Fault time since previous device reset
- Last measured rail voltage

The total number of device resets is also stored to flash memory. The value can be reset using PMBus.

With the Brownout function enabled, the run-time clock value, peak monitor values and faults are only logged to flash when a power-down is detected. The device run-time clock value is stored across resets or power cycles unless the Brownout function is disabled, in which case the run-time clock is returned to zero after each reset.

It is also possible to update and calibrate the UCD90120 internal run time clock via a PMBus host. For example, a host processor with a Real Time Clock could periodically update the UCD90120 run time clock to a value that corresponds to the actual date and time. The host must translate the UCD90120 timer value back into the appropriate units based on the usage scenario chosen. Please see the REAL_TIME_CLOCK command in the UCD9012x PMBus Command Reference for more details.

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BROWNOUT FUNCTION

The UCD90120 can be enabled to turn off all non-volatile logging until a brownout event is detected. A brownout event occurs if V_{cc} drops below 2.9V. In order to enable this feature, the user must provide enough local capacitance to deliver up to 80mA for 5ms while maintaining a minimum of 2.6V at the device.

With this feature enabled, the UCD90120 will save faults, peaks, and other log data to SRAM during normal operation of the device. Once a brown out event is detected, all data will be copied from SRAM to Flash. Use of this feature allows the UCD90120 to keep track of a single run time clock that spans device resets or system power down (rather than resetting the run time clock after device reset). It can also improve the UCD90120 internal response time to events since Flash writes will be disabled during normal system operation. This is an optional feature and can be enabled using the MISC_CONFIG command. For more details, please see the UCD9012x PMBus Command Reference.

PMBUS INTERFACE

The PMBus is a serial interface specifically designed to support power management. It is based on the SMBus interface, which is built on the I^2C physical specification. The UCD90120 supports revision 1.1 of the PMBus standard. Wherever possible, standard PMBus commands are used to support the function of the device. Standard PMBus commands can be found in *PMBus_Specification_Part_I_Rev_1_ 0_20050324* and *PMBus_Specification_Part_II_Rev_1-1_20070205*, which can be downloaded from http://pmbus.org/specs.html. Some of the operational and functional descriptions for this datasheet were closely based on the PMBus specification. For unique features of the UCD90120, MFR_SPECIFIC commands are defined to configure or activate those features. These commands are defined in the UCD90120 PMBus Command Reference.

The UCD90120 is PMBus compliant, in accordance with the "Compliance" section of the PMBus specification. The firmware is also compliant with the SMBus 1.1 specification, including support for the SMBus ALERT (SMBALERT#) function. The hardware can support 100kHz and 400kHz operation. Two pins are allocated to decode the PMBus address. At power-up the device applies a bias current to each address detect pin and the voltage on that pin is captured by the internal 12-bit ADC. The PMBus address is calculated as follows.

$$\text{PMBus Address} = 12 \times \text{bin}(V_{AD01}) + \text{bin}(V_{AD00})$$

Where $\text{bin}(V_{AD0x})$ is the address bin for one of 8 address as shown in Table 5. The address bins are defined by the MIN and MAX VOLTAGE RANGE (V). Each bin is a constant ratio of 1.25 from the previous bin. This method maintains the width of each bin relative to the tolerance of standard 1% resistors.

Table 5. PMBus Address Bins

ADDRESS BIN	VPMBus PMBus VOLTAGE RANGE (V)		RPMBus PMBus RESISTANCE (kΩ)
	MIN	MAX	
open	2.226	3.300	
11	1.746	2.225	210
10	1.342	1.746	158
9	1.030	1.341	115
8	0.792	1.030	84.5
7	0.609	0.792	63.4
6	0.468	0.608	47.5
5	0.359	0.467	36.5
4	0.276	0.358	27.4
short	0	0.097	

A low impedance (short) on either address pin that produces a voltage below the minimum voltage will cause the PMBus address to default to address 126 (0x7F). A high impedance (open) on either address pin that produces a voltage above the maximum voltage will also cause the PMBus address to default to address 126 (0x7F).

Address 0 is not used because it is the PMBus General Call address. Addresses 11 and 127 can not be used by this device or any other device that shares the PMBus with it, since those are reserved for manufacturing programming and test. It is recommended that address 126 not be used for any devices on the PMBus since this

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is the address that the UCD90120 defaults to if the address lines are shorted to ground or left open. Other SMBus/PMBus addresses have been assigned for specific devices. For a system with other types of devices connected to the same PMBus, refer to the SMBus device address assignments table in Appendix C of the latest version of the System Management Bus (SMBus) specification. The SMBus specification can be downloaded at http://smbus.org/specs/smbus20.pdf.

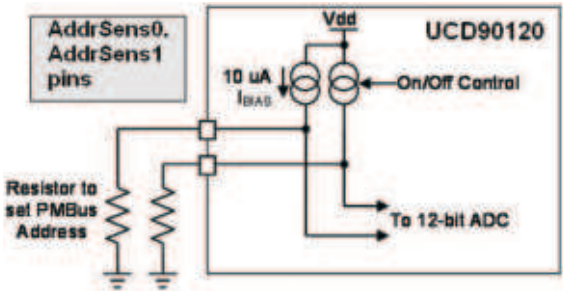


Figure 18. PMBus Address Detection Method

HIGH VOLTAGE SUPPLY VOLTAGE REGULATOR

The UCD90120 requires 3.3V to operate. It can be provided directly on the various V_{33x} pins, or it can be generated from a higher voltage using a built-in series regulator and an external transistor. The external transistor must be an NPN device with a beta of at least 40 and a V_{CE} rating appropriate for the high supply voltage. Figure 19 shows the typical circuit using the external series pass transistor. The NPN emitter output becomes the 3.3 V supply for the chip. A 4.7µF bypass capacitor is required to stabilize the series regulator.

Some circuits in the device require 1.8V, which is generated internally from the 3.3V supply. This voltage requires a 0.1µF to 1µF bypass capacitor from BPCAP to ground.

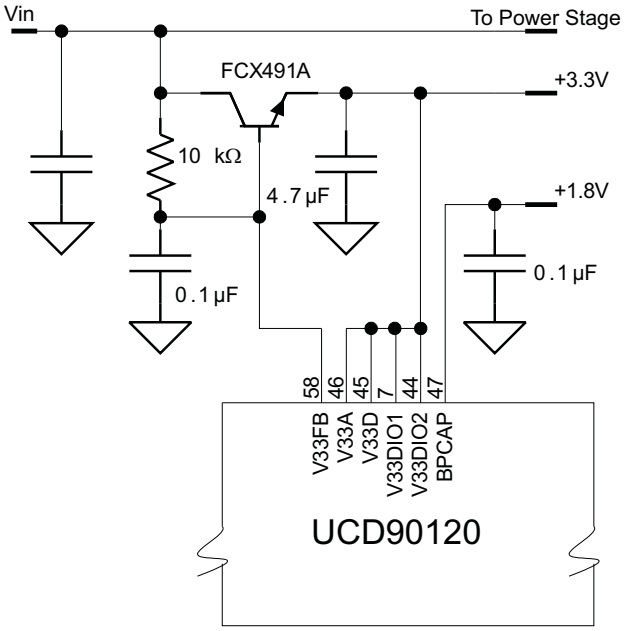


Figure 19. High-Voltage Supply With External Transistor

DEVICE RESET

The UCD90120 has an integrated power-on reset (POR) circuit which monitors the supply voltage. At power-up, the POR detects the V_{33D} rise. When V_{33D} is greater than V_{RESET} the device comes out of reset.

The device can be forced into the reset state by an external circuit connected to the nRESET pin. A logic low voltage on this pin for longer than t_{RESET} holds the device in reset. It comes out of reset within 1ms after nRESET is released and can return to a logic high level. To avoid an erroneous trigger caused by noise, a pull up resistor to 3.3V is recommended.

Anytime the device comes out of reset it begins an initialization routine that lasts about 20ms. During the initialization routine, the FPWM pins are held low and all other GPIO and GPI pins are open circuit. At the end of initialization, the device begins normal operation as defined by the device configuration.

DEVICE CONFIGURATION AND PROGRAMMING

From the factory, the device contains the sequencing and monitoring firmware. It is also configured so that all GPOs are high-impedance with no sequencing or fault response operation. See *Configuration Programming of UCD Devices* available at www.ti.com for full UCD90120 configuration details.

After the user has designed a configuration file using Fusion, there are three general device configuration programming options. Devices can be programmed in-circuit by a host microcontroller using PMBus commands over I^2C to configure the device (see the UCD90120 PMBus Command Reference).

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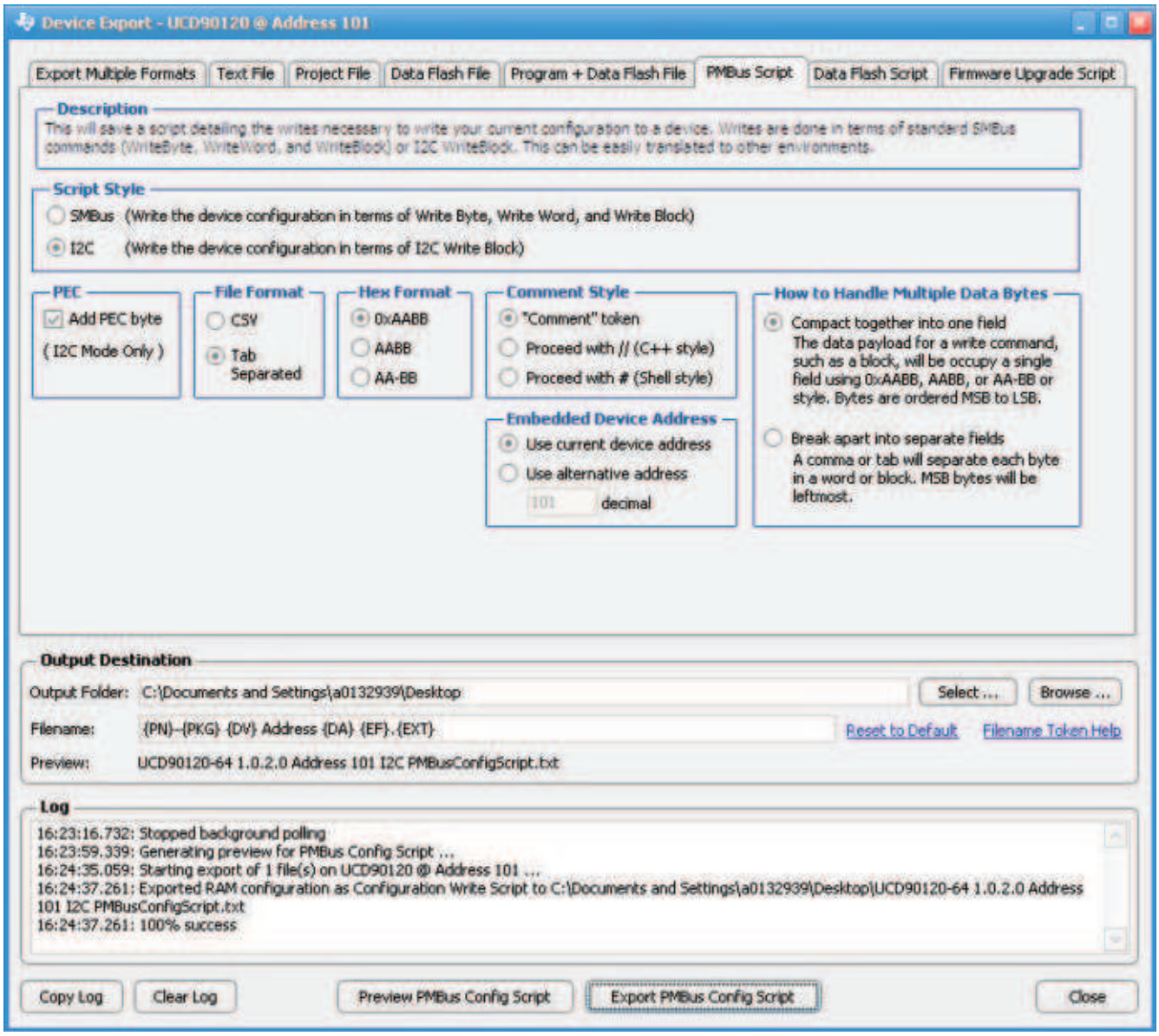


Figure 20. Fusion PMBus Configuration Script Export Tool

Each parameter write replaces the data in the associated memory (RAM) location. After all the required configuration data has been sent to the device, it is transferred to the associated non-volatile memory (data flash) by issuing a special command, STORE_DEFAULT_ALL. This is how the Fusion GUI normally reads and writes a device configuration.

Fusion can create a PMBus or I2C command script file that can be used by the I2C master to configure the device (Figure 21). An example of a partial command script file is shown here:

```
Comment    Format=Tab; Hex=CoderUpper; BreakOutBytes=False [DO NOT REMOVE THIS LINE IF YOU WANT TO
IMPORT USING THE FUSION GUI]
Comment    SMBus Fields are Request,Address,Command,Data
Comment    For reads, the last field is what is expected back from the device
Comment    Write MONITOR_CONFIG [MFR 05] Pin 1 MON1: Rail #1, Type Voltage; Pin 2 MON2: Rail #2, Type
Voltage; Pin 3 MON3: Rail #3, Type Voltage; Pin 4 MON4: Rail #4, Type Voltage; Pin 5 MON5: Rail #5,
Type Voltage; Pin 6 MON6: Rail #6, Type Voltage; Pin 59 MON7: Rail #7, Type Voltage; Pin 62 MON8: Rail
#8, Type Voltage; Pin 63 MON9: Rail #9, Type Voltage; Pin 50 MON10: Rail #10, Type Voltage; Pin 52
MON11: Rail #11, Type Voltage; Pin 54 MON12: Rail #12, Type Voltage; Pin 56 MON13: Rail #1, Type
Temperature
```

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```
BlockWrite    0x65    0xD5    0x20212223242526272829 2A2B40
Comment    Write GPI_CONFIG [MFR 41] Inputs: <None>
BlockWrite    0x65    0xF9    0x00000000000000000000000000
Comment    Write SEQ_CONFIG [MFR 38,Rail #1] Rail Dep: <None> | Pin Dep: <None> | Fault Dep: <None> |
Enable: Pin 11 GPIO1 ActiveHigh ActivelyDrivenOutput
WriteByte    0x65    0x00    0x00
BlockWrite    0x65    0xF6    0x000000000096
Comment    Write SEQ_CONFIG [MFR 38,Rail #4] Rail Dep: <None> | Pin Dep: <None> | Fault Dep: <None> |
Enable: Pin 14 GPIO4 ActiveHigh ActivelyDrivenOutput
WriteByte    0x65    0x00    0x03
BlockWrite    0x65    0xF6    0x0000000000AE
Comment    Write VOUT_SCALE_MONITOR [Rail #12] 0.500
WriteWord    0x65    0x2A    0x00B2
.
.
.
Comment    Store configuration to data flash
Pause    100    Pausing 100 ms
Comment    Execute STORE_DEFAULT_ALL
SendByte    0x65    0x11
Pause    1000    Pausing 1,000 ms for StoreDefaultAll
```

Another in-circuit programming option is for Fusion to create a data flash image from the configuration file (Figure 21). The image file can be downloaded into the device using I^2C or JTAG. Fusion Tools can be used on board if Fusion can gain ownership of the target board's I2C bus.

Devices can be programmed off board using TI Fusion Tools or a dedicated device programmer. For small runs, a ZIF socketed board with an I^2C header can be used with the standard Fusion GUI or Manufacturing GUI. Fusion can also create a data flash file that can then be loaded into the UCD90120 using a dedicated device programmer.

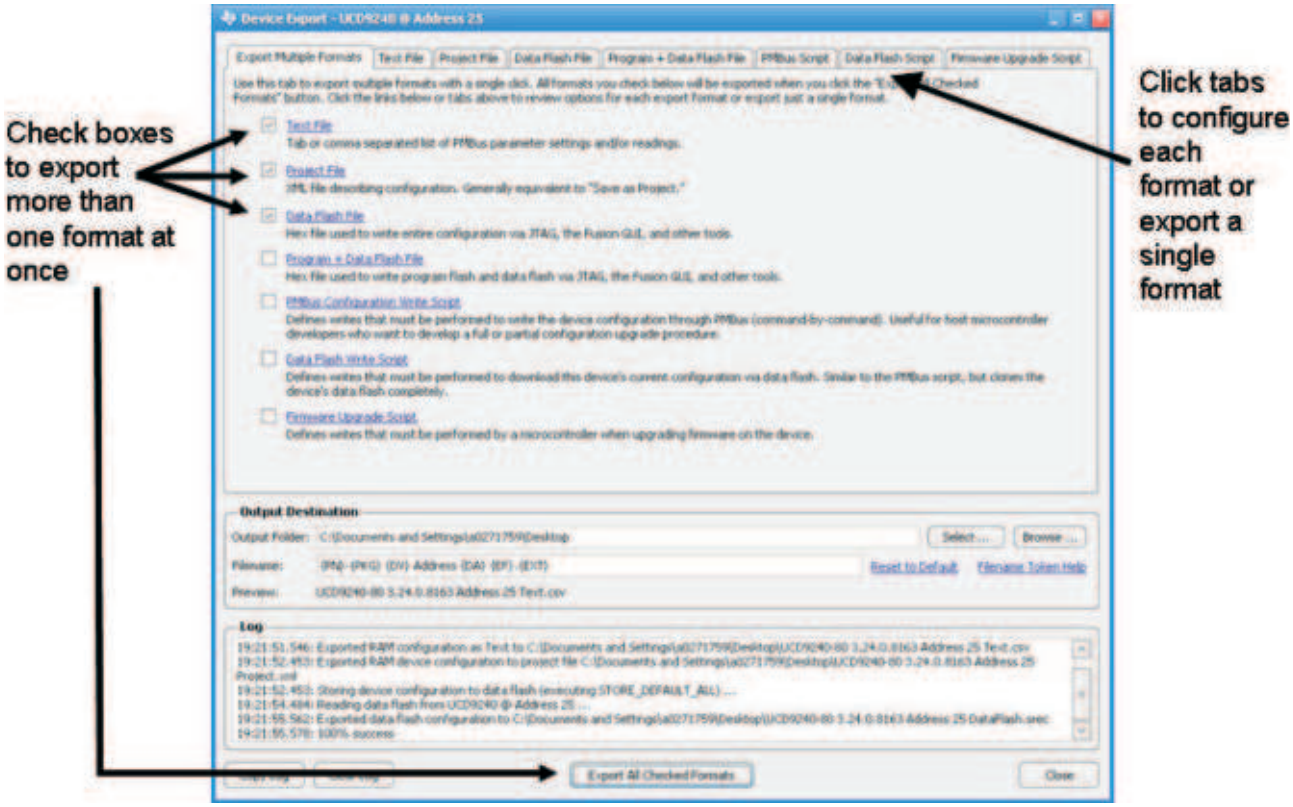


Figure 21. Fusion Device Configuration Export Tool

To configure the device over I^2C or PMBus, the UCD90120 must be powered. The PMBus clock and data pins must be accessible and need to be pulled high to the same V_{dd} supply as the device is powered from with pull-up

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resistors between 1kΩ and 2kΩ. Care should be taken to not introduce additional bus capacitance (< 100pF). The user configuration can be written to data flash using a gang programmer via JTAG or I^2C before the device is installed in circuit. To use I^2C, the clock and data lines must be multiplexed or the device addresses must be assigned by socket. Fusion tools can be used for socket addressing. Pre-programming can also be done using a single device test fixture.

Table 6. Configuration Options

	Data Flash via JTAG	Data Flash via I^2C	PMBus Commands via I^2C
Off-Board Configuration	Data Flash Export	Data Flash Export	Project File I2C/PMBus Script
	Dedicated Programmer	Fusion Tools Dedicated Programmer Microcontroller	Fusion Tools Microcontroller
On-Board Configuration	Data Flash Export	Microcontroller Fusion Tools (with exclusive bus access via USB I2C adapter)	Microcontroller Fusion Tools (with exclusive bus access via USB I2C adapter)
	IC		

The advantages of off-board configuration include:

- Does not require access to device's I^2C bus on board.
- Once soldered on board, full board power is available without further configuration.
- Can be partially reconfigured once the device is mounted.

JTAG INTERFACE

The JTAG port can be used for production programming. Four of the six JTAG pins can also be used as GPIOs during normal operation. Refer to the PIN FUNCTIONS table at the beginning of the document and Table 2 for a list of the JTAG signals and which can be used as GPIOs. The JTAG port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture specification. Boundary scan is not supported on this device.

The JTAG interface can provide an alternate interface for programming the device. It is disabled by default in order to enable the GPIO pins with which it is multiplexed. There are three conditions under which the JTAG interface is enabled:

1. When the ROM_MODE PMBus command is issued
2. On power-up if the Data Flash is blank, allowing JTAG to be used for writing the configuration parameters to a programmed device with no PMBus interaction.
3. When an invalid address is detected at power-up. By shorting one of the address pins to ground, an invalid address can be generated that enables JTAG.

INTERNAL FAULT MANAGEMENT AND MEMORY ERROR CORRECTION (ECC)

The UCD90120 verifies the firmware checksum at each power up. If it does not match, then the device waits for I^2C commands but does not execute the firmware. A device configuration checksum verification is also performed at power up. If it does not match, the factory default configuration is loaded. The PMBALERT# pin is asserted and a flag is set in the status register. The error log checksum validates the contents of the error log to make sure that section of Flash is not corrupted.

There is an internal firmware Watch Dog Timer. If it times out, the device resets so that if the firmware program gets corrupted, the device goes back to a known state. This is a normal device reset so all of the GPIO pins are open drain and the FPWM pins are driven low while the device is in reset. Checks are also done on each parameter that gets passed to make sure it falls within the acceptable range.

Error Correcting Code (ECC) is used to improve data integrity and provide high reliability storage of Data Flash contents. ECC uses dedicated hardware to generate extra check bits for the user data as it is written into the Flash memory. This adds an additional six bits to each 32-bit memory word stored into the Flash array. These extra check bits, along with the hardware ECC algorithm, allow for any single bit error to be detected and corrected when the Data Flash is read.

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APPLICATION INFORMATION

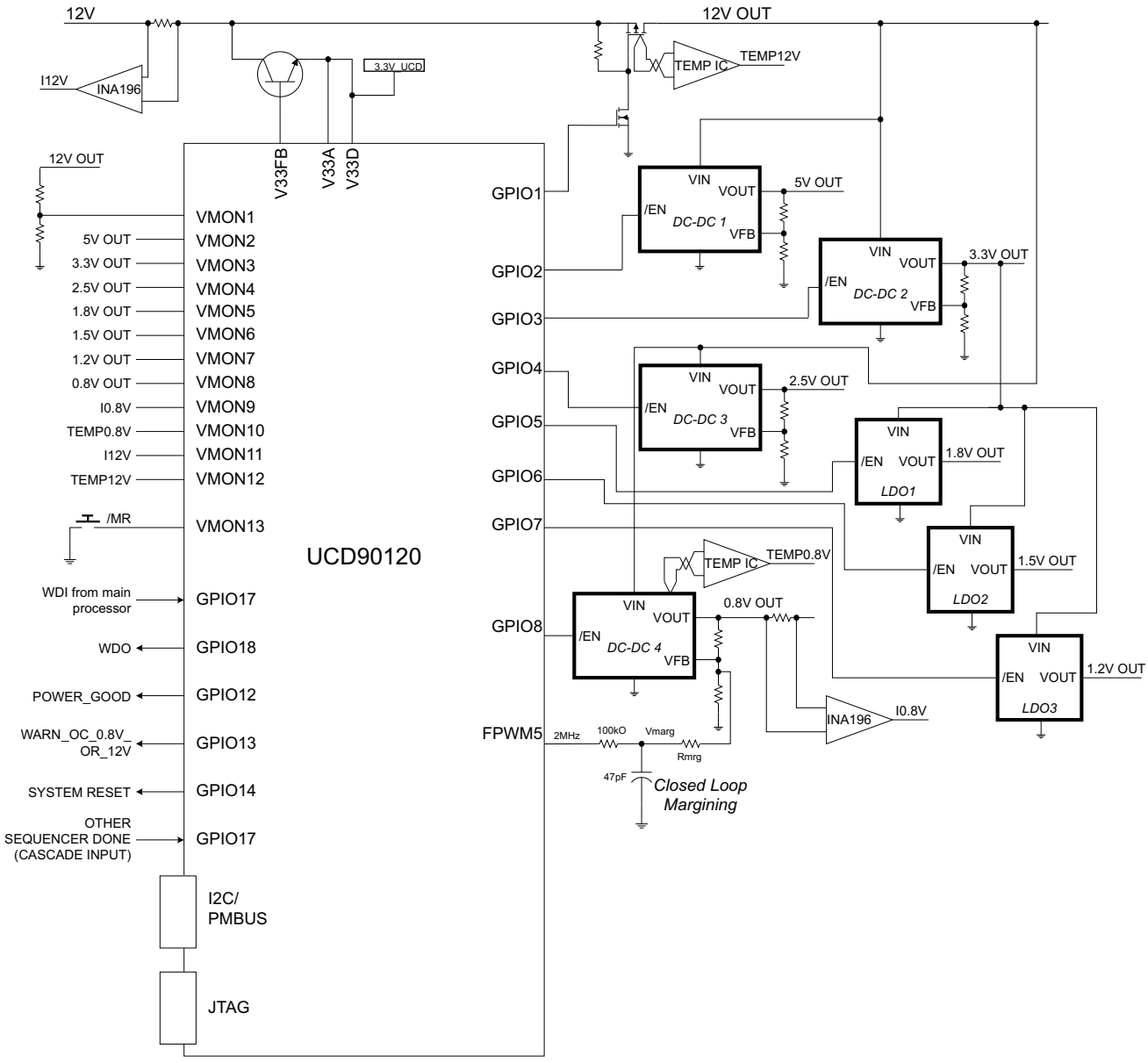


Figure 22. Typical Application Schematic

Layout guidelines

The thermal pad provides a thermal and mechanical interface between the device and the printed circuit board (PCB). While device power dissipation is not of primary concern, a more robust thermal interface can help the internal temperature sensor provide a better representation of PCB temperature. Connect the exposed thermal pad of the PCB to the device V_{SS} pins and provide at least a 4 x 4 pattern of PCB vias to connect the thermal pad and V_{SS} pins to the circuit ground on other PCB layers.

For supply voltage decoupling, provide power supply pin bypass to the device as follows:

- 0.1µF, X7R ceramic in parallel with 0.01µF, X7R ceramic at pin 47 (BPCAP)
- 0.1µF, X7R ceramic in parallel with 4.7µF, X5R ceramic at pin 44 (V_{33D})
- 0.1µF, X7R ceramic at pin 7 (V_{33DIO})
- 0.1µF, X7R ceramic in parallel with 4.7µF, X5R ceramic at pin 46 (V_{33A})

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Depending on use and application of the various GPIO signals used as digital outputs, some impedance control may be desired to quiet fast signal edges. For example, when using the FPWM pins for fan control or voltage margining the pin will be configured as a digital “clock” signal. Route these signals away from sensitive analog signals. It is also good design practice to provide a series impedance of 20-33 ohms at the signal source to slow fast digital edges.

Estimating ADC Reporting Accuracy

The UCD90120 uses a 12-bit ADC and an internal 2.5V reference (V_{REF}) to convert MON pin inputs into digitally reported voltages. The least significant bit (LSB) value is $V_{LSB} = V_{REF}/2^N$ where N = 12, resulting in a VLSB = 610μV. The error in the reported voltage is a function of the ADC linearity errors and any variations in VREF. The total unadjusted error (E_{TUE}) for the UCD90120 ADC is ±5 LSB and the variation of VREF is ±0.5% between 0°C and 125°C and ±1% between –40°C and 125°C. V_{TUE} is calculated as V_{LSB} x E_{TUE}. The total reported voltage error with be the sum of the reference voltage error and V_{TUE}. At lower monitored voltages, V_{TUE} will dominate reported error while at higher monitored voltages the tolerance of V_{REF} will dominate the reported error. Reported error can be calculated using Equation 1 where REFTOL is the tolerance of V_{REF}, V_{ACT} is the actual voltage being monitored at the MON pin and V_{REF} is the nominal voltage of the ADC reference.

$$RPT_{ERR} = \left(\frac{1+REFTOL}{V_{ACT}}\right) \times \left(\frac{V_{REF} \times E_{TUE}}{4096} + V_{ACT}\right) - 1 \quad (1)$$

From Equation 1, for temperatures between 0°C and 125°C if V_{ACT} = 0.5V, then RPT_{ERR} = 1.11%. If V_{ACT} = 2.2V, then RPT_{ERR} = 0.64%. For the full operating temperature range of –40°C to +125°C, if VACT = 0.5V, then RPT_{ERR} = 1.62%. If V_{ACT} = 2.2V, then RPT_{ERR} = 1.14%.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD90120RGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90120
UCD90120RGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90120
UCD90120RGCR.B	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90120
UCD90120RGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90120
UCD90120RGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90120
UCD90120RGCT.B	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD90120

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

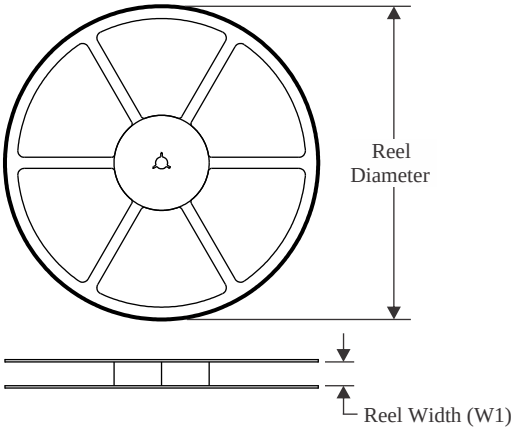
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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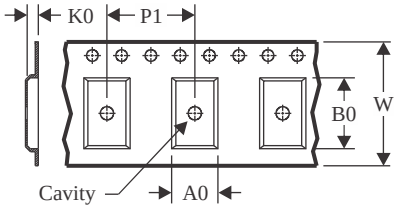
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

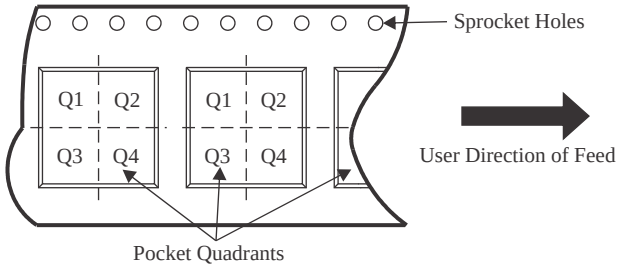


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

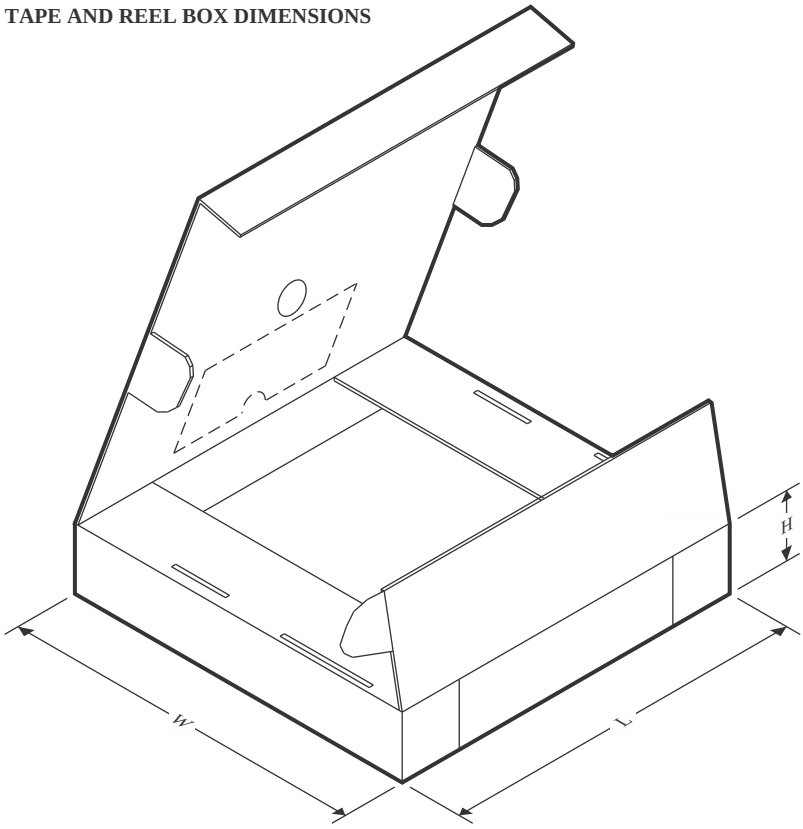
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD90120RGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
UCD90120RGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD90120RGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
UCD90120RGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD90120RGCR	VQFN	RGC	64	2000	353.0	353.0	32.0
UCD90120RGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
UCD90120RGCT	VQFN	RGC	64	250	210.0	185.0	35.0
UCD90120RGCT	VQFN	RGC	64	250	213.0	191.0	35.0

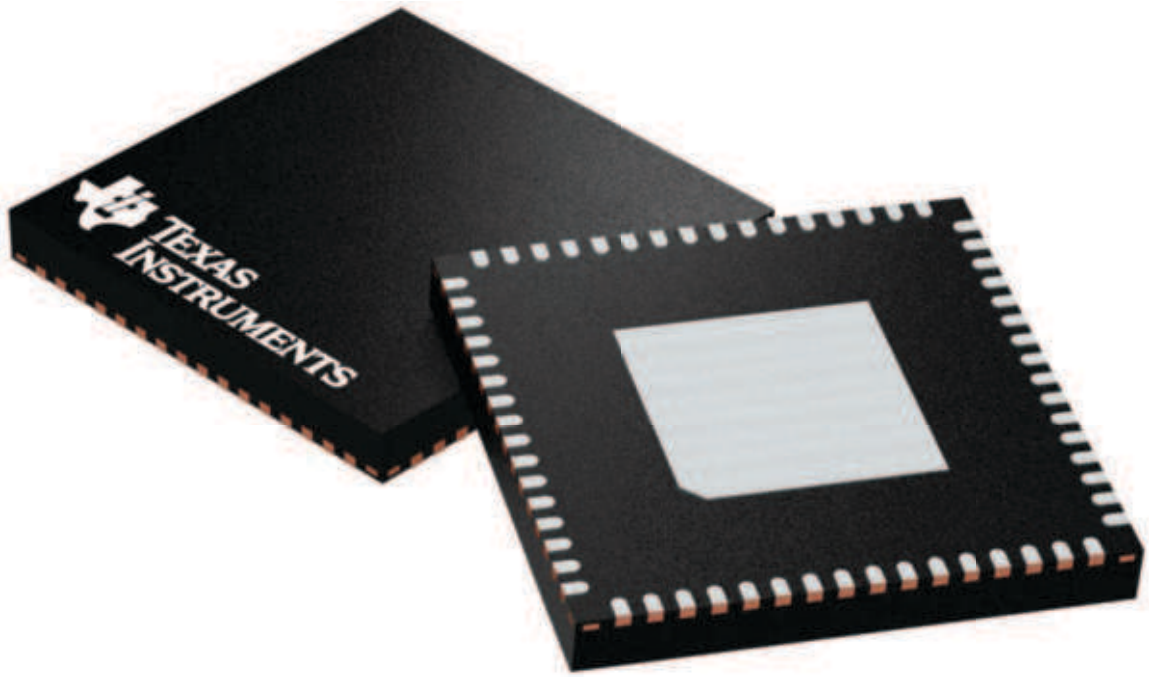
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

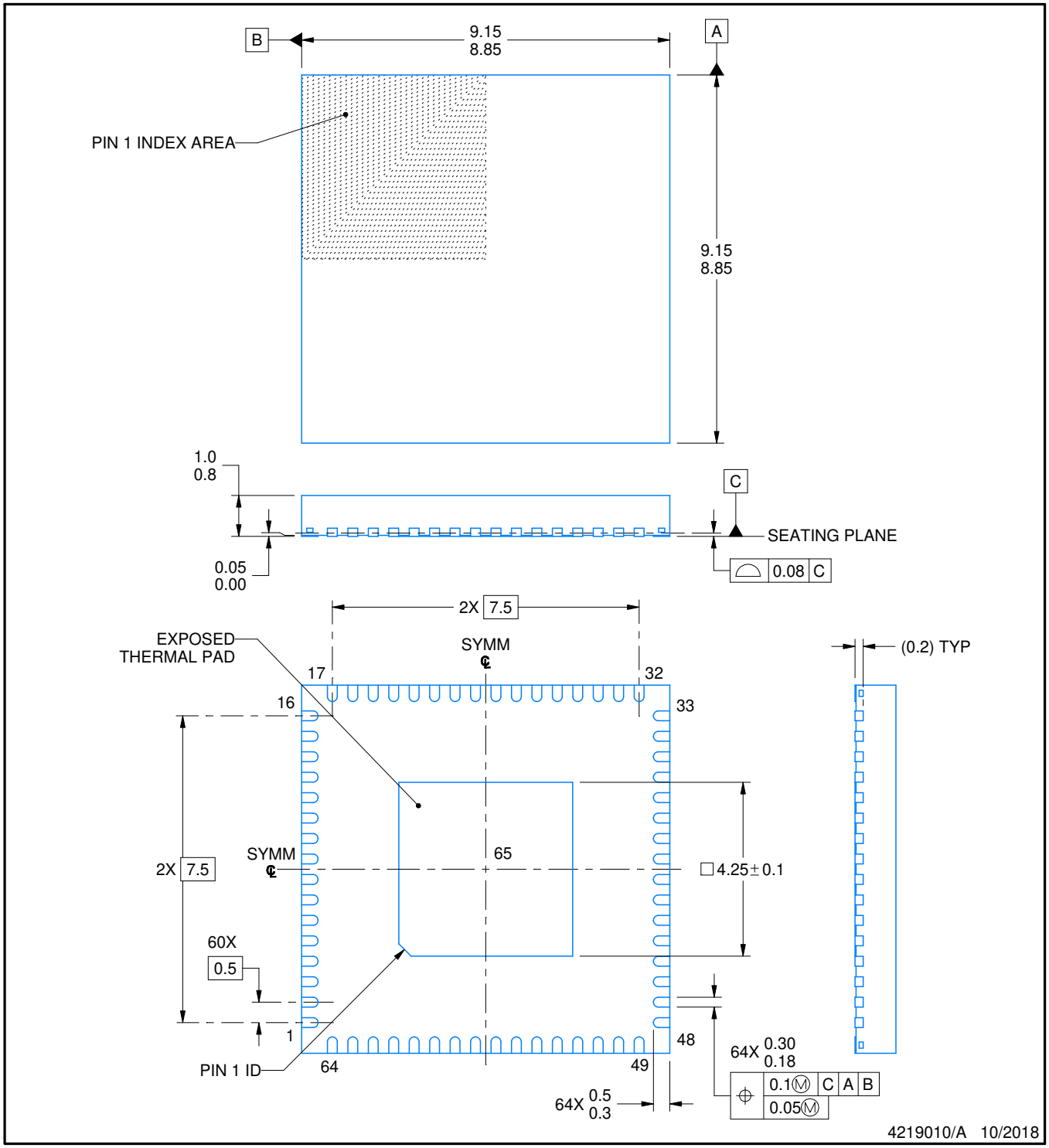
4224597/A

PACKAGE OUTLINE

RGC0064B

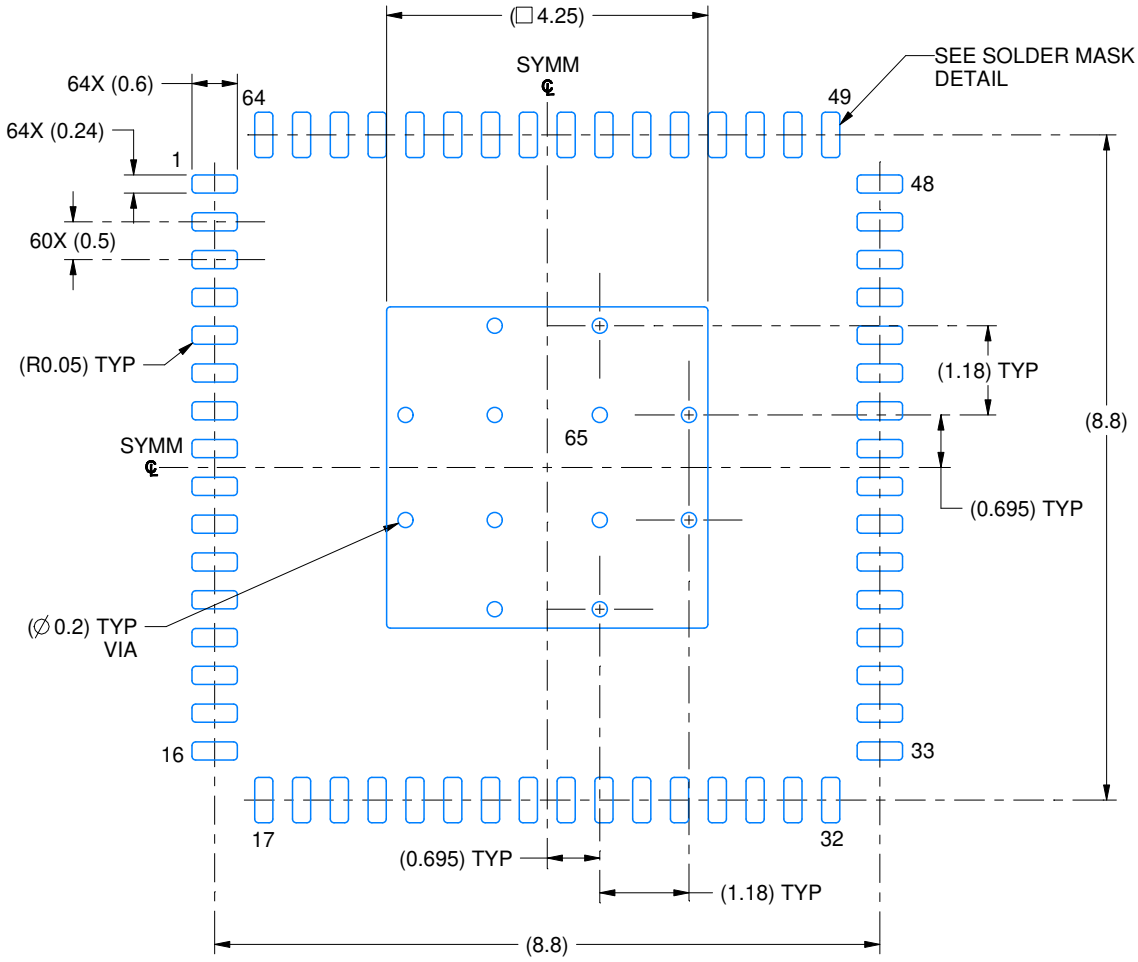
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

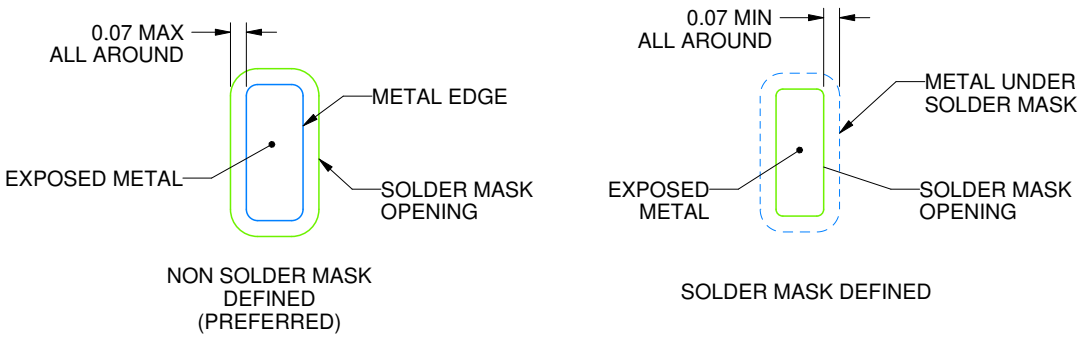


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

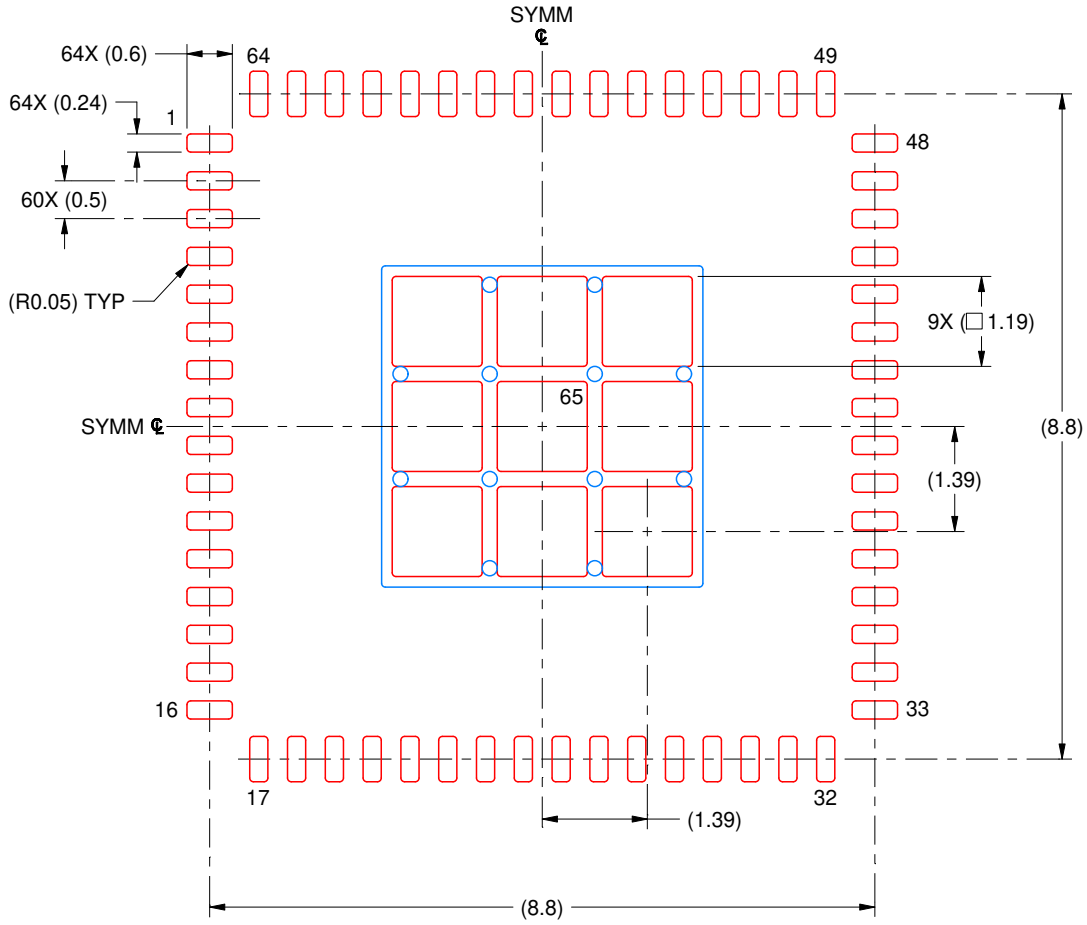


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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