VIPER222

Datasheet

High voltage converter



Features

- 730 V avalanche rugged power MOSFET
- PWM controller
- 1.2 V reference voltage
- Frequency jittering
- 40 mW no load input power at 230 V_{AC}
- Short-circuit protection
- Thermal shutdown

Application

- Auxiliary SMPS for home appliances, consumer, industrial, lighting.

Description

The VIPER222 device is a high performance high voltage converter that combines a 730 V rugged power MOSFET with a PWM control. The device embeds the high voltage startup and the current sense circuit, avoiding the use of extra components in the BoM. Frequency jittering spreads the EMI and allows the use of a small filter. The burst mode technique allows to obtain a very low input power consumption at light load.

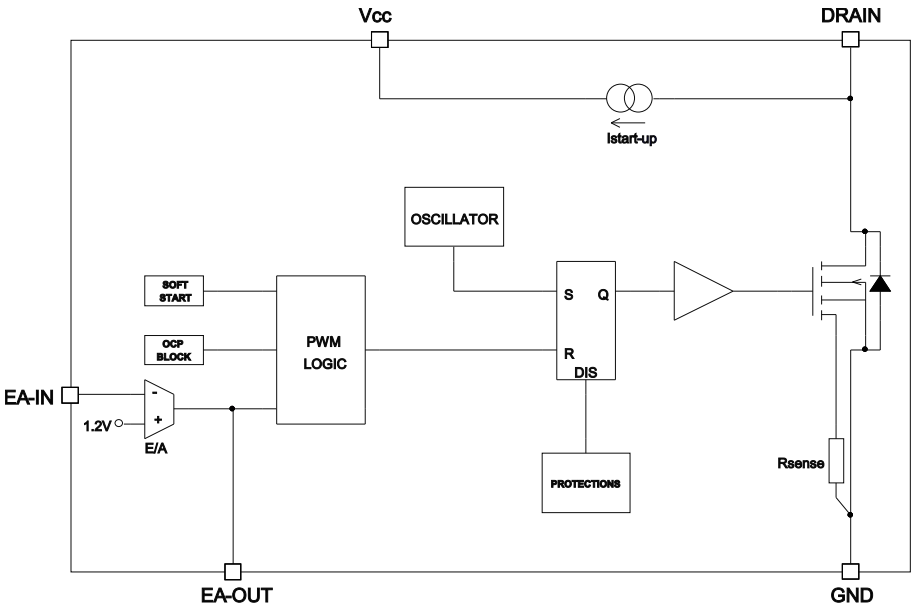
Product status link

VIPER222

Product label

SUSTAINABLE TECHNOLOGY

Figure 1. Block diagram



1 Pin setting

Figure 2. **Connection diagram**

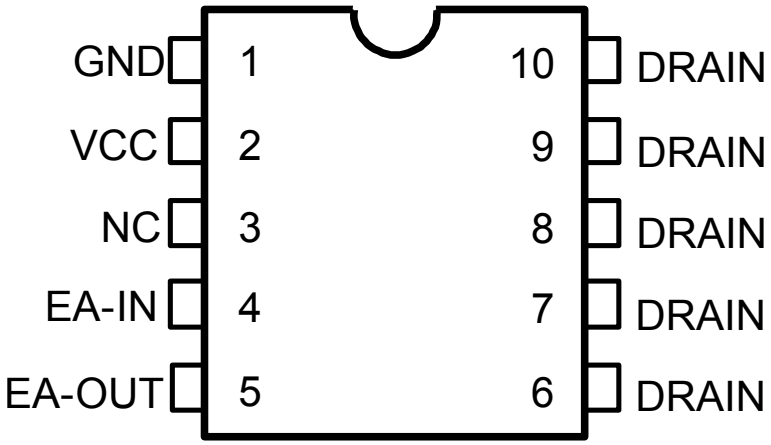


Table 1. **Pin description**

SSOP10	Name	Function
1	GND	Connected to the source of the internal power MOSFET and controller ground reference.
2	VCC	Supply voltage of the control section. This pin provides the charging current of the external capacitor.
3	NC	Not connected. The pin must be connected to GND pin.
4	EA-IN	Input of the error amplifier.
5	EA-OUT	Output of the error amplifier.
6-10	DRAIN	High voltage drain pin. The start-up bias current is drawn from this pin too. Connect to a PCB copper area to facilitate the heat dissipation.

2 Typical power capability

Table 2. Typical power

V_{IN}: 230 V_{AC}		V_{IN}: 85 - 265 V_{AC}	
Adapter (1)	Open frame (2)	Adapter (1)	Open frame (2)
11 W	13 W	7 W	8 W

1. *Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.*
2. *Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat-sinking*

3 Electrical and thermal ratings

Table 3. Absolute maximum rating

Symbol	Pin	Parameter	Value		Unit
			Min.	Max.	
V_{DS}	6-10	Drain-to-source (ground) voltage		730	V
I_D	6-10	Pulse drain current (limited by T_J = 150 °C)		2	A
V_{EA-IN}	4	Input pin voltage	-0.3	4.8	V
V_{EA-OUT}	5	Out pin voltage	-0.3	4.8	V
V_{CC}	2	Supply voltage	-0.3	Self limited	V
I_{CC}	2	Input current		45	mA
P_{TOT}		Power dissipation at T_{AMB} < 50 °C		1 (1)	W
T_J		Junction temperature range	-40	150	°C
T_{STG}		Storage temperature	-55	150	°C

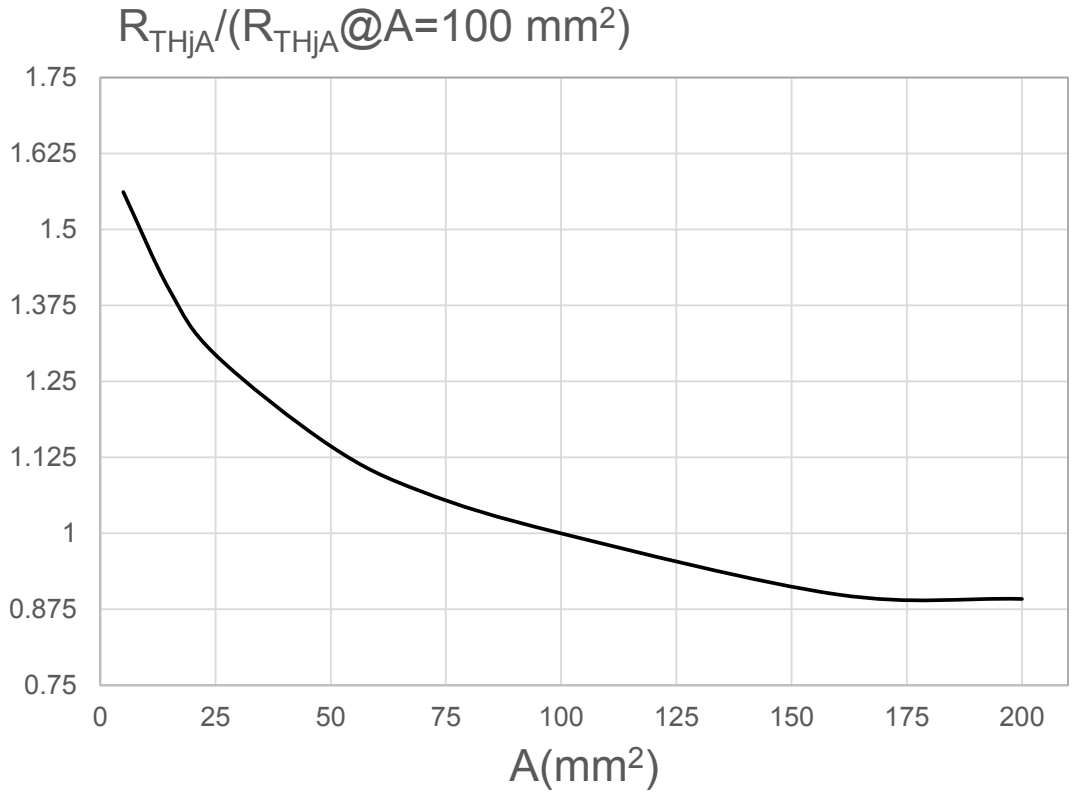
1. *When mounted on a standard single side FR4 board with 100 mm² (0.1552 inch) of Cu (35 µm thick)..*

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
R_{TH-JC}	Thermal resistance junction to case (1) (Dissipated power = 1 W)	10	°C/W
R_{TH-JC}	Thermal resistance junction ambient (1) (Dissipated power = 1 W)	155	°C/W
R_{TH-JC}	Thermal resistance junction to case (2) (Dissipated power = 1 W)	5	°C/W
R_{TH-JC}	Thermal resistance junction ambient (2) (Dissipated power = 1 W)	95	°C/W

1. *When mounted on a standard single side FR4 board with minimum copper area.*
2. *When mounted on a standard single side FR4 board with 100 mm² (0.155sq in) of Cu (35 µm thick).*

Figure 3. **Rth vs. area**



4 Electrical characteristics

(TJ = 25 °C, VCC = 9 V; unless otherwise specified)

Table 5. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_D = 1 mA, EA-OUT= GND	730			V
$R_{DS(on)}$	Drain-Source ON state resistance	I_D = 0.2 A; T_J = 25 °C			15	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 100 V		13		pF
I_{DSS}	OFF state DRAIN leakage current	V_{DRAIN} = 730 V			50	µA
V_{START}	Drain-source start voltage				30	V
I_{CH1}	Startup charging current	V_{DRAIN} = 100 V V_{CC}=0 V	-0.6		-1.4	mA
I_{CH2}	Charging current during operation	V_{DRAIN} = 100 V V_{CC} = 6 V	-2		-4	mA
I_{CH3}	Charging current during self-supply	V_{DRAIN} = 100 V V_{CC} = 6 V	-6		-9	mA
V_{CC}	Operating voltage range		4.5		30	V
V_{CLAMP}	VCC clamp voltage	I_{CC} = 35 mA	30			V
V_{ON}	VCC ON threshold		15	16	17	V
V_{CCL}	VCC low value		4	4.25	4.5	V
V_{OFF}	UVLO		3.75	4	4.25	V
I_{CC0}	Operating supply current, not switching	Not switching			0.5	mA
I_{CC1}	Operating supply current, switching	V_{DS} = 150 V V_{EA-OUT} = 1.2 V F_{OSC} = 30 kHz			1.3	
		V_{DS} = 150 V V_{EA-OUT} = 1.2 V F_{OSC} = 60 kHz			1.6	mA
I_{CC_FAIL}	VCC clamp protection		30			mA
I_{LIM}	Drain current limit (OCP)	T_J =25 °C	0.59	0.62	0.65	A
I_{LIM_BM}	Drain current limit at low load	T_J = 25 °C V_{EA-OUT} = V_{EA_BM}	105	130	155	mA
$T_{ON(MIN)}$	Minimum turn ON time				350	ns
$t_{RESTART}$	Restart time after fault				1.2	s
t_{OVL}	Overload delay time				55	ms

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{OVLmax}	Maximum overload delay time	VIPER222XSTR $F_{OSC} = F_{OSCmin}$			220	ms
		VIPER222LSTR $F_{OSC} = F_{OSCmin}$			440	
t_{SS}	Soft-start time		5		11	ms
t_{CC_FAIL}	Clamp time before shutdown		325	500	675	µs
F_{OSC}	Switching frequency	VIPER222XSTR	27	30	33	kHz
		VIPER222LSTR	54	60	66	
F_{OSCmin}	Minimum switching frequency		13.5	15	16.5	kHz
F_D	Modulation depth	(1)		±7		kHz
F_M	Modulationfrequency	(1)		260		Hz
D_{MAX}	Max. duty cycle	(1)	70		80	%
V_{REF}	E/A reference voltage		1.175	1.2	1.225	V
$I_{PULL\ UP}$	EA-IN pin current pull-up			-1		µA
G_M	E/A Trans conductance	(1)		0.5		mA/V
V_{EA-SAT}	EA-OUT pin saturation limit			3		V
V_{EA-BM}	Burstmode threshold			0.8		V
R_{DYN}	Dynamic resistance	V_{EA-OUT} =2.7V V_{EA-IN} =GND		65		kΩ
H_{EA-OUT}	$\Delta V_{EA-OUT} / \Delta I_D$	(1)	3.8		7	V/A
I_{EA-OUT}	EA-OUT pin source / sink current			100		µA
T_{SD}	Thermal shutdown temperature	(1)	150	160		°C

1. *Specification assured by characterization.*

5 Typical electrical characteristics

Figure 4. I_{LIM} vs. T_J

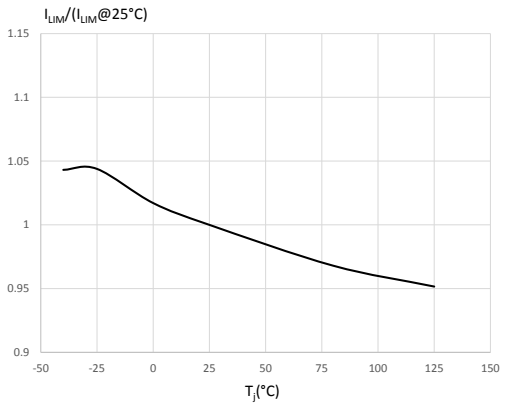


Figure 5. V_{REF} vs. T_J

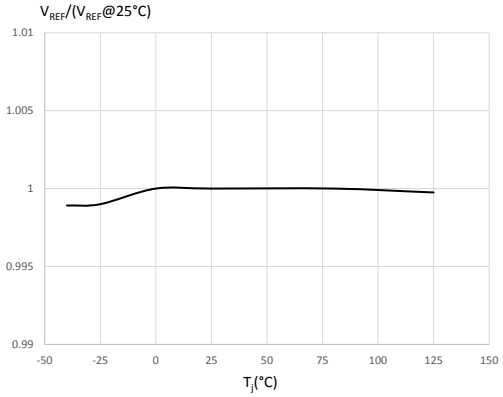


Figure 6. I_{CC0} vs. T_J

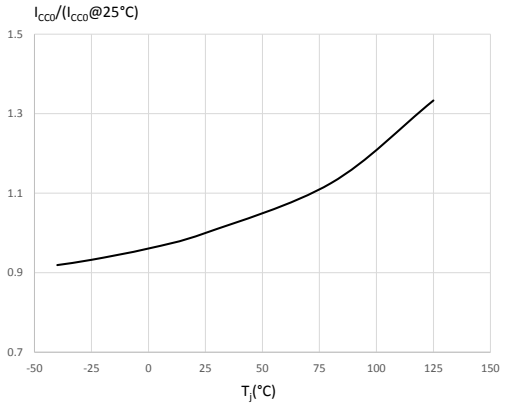


Figure 7. I_{CC1} vs. T_J

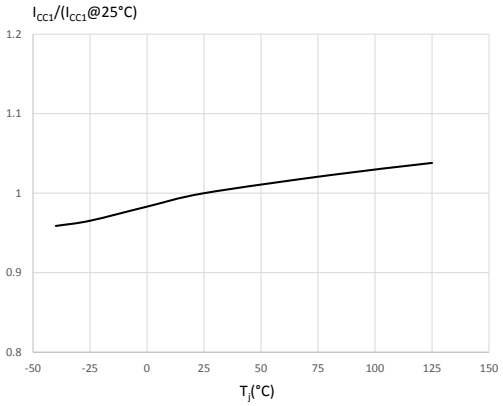


Figure 8. $R_{DS(on)}$ vs. T_J

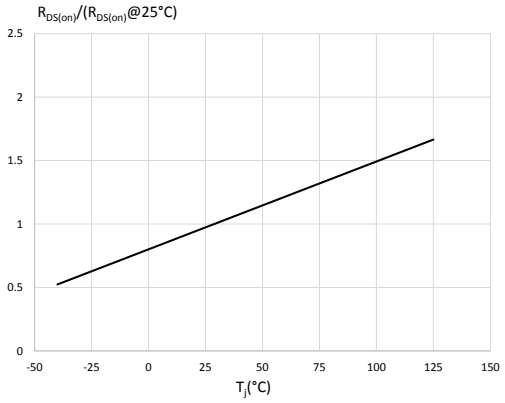
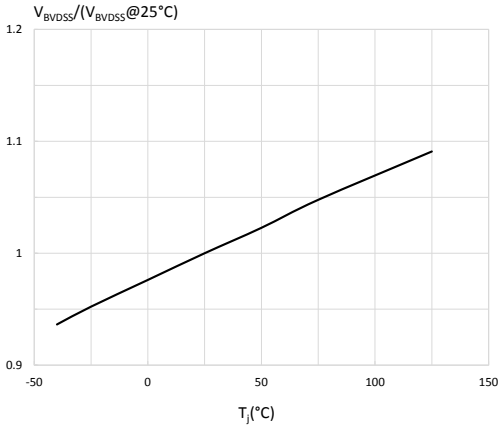


Figure 9. V_{BVDSS} vs. T_j



6 General description

VIPER222 is a 730 V high voltage converter optimized for flyback and buck topologies that operates at 60 kHz (L type) or 30 kHz (X type) switching frequency and integrates the jittering feature in order to reduce the EMI level.

The low IC consumption combined with the burst mode technique allow to obtain very low input power at no load and very good efficiency at light load.

6.1 Startup

At the first startup the integrated high voltage current source charges the VCC capacitor. At the beginning of startup, when the capacitor is fully discharged, the charging current is low, I_{CH1}, in order to avoid IC damaging in case V_{CC} is accidentally shorted to GND. As V_{CC} exceeds 1 V, I_{CH1} is increased to I_{CH2} in order to speed up the charging. The charge current is stopped as soon as V_{CC} reaches V_{ON}.

As soon as the VCC capacitor is charged up to V_{ON}, the high voltage current source is disabled, the device is powered by the energy stored in the capacitor and the primary MOSFET starts switching.

The internal soft-start function of the device progressively increases the cycle-by-cycle current limitation set point from zero up to I_{LIM} in 8 steps. The soft-start time, t_{SS}, is internally set at 8 ms. This function is activated at any attempt of converter startup and at any restart after a fault event.

6.2 Feedback loop

The device operates in current mode, so the primary current is internally sensed and converted in voltage that is applied to the non-inverting pin of the PWM comparator. The sensed voltage is compared through a voltage divider and on cycle-by-cycle basis with the one present on the EA-IN pin.

The OCP comparator works in parallel with the PWM comparator and it limits the primary current below the I_{LIM} threshold.

There are two ways to close the loop and get the output regulated: through resistor divider or through external error amplifier plus optocoupler

Resistor divider

For non-isolated topologies (fly-back, buck or buck-boost converters) the output voltage can be directly set connecting a resistor divider (referenced to GND pin) between the converter output and the EA-IN pin, which is the inverting input of the integrated error amplifier (EA).

Primary side regulation can be realized connecting the resistor divider between VCC, EA-IN and GND pins.

The loop compensation network is connected across EA-OUT and GND pins.

External error amplifier plus optocoupler

In case of isolated fly-back, EA-IN must be connected to GND, which disables the internal error amplifier, and the output voltage is set through an external error amplifier (TL431 or similar) placed on the secondary side. Its error signal, reported to the primary through an optocoupler, is used to set the EA-OUT pin voltage to the value corresponding to the DRAIN peak current required by the control loop to deliver the given output power.

The EA-OUT pin dynamics range between the values $V_{EA\text{-}BM}$ and $V_{EA\text{-}SAT}$: below the $V_{EA\text{-}BM}$ level the device enters burst mode; above the $V_{EA\text{-}SAT}$ level, the primary drain current reaches its limit I_{LIM}.

6.3 Pulse skipping

The protection is intended to avoid the so called “flux-runaway” condition often present at converter startup, because of the low output voltage, and due to the fact that the primary MOSFET, cannot be turned off before the minimum on-time. During the on-time, the inductor is charged by the input voltage and if it cannot be discharged by the same amount during the off-time, in every switching cycle there is a net increase of the average inductor current, that can reach dangerously high values.

Thanks to this protection, each time the DRAIN peak current exceeds I_{LIM} level within t_{ON_MIN}, one switching cycle is skipped. The cycles can be skipped until the minimum switching frequency F_{OSCmin} (15 kHz typ.) is reached. Each time the DRAIN peak current does not exceed I_{LIM} within t_{ON_MIN}, one switching cycle is restored. The cycles can be restored until the nominal switching frequency is reached, F_{OSC} (30 or 60 kHz).

6.4 Burst mode at light load

When the load decreases, the feedback loop reacts lowering the EA-OUT pin voltage. If it goes below the $V_{EA\text{-}BM}$ threshold, the DRAIN peak current is reduced to I_{LIM_BM}, avoiding audible noise which could arise from low switching frequency. When the load is increased, V_{EA_OUT} increases. As it reaches the V_{EA_SAT} threshold, the DRAIN peak current reaches its maximum value, I_{LIM}.

6.5 Short-circuit protection

In case of overload or short-circuit on the output, the IC runs at I_{LIM}.

If this condition is removed before 50ms, the IC continues its normal operation.

If this condition lasts for t_{OVL} (50ms, typ.), the protection is tripped, the device stops switching for $t_{RESTART}$ (1 sec. typ.), then resumes switching with soft-start phase. If the fault is still present, after t_{OVL}, the IC is disabled again for $t_{RESTART}$; otherwise it resumes normal operation.

If the converter is definitively operated at F_{OSC_MIN}, (see Section 6.3), the overload time will increase to t_{OVL_MAX} (100 ms typ. for VIPER222XSTR; 200 ms typ. for VIPER222LSTR).

During the fault event, the VCC voltage is maintained between V_{CCL} (4.25 V) and V_{ON} (16 V) by the periodical activation of the high voltage current source.

6.6 VCC clamp protection

If V_{CC} reaches the clamp level V_{CLAMP} and the current injected into the pin exceeds the internal threshold I_{CC_FAIL} for more than t_{CC_FAIL}, a fault condition is detected. The PWM is disabled for $t_{RESTART}$ and then activated again in soft-start phase. The protection is disabled during the soft-start time.

7 Basic application schematics

Figure 10. **Non isolated flyback converter**

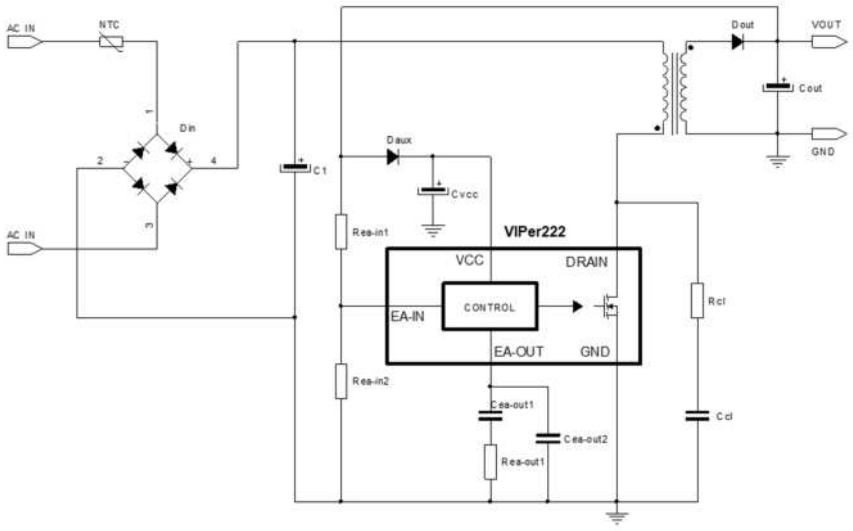


Figure 11. **Primary side flyback converter**

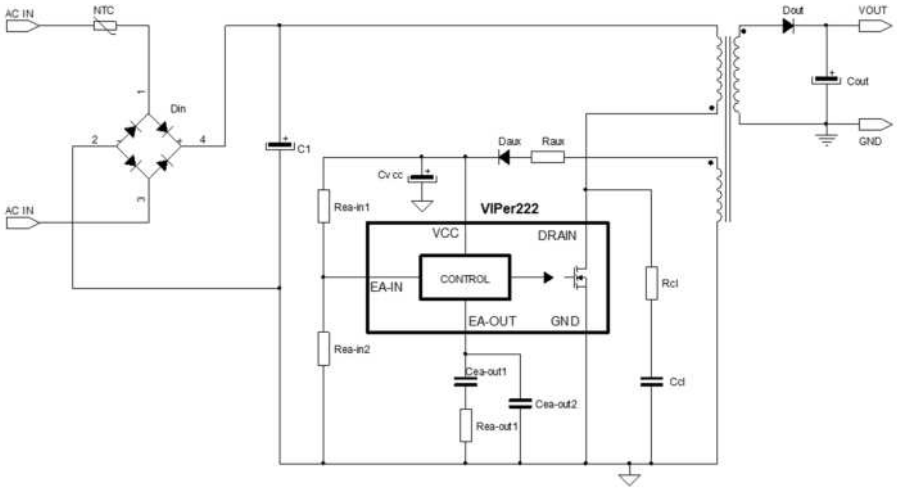


Figure 12. **Isolated flyback converter**

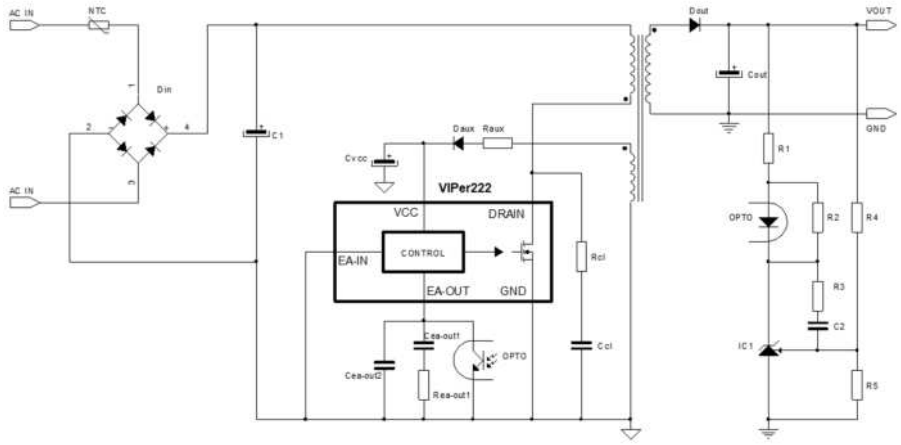


Figure 13. **Buck converter**

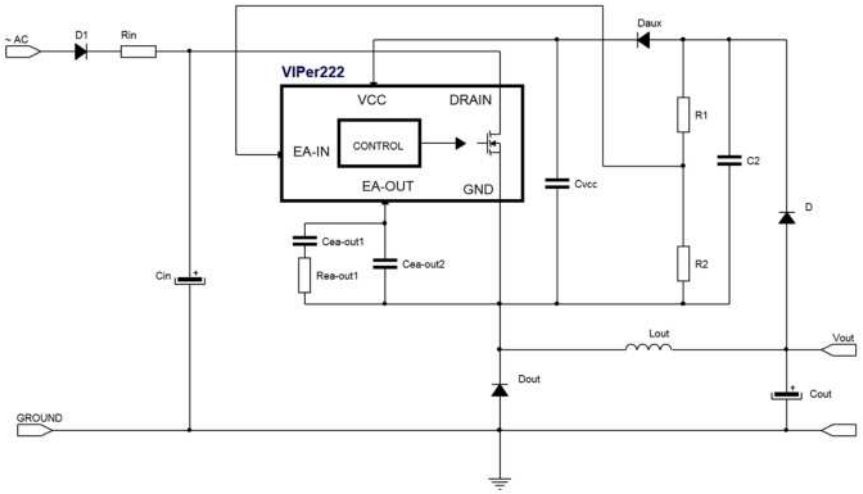
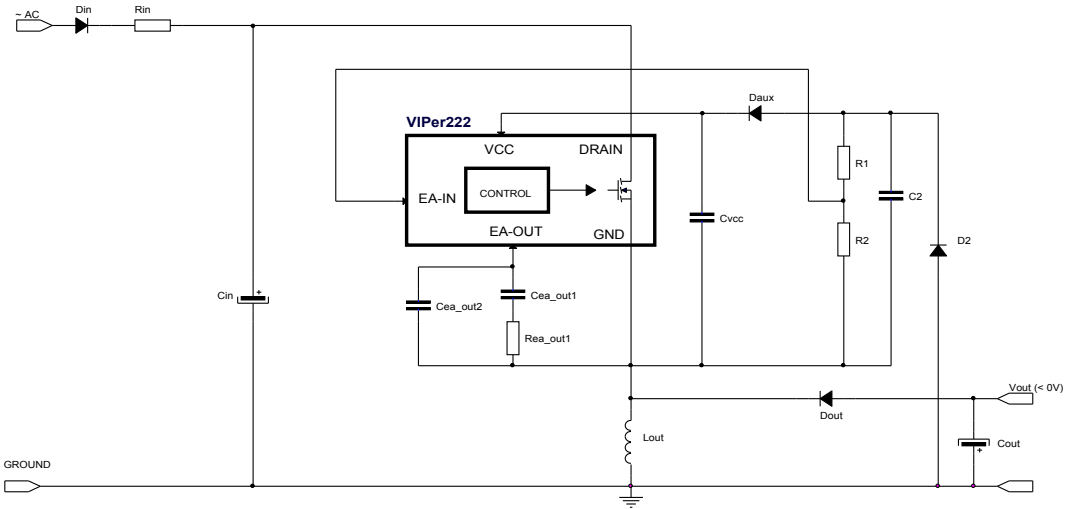


Figure 14. **Buck-Boost converter**



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

8.1 SSOP10 package information

Figure 15. **SSOP10 package outline**

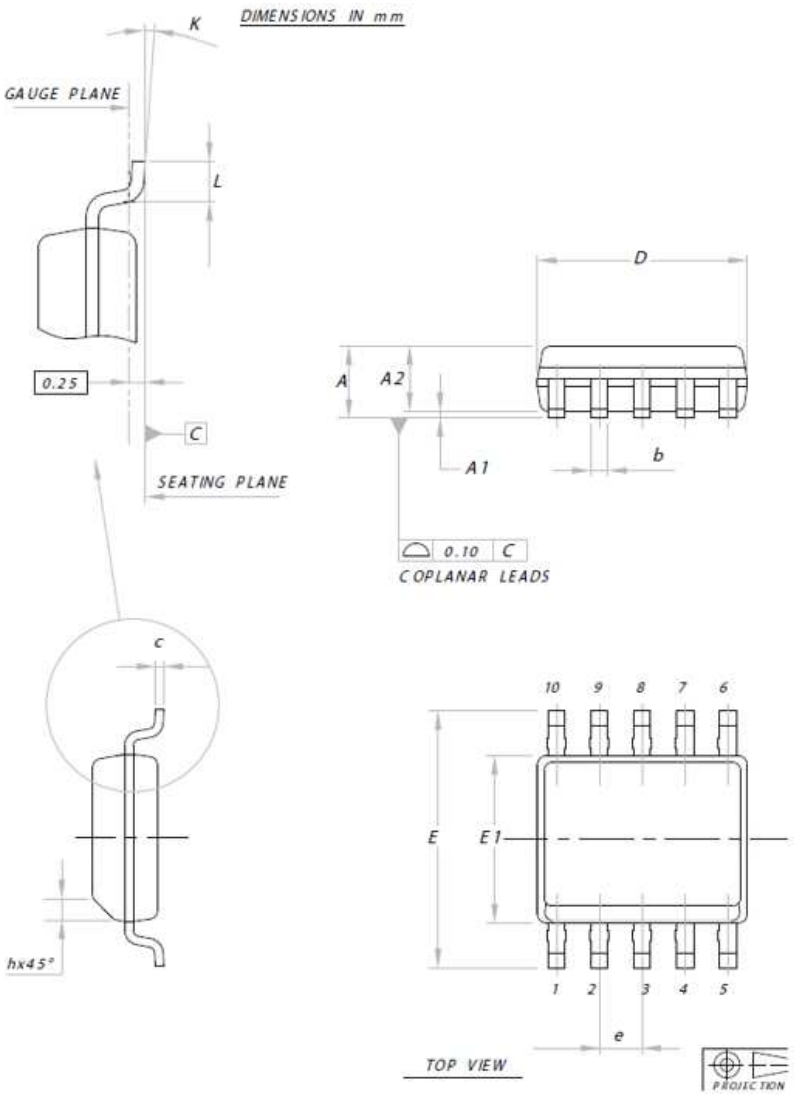


Table 6. **SSO10 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e		1	
H	0.25		0.50
L	0.40		0.90
K	0°		8°

Figure 16. **SSOP10 recommended footprint**

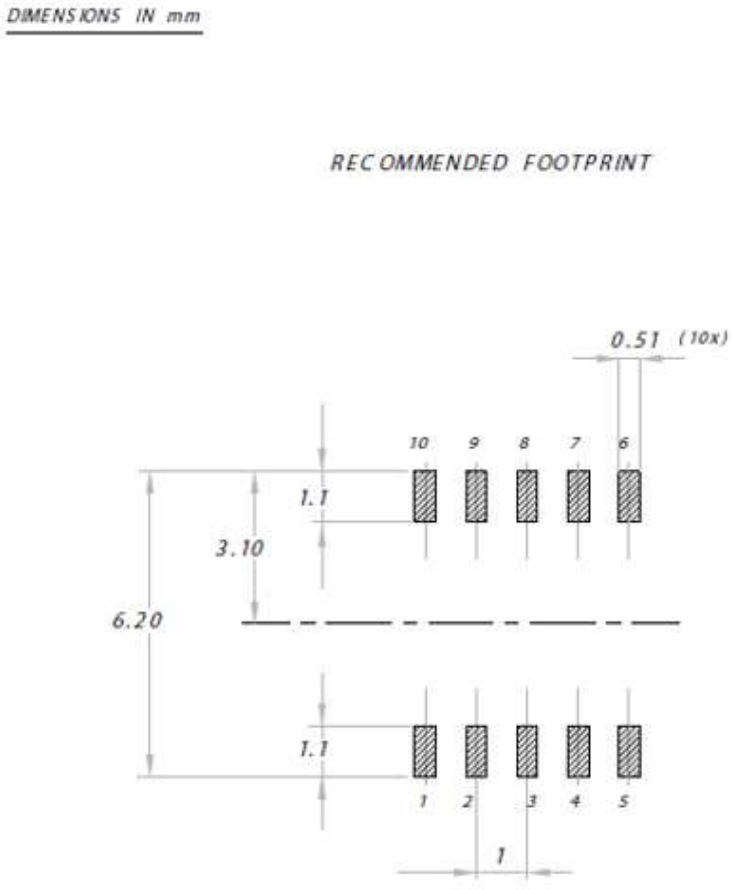


Table 7. **Ordering information**

Order code	Package	Packaging
VIPER222XSTR	SSOP10	Tape & Reel
VIPER222LSTR	SSOP10	Tape & Reel

Revision history

Table 8. **Document revision history**

Date	Version	Changes
20-Dec-2019	1	Initial release.
17-Jan-2020	2	Changed min value ILIM parameter in Table 5

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