# XIO2001 PCI Express to PCI Bus Translation Bridge

## 1 Features

- Full ×1 PCI Express™ Throughput
- Fully Compliant With *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0
- Fully Compliant With *PCI Express Base Specification*, Revision 2.0
- Fully Compliant With *PCI Local Bus Specification*, Revision 2.3
- PCI Express Advanced Error Reporting Capability Including ECRC Support
- Support for D1, D2, $D3_{hot}$, and $D3_{cold}$
- Active-State Link Power Management Saves Power When Packet Activity on the PCI Express Link is Idle, Using Both L0s and L1 States
- Wake Event and Beacon Support
- Error Forwarding Including PCI Express Data Poisoning and PCI Bus Parity Errors
- Uses 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended, Reference Clock
- Optional Spread Spectrum Reference Clock is Supported
- Robust Pipeline Architecture to Minimize Transaction Latency
- Full PCI Local Bus 66-MHz/32-Bit Throughput
- Support for Six Subordinate PCI Bus Masters with Internal Configurable, 2-Level Prioritization Scheme
- Internal PCI Arbiter Supporting Up to 6 External PCI Masters
- Advanced PCI Express Message Signaled Interrupt Generation for Serial IRQ Interrupts
- External PCI Bus Arbiter Option
- PCI Bus $\overline{\text{LOCK}}$ Support
- JTAG/BS for Production Test
- PCI-Express $\overline{\text{CLKREQ}}$ Support
- Clock Run and Power Override Support
- Six Buffered PCI Clock Outputs (25 MHz, 33 MHz, 50 MHz, or 66 MHz)
- PCI Bus Interface 3.3-V and 5.0-V (25 MHz or 33 MHz only at 5.0 V) Tolerance Options
- Integrated AUX Power Switch Drains $V_{AUX}$ Power Only When Main Power Is Off
- Five 3.3-V, Multifunction, General-Purpose I/O Terminals
- Memory-Mapped EEPROM Serial-Bus Controller Supporting PCI Express Power Budget/Limit Extensions for Add-In Cards
- Compact Footprint, Lead-Free 144-Ball, ZAJ nFBGA, Lead-Free 169-Ball ZWS nFBGA, and PowerPad™ HTQFP 128-Pin PNP Package

## 2 Applications

- Enterprise systems
  - Data center & enterprise computing
- Personal electronics
  - PC and notebooks
- Industrial applications
  - Factory automation and control
  - Retail automation & payment
  - Industrial transport (non-car & non-light truck)

## 3 Description

The XIO2001 is a single-function PCI Express to PCI translation bridge that is fully compliant to the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. For downstream traffic, the bridge simultaneously supports up to eight posted and four non-posted transactions. For upstream traffic, up to six posted and four non-posted transactions are simultaneously supported.

The PCI Express interface is fully compliant to the *PCI Express Base Specification*, Revision 2.0.

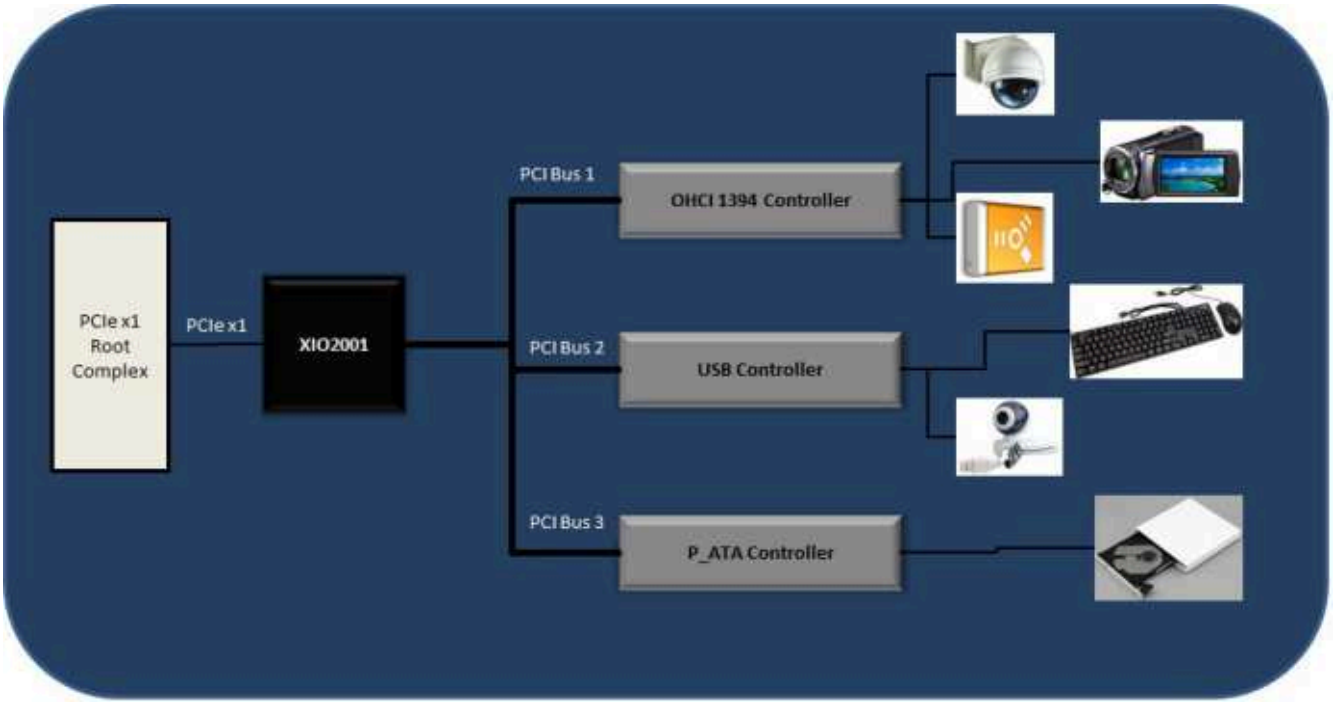
The PCI Express interface supports a ×1 link operating at full 250 MB/s packet throughput in each direction simultaneously. Also, the bridge supports the advanced error reporting including extended CRC (ECRC) as defined in the *PCI Express Base Specification*. Supplemental firmware or software is required to fully use both of these features.

**Device Information** (1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| XIO2001 | HTQFP (128) | 14.00 mm × 14.00 mm |
| | nFBGA (144) | 7.00 mm × 7.00 mm |
| | nFBGA (169) | 12.00 mm × 12.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.




**Typical Diagram**


Copyright © 2021 Texas Instruments Incorporated

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Revision History**....3
**5 Pin Configuration and Functions**....5
**6 Specifications**....15
6.1 Absolute Maximum Ratings....15
6.2 Handling Ratings....15
6.3 Recommended Operating Conditions....15
6.4 Thermal Information (1)....16
6.5 Nominal Power Consumption....16
6.6 PCI Express Differential Transmitter Output Ranges....17
6.7 PCI Express Differential Receiver Input Ranges....18
6.8 PCI Express Differential Reference Clock Input Ranges (1)....19
6.9 PCI Bus Electrical Characteristics....20
6.10 3.3-V I/O Electrical Characteristics....20
6.11 PCI Bus Timing Requirements....21
6.12 Power-Up/-Down Sequencing....21
**7 Parameter Measurement Information**....24
**8 Detailed Description**....26
8.1 Overview....26
8.2 Functional Block Diagram....26
8.3 Feature Description....26
8.4 Register Maps....42
8.5 PCI Express Extended Configuration Space....91
8.6 Memory-Mapped TI Proprietary Register Space....102
**9 Application, Implementation, and Layout**....114
9.1 Application Information....114
9.2 Typical Application....114
9.3 Layout....124
9.4 Power Supply Recommendations....126
**10 Device and Documentation Support**....130
10.1 Documents Conventions....130
10.2 Documentation Support....131
10.3 Support Resources....131
10.4 Trademarks....131
10.5 Electrostatic Discharge Caution....131
10.6 Glossary....131
**11 Mechanical, Packaging, and Orderable Information**....131

## 4 Revision History

| REVISION DATE | REVISION NUMBER | REVISION COMMENTS |
|---|---|---|
| 5/2009 | – | Initial release |
| 5/2009 | A | Corrected typos |
| 9/2009 | B | |
| 10/2009 | C | Added PNP Package and ESD Ratings<br>Removed terminal assignment tables for all packages |
| 1/2010 | D | Corrected PNP pinout, replaced Ordering Information with Package Option Addendum |
| 11/2011 | E | Corrected Vi PCI Express REFCLK(differential) parameters<br>Corrected VRX-DIFFp-p parameters<br>Removed label N13 on the signal VDD_15 for the ZAJ package |
| 5/2012 | F | Added missing PNP pin numbers to the Table 2-1 and to the Table 2-2 |
| 5/2012 | G | Changed external parts for CLKRUN_EN to include pulldown resostor<br>Deleted Note from CLKRUIN_EN terminal's description<br>Changed external Parts for EXT_ARB_EN to include pulldown resistor<br>Deleted Note from EXT_ARB_EN terminal's description |
| 8/2014 | H | Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section<br>Updated Power-Up Sequence section<br>Identified VDD_15_PLL pins |

Copyright © 2021 Texas Instruments Incorporated

| REVISION DATE | REVISION NUMBER | REVISION COMMENTS |
|---|---|---|
| 9/2014 | I | Changed pin F10 From: VDD_15 To: VDD_15_PLL in the ZGU package<br>Changed pin F11 From: VDD_15 To: VDD_15_PLL in the ZAJ package<br>Changed pin 84 From: VDDA_15 To: VDD_15_PLL in the PNP package<br>Changed the pin name from VDD_15_PULL to VDD_15_PLL in the Pin Functions table.<br>Changed PCIR description in the Pin Functions table From: "Connect this terminals to the secondary PCI bus..." To: "Connect each one of these terminals to the secondary PCI bus.."<br>Deleted text from the LOCK pin description in the Pin Functions table: "when bit 12 (LOCK_EN) is set in the general control register (see *Section 8.4.66*)." |

**Changes from Revision I (September 2014) to Revision J (January 2021)** **Page**

- NOTE: The device in the MicroStar Jr. BGA packaging were redesigned using a laminate nFBGA package. This nFBGA package offers datasheet-equivalent electrical performance. It is also footprint equivalent to the MicroStar Jr. BGA. The new package designator in place of the discontinued package designator will be updated throughout the datasheet..... 1
- Changed u*jr ZGU to nFBGA ZWS..... 1
- Changed u*jr ZGU to nFBGA ZWS..... 1
- Changed u*jr ZGU to nFBGA ZWS..... 8
- Changed PCIE RX max abs in the *Section 6.1* table From: 0.6 to 1.2..... 15
- Changed u*jr ZGU to nFBGA ZWS Thermal Model and Corrected ZGU to ZAJ part numbers..... 16


Copyright © 2021 Texas Instruments Incorporated

# 5 Pin Configuration and Functions

## Pin Assignments

The XIO2001 is available in either a 169-ball ZWS nFBGA or a 144−ball ZAJ nFBGA package.

Figure 5-1 shows a pin diagram of the ZWS package.

Figure 5-2 shows a pin diagram of the ZAJ package.

Figure 5-3 shows a pin diagram of the PNP package.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| N | C/BE[3] | AD25 | AD27 | AD30 | AD31 | INTB | PRST | SERIRQ | GPIO0// CLKRUN | GPIO2 | GPIO3//SDA | JTAG_TDI | GRST | N |
| M | AD20 | AD22 | AD24 | AD26 | AD28 | INTA | INTC | LOCK | GPIO1// PWR_OVRD | GPIO4// SCL | JTAG_TDO | JTAG_TCK | WAKE | M |
| L | AD18 | AD19 | AD21 | AD23 | AD29 | M66EN | INTD | VDD_33 | JTAG_ TRST# | JTAG_TMS | VSS | PME | VDD_15_ COMB | L |
| K | AD16 | AD17 | PCIR | VSS | VSS | VSS | VDD_15 | VSS | VDD_33 | VSSA | VDD_33_ COMB_IO | REF0_PCIE | REF1_PCIE | K |
| J | IRDY | FRAME | C/BE[2] | VDD_33 | VSS | VSS | VSS | VSS | VSS | VSS | VDD_33_ AUX | VDD_33 | VDD_33_ COMB | J |
| H | TRDY | DEVSEL | VDD_33 | VSS | VSS | VSS | VSS | VSS | VSS | VDD_15 | PERST | VSSA | VDDA_15 | H |
| G | STOP | PERR | SERR# | VDD_15 | VSS | VSS | VSS | VSS | VSS | VDD_15 | VSSA | TXN | TXP | G |
| F | PAR | C/BE[1] | CLK | VSS | VSS | VSS | VSS | VSS | VSS | VDD_15_PLL | VSS | VSS | VDDA_15 | F |
| E | AD15 | AD14 | AD13 | VDD_33 | VSS | VSS | VSS | VSS | VSS | VSSA | VSSA | RXN | RXP | E |
| D | AD12 | AD11 | AD8 | VSS | VDD_33 | VSS | VDD_15 | VSS | VDD_33 | VSS | CLKREQ | VREG_PD33 | VDDA_33 | D |
| C | AD10 | AD9 | AD7 | AD5 | AD0 | GNT1 | VDD_33 | REQ3 | REQ4 | EXT_ARB_EN | VSSA | REFCLK− | REFCLK+ | C |
| B | C/BE[0] | AD6 | AD3 | AD2 | CLKOUT0 | CLKOUT1 | CLKOUT3 | GNT2 | GNT3 | GNT5 | CLKOUT6 | PCLK66_SEL | REFCLK125 _SEL | B |
| A | PCIR | AD4 | AD1 | REQ0 | GNT0 | REQ1 | CLKOUT2 | REQ2 | CLKOUT4 | CLKOUT5 | GNT4 | REQ5 | CLKRUN_EN | A |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | |

**Figure 5-1. XIO2001 ZWS nFBGA Package (Bottom View)**

Copyright © 2021 Texas Instruments Incorporated

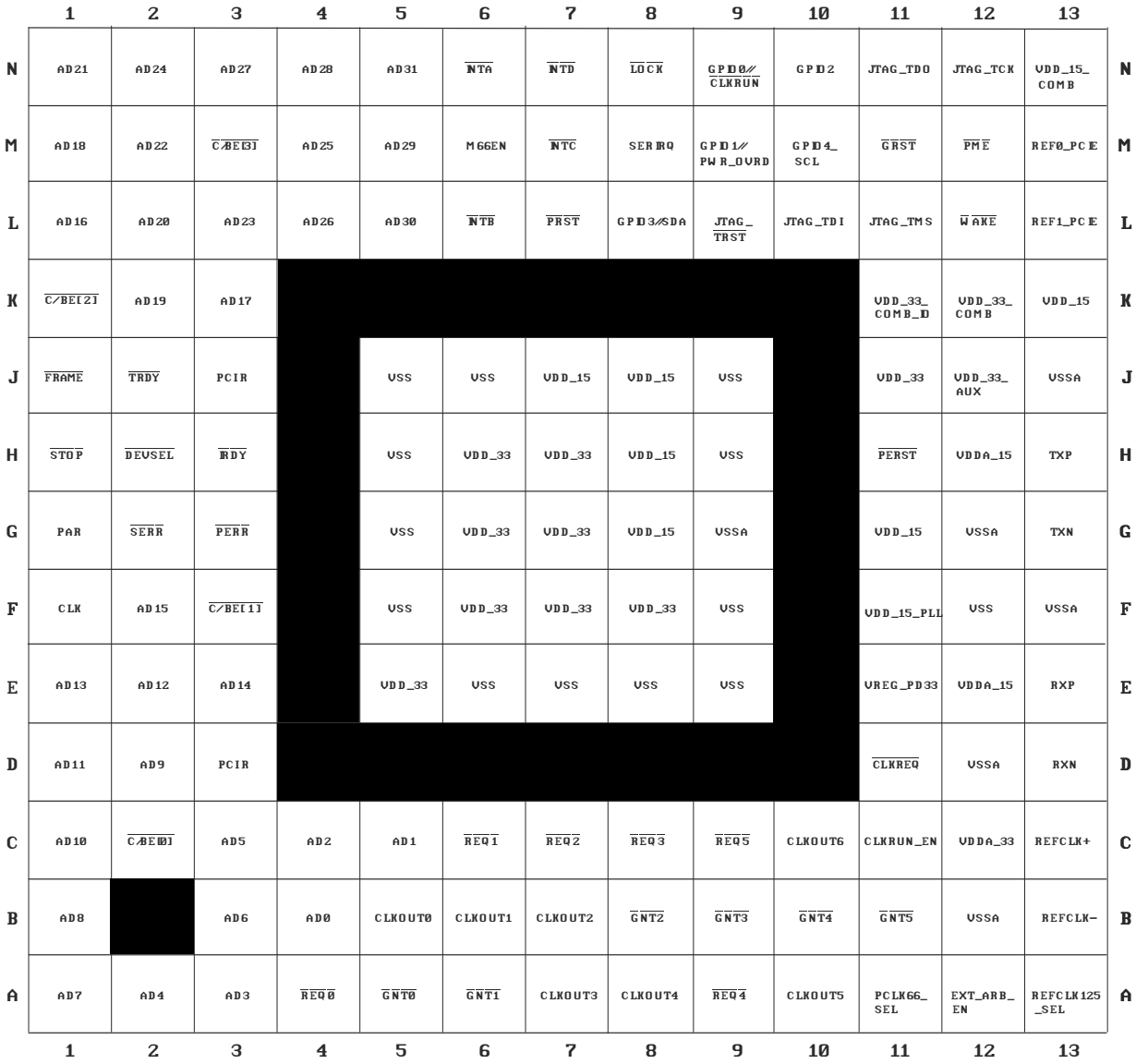



**Figure 5-2. XIO2001 ZAJ nFBGA Package (Bottom View)**


Copyright © 2021 Texas Instruments Incorporated

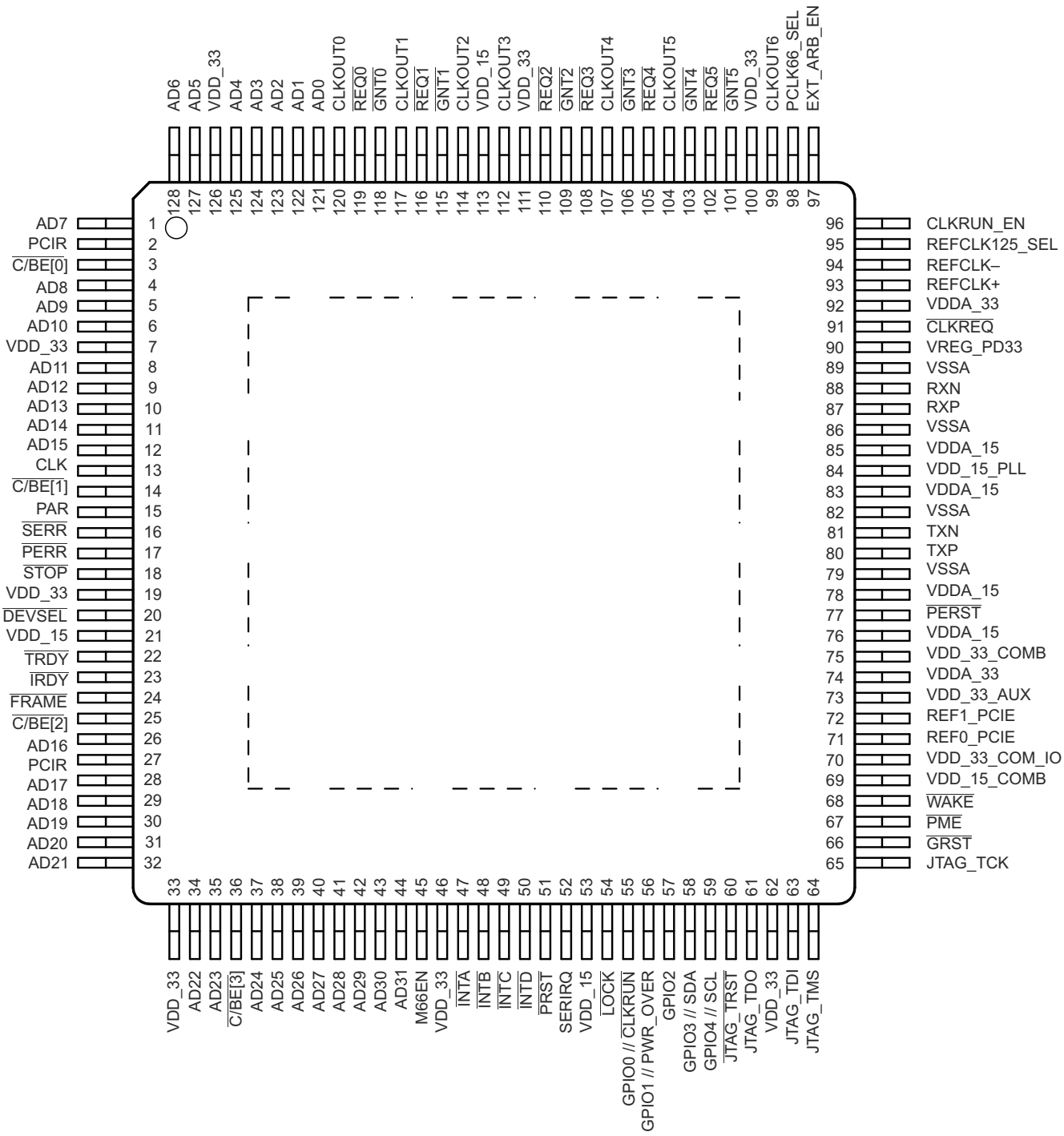



**Figure 5-3. XIO2001 PNP PowerPAD™ HTQFP Package (Top View)**

## Pin Descriptions

The following list describes the different input/output cell types that appear in the pin function tables:

- HS DIFF IN = High speed differential input
- HS DIFF OUT = High speed differential output
- PCI BUS = PCI bus tri-state bidirectional buffer with 3.3-V or 5.0-V clamp rail.
- LV CMOS = 3.3-V low voltage CMOS input or output with 3.3-V clamp rail
- BIAS = Input/output terminals that generate a bias voltage to determine a driver's operating current
- Feed through = These terminals connect directly to macros within the part and not through an input or output cell.
- PWR = Power terminal
- GND = Ground terminal

**Pin Functions**

| SIGNAL | ZWS BALL NO. | ZAJ BALL NO. | PNP PIN NO. | I/O TYPE | EXTERNAL PARTS | DESCRIPTION |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| PCIR | A01, K03 | D03, J03 | 2, 27 | I/O | Resistor | PCI Rail. 5.0-V or 3.3-V PCI bus clamp voltage to set maximum I/O voltage tolerance of the secondary PCI bus signals. Connect each one of these terminals to the secondary PCI bus I/O clamp rail through a 1kΩ resistor. |
| $V_{DD_15}$ | G04, K07, D07, H10, G10 | J08, H08, J07, G08, K13, G11 | 21, 53, 113 | PWR | Bypass capacitors | 1.5-V digital core power terminals |
| $V_{DD_15_PLL}$ | F10 | F11 | 84 | PWR | Pi filter | 1.5-V power terminal for internal PLL. This terminal must be isolated from analog and digital power. |
| $V_{DDA_15}$ | F13, H13 | E12, H12 | 76, 78, 83, 85 | PWR | Pi filter | 1.5-V analog power terminal |
| $V_{DD_33}$ | E04, H03, J04, L08, K09, D09, C07, D05, J12 | E05, G06, H07, G07, H06, F08, F07, F06, J11 | 7, 19, 33, 46, 62, 100, 111, 126 | PWR | Bypass capacitors | 3.3-V digital I/O power terminal |
| $V_{DD_33_AUX}$ | J11 | J12 | 73 | PWR | Bypass capacitors | 3.3-V auxiliary power terminal **Note:** This terminal is connected to $V_{SS}$ through a pulldown resistor if no auxiliary supply is present. |
| $V_{DDA_33}$ | D13 | C12 | 74, 92 | PWR | Pi filter | 3.3-V analog power terminal |
| **GROUND** | | | | | | |
| $V_{SS}$ | D04, F04, H04, K04, K05, K06, K08, L11, J10, D10, D08, D06, F11, F12 | E06, F05, G05, H05, J05, J06, J09, H09, E09, E08, E07, F12 ,F09 | | GND | Digital ground terminals | |


Copyright © 2021 Texas Instruments Incorporated

**Pin Functions (continued)**

| SIGNAL | ZWS BALL NO. | ZAJ BALL NO. | PNP PIN NO. | I/O TYPE | EXTERNAL PARTS | DESCRIPTION |
|---|---|---|---|---|---|---|
| $V_{SS}$ | E05, E06, E07, E08, E09, F05, F06, F07, F08, F09, G05, G06, G07, G08, G09, H05, H06, H07, H08, H09, J05, J06, J07, J08, J09 | | | GND | Ground terminals for thermally-enhanced package | |
| $V_{SSA}$ | K10, C11, H12, G11, E11, E10 | G09, B12, J13, G12, F13, D12 | 79, 82, 86, 89 | GND | Analog ground terminal | |
| **COMBINED POWER OUTPUT** | | | | | | |
| $V_{DD_15_COMB}$ | L13 | N13 | 69 | Feed through | Bypass capacitors | Internally-combined 1.5-V main and $V_{AUX}$ power output for external bypass capacitor filtering. Supplies all internal 1.5-V circuitry powered by $V_{AUX}$. **Caution:** Do not use this terminal to supply external power to other devices. |
| $V_{DD_33_COMB}$ | J13 | K12 | 75 | Feed through | Bypass capacitors | Internally-combined 3.3-V main and $V_{AUX}$ power output for external bypass capacitor filtering. Supplies all internal 3.3-V circuitry powered by $V_{AUX}$. **Caution:** Do not use this terminal to supply external power to other devices. |
| $V_{DD_33_COMBIO}$ | K11 | K11 | 70 | Feed through | Bypass capacitors | Internally-combined 3.3-V main and $V_{AUX}$ power output for external bypass capacitor filtering. Supplies all internal 3.3-V input/output circuitry powered by $V_{AUX}$. **Caution:** Do not use this terminal to supply external power to other devices. |

Copyright © 2021 Texas Instruments Incorporated

## Pin Functions

| SIGNAL | ZWS BALL NO. | ZAJ BALL NO. | PNP PIN NO. | I/O TYPE | CELL TYPE | CLAMP RAIL | EXTERNAL PARTS | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| **PCI EXPRESS** | | | | | | | | |
| $\overline{\text{CLKREQ}}$ | D11 | D11 | 91 | 0 | LV CMOS | $V_{DD_33_COMBIO}$ | – | Clock request. When asserted low, requests upstream device start clock in cases where clock may be removed in L1.<br>**Note:** Since $\overline{\text{CLKREQ}}$ is an open-drain output buffer, a system side pullup resistor is required. |
| $\overline{\text{PERST}}$ | H11 | H11 | 77 | I | LV CMOS | $V_{DD_33_COMBIO}$ | – | PCI Express reset input. The $\overline{\text{PERST}}$ signal identifies when the system power is stable and generates an internal power on reset.<br>**Note:** The $\overline{\text{PERST}}$ input buffer has hysteresis. |
| REFCLK125_SEL | B13 | A13 | 95 | I | LV CMOS | $V_{DD_33}$ | Pullup or pulldown resistor | Reference clock select. This terminal selects the reference clock input.<br>0 = 100-MHz differential common reference clock used.<br>1 = 125-MHz single-ended, reference clock used. |
| REFCLK+ | C13 | C13 | 93 | DI | HS DIFF IN | $V_{DD_33}$ | – | Reference clock. REFCLK+ and REFCLK– comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, use the REFCLK+ input. |
| REFCLK– | C12 | B13 | 94 | DI | HS DIFF IN | $V_{DD_33}$ | Capacitor for $V_{SS}$ for single-ended node | Reference clock. REFCLK+ and REFCLK– comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, attach a capacitor from REFCLK– to $V_{SS}$. |
| REF0_PCIE<br>REF1_PCIE | K12<br>K13 | M13<br>L13 | 71<br>72 | I/O | BIAS | – | External resistor | External reference resistor + and – terminals for setting TX driver current. An external resistance of 14,532-Ω is connected between REF0_PCIE and REF1_PCIE terminals. To eliminate the need for a custom resistor, two series resistors are recommended: a 14.3-kΩ, 1% resistor and a 232-Ω, 1% resistor. |
| RXP<br>RXN | E13<br>E12 | E13<br>D13 | 87<br>88 | DI | HS DIFF IN | $V_{SS}$ | – | High-speed receive pair. RXP and RXN comprise the differential receive pair for the single PCI Express lane supported. |
| TXP<br>TXN | G13<br>G12 | H13<br>G13 | 80<br>81 | DO | HS DIFF OUT | $V_{DD_15}$ | Series capacitor | High-speed transmit pair. TXP and TXN comprise the differential transmit pair for the single PCI Express lane supported. |
| $\overline{\text{WAKE}}$ | M13 | L12 | 68 | O | LV CMOS | $V_{DD_33_COMBIO}$ | – | Wake is an active low signal that is driven low to reactivate the PCI Express link hierarchy's main power rails and reference clocks.<br>**Note**: Since $\overline{\text{WAKE}}$ is an open-drain output buffer, a system side pullup resistor is required. |


Copyright © 2021 Texas Instruments Incorporated

## Pin Functions (continued)

| SIGNAL | ZWS BALL NO. | ZAJ BALL NO. | PNP PIN NO. | I/O TYPE | CELL TYPE | CLAMP RAIL | EXTERNAL PARTS | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| **PCI SYSTEM** | | | | | | | | |
| AD31<br>AD30<br>AD29<br>AD28<br>AD27<br>AD26<br>AD25<br>AD24<br>AD23<br>AD22<br>AD21<br>AD20<br>AD19<br>AD18<br>AD17<br>AD16<br>AD15<br>AD14<br>AD13<br>AD12<br>AD11<br>AD10<br>AD9<br>AD8<br>AD7<br>AD6<br>AD5<br>AD4<br>AD3<br>AD2<br>AD1<br>AD0 | N05<br>N04<br>L05<br>M05<br>N03<br>M04<br>N02<br>M03<br>L04<br>M02<br>L03<br>M01<br>L02<br>L01<br>K02<br>K01<br>E01<br>E02<br>E03<br>D01<br>D02<br>C01<br>C02<br>D03<br>C03<br>B02<br>C04<br>A02<br>B03<br>B04<br>A03<br>C05 | N05<br>L05<br>M05<br>N04<br>N03<br>L04<br>M04<br>N02<br>L03<br>M02<br>N01<br>L02<br>K02<br>M01<br>K03<br>L01<br>F02<br>E03<br>E01<br>E02<br>D01<br>C01<br>D02<br>B01<br>A01<br>B03<br>C03<br>A02<br>A03<br>C04<br>C05<br>B04 | 44<br>43<br>42<br>41<br>40<br>39<br>38<br>37<br>35<br>34<br>32<br>31<br>30<br>29<br>28<br>26<br>12<br>11<br>10<br>9<br>8<br>6<br>5<br>4<br>1<br>128<br>127<br>125<br>124<br>123<br>122<br>121 | I/O | PCI Bus | PCIR | – | PCI address data lines |
| $\overline{C/BE[3]}$<br>$\overline{C/BE[2]}$<br>$\overline{C/BE[1]}$<br>$\overline{C/BE[0]}$ | N01<br>J03<br>F02<br>B01 | M03<br>K01<br>F03<br>C02 | 36<br>25<br>14<br>3 | I/O | PCI Bus | PCIR | – | PCI command byte enables |
| CLK | F03 | F01 | 13 | I | PCI Bus | PCIR | – | PCI clock input. This is the clock input to the PCI bus core. |
| CLKOUT0<br>CLKOUT1<br>CLKOUT2<br>CLKOUT3<br>CLKOUT4<br>CLKOUT5<br>CLKOUT6 | B05<br>B06<br>A07<br>B07<br>A09<br>A10<br>B11 | B05<br>B06<br>B07<br>A07<br>A08<br>A10<br>C10 | 120<br>117<br>114<br>112<br>107<br>104<br>99 | O | PCI Bus | PCIR | – | PCI clock outputs. These clock outputs are used to clock the PCI bus. If the bridge PCI bus clock outputs are used, then CLKOUT6 must be connected to the CLK input. |
| $\overline{DEVSEL}$ | H02 | H02 | 20 | I/O | PCI Bus | PCIR | Pullup resistor per PCI spec | PCI device select |
| $\overline{FRAME}$ | J02 | J01 | 24 | I/O | PCI Bus | PCIR | Pullup resistor per PCI spec | PCI frame |
| $\overline{GNT5}$<br>$\overline{GNT4}$<br>$\overline{GNT3}$<br>$\overline{GNT2}$<br>$\overline{GNT1}$<br>$\overline{GNT0}$ | B10<br>A11<br>B09<br>B08<br>C06<br>A05 | B11<br>B10<br>B09<br>B08<br>A06<br>A05 | 101<br>103<br>106<br>109<br>115<br>118 | O | PCI Bus | PCIR | – | PCI grant outputs. These signals are used for arbitration when the PCI bus is the secondary bus and an external arbiter is not used. $\overline{GNT0}$ is used as the $\overline{REQ}$ for the bridge when an external arbiter is used. |
| $\overline{INTA}$<br>$\overline{INTB}$<br>$\overline{INTC}$<br>$\overline{INTD}$ | M06<br>N06<br>M07<br>L07 | N06<br>L06<br>M07<br>N07 | 47<br>48<br>49<br>50 | I | PCI Bus | PCIR | Pullup resistor per PCI spec | PCI interrupts A–D. These signals are interrupt inputs to the bridge on the secondary PCI bus. |
| $\overline{IRDY}$ | J01 | H03 | 23 | I/O | PCI Bus | PCIR | Pullup resistor per PCI spec | PCI initiator ready |
| $\overline{LOCK}$ | M08 | N08 | 54 | I/O | PCI Bus | PCIR | Pullup resistor per PCI spec | This terminal functions as PCI $\overline{LOCK}$<br>**Note**: In lock mode, an external pullup resistor is required to prevent the $\overline{LOCK}$ signal from floating. |

Copyright © 2021 Texas Instruments Incorporated

## Pin Functions (continued)

| SIGNAL | ZWS BALL NO. | ZAJ BALL NO. | PNP PIN NO. | I/O TYPE | CELL TYPE | CLAMP RAIL | EXTERNAL PARTS | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| M66EN | L06 | M06 | 45 | I | PCI Bus | PCIR | Pullup resistor per PCI spec | 66-MHz mode enable<br>0 = Secondary PCI bus and clock outputs operate at 33 MHz. If PCLK66_SEL is low then the frequency will be 25 MHz.<br>1 = Secondary PCI bus and clock outputs operate at 66 MHz. If PCLK66_SEL is low then the frequency will be 50 MHz. |
| PAR | F01 | G01 | 15 | I/O | PCI Bus | PCIR | – | PCI bus parity |
| $\overline{\text{PERR}}$ | G02 | G03 | 17 | I/O | PCI Bus | PCIR | Pullup resistor per PCI spec | PCI parity error |
| $\overline{\text{PME}}$ | L12 | M12 | 67 | I | LV CMOS | $V_{DD_33_COMBIO}$ | Pullup resistor per PCI spec | Pullup resistor per PCI spec PCI power management event. This terminal may be used to detect $\overline{\text{PME}}$ events from a PCI device on the secondary bus.<br>**Note:** The $\overline{\text{PME}}$ input buffer has hysteresis. |
| $\overline{\text{REQ5}}$<br>$\overline{\text{REQ4}}$<br>$\overline{\text{REQ3}}$<br>$\overline{\text{REQ2}}$<br>$\overline{\text{REQ1}}$<br>$\overline{\text{REQ0}}$ | A12<br>C09<br>C08<br>A08<br>A06<br>A04 | C09<br>A09<br>C08<br>C07<br>C06<br>A04 | 102<br>105<br>108<br>110<br>116<br>119 | I | PCI Bus | PCIR | If unused, a weak pullup resistor per PCI spec | PCI request inputs. These signals are used for arbitration on the secondary PCI bus when an external arbiter is not used. $\overline{\text{REQ0}}$ is used as the $\overline{\text{GNT}}$ for the bridge when an external arbiter is used. |
| $\overline{\text{PRST}}$ | N07 | L07 | 51 | O | PCI Bus | PCIR | – | PCI reset. This terminal is an output to the secondary PCI bus. |
| $\overline{\text{SERR}}$ | G03 | G02 | 16 | I/O | PCI Bus | PCIR | Pullup resistor per PCI spec | PCI system error |
| $\overline{\text{STOP}}$ | G01 | H01 | 18 | I/O | PCI Bus | PCIR | Pullup resistor per PCI spec | PCI stop |
| $\overline{\text{TRDY}}$ | H01 | J02 | 22 | I/O | PCI Bus | PCIR | Pullup resistor per PCI spec | PCI target ready |
| **JTAG** | | | | | | | | |
| JTAG_TCK | M12 | N12 | 65 | I | LV CMOS | $V_{DD_33}$ | Optional pullup resistor | JTAG test clock input. This signal provides the clock for the internal TAP controller.<br>**Note**: This terminal has an internal active pullup resistor. The pullup is active at all times.<br>**Note**: This terminal should be tied to ground or pulled low if JTAG is not required. |
| JTAG_TDI | N12 | L10 | 63 | I | LV CMOS | $V_{DD_33}$ | Optional pullup resistor | JTAG test data input. Serial test instructions and data are received on this terminal.<br>**Note**: This terminal has an internal active pullup resistor. The pullup is active at all times.<br>**Note**: This terminal can be left unconnected if JTAG is not required. |
| JTAG_TDO | M11 | N11 | 61 | O | LV CMOS | $V_{DD_33}$ | – | JTAG test data output. This terminal the serial output for test instructions and data.<br>**Note**: This terminal can be left unconnected if JTAG is not required. |
| JTAG_TMS | L10 | L11 | 64 | I | LV CMOS | $V_{DD_33}$ | Optional pullup resistor | JTAG test mode select. The signal received at JTAG_TMS is decoded by the internal TAP controller to control test operations.<br>**Note**: This terminal has an internal active pullup resistor. The pullup is active at all times.<br>**Note**: This terminal can be left unconnected if JTAG is not required. |
| $\overline{\text{JTAG_TRST}}$ | L09 | L09 | 60 | I | LV CMOS | $V_{DD_33}$ | Optional pullup resistor | JTAG test reset. This terminal provides Optional for asynchronous initialization of the TAP controller.<br>**Note**: This terminal has an internal active pullup resistor. The pullup is active at all times.<br>**Note**: This terminal should be tied to ground or pulled low if JTAG is not required. |


Copyright © 2021 Texas Instruments Incorporated

**Miscellaneous Pins**

| SIGNAL | ZWS BALL NO. | ZAJ BALL NO. | PNP PIN NO. | I/O TYPE | CELL TYPE | CLAMP RAIL | EXTERNAL PARTS | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| CLKRUN_ EN | A13 | C11 | 96 | I | LV CMOS | $V_{DD_33}$ | Optional pullup/ pulldown resistor | Clock run enable<br>0 = Clock run support disabled<br>1 = Clock run support enabled |
| EXT_ARB_EN | C10 | A12 | 97 | I | LV CMOS | $V_{DD_33}$ | Optional pullup/ pulldown resistor | External arbiter enable<br>0 = Internal arbiter enabled<br>1 = External arbiter enabled |
| GPIO0 // $\overline{\text{CLKRUN}}$ | N09 | N09 | 55 | I/O | LV CMOS | $V_{DD_33}$ | Optional pullup resistor | General-purpose I/O 0/clock run. This terminal functions as a GPIO controlled by bit 0 (GPIO0_DIR) in the GPIO control register (see *Section 8.4.60*) or the clock run terminal. This terminal is used as clock run input when the bridge is placed in clock run mode.<br>**Note**: In clock run mode, an external pullup resistor is required to prevent the $\overline{\text{CLKRUN}}$ signal from floating.<br>**Note**: This terminal has an internal active pullup resistor. The pullup is only active when reset is asserted or when the GPIO is configured as an input. |
| GPIO1 // PWR_ OVRD | M09 | M09 | 56 | I/O | LV CMOS | $V_{DD_33}$ | – | General-purpose I/O 1/power override. This terminal functions as a GPIO controlled by bit 1 (GPIO1_DIR) in the GPIO control register (see *Section 8.4.60*) or the power override output terminal. GPIO1 becomes PWR_OVRD when bits 22:20 (POWER_OVRD) in the general control register are set to 001b or 011b (see *Section 8.4.66*).<br>**Note**: This terminal has an internal active pullup resistor. The pullup is only active when reset is asserted or when the GPIO is configured as an input. |
| GPIO2 | N10 | N10 | 57 | I/O | LV CMOS | $V_{DD_33}$ | – | General-purpose I/O 2. This terminal functions as a GPIO controlled by bit 2 (GPIO2_DIR) in the GPIO control register (see *Section 8.4.60*).<br>**Note**: This terminal has an internal active pullup resistor. The pullup is only active when reset is asserted or when the GPIO is configured as an input. |
| GPIO3 // SDA | N11 | L08 | 58 | I/O | LV CMOS | $V_{DD_33}$ | Optional pullup resistor | GPIO3 or serial-bus data. This terminal functions as serial-bus data if a pullup resistor is detected on SCL or when the SBDETECT bit is set in the Serial Bus Control and Status Register (see *Section 8.4.59*). If no pullup is detected then this terminal functions as GPIO3.<br>**Note**: In serial-bus mode, an external pullup resistor is required to prevent the SDA signal from floating. |

Copyright © 2021 Texas Instruments Incorporated

**Miscellaneous Pins (continued)**

| SIGNAL | ZWS BALL NO. | ZAJ BALL NO. | PNP PIN NO. | I/O TYPE | CELL TYPE | CLAMP RAIL | EXTERNAL PARTS | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| GPIO4 // SCL | M10 | M10 | 59 | I/O | LV CMOS | $V_{DD_33}$ | Optional pullup resistor | GPIO4 or serial-bus clock. This terminal functions as serial-bus clock if a pullup resistor is detected on SCL or when the SBDETECT bit is set in the Serial Bus Control and Status Register (see *Section 8.4.59*). If no pullup is detected then this terminal functions as GPIO4. **Note**: In serial-bus mode, an external pullup resistor is required to prevent the SCL signal from floating. **Note**: This terminal has an internal active pullup resistor. The pullup is only active when reset is asserted or when the GPIO is configured as an input. |
| $\overline{\text{GRST}}$ | N13 | M11 | 66 | I | LV CMOS | $V_{DD_33_COMBIO}$ | – | Global reset input. Asynchronously resets all logic in device, including sticky bits and power management state machines. **Note**: The GRST input buffer has both hysteresis and an internal active pullup. The pullup is active at all times. |
| PCLK66_ SEL | B12 | A11 | 98 | I | LV CMOS | $V_{DD_33}$ | Optional pulldown resistor | PCI clock select. This terminal determines the default PCI clock frequency driven out the CLKOUTx terminals. 0 = 50 MHz PCI Clock 1 = 66 MHz PCI Clock **Note**: This terminal has an internal active pullup resistor. This pullup is active at all times. **Note**: M66EN terminal also has an affect of PCI clock frequency. |
| SERIRQ | N08 | M08 | 52 | I/O | PCI Bus | PCIR | Pullup or pulldown resistor | Serial IRQ interface. This terminal functions as a serial IRQ interface if a pullup is detected when $\overline{\text{PERST}}$ is deasserted. If a pulldown is detected, then the serial IRQ interface is disabled. |
| VREG_ PD33 | D12 | E11 | 90 | I | LV CMOS | $V_{DD_33_COMBIO}$ | Pulldown resistor | 3.3-V voltage regulator powerdown. This terminal should always be tied directly to ground or an optional pulldown resistor can be used. |


Copyright © 2021 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD_33}$ | Supply voltage range | | –0.5 | 3.6 | V |
| $V_{DD_15}$ | | | –0.5 | 1.65 | V |
| $V_I$ | Input voltage range | PCI | –0.5 | PCIR + 0.5 | V |
| | | PCI Express (RX) | –0.6 | 1.2 | V |
| | | PCI Express REFCLK (single-ended) | –0.5 | $V_{DD_33}$ + 0.5 | V |
| | | PCI Express REFCLK (differential) | –0.5 | $V_{DD_15}$ + 0.5 | V |
| | | Miscellaneous 3.3-V IO | –0.5 | $V_{DD_33}$ + 0.5 | V |
| $V_O$ | Output voltage range | PCI | –0.5 | $V_{DD_33}$ + 0.5 | V |
| | | PCI Express (TX) | –0.55 | $V_{DD_15}$ + 0. | V |
| | | Miscellaneous 3.3-V IO | –0.5 | $V_{DD_33}$ + 0.5 | V |
| | Input clamp current, ($V_I$ < 0 or $V_I$ > VDD)(2) | | | ±20 | mA |
| | Output clamp current, ($V_O$ < 0 or $V_O$ > VDD)(3) | | | ±20 | mA |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Applies for external input and bidirectional buffers. $V_I$ < 0 or $V_I$ > $V_{DD}$ or $V_I$ > PCIR.

(3) Applies for external input and bidirectional buffers. $V_O$ < 0 or $V_O$ > $V_{DD}$ or $V_O$ > PCIR.

## 6.2 Handling Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | –65 | 150 | °C |
| $V_{ESD-HBM}$ (1) | Human body model ESD rating (R = 1.5 K, C = 100 pF) | | 2 | kV |
| $V_{ESD-CDM}$ (1) | Charged device model ESD rating (200 pF) | | 500 | V |

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.

## 6.3 Recommended Operating Conditions

| | | OPERATION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD_15}$ | Supply voltage | 1.5 V | 1.35 | 1.5 | 1.65 | V |
| $V_{DDA_15}$ | | | | | | |
| $V_{DD_33}$ | Supply voltage | 3.3 V | 3 | 3.3 | 3.6 | V |
| $V_{DDA_33}$ | | | | | | |
| $V_{DDA_33_AUX}$ | | | | | | |
| PCIR | PCI bus clamping rail voltage (with 1 kΩ resistor) | 3.3 V | 3 | 3.3 | 3.6 | V |
| | | 5 V | 4.75 | 5 | 5.25 | |

Copyright © 2021 Texas Instruments Incorporated

## 6.4 Thermal Information (1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PNP** | | | | | | |
| $\theta_{JA}$ | Junction-to-free-air thermal resistance | Low-K JEDEC test board, 1s (single signal layer), no air flow | | 50.8 | | °C/W |
| | | High-K JEDEC test board, 2s2p (double signal layer, double buried power plane), no air flow | | 24.9 | | |
| $\theta_{JC}$ | Junction-to-case thermal resistance | Cu cold plate measurement process | | 18.9 | | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | EIA/JESD 51-8 | | 14.6 | | °C/W |
| $\psi_{JT}$ | Junction-to-top of package | EIA/JESD 51-2 | | 0.26 | | °C/W |
| $\psi_{JB}$ | Junction-to-board | EIA/JESD 51-6 | | 7.93 | | °C/W |
| $T_A$ | Operating ambient temperature range | XIO2001PNP | 0 | | 70 | °C |
| | | XIO2001IPNP | –40 | | 85 | |
| $T_J$ | Virtual junction temperature | XIO2001PNP | 0 | | 105 | °C |
| | | XIO2001IPNP | –40 | | 105 | |
| **ZAJ** | | | | | | |
| $\theta_{JA}$ | Junction-to-free-air thermal resistance | Low-K JEDEC test board, 1s (single signal layer), no air flow | | 82 | | °C/W |
| | | High-K JEDEC test board, 2s2p (double signal layer, double buried power plane), no air flow | | 58.8 | | |
| $\theta_{JC}$ | Junction-to-case thermal resistance | Cu cold plate measurement process | | 19 | | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | EIA/JESD 51-8 | | 32 | | °C/W |
| $\psi_{JT}$ | Junction-to-top of package | EIA/JESD 51-2 | | 0.5 | | °C/W |
| $\psi_{JB}$ | Junction-to-board | EIA/JESD 51-6 | | 30 | | °C/W |
| $T_A$ | Operating ambient temperature range | XIO2001ZAJ | 0 | | 70 | °C |
| | | XIO2001IZAJ | –40 | | 85 | |
| $T_J$ | Virtual junction temperature | XIO2001ZAJ | 0 | | 105 | °C |
| | | XIO2001IZAJ | –40 | | 105 | |
| **ZWS** | | | | | | |
| $\theta_{JA}$ | Junction-to-free-air thermal resistance | High-K JEDEC test board, 2s2p (double signal layer, double buried power plane), no air flow | | 36.2 | | °C/W |
| $\theta_{JC}$ | Junction-to-case thermal resistance | Cu cold plate measurement process | | 18.3 | | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | EIA/JESD 51-8 | | 20.3 | | °C/W |
| $\psi_{JT}$ | Junction-to-top of package | EIA/JESD 51-2 | | 0.4 | | °C/W |
| $\psi_{JB}$ | Junction-to-board | EIA/JESD 51-6 | | 20.1 | | °C/W |
| $T_A$ | Operating ambient temperature range | XIO2001ZWS | 0 | | 70 | °C |
| | | XIO2001IZWS | –40 | | 85 | |
| $T_J$ | Virtual junction temperature | XIO2001ZWS | 0 | | 105 | °C |
| | | XIO2001IZWS | –40 | | 105 | |

(1) For more details, refer to TI application note *IC Package Thermal Metrics* (SPRA953).

## 6.5 Nominal Power Consumption

| DEVICES | POWER STATE(1) | VOLTS | AMPERES | WATTS |
|---|---|---|---|---|
| No downstream PCI devices | D0 idle | 1.5 | 0.147 | 0.221 |
| | | 3.3 | 0.062 | 0.205 |
| | | **TOTALS:** | 0.209 | 0.426 |


Copyright © 2021 Texas Instruments Incorporated

| DEVICES | POWER STATE(1) | VOLTS | AMPERES | WATTS |
|---|---|---|---|---|
| One downstream PCI device | D0 idle | 1.5 | 0.148 | 0.222 |
| | | 3.3 | 0.077 | 0.254 |
| | | **TOTALS:** | 0.225 | 0.476 |
| One downstream PCI device | D0 active | 1.5 | 0.157 | 0.236 |
| | | 3.3 | 0.165 | 0.545 |
| | | **TOTALS:** | 0.322 | 0.780 |
| One downstream (max voltage) | D0 active | 1.65 | 0.168 | 0.277 |
| | | 3.6 | 0.188 | 0.677 |
| | | **TOTALS:** | 0.356 | 0.954 |

(1) D0 idle power state: Downstream PCI device is in PCI state D0. Downstream device driver is loaded. Downstream device is not actively transferring data.
D0 active power state: Downstream PCI device is in PCI state D0. Downstream device driver is loaded. Downstream device is acitvely transferring data (worst case scenario).

## 6.6 PCI Express Differential Transmitter Output Ranges

| PARAMETER | TERMINALS | MIN | NOM | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| $UI$(1)<br>Unit interval | TXP, TXN | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations. |
| $V_{TX-DIFF-PP}$<br>Differential peak-to-peak output voltage | TXP, TXN | 0.8 | | 1.2 | V | $V_{TX-DIFF-PP} = 2*\|V_{TXP} – V_{TXN}\|$ |
| $V_{TX-DIFF-PP-LOW}$<br>Low-power differential peak-to-peak TX voltage swing | TXP, TXN | 0.4 | | 1.2 | V | $V_{TX-DIFF-PP} = 2*\|V_{TXP} – V_{TXN}\|$ |
| $V_{TX-DE-RATIO-3.5dB}$<br>TX de-emphasis level ratio | TXP, TXN | 3 | | 4 | dB | This is the ratio of the $V_{TX-DIFF-PP}$ of the second and following bits after a transition divided by the $V_{TX-DIFF-PP}$ of the first bit after a transition. |
| $T_{TX-EYE}$ (2) (3) (4)<br>Minimum TX eye width | TXP, TXN | 0.75 | | | UI | Does not include SSC or $Ref_{CLK}$ jitter. Includes $R_j$ at $10^{-12}$. |
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ (2)<br>Maximum time between the jitter median and maximum deviation from the median | TXP, TXN | | | 0.125 | UI | Measured differentially at zero crossing points after applying the 2.5 GT/s clock recovery function. |
| $T_{TX-RISE-FALL}$ (2)<br>TX output rise/fall time | TXP, TXN | 0.125 | | | UI | Measured differentially from 20% to 80% of swing. |
| $BW_{TX-PLL}$ (6)<br>Maximum TX PLL bandwidth | TXP, TXN | | | 22 | MHz | Second order PLL jitter transfer bounding function. |
| $BW_{TX-PLL-LO-3DB}$ (6) (7)<br>Minimum TX PLL bandwidth | TXP, TXN | 1.5 | | | MHz | Second order PLL jitter transfer bounding function. |
| $RL_{TX-DIFF}$<br>Tx package plus Si differential return loss | TXP, TXN | 10 | | | dB | |
| $RL_{TX-CM}$<br>Tx package plus Si common mode return loss | TXP, TXN | 6 | | | dB | Measured over 0.05–1.25 GHz range |
| $Z_{TX-DIFF_DC}$<br>DC differential TX impedance | TXP, TXN | 80 | | 120 | Ω | Low impedance defined during signaling. |
| $V_{TX-CM-AC-P}$ (5)<br>$T_X$ AC common mode voltage | TXP, TXN | | | 20 | mV | |
| $I_{TX-SHORT}$<br>Transmitter short-circuit current limit | TXP, TXN | | | 90 | mA | The total current transmitter can supply when shorted to ground. |
| $V_{TX-DC-CM}$<br>Transmitter DC common-mode voltage | TXP, TXN | 0 | | 3.6 | V | The allowed DC common-mode voltage at the transmitter pins under any conditions. |
| $V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$<br>Absolute delta of DC common mode voltage during L0 and electrical idle | TXP, TXN | 0 | | 100 | mV | \|VTX-CM-DC – VTX-CM-Idle-DC\| ≤ 100 mV<br>$V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ [during L0]<br>$V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ [during electrical idle] |
| $V_{TX-CM-DC-LINE-DELTA}$<br>Absolute delta of DC common mode voltage between P and N | TXP, TXN | 0 | | 25 | mV | $\|V_{TXP-CM-DC} – V_{TXN-CM-DC}\|$ ≤25 mV when<br>$V_{TXP-CM-DC} = DC_{(avg)}$ of $\|V_{TXP}\|$ [during L0]<br>$V_{TXN-CM-DC} = DC_{(avg)}$ of $\|V_{TXN}\|$ [during L0] |

Copyright © 2021 Texas Instruments Incorporated

| PARAMETER | TERMINALS | MIN | NOM | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| $V_{TX-IDLE-DIFF-AC-p}$ Electrical idle differential peak output voltage | TXP, TXN | 0 | | 20 | mV | $V_{TX-IDLE-DIFFp} = \|V_{TXP-Idle} – V_{TXN-Idle}\| \leq 20$ mV |
| $V_{TX-RCV-DETECT}$ The amount of voltage change allowed during receiver detection | TXP, TXN | | | 600 | mV | The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. |
| $T_{TX-IDLE-MIN}$ Minimum time spent in electrical idle | TXP, TXN | 20 | | | ns | Minimum time a transmitter must be in electrical idle. |
| $T_{TX-IDLE-SET-TO-IDLE}$ Maximum time to transition to a valid electrical idle after sending an EIOS | TXP, TXN | | | 8 | ns | After sending the required number of EIOSs, the transmitter must meet all electrical idle specifications within this time. This is measured from the end of the last EIOS to the transmitter in electrical idle. |
| $T_{TX-IDLE-TO-DIFF-DATA}$ Maximum time to transition to a valid diff signaling after leaving electrical idle | TXP, TXN | | | 8 | ns | Maximum time to transistion to valid diff signaling after leaving electrical idle. This is considered a debounce time to the Tx. |
| $C_{TX}$ AC coupling capacitor | TXP, TXN | 75 | | 200 | nF | All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. |

(1) SCC permits a 0, –5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.
(2) Measurements at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although deconvolution is recommended.
(3) Transmitter jitter is measured by driving the transmitter under test with a low jitter "ideal" clock and connecting the DUT to a reference board.
(4) Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.
(5) Measurement is made over at least 10 UI.
(6) The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table.
(7) A single combination of PLL BW and peaking is specified for 2.5 GT/s implemenations.

## 6.7 PCI Express Differential Receiver Input Ranges

| PARAMETER | TERMINALS | MIN | NOM | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| UI(1) Unit interval | RXP, RXN | 399.88 | | 400.12 | ps | Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations. |
| $V_{RX-DIFF-PP-CC}$ (2) Differential input peak-to-peak voltage | RXP, RXN | 0.175 | | 1.200 | V | $V_{RX-DIFFp-p} = 2*\|V_{RXP} – V_{RXN}\|$ |
| $T_{RX-EYE}$ (2) (3) Minimum receiver eye width | RXP, RXN | 0.4 | | | UI | The maximum interconnect media and transmitter jitter that can be tolerated by the receiver is derived as $T_{RX-MAX-JITTER} = 1 – T_{RX-EYE} = 0.6$ UI |
| $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ (2) (3) Maximum time between the jitter median and maximum deviation from the median | RXP, RXN | | | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the TX UI. |
| $BW_{RX-PLL-HI}$ (6) Maximum Rx PLL bandwidth | RXP, RXN | | | 22 | MHz | Second order PLL jitter transfer bounding function. |
| $BW_{RX-PLL-LO-3DB}$ (6) Minimum Rx PLL for 3 dB peaking | RXP, RXN | 1.5 | | | MHz | Second order PLL jitter transfer bounding function. |
| $V_{RX-CM-AC-P}$ (2) AC peak common mode input voltage | RXP, RXN | | | 150 | mV | $V_{RX-CM-AC-P} = RMS(\|V_{RXP} + V_{RXN}\|/2 – V_{RX-CM-DC})$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{RXP} + V_{RXN}\|/2$. |
| $RL_{RX-DIFF}$ (4) Differential return loss | RXP, RXN | 10 | | | dB | Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and –300 mV, respectively. |
| $RL_{RX-CM}$ (4) Common mode return loss | RXP, RXN | 6 | | | dB | Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and –300 mV, respectively. |
| $Z_{RX-DIFF-DC}$ (5) DC differential input impedance | RXP, RXN | 80 | | 120 | Ω | RX dc differential mode impedance |
| $Z_{RX-DC}$ (4) (5) DC input impedance | RXP, RXN | 40 | | 60 | Ω | Required RXP as well as RXN dc impedance (50 Ω ±20% tolerance). |


Copyright © 2021 Texas Instruments Incorporated

| PARAMETER | TERMINALS | MIN | NOM | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| $Z_{RX-HIGH-IMP-DC-POS}$ (7) DC input CM input impedance for V > 0 during reset or powerdown | RXP, RXN | 50 | | | kΩ | Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 to 200 mV with respect to ground. |
| $Z_{RX-HIGH-IMP-DC-NEG}$ (7) DC input CM input impedance for V > 0 during reset or powerdown | RXP, RXN | 1 | | | kΩ | Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 to 200 mV with respect to ground. |
| $V_{RX-IDLE-DET-DIFFp-p}$ Electrical idle detect threshold | RXP, RXN | 65 | | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p}$ = 2*\|$V_{RXP}$ – $V_{RXN}$\| measured at the receiver package terminals |
| $T_{RX-IDLE-DET-DIFF-ENTER-TIME}$ Unexpected electrical idle enter detect threshold integration time | RXP, RXN | | | 10 | ms | An unexpected electrical idle ($V_{RX-DIFFp-p}$ < $V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTER-TIME}$ to signal an unexpected idle condition. |

(1) No test load is necessarily associated with this value.

(2) Specified at the measurement point and measured over any 250 consecutive UIs. A test load must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UIs is used as a reference for the eye diagram.

(3) A TRX-EYE = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UIs must be used as the reference for the eye diagram.

(4) The receiver input impedance results in a differential return loss greater than or equal to 15 dB with the P line biased to 300 mV and the N line biased to .300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 . to ground for both the P and N line (i.e., as measured by a Vector Network Analyzer with 50-. probes). The series capacitors CTX is optional for the return loss measurement.

(5) Impedance during all link training status state machine (LTSSM) states. When transitioning from a PCI Express reset to the detect state (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on the unconfigured lane of a port.

(6) A single PLL bandwidth and peaking value of 1.5 to 22 MHz and 3 dB are defined.

(7) $Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined respectively for negative and postive voltages at the input of the receiver.

## 6.8 PCI Express Differential Reference Clock Input Ranges (1)

| PARAMETER | TERMINALS | MIN | NOM | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|---|
| $f_{IN-DIFF}$ Differential input frequency | REFCLK+ REFCLK– | | 100 | | MHz | The input frequency is 100 MHz + 300 ppm and –2800 ppm including SSC-dictated variations. |
| $f_{IN-SE}$ Single-ended input frequency | REFCLK+ | | 125 | | MHz | The input frequency is 125 MHz + 300 ppm and –300 ppm. |
| $V_{RX-DIFFp-p}$ Differential input peak-to-peak voltage | REFCLK+ REFCLK– | 0.175 | | 1.2 | V | $V_{RX-DIFFp-p}$ = 2*\|$V_{REFCLK+}$ – $V_{REFCLK-}$\| |
| $V_{IH-SE}$ | REFCLK+ | 0.7 $V_{DDA_33}$ | | $V_{DDA_33}$ | V | Single-ended, reference clock mode high-level input voltage |
| $V_{IL-SE}$ | REFCLK+ | 0 | | 0.3 $V_{DDA_33}$ | V | Single-ended, reference clock mode low-level input voltage |
| $V_{RX-CM-ACp}$ AC peak common mode input voltage | REFCLK+ REFCLK– | | | 140 | mV | $V_{RX-CM-ACp}$ = RMS(\|$V_{REFCLK+}$ + $V_{REFCLK-}$\|/2 $V_{RX-CM-DC}$) $V_{RX-CM-DC}$ = $DC_{(avg)}$ of \|$V_{REFCLK+}$ + $V_{REFCLK-}$\|/2 |
| Duty cycle | REFCLK+ REFCLK– | 40% | | 60% | | Differential and single-ended waveform input duty cycle |
| $Z_{C-DC}$ Clock source DC impedance | REFCLK+ REFCLK– | 40 | | 60 | Ω | REFCLK± dc differential mode impedance |
| $Z_{RX-DC}$ DC input impedance | REFCLK+ REFCLK– | | 20 | | kΩ | REFCLK+ dc single-ended mode impedance |

(1) The XIO2001 is compliant with the defined system jitter models for a PCI-Express reference clock and associated TX/RX link. Any usage of the XIO2001 in a system configuration that does not conform to the defined system jitter models requires the system designer to validate the system jitter budgets.

Copyright © 2021 Texas Instruments Incorporated

## 6.9 PCI Bus Electrical Characteristics

over recommended operating conditions(3)

| PARAMETER | | OPERATION | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage(1) | PCIR = 3.3 V | | 0.5 × $V_{DD_33}$ | PCIR + 0.5 | V |
| | | PCIR = 5 V | | 2.0 | PCIR + 0.5 | |
| $V_{IL}$ | Low-level input voltage(1) | PCIR = 3.3 V | | –0.5 | 0.3 × $V_{DD_33}$ | V |
| | | PCIR = 5 V | | –0.5 | 0.8 | |
| $V_I$ | Input voltage | | | 0 | PCIR | V |
| $V_O$ | Output voltage(2) | | | 0 | $V_{DD_33}$ | V |
| $t_t$ | Input transition time ($t_{rise}$ and $t_{fall}$) | | | 1 | 4 | ns |
| $V_{OH}$ | High-level output voltage | PCIR = 3.3 V | $I_{OH}$ = –500 µA | 0.9 × $V_{DD_33}$ | | V |
| | | PCIR = 5 V | $I_{OH}$ = –2 mA | 2.4 | | |
| $V_{OL}$ | Low-level output voltage | PCIR = 3.3 V | $I_{OH}$ = 1500 µA | | 0.1 × $V_{DD_33}$ | V |
| | | PCIR = 5 V | $I_{OH}$ = 6 mA | | 0.55 | |
| $I_{OZ}$ | High-impedance, output current(2) | PCIR = 3.3 V | | | ±10 | µA |
| | | PCIR = 5 V | | | ±70 | |
| $I_I$ | Input current | PCIR = 3.3 V | | | ±10 | µA |
| | | PCIR = 5 V | | | ±70 | |

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) This table applies to CLK, CLKOUT6:0, AD31:0, C/BE[3:0], DEVSEL, FRAME, GNT5:0, INTD:A, IRDY, PAR, PERR, REQ5:0, PRST, SERR, STOP, TRDY, SERIRQ, M66EN, and LOCK terminals.

## 6.10 3.3-V I/O Electrical Characteristics

over recommended operating conditions(5)

| PARAMETER | | OPERATION | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage(1) | $V_{DD_33}$ | | 0.7 $V_{DD_33}$ | $V_{DD_33}$ | V |
| $V_{IL}$ | VIL Low-level input voltage (1) | $V_{DD_33}$ | | 0 | 0.3 $V_{DD_33}$ | V |
| $V_I$ | Input voltage | | | 0 | $V_{DD_33}$ | V |
| $V_O$ | Output voltage(2) | | | 0 | $V_{DD_33}$ | V |
| $t_t$ | Input transition time ($t_{rise}$ and $t_{fall}$) | | | 0 | 25 | ns |
| $V_{hys}$ | Input hysteresis(4) | | | | 0.13 $V_{DD_33}$ | V |
| $V_{OH}$ | High-level output voltage | $V_{DD_33}$ | $I_{OH}$ = –4 mA | 0.8 $V_{DD_33}$ | | V |
| $V_{OL}$ | Low-level output voltage | $V_{DD_33}$ | $I_{OL}$ = 4 mA | | 0.22 $V_{DD_33}$ | V |
| $I_{OZ}$ | High-impedance, output current(2) | $V_{DD_33}$ | $V_I$ = 0 to $V_{DD_33}$ | | ±20 | µA |
| $I_{OZP}$ | High-impedance, output current with internal pullup or pulldown resistor(5) | $V_{DD_33}$ | $V_I$ = 0 to $V_{DD_33}$ | | ±100 | µA |
| $I_I$ | Input current(3) | $V_{DD_33}$ | $V_I$ = 0 to $V_{DD_33}$ | | ±1 | µA |

(1) Applies to external inputs and bidirectional buffers.
(2) Applies to external outputs and bidirectional buffers.
(3) Applies to external input buffers.
(4) Applies to PERST, GRST, and PME.
(5) Applies to GRST (pullup), EXT_ARB_EN (pulldown), CLKRUN_EN (pulldown), and most GPIO (pullup).


Copyright © 2021 Texas Instruments Incorporated

## 6.11 PCI Bus Timing Requirements

over recommended operating conditions(1)

| PARAMETER | | TEST CONDITION | 33 MHz | | 66 MHz | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | CLK to shared signal valid propagation delay time | $C_L$ = 50 pF | | 11 | | | ns |
| | | $C_L$ = 30 pF | | | | 6 | |
| | CLK to shared signal invalid propagation delay time | $C_L$ = 50 pF | 2 | | | | |
| | | $C_L$ = 30 pF | | | 1 | | |
| $t_{ON}$ | tEnable time, high-impedance-to-active delay time from CLK | $C_L$ = 50 pF | 2 | | | | ns |
| | | $C_L$ = 30 pF | | | 1 | | |
| $t_{OFF}$ | Disable time, active-to-high-impedance delay time from CLK | $C_L$ = 50 pF | | 28 | | | ns |
| | | $C_L$ = 30 pF | | | | 14 | |
| $t_{su}$ | Setup time on shared signals before CLK valid (rising edge) | | 7 | | 3 | | ns |
| $t_h$ | Hold time on shared signals after CLK valid (rising edge) | | 0 | | 0 | | ns |

(1) The PCI shared signals are AD31:0, $\overline{C/BE[3:0]}$, $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{STOP}$, IDSEL, $\overline{DEVSEL}$, $\overline{LOCK}$, SERIRQ, PAR, $\overline{PERR}$, $\overline{SERR}$, and $\overline{CLKRUN}$.

## 6.12 Power-Up/-Down Sequencing

The bridge contains both 1.5-V and 3.3-V power terminals. The following power-up and power-down sequences describe how power is applied to these terminals.

In addition, the bridge has three resets: $\overline{PERST}$, $\overline{GRST}$ and an internal power-on reset. These resets are fully described in *Section 8.3.1*. The following power-up and power-down sequences describe how $\overline{PERST}$ is applied to the bridge.

The application of the PCI Express reference clock (REFCLK) is important to the power-up/-down sequence and is included in the following power-up and power-down descriptions.

### 6.12.1 Power-Up Sequence

1. Assert $\overline{GRST}$ and $\overline{PERST}$ to the device.
2. Apply 1.5-V and 3.3-V voltages.
3. Deassert $\overline{GRST}$.
4. Apply a stable PCI Express reference clock.
5. To meet PCI Express specification requirements, $\overline{PERST}$ cannot be deasserted until the following two delay requirements are satisfied:
   - Wait a minimum of 100 µs after applying a stable PCI Express reference clock. The 100-µs limit satisfies the requirement for stable device clocks by the deassertion of $\overline{PERST}$.
   - Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the deassertion of $\overline{PERST}$.

See the power-up sequencing diagram in Figure 6-1.

Copyright © 2021 Texas Instruments Incorporated

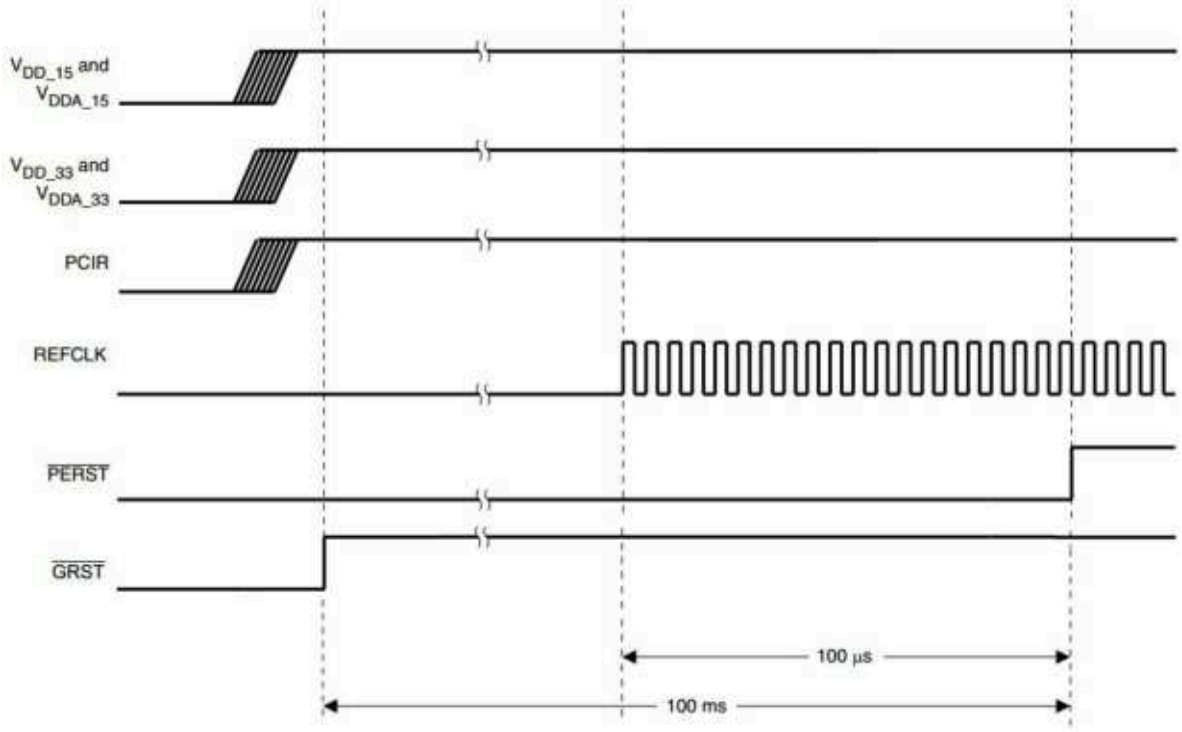



**Figure 6-1. Power-Up Sequence**


Copyright © 2021 Texas Instruments Incorporated

### 6.12.2 Power-Down Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Remove the reference clock.
3. Remove PCIR clamp voltage.
4. Remove 3.3-V and 1.5-V voltages.

See the power-down sequencing diagram in Figure 6-2. If the $V_{DD_33_AUX}$ terminal is to remain powered after a system shutdown, then the bridge power-down sequence is exactly the same as shown in Figure 6-2.

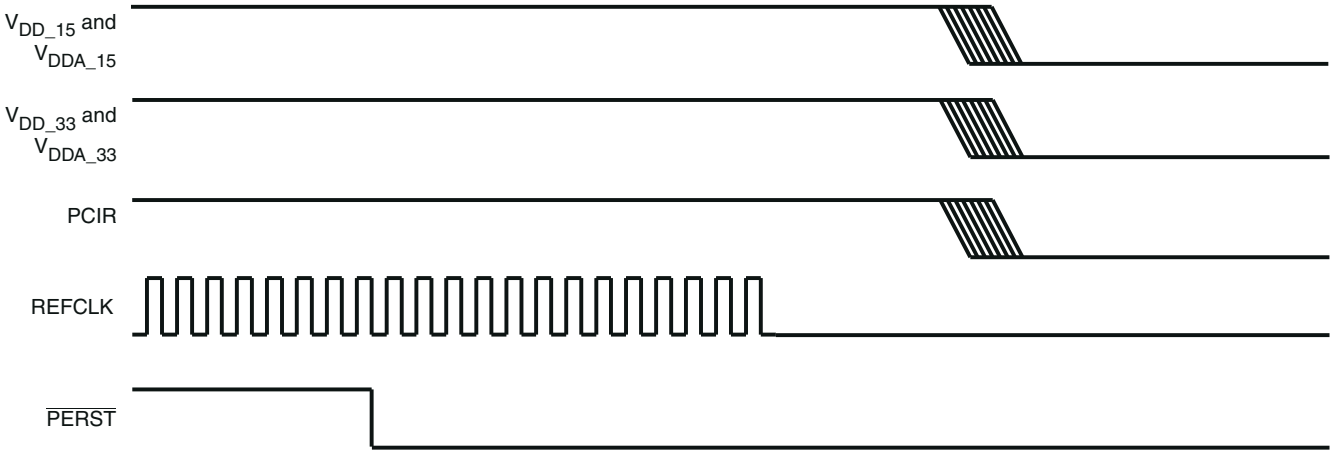



**Figure 6-2. Power-Down Sequence**

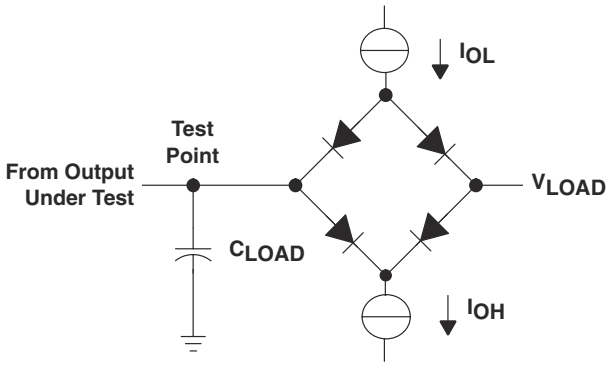
# 7 Parameter Measurement Information

**LOAD CIRCUIT PARAMETERS**

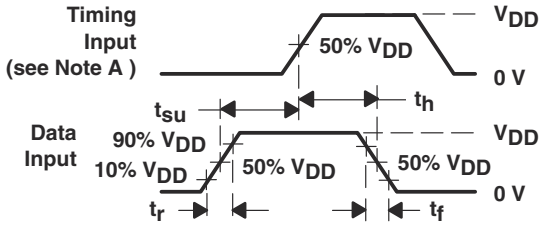
| TIMING PARAMETER | | $C_{LOAD}$† (pF) | $I_{OL}$ (mA) | $I_{OH}$ (mA) | $V_{LOAD}$ (V) |
|---|---|---|---|---|---|
| $t_{en}$ | $t_{PZH}$ | 30/50 | 12 | - 12 | 0 |
| | $t_{PZL}$ | | | | 3 |
| $t_{dis}$ | $t_{PHZ}$ | 30/50 | 12 | - 12 | 1.5 |
| | $t_{PLZ}$ | | | | |
| $t_{pd}$ | | 30/50 | 12 | - 12 | ‡ |

† $C_{LOAD}$ includes the typical load-circuit distributed capacitance.

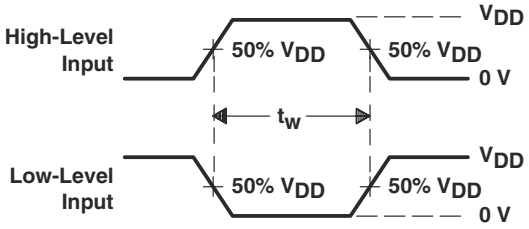
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}}$ = 50 Ω, where $V_{OL}$ = 0.6 V, $I_{OL}$ = 12 mA



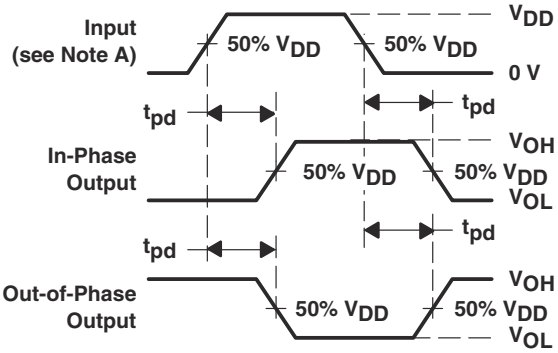

**LOAD CIRCUIT**



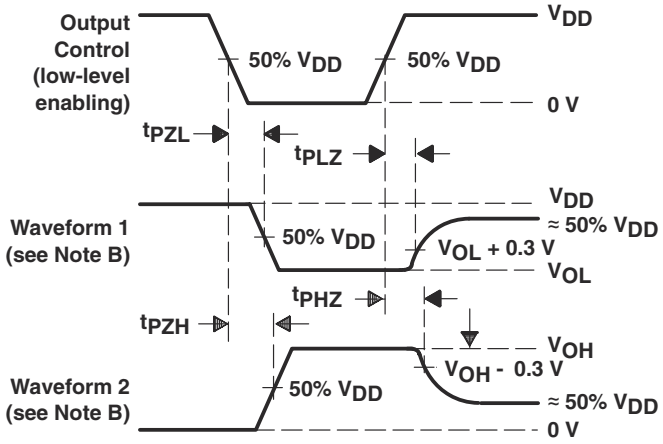

**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**
**INPUT RISE AND FALL TIMES**




**VOLTAGE WAVEFORMS**
**PULSE DURATION**




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**




**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, $Z_O$ = 50 Ω, $t_r \le 6$ ns, $t_f \le 6$ ns.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. For $t_{PLZ}$ and $t_{PHZ}$, $V_{OL}$ and $V_{OH}$ are measured values.

**Figure 7-1. Load Circuit And Voltage Waveforms**


Copyright © 2021 Texas Instruments Incorporated

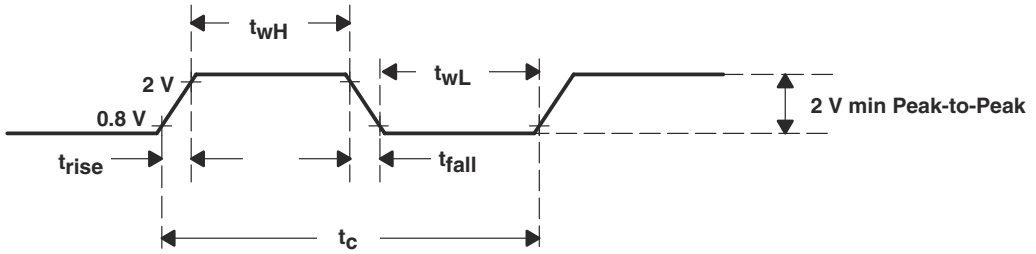



**Figure 7-2. CLK Timing Waveform**

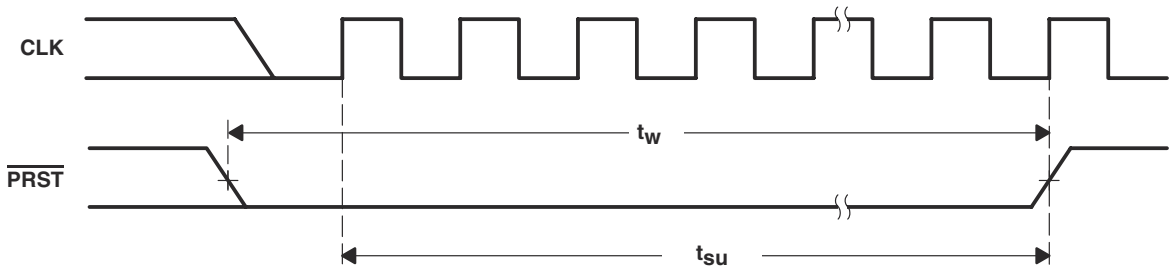



**Figure 7-3. $\overline{\text{PRST}}$ Timing Waveforms**

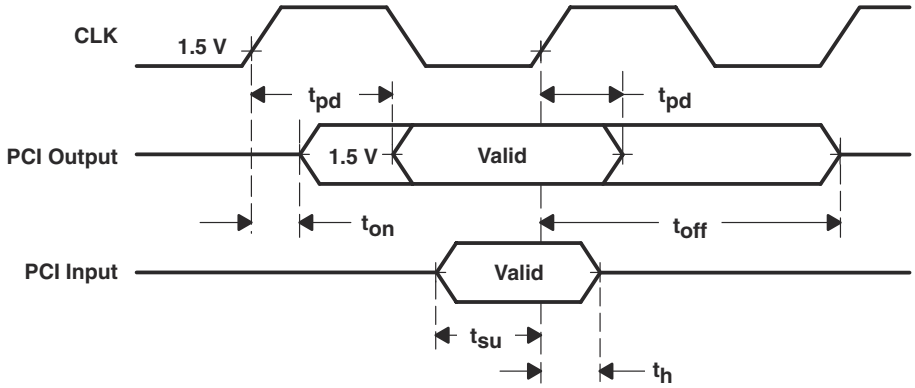



**Figure 7-4. Shared Signals Timing Waveforms**

Copyright © 2021 Texas Instruments Incorporated

# 8 Detailed Description

## 8.1 Overview

The Texas Instruments XIO2001 is a PCI Express to PCI local bus translation bridge that provides full PCI Express and PCI local bus functionality and performance.

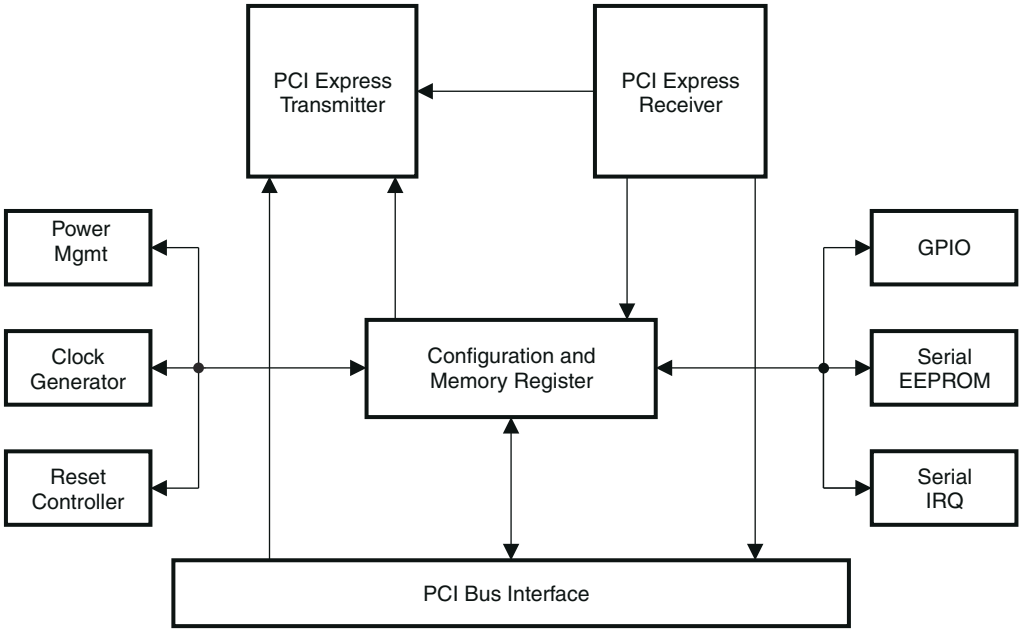
Power management (PM) features include active state link PM, PME mechanisms, the beacon and wake protocols, and all conventional PCI D-states. If the active state link PM is enabled, then the link automatically saves power when idle using the L0s and L1 states. PM active state NAK, PM PME, and PME-to-ACK messages are supported. Standard PCI bus power management features provide several low power modes, which enable the host system to further reduce power consumption.

The bridge has additional capabilities including, but not limited to, serial IRQ with MSI messages, serial EEPROM, power override, clock run, PCI Express clock request and PCI bus $\overline{\text{LOCK}}$. Also, five general-purpose inputs and outputs (GPIOs) are provided for further system control and customization.

Robust pipeline architecture is implemented to minimize system latency across the bridge. If parity errors are detected, then packet poisoning is supported for both upstream and downstream operations.

The PCI local bus is fully compliant with the *PCI Local Bus Specification* (Revision 2.3) and associated programming model. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The PCI bus interface is 32-bit and can operate at either 25 MHz, 33 MHz, 50 MHz, or 66 MHz. Also, the PCI interface provides fair arbitration and buffered clock outputs for up to 6 subordinate devices.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Bridge Reset Features

There are five bridge reset options that include internally-generated power-on reset, resets generated by asserting input terminals, and software-initiated resets that are controlled by sending a PCI Express hot reset or setting a configuration register bit. Table 8-1 identifies these reset sources and describes how the bridge responds to each reset.


Copyright © 2021 Texas Instruments Incorporated

**Table 8-1. XIO2001 Reset Options**

| RESET OPTION | XIO2001 FEATURE | RESET RESPONSE |
|---|---|---|
| Bridge internally-generated power-on reset | During a power-on cycle, the bridge asserts an internal reset and monitors the $V_{DD_15_COMB}$ terminal. When this terminal reaches 90% of the nominal input voltage specification, power is considered stable. After stable power, the bridge monitors the PCI Express reference clock (REFCLK) and waits 10 µs after active clocks are detected. Then, internal power-on reset is deasserted. | When the internal power-on reset is asserted, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state.<br>In addition, the XIO2001 asserts the internal PCI bus reset. |
| Global reset input $\overline{GRST}$ | When $\overline{GRST}$ is asserted low, an internal power-on reset occurs. This reset is asynchronous and functions during both normal power states and $V_{AUX}$ power states. | When $\overline{GRST}$ is asserted low, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. In addition, the bridge asserts PCI bus reset ( $\overline{PRST}$). When the rising edge of $\overline{GRST}$ occurs, the bridge samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The bridge starts link training within 80 ms after $\overline{GRST}$ is deasserted. |
| PCI Express reset input $\overline{PERST}$ | This XIO2001 input terminal is used by an upstream PCI Express device to generate a PCI Express reset and to signal a system power good condition.<br>When $\overline{PERST}$ is asserted low, the XIO2001 generates an internal PCI Express reset as defined in the PCI Express specification.<br>When $\overline{PERST}$ transitions from low to high, a system power good condition is assumed by the XIO2001.<br>**Note:** The system must assert $\overline{PERST}$ before power is removed, before REFCLK is removed or before REFCLK becomes unstable. | When $\overline{PERST}$ is asserted low, all control register bits that are not sticky are reset. Within the configuration register maps, the sticky bits are indicated by the ☆ symbol. Also, all state machines that are not associated with sticky functionality are reset.<br>In addition, the XIO2001 asserts the internal PCI bus reset.<br>When the rising edge of $\overline{PERST}$ occurs, the XIO2001 samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The XIO2001 starts link training within 80 ms after $\overline{PERST}$ is deasserted. |
| PCI Express training control hot reset | The XIO2001 responds to a training control hot reset received on the PCI Express interface. After a training control hot reset, the PCI Express interface enters the DL_DOWN state. | In the DL_DOWN state, all remaining configuration register bits and state machines are reset. All remaining bits exclude sticky bits and EEPROM loadable bits. All remaining state machines exclude sticky functionality and EEPROM functionality.<br>Within the configuration register maps, the sticky bits are indicated by the ☆ symbol and the EEPROM loadable bits are indicated by the † symbol.<br>In addition, the XIO2001 asserts the internal PCI bus reset. |
| PCI bus reset $\overline{PRST}$ | System software has the ability to assert and deassert the $\overline{PRST}$ terminal on the secondary PCI bus interface. This terminal is the PCI bus reset. | When bit 6 (SRST) in the bridge control register at offset 3Eh (see *Section 8.4.30*) is asserted, the bridge asserts the $\overline{PRST}$ terminal. A 0 in the SRST bit deasserts the $\overline{PRST}$ terminal. |

### 8.3.2 PCI Express Interface

The XIO2001 has an x1 PCI Express interface that runs at 2.5 Gb/s and is fully compliant to the PCI Express Base Specification , Revision 2.0. The remainder of this section describes implementation considerations for the XIO2001 primary PCI Express interface.

#### *8.3.2.1 2.5-Gb/s Transmit and Receive Links*

The XIO2001 TX and RX terminals attach to the upstream PCI Express device over a 2.5-Gb/s high- speed differential transmit and receive PCI Express × 1 Link. The connection details are provided in Table 8-2.

Copyright © 2021 Texas Instruments Incorporated

**Table 8-2. XIO2001/PCI Express Device Pin Connection Details**

| PIN NAME | | COMMENTS |
|---|---|---|
| XIO2001 | UPSTREAM PCI EXPRESS DEVICE | |
| TXP | RXP | XIO2001's transmit positive differential pin connects to the upstream device's receive positive differential pin. |
| TXN | RXN | XIO2001's transmit positive differential pin connects to the upstream device's receive negative differential pin. |
| RXP | TXP | XIO2001's transmit positive differential pin connects to the upstream device's receive positive differential pin. |
| RXN | TXN | XIO2001's transmit positive differential pin connects to the upstream device's receive negative differential pin. |

The XIO2001 TXP and TXN terminals comprise a low-voltage, 100- Ω differentially driven signal pair. The RXP and RXN terminals for the XIO2001 receive a low-voltage, 100- Ω differentially driven signal pair. The XIO2001 has integrated 50- Ω termination resistors to $V_{SS}$ on both the RXP and RXN terminals eliminating the need for external components.

Each lane of the differential signal pair must be ac-coupled. The recommended value for the series capacitor is 0.1 µF. To minimize stray capacitance associated with the series capacitor circuit board solder pads, 0402-sized capacitors are recommended.

When routing a 2.5-Gb/s low-voltage, 100- Ω differentially driven signal pair, the following circuit board design guidelines must be considered:

1. The PCI-Express drivers and receivers are designed to operate with adequate bit error rate margins over a 20 ” maximum length signal pair routed through FR4 circuit board material.
2. Each differential signal pair must be 100- Ω differential impedance with each single-ended lane measuring in the range of 50 Ω to 55 Ω impedance to ground.
3. The differential signal trace lengths associated with a PCI Express high-speed link must be length matched to minimize signal jitter. This length matching requirement applies only to the P and N signals within a differential pair. The transmitter differential pair does not need to be length matched to the receiver differential pair. The absolute maximum trace length difference between the TXP signal and TXN signal must be less than 5 mils. This also applies to the RXP and RXN signal pair.
4. If a differential signal pair is broken into segments by vias, series capacitors, or connectors, the length of the positive signal trace must be length matched to the negative signal trace for each segment. Trace length differences over all segments are additive and must be less than 5 mils.
5. The location of the series capacitors is critical. For add-in cards, the series capacitors are located between the TXP/TXN terminals and the PCI-Express connector. In addition, the capacitors are placed near the PCI Express connector. This translates to two capacitors on the motherboard for the downstream link and two capacitors on the add-in card for the upstream link. If both the upstream device and the downstream device reside on the same circuit board, the capacitors are located near the TXP/TXN terminals for each link.
6. The number of vias must be minimized. Each signal trace via reduces the maximum trace length by approximately 2 inches. For example: if 6 vias are needed, the maximum trace length is 8 inches.
7. When routing a differential signal pair, 45 degree angles are preferred over 90 degree angles. Signal trace length matching is easier with 45-degree angles and overall signal trace length is reduced.
8. The differential signal pairs must not be routed over gaps in the power planes or ground planes. This causes impedance mismatches.
9. If vias are used to change from one signal layer to another signal layer, it is important to maintain the same 50- Ω impedance reference to the ground plane. Changing reference planes causes signal trace impedance mismatches. If changing reference planes cannot be prevented, bypass capacitors connecting the two reference planes next to the signal trace vias will help reduce the impedance mismatch.
10. If possible, the differential signal pairs must be routed on the top and bottom layers of a circuit board. Signal propagation speeds are faster on external signal layers.


Copyright © 2021 Texas Instruments Incorporated

#### 8.3.2.2 Transmitter Reference Resistor

The REF0_PCIE and REF1_PCIE terminals connect to an external resistor to set the drive current for the PCI Express TX driver. The recommended resistor value is 14,532 Ω with 1% tolerance.

A 14,532- Ω resistor is a custom value. To eliminate the need for a custom resistor, two series resistors are recommended: a 14,300- Ω , 1% resistor and a 232- Ω , 1% resistor. Trace lengths must be kept short to minimize noise coupling into the reference resistor terminals.

#### 8.3.2.3 Reference Clock

The XIO2001 requires an external reference clock for the PCI-Express interface. The section provide information concerning the requirements for this reference clock. The XIO2001 is designed to meet all stated specifications when the reference clock input is within all PCI Express operating parameters. This includes both standard clock oscillator sources or spread spectrum clock oscillator sources.

The XIO2001 supports two options for the PCI Express reference clock: a 100-MHz common differential reference clock or a 125-MHz asynchronous single-ended reference clock. Both implementations are described below.

The first option is a system-wide, 100-MHz differential reference clock. A single clock source with multiple differential clock outputs is connected to all PCI Express devices in the system. The differential connection between the clock source and each PCI Express device is point-topoint. This system implementation is referred to as a common clock design.

The XIO2001 is optimized for this type of system clock design. The REFCLK+ and REFCLK– pins provide differential reference clock inputs to the XIO2001. The circuit board routing rules associated with the 100-MHz differential reference clock are the same as the 2.5-Gb/s TX and RX link routing rules itemized in *Section 8.3.2.1*. The only difference is that the differential reference clock does not require series capacitors. The requirement is a DC connection from the clock driver output to the XIO2001 receiver input.

Terminating the differential clock signal is circuit board design specific. But, the XIO2001 design has no internal 50- Ω -to-ground termination resistors. Both REFCLK inputs, at approximately 20 k Ω to ground, are high-impedance inputs.

The second option is a 125-MHz asynchronous single-ended reference clock. For this case, the devices at each end of the PCI Express link have different clock sources. The XIO2001 has a 125-MHz single-ended reference clock option for asynchronous clocking designs. When the REFCLK125_SEL input terminal is tied to $V_{DD_33}$, this clocking mode is enabled.

The single-ended reference clock is attached to the REFCLK+ terminal. The REFCLK+ input, at approximately 20 k Ω , is a high-impedance input. Any clock termination design must account for a high- impedance input. The REFCLK– pin is attached to a 0.1- µ F capacitor. The capacitor's second pin is connected to $V_{SSA}$.

#### 8.3.2.4 Reset

The XIO2001 PCI Express reset ( $\overline{\text{PERST}}$) terminal connects to the upstream PCI Express device's $\overline{\text{PERST}}$ output. The $\overline{\text{PERST}}$ input cell has hysteresis and is operational during both the main power state and $V_{AUX}$ power state. No external components are required.

Please reference the section to fully understand the $\overline{\text{PERST}}$ electrical requirements and timing requirements associated with power-up and power-down sequencing. Also, the data manual identifies all configuration and memory-mapped register bits that are reset by $\overline{\text{PERST}}$.

#### 8.3.2.5 Beacon

The bridge supports the PCI Express in-band beacon feature. Beacon is driven on the upstream PCI Express link by the bridge to request the reapplication of main power when in the L2 link state. To enable the beacon feature, bit 10 (BEACON_ENABLE) in the general control register at offset D4h is asserted. See *Section 8.4.66*, General Control Register, for details.

If the bridge is in the L2 link state and beacon is enabled, when a secondary PCI bus device asserts PME, then the bridge outputs the beacon signal on the upstream PCI Express link. The beacon signal frequency is

Copyright © 2021 Texas Instruments Incorporated

approximately 500 kHz ± 50% with a differential peak-to-peak amplitude of 500 mV and no de-emphasis. Once the beacon is activated, the bridge continues to send the beacon signal until main power is restored as indicated by $\overline{\text{PERST}}$ going inactive. At this time, the beacon signal is deactivated.

#### *8.3.2.6 Wake*

PCI Express WAKE is an open-drain output from the XIO2001 that is driven low to re-activate the PCI Express link hierarchy's main power rails and reference clocks. This PCI Express side-band signal is connected to the $\overline{\text{WAKE}}$ input on the upstream PCIe device. $\overline{\text{WAKE}}$ is operational during both the main power state and $V_{AUX}$ power state.

Since $\overline{\text{WAKE}}$ is an open-drain output, a system side pullup resistor is required to prevent the signal from floating. The drive capability of this open-drain output is 4 mA. Therefore, the value of the selected pullup resistor must be large enough to assure a logic low signal level at the receiver. A robust system design will select a pullup resistor value that de-rates the output driver current capability by a minimum of 50%. At 3.3 V with a de-rated drive current equal to 2 mA, the minimum resistor value is 1.65 k Ω . Larger resistor values are recommended to reduce the current drain on the $V_{AUX}$ supply.

#### *8.3.2.7 Initial Flow Control Credits*

The bridge flow control credits are initialized using the rules defined in the *PCI Express Base Specification*. Table 8-3 identifies the initial flow control credit advertisement for the bridge.

**Table 8-3. Initial Flow Control Credit Advertisements**

| CREDIT TYPE | INITIAL ADVERTISEMENT |
|---|---|
| Posted request headers (PH) | 8 |
| Posted request data (PD) | 128 |
| Non-posted header (NPH) | 4 |
| Non-posted data (NPD) | 4 |
| Completion header (CPLH) | 0 (infinite) |
| Completion data (CPLD) | 0 (infinite) |

#### *8.3.2.8 PCI Express Message Transactions*

PCI Express messages are both initiated and received by the bridge. Table 8-4 outlines message support within the bridge.

**Table 8-4. Messages Supported by the Bridge**

| MESSAGE | SUPPORTED | BRIDGE ACTION |
|---|---|---|
| Assert_INTx | Yes | Transmitted upstream |
| Deassert_INTx | Yes | Transmitted upstream |
| PM_Active_State_Nak | Yes | Received and processed |
| PM_PME | Yes | Transmitted upstream |
| PME_Turn_Off | Yes | Received and processed |
| PME_TO_Ack | Yes | Transmitted upstream |
| ERR_COR | Yes | Transmitted upstream |
| ERR_NONFATAL | Yes | Transmitted upstream |
| ERR_FATAL | Yes | Transmitted upstream |
| Set_Slot_Power_Limit | Yes | Received and processed |
| Unlock | No | Discarded |
| Hot plug messages | No | Discarded |
| Advanced switching messages | No | Discarded |
| Vendor defined type 0 | No | Unsupported request |
| Vendor defined type 1 | No | Discarded |


Copyright © 2021 Texas Instruments Incorporated

All supported message transactions are processed per the *PCI Express Base Specification*.

### 8.3.3 PCI Port Arbitration

The internal PCI port arbitration logic supports up to six external PCI bus devices plus the bridge. This bridge supports a classic PCI arbiter.

#### *8.3.3.1 Classic PCI Arbiter*

The classic PCI arbiter is configured through the classic PCI configuration space at offset DCh. Table 8-5 identifies and describes the registers associated with classic PCI arbitration mode.

**Table 8-5. Classic PCI Arbiter Registers**

| PCI OFFSET | REGISTER NAME | DESCRIPTION |
|---|---|---|
| Classic PCI configuration register DCh | Arbiter control (see *Section 8.4.70*) | Contains a two-tier priority scheme for the bridge and six PCI bus devices. The bridge defaults to the high priority tier. The six PCI bus devices default to the low priority tier. A bus parking control bit (bit 7, PARK) is provided. |
| Classic PCI configuration register DDh | Arbiter request mask (see *Section 8.4.71*) | Six mask bits provide individual control to block each PCI Bus REQ input. Bit 7 (ARB_TIMEOUT) in the arbiter request mask register enables generating timeout status if a PCI device does not respond within 16 PCI bus clocks. Bit 6 (AUTO_MASK) in the arbiter request mask register automatically masks a PCI bus REQ if the device does not respond after GNT is issued. The AUTO_MASK bit is cleared to disable any automatically generated mask. |
| Classic PCI configuration register DEh | Arbiter time-out status (see *Section 8.4.72*) | When bit 7 (ARB_TIMEOUT) in the arbiter request mask register is asserted, timeout status for each PCI bus device is reported in this register. |

### 8.3.4 Configuration Register Translation

PCI Express configuration register transactions received by the bridge are decoded based on the transaction's destination ID. These configuration transactions can be broken into three subcategories: type 0 transactions, type 1 transactions that target the secondary bus, and type 1 transactions that target a downstream bus other than the secondary bus.

PCI Express type 0 configuration register transactions always target the configuration space and are never passed on to the secondary interface.

Type 1 configuration register transactions that target a device on the secondary bus are converted to type 0 configuration register transactions on the PCI bus. Figure 8-1 shows the address phase of a type 0 configuration transaction on the PCI bus as defined by the PCI specification.

| 31 16 | 15 11 | 10 8 | 7 2 | 1 | 0 |
|---|---|---|---|---|---|
| IDSEL | Reserved | Function Number | Register Number | 0 | 0 |

**Figure 8-1. Type 0 Configuration Transaction Address Phase Encoding**

In addition, the bridge converts the destination ID device number to one of the AD[31:16] lines as the IDSEL signal. The implemented IDSEL signal mapping is shown in Table 8-6.

Copyright © 2021 Texas Instruments Incorporated

**Table 8-6. Type 0 Configuration Transaction IDSEL Mapping**

| DEVICE NUMBER | AD[31:16] |
|---|---|
| 00000 | 0000 0000 0000 0001 |
| 00001 | 0000 0000 0000 0010 |
| 00010 | 0000 0000 0000 0100 |
| 00011 | 0000 0000 0000 1000 |
| 00100 | 0000 0000 0001 0000 |
| 00101 | 0000 0000 0010 0000 |
| 00110 | 0000 0000 0100 0000 |
| 00111 | 0000 0000 1000 0000 |
| 01000 | 0000 0001 0000 0000 |
| 01001 | 0000 0010 0000 0000 |
| 01010 | 0000 0100 0000 0000 |
| 01011 | 0000 1000 0000 0000 |
| 01100 | 0001 0000 0000 0000 |
| 01101 | 0010 0000 0000 0000 |
| 01110 | 0100 0000 0000 0000 |
| 01111 | 1000 0000 0000 0000 |
| 1xxxx | 0000 0000 0000 0000 |

Type 1 configuration registers transactions that target a downstream bus other then the secondary bus are output on the PCI bus as type 1 PCI configuration transactions. Figure 8-2 shows the address phase of a type 1 configuration transaction on the PCI bus as defined by the PCI specification.

| 31 24 | 23 16 | 15 11 | 10 8 | 7 2 | 1 | 0 |
|---|---|---|---|---|---|---|
| Reserved | Bus Number | Device Number | Function Number | Register Number | 0 | 1 |

**Figure 8-2. Type 1 Configuration Transaction Address Phase Encoding**


Copyright © 2021 Texas Instruments Incorporated

### 8.3.5 PCI Interrupt Conversion to PCI Express Messages

The bridge converts interrupts from the PCI bus sideband interrupt signals to PCI Express interrupt messages.

Table 8-7, Figure 8-3, and Figure 8-4 illustrate the format for both the assert and deassert INTx messages.

**Table 8-7. Interrupt Mapping In The Code Field**

| INTERRUPT | CODE FIELD |
|---|---|
| $\overline{\text{INTA}}$ | 00 |
| $\overline{\text{INTB}}$ | 01 |
| $\overline{\text{INTC}}$ | 10 |
| $\overline{\text{INTD}}$ | 11 |

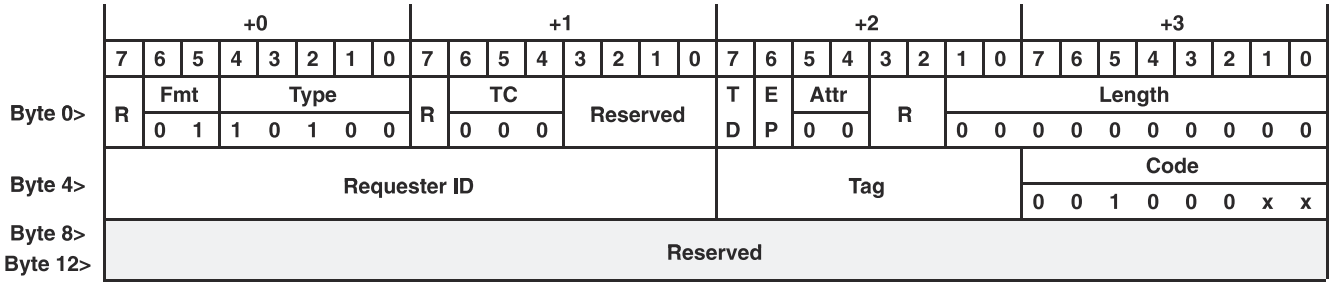



**Figure 8-3. PCI Express ASSERT_INTX Message**

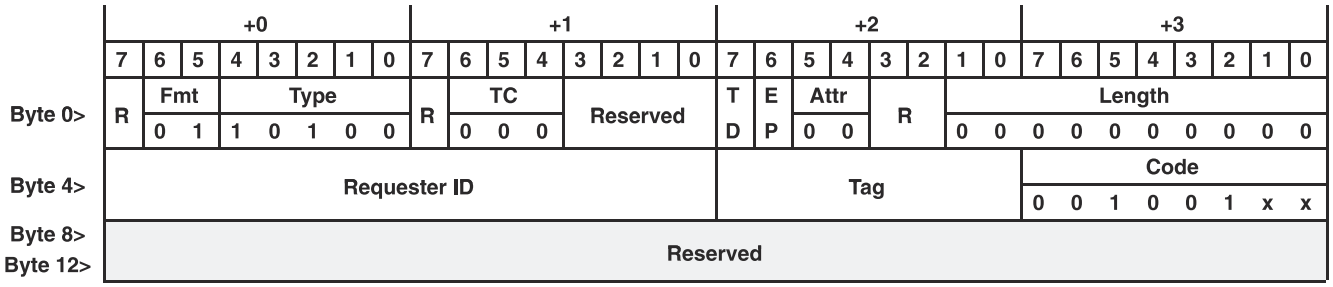



**Figure 8-4. PCI Express DEASSERT_INTX Message**

### 8.3.6 $\overline{\text{PME}}$ Conversion to PCI Express Messages

When the PCI bus $\overline{\text{PME}}$ input transitions low, the bridge generates and sends a PCI Express PME message upstream. The requester ID portion of the PME message uses the stored value in the secondary bus number register as the bus number, 0 as the device number, and 0 as the function number. The Tag field for each PME message is 00h. A $\overline{\text{PME}}$ message is sent periodically until the $\overline{\text{PME}}$ signal transitions high.

Figure 8-5 illustrates the format for a PCI Express PME message.

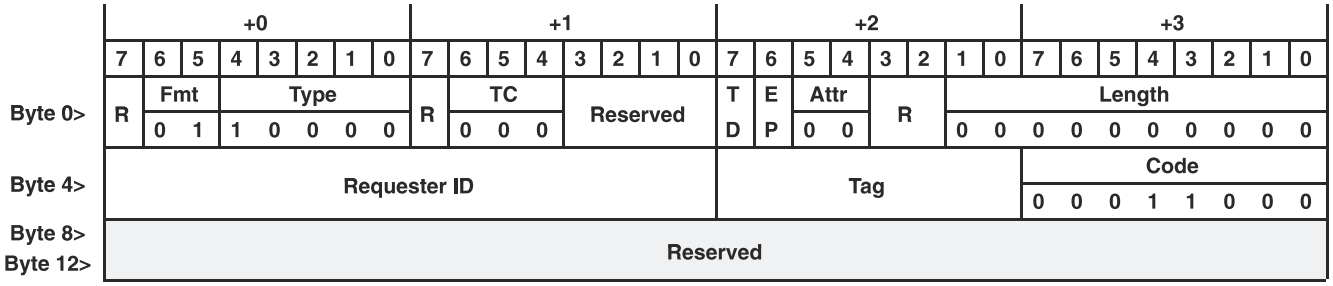



**Figure 8-5. PCI Express PME Message**

Copyright © 2021 Texas Instruments Incorporated

### 8.3.7 PCI Express to PCI Bus Lock Conversion

The bus-locking protocol defined in the *PCI Express Base Specification* and *PCI Local Bus Specification* is provided on the bridge as an additional compatibility feature. The PCI bus $\overline{\text{LOCK}}$ signal is a dedicated output that is enabled by setting bit 12 in the general control register at offset D4h. See *Section 8.4.66*, for details.

**Note**

The use of $\overline{\text{LOCK}}$ is only supported by PCI-Express to PCI Bridges in the downstream direction (away from the root complex).

PCI Express locked-memory read request transactions are treated the same as PCI Express memory read transactions except that the bridge returns a completion for a locked-memory read. Also, the bridge uses the PCI $\overline{\text{LOCK}}$ protocol when initiating the memory read transaction on the PCI bus.

When a PCI Express locked-memory read request transaction is received and the bridge is not already locked, the bridge arbitrates for use of the $\overline{\text{LOCK}}$ terminal by asserting $\overline{\text{REQ}}$. If the bridge receives $\overline{\text{GNT}}$ and the $\overline{\text{LOCK}}$ terminal is high, then the bridge drives the $\overline{\text{LOCK}}$ terminal low after the address phase of the first locked-memory read transaction to take ownership of $\overline{\text{LOCK}}$. The bridge continues to assert $\overline{\text{LOCK}}$ except during the address phase of locked transactions. If the bridge receives $\overline{\text{GNT}}$ and the $\overline{\text{LOCK}}$ terminal is low, then the bridge deasserts its $\overline{\text{REQ}}$ and waits until $\overline{\text{LOCK}}$ is high and the bus is idle before re-arbitrating for the use of $\overline{\text{LOCK}}$.

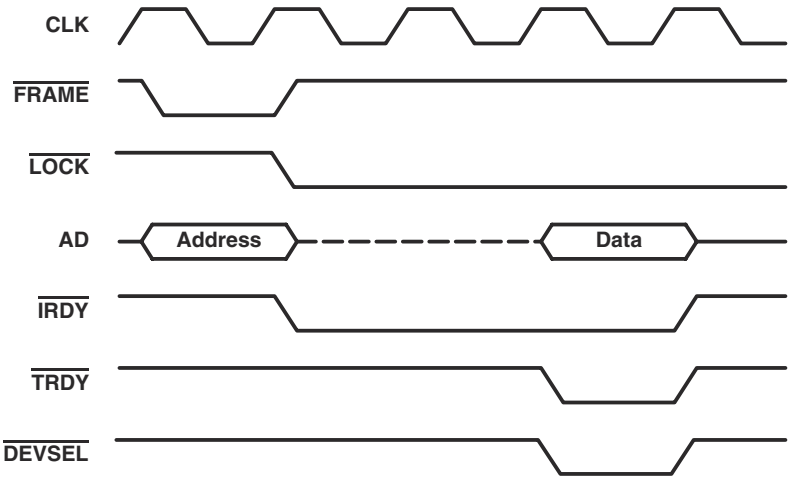



**Figure 8-6. Starting a Locked Sequence**

Once the bridge has ownership of $\overline{\text{LOCK}}$, the bridge initiates the lock read as a memory read transaction on the PCI bus. When the target of the locked-memory read returns data, the bridge is considered locked and all transactions not associated with the locked sequence are blocked by the bridge.


Copyright © 2021 Texas Instruments Incorporated

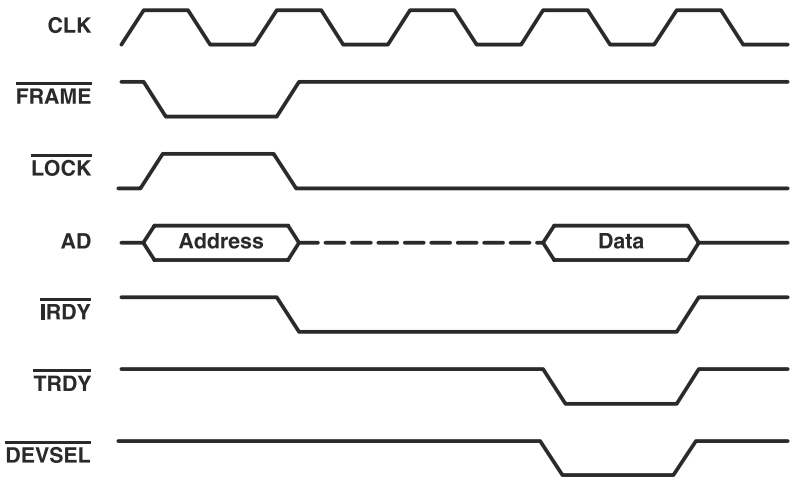



**Figure 8-7. Continuing a Locked Sequence**

Because PCI Express does not have a unique locked-memory write request packet, all PCI Express memory write requests that are received while the bridge is locked are considered part of the locked sequence and are transmitted to PCI as locked-memory write transactions.

The bridge terminates the locked sequence when an unlock message is received from PCI Express and all previous locked transactions have been completed.

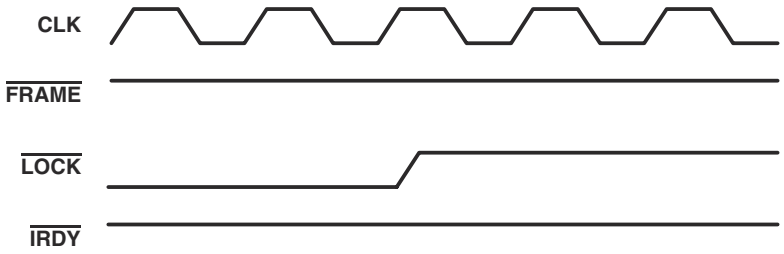



**Figure 8-8. Terminating a Locked Sequence**

In the erroneous case that a normal downstream memory read request is received during a locked sequence, the bridge responds with an unsupported request completion status. Note that this condition must never occur, because the *PCI Express Specification* requires the root complex to block normal memory read requests at the source. All locked sequences that end successfully or with an error condition must be immediately followed by an unlock message. This unlock message is required to return the bridge to a known unlocked state.

### 8.3.8 Two-Wire Serial-Bus Interface

The bridge provides a two-wire serial-bus interface to load subsystem identification information and specific register defaults from an external EEPROM. The serial-bus interface signals (SDA and SCL) are shared with two of the GPIO terminals (3 and 4). If the serial bus interface is enabled, then the GPIO3 and GPIO4 terminals are disabled. If the serial bus interface is disabled, then the GPIO terminals operate as described in *Section 8.3.11*.

#### *8.3.8.1 Serial-Bus Interface Implementation*

To enable the serial-bus interface, a pullup resistor must be implemented on the SCL signal. At the rising edge of $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$, whichever occurs later in time, the SCL terminal is checked for a pullup resistor. If one is detected, then bit 3 (SBDETECT) in the serial-bus control and status register (see *Section 8.4.59*) is set. Software may disable the serial-bus interface at any time by writing a 0b to the SBDETECT bit. If no external EEPROM is required, then the serial-bus interface is permanently disabled by attaching a pulldown resistor to the SCL signal.

The bridge implements a two-terminal serial interface with one clock signal (SCL) and one data signal (SDA). The SCL signal is a unidirectional output from the bridge and the SDA signal is bidirectional. Both are open-drain

Copyright © 2021 Texas Instruments Incorporated

signals and require pullup resistors. The bridge is a bus master device and drives SCL at approximately 60 kHz during data transfers and places SCL in a high-impedance state (0 frequency) during bus idle states. The serial EEPROM is a bus slave device and must acknowledge a slave address equal to A0h. Figure 8-9 illustrates an example application implementing the two-wire serial bus.

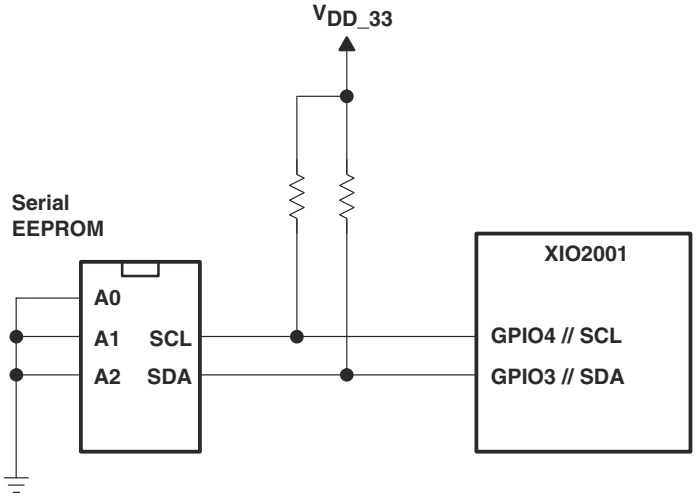



**Figure 8-9. Serial EEPROM Application**

### *8.3.8.2 Serial-Bus Interface Protocol*

All data transfers are initiated by the serial-bus master. The beginning of a data transfer is indicated by a start condition, which is signaled when the SDA line transitions to the low state while SCL is in the high state, as illustrated in Figure 8-10. The end of a requested data transfer is indicated by a stop condition, which is signaled by a low-to-high transition of SDA while SCL is in the high state, as shown in Figure 8-10. Data on SDA must remain stable during the high state of the SCL signal, as changes on the SDA signal during the high state of SCL are interpreted as control signals, that is, a start or stop condition.

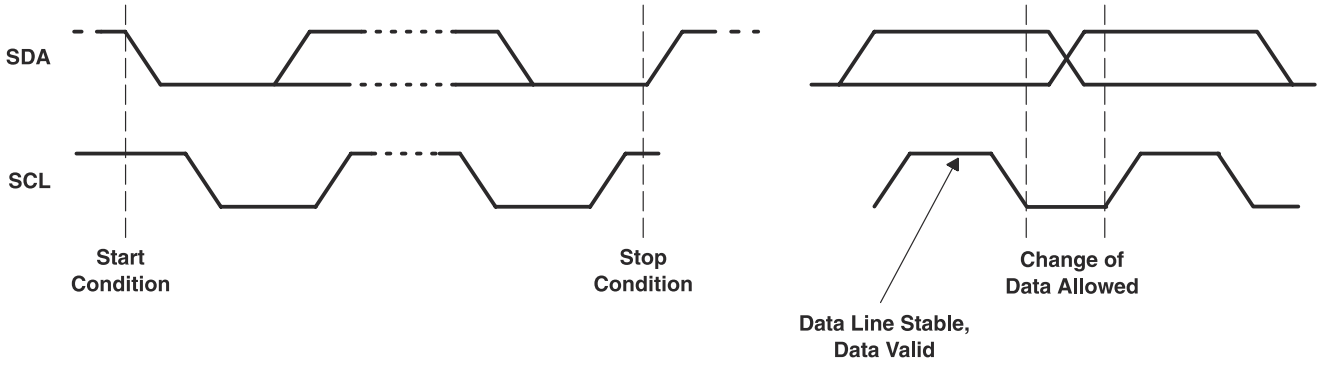



**Figure 8-10. Serial-Bus Start/Stop Conditions and Bit Transfers**

Data is transferred serially in 8-bit bytes. During a data transfer operation, the exact number of bytes that are transmitted is unlimited. However, each byte must be followed by an acknowledge bit to continue the data transfer operation. An acknowledge (ACK) is indicated by the data byte receiver pulling the SDA signal low, so that it remains low during the high state of the SCL signal. Figure 8-11 illustrates the acknowledge protocol.


Copyright © 2021 Texas Instruments Incorporated

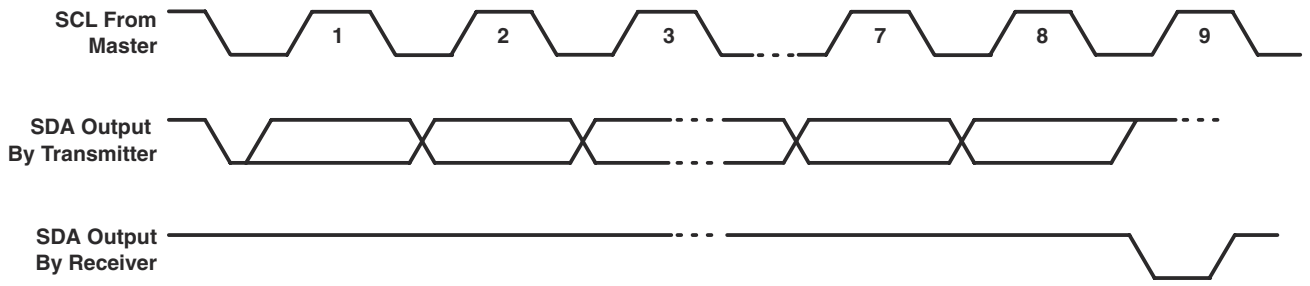



**Figure 8-11. Serial-Bus Protocol Acknowledge**

The bridge performs three basic serial-bus operations: single byte reads, single byte writes, and multibyte reads. The single byte operations occur under software control. The multibyte read operations are performed by the serial EEPROM initialization circuitry immediately after a PCI Express reset. See *Section 8.3.8.3*, *Serial-Bus EEPROM Application*, for details on how the bridge automatically loads the subsystem identification and other register defaults from the serial-bus EEPROM.

Figure 8-12 illustrates a single byte write. The bridge issues a start condition and sends the 7-bit slave device address and the R/W command bit is equal to 0b. A 0b in the R/W command bit indicates that the data transfer is a write. The slave device acknowledges if it recognizes the slave address. If no acknowledgment is received by the bridge, then bit 1 (SB_ERR) is set in the serial-bus control and status register (PCI offset B3h, see *Section 8.4.59*). Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then the bridge delivers the data byte MSB first and expects a final acknowledgment before issuing the stop condition.

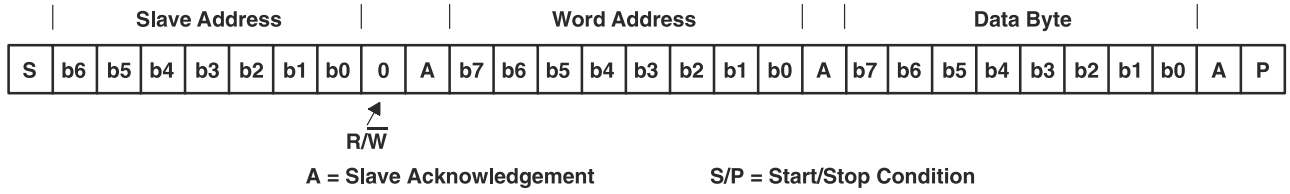



**Figure 8-12. Serial-Bus Protocol – Byte Write**

Figure 8-13 illustrates a single byte read. The bridge issues a start condition and sends the 7-bit slave device address and the R/ $\overline{W}$ command bit is equal to 0b (write). The slave device acknowledges if it recognizes the slave address. Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then, the bridge issues a restart condition followed by the 7-bit slave address and the R/ $\overline{W}$ command bit is equal to 1b (read). Once again, the slave device responds with an acknowledge. Next, the slave device sends the 8-bit data byte, MSB first. Since this is a 1-byte read, the bridge responds with no acknowledge (logic high) indicating the last data byte. Finally, the bridge issues a stop condition.

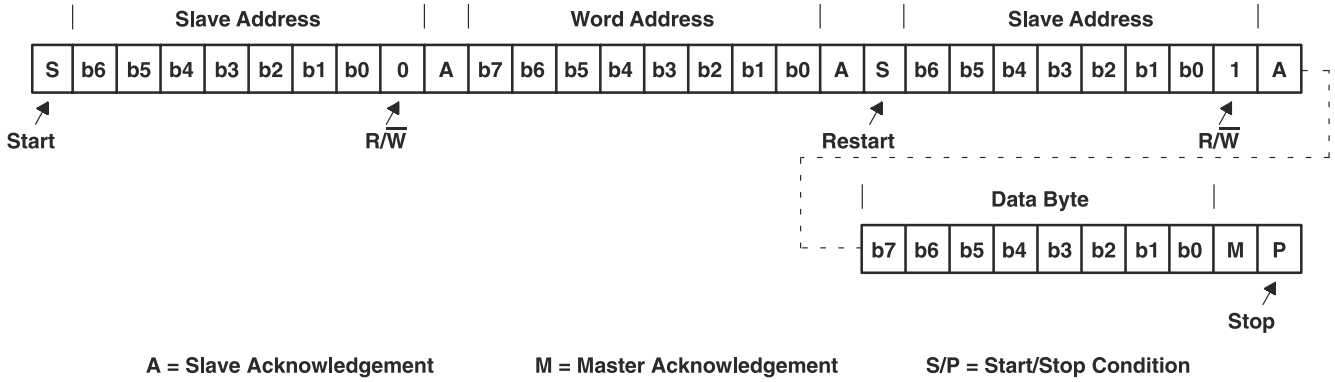



**Figure 8-13. Serial-Bus Protocol – Byte Read**

Copyright © 2021 Texas Instruments Incorporated

Figure 8-14 illustrates the serial interface protocol during a multi-byte serial EEPROM download. The serial-bus protocol starts exactly the same as a 1-byte read. The only difference is that multiple data bytes are transferred. The number of transferred data bytes is controlled by the bridge master. After each data byte, the bridge master issues acknowledge (logic low) if more data bytes are requested. The transfer ends after a bridge master no acknowledge (logic high) followed by a stop condition.

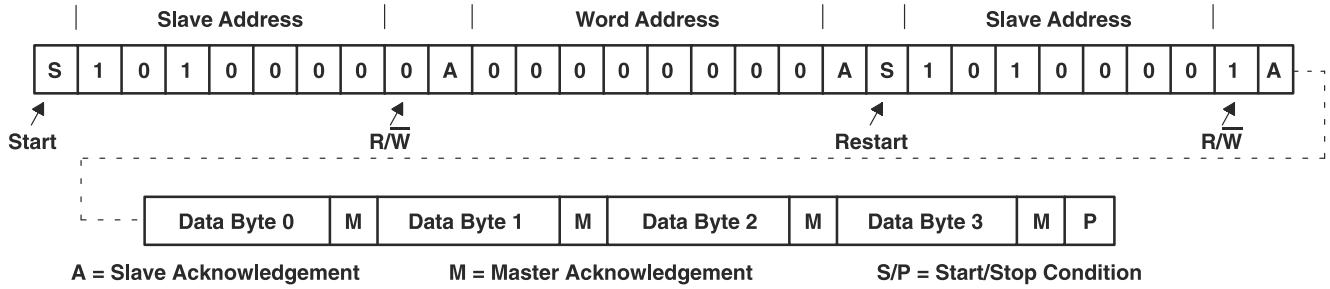



**Figure 8-14. Serial-Bus Protocol – Multibyte Read**

Bit 7 (PROT_SEL) in the serial-bus control and status register changes the serial-bus protocol. Each of the three previous serial-bus protocol figures illustrates the PROT_SEL bit default (logic low). When this control bit is asserted, the word address and corresponding acknowledge are removed from the serial-bus protocol. This feature allows the system designer a second serial-bus protocol option when selecting external EEPROM devices.

### *8.3.8.3 Serial-Bus EEPROM Application*

The registers and corresponding bits that are loaded through the EEPROM are provided in Table 8-8.

**Table 8-8. EEPROM Register Loading Map**

| SERIAL EEPROM WORD ADDRESS | BYTE DESCRIPTION |
|---|---|
| 00h | PCI-Express to PCI bridge function indicator (00h) |
| 01h | Number of bytes to download (25h) |
| 02h | PCI 44h, subsystem vendor ID, byte 0 |
| 03h | PCI 45h, subsystem vendor ID, byte 1 |
| 04h | PCI 46h, subsystem ID, byte 0s |
| 05h | PCI 47h, subsystem ID, byte 1s |
| 06h | PCI D4h, general control, byte 0 |
| 07h | PCI D5h, general control, byte 1 |
| 08h | PCI D6h, general control, byte 2 |
| 09h | PCI D7h, general control, byte 3 |
| 0Ah | PCI D8h, clock control |
| 0Bh | PCI D9h, clock mask |
| 0Ch | Reserved—no bits loaded |
| 0Dh | PCI DCh, arbiter control |
| 0Eh | PCI DDh, arbiter request mask |
| 0Fh | PCI C0h, control and diagnostic register, byte 0 |
| 10h | PCI C1h, control and diagnostic register, byte 1 |
| 11h | PCI C2h, control and diagnostic register, byte 2 |
| 12h | PCI C3h, control and diagnostic register, byte 3 |
| 13h | PCI C4h, control and diagnostic register, byte 0 |
| 14h | PCI C5h, control and diagnostic register, byte 1 |
| 15h | PCI C6h, control and diagnostic register, byte 2 |
| 15h | PCI C6h, control and diagnostic register, byte 2 |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-8. EEPROM Register Loading Map (continued)**

| SERIAL EEPROM WORD ADDRESS | BYTE DESCRIPTION |
|---|---|
| 16h | PCI C7h, control and diagnostic register, byte 3 |
| 17h | PCI C8h, control and diagnostic register, byte 0 |
| 18h | PCI C9h, control and diagnostic register, byte 1 |
| 19h | PCI CAh, control and diagnostic register, byte 2 |
| 1Ah | PCI CBh, control and diagnostic register, byte 3 |
| 1Bh | Reserved—no bits loaded |
| 1Ch | Reserved—no bits loaded |
| 1Dh | PCI E0h, serial IRQ mode control |
| 1Eh | PCI E2h, serial IRQ edge control, byte 0 |
| 1Fh | PCI E3h, serial IRQ edge control, byte 1 |
| 20h | PCI E8h, PFA_REQ_LENGTH_LIMIT |
| 21h | PCI E9h, PFA_REQ_CNT_LIMIT |
| 22h | PCI EAh, CACHE_TMR_XFR_LIMIT |
| 23h | PCI ECh, CACHE_TIMER_LOWER_LIMIT, Byte 0 |
| 24h | PCI EDh, CACHE_TIMER_LOWER_LIMIT, Byte 1 |
| 25h | PCI EEh, CACHE_TIMER_UPPER_LIMIT, Byte 0 |
| 26h | PCI EFh, CACHE_TIMER_UPPER_LIMIT, Byte 1 |
| 27h | End-of-list indicator (80h) |

This format must be explicitly followed for the bridge to correctly load initialization values from a serial EEPROM. All byte locations must be considered when programming the EEPROM.

The serial EEPROM is addressed by the bridge at slave address 1010 000b. This slave address is internally hardwired and cannot be changed by the system designer. Therefore, all three hardware address bits for the EEPROM are tied to $V_{SS}$ to achieve this address. The serial EEPROM in the sample application circuit (Figure 8-9) assumes the 1010b high-address nibble. The lower three address bits are terminal inputs to the chip, and the sample application shows these terminal inputs tied to $V_{SS}$.

During an EEPROM download operation, bit 4 (ROMBUSY) in the serial-bus control and status register is asserted. After the download is finished, bit 0 (ROM_ERR) in the serial-bus control and status register may be monitored to verify a successful download.

#### *8.3.8.4 Accessing Serial-Bus Devices Through Software*

The bridge provides a programming mechanism to control serial-bus devices through system software. The programming is accomplished through a doubleword of PCI configuration space at offset B0h. Table 8-9 lists the registers that program a serial-bus device through software.

**Table 8-9. Registers Used To Program Serial-Bus Devices**

| PCI OFFSET | REGISTER NAME | DESCRIPTION |
|---|---|---|
| B0h | Serial-bus data (see *Section 8.4.56*) | Contains the data byte to send on write commands or the received data byte on read commands. |
| B1h | Serial-bus word address (see *Section 8.4.57*) | The content of this register is sent as the word address on byte writes or reads. This register is not used in the quick command protocol. Bit 7 (PROT_SEL) in the serial-bus control and status register (offset B3h, see *Section 8.4.59*) is set to 1b to enable the slave address to be sent. |
| B2h | Serial-bus slave address (see *Section 8.4.58*) | Write transactions to this register initiate a serial-bus transaction. The slave device address and the R/ $\overline{W}$ command selector are programmed through this register. |
| B3h | Serial-bus control and status (see *Section 8.4.59*) | Serial interface enable, busy, and error status are communicated through this register. In addition, the protocol-select bit (PROT_SEL) and serial-bus test bit (SBTEST) are programmed through this register. |

Copyright © 2021 Texas Instruments Incorporated

To access the serial EEPROM through the software interface, the following steps are performed:

1. The control and status byte is read to verify the EEPROM interface is enabled (SBDETECT asserted) and not busy (REQBUSY and ROMBUSY deasserted).
2. The serial-bus word address is loaded. If the access is a write, then the data byte is also loaded.
3. The serial-bus slave address and R/W command selector byte is written.
4. REQBUSY is monitored until this bit is deasserted.
5. SB_ERR is checked to verify that the serial-bus operation completed without error. If the operation is a read, then the serial-bus data byte is now valid.

### 8.3.9 Advanced Error Reporting Registers

In the extended PCI Express configuration space, the bridge supports the advanced error reporting capabilities structure. For the PCI Express interface, both correctable and uncorrectable error statuses are provided. For the PCI bus interface, secondary uncorrectable error status is provided. All uncorrectable status bits have corresponding mask and severity control bits. For correctable status bits, only mask bits are provided.

Both the primary and secondary interfaces include first error pointer and header log registers. When the first error is detected, the corresponding bit position within the uncorrectable status register is loaded into the first error pointer register. Likewise, the header information associated with the first failing transaction is loaded into the header log. To reset this first error control logic, the corresponding status bit in the uncorrectable status register is cleared by a writeback of 1b.

For systems that require high data reliability, ECRC is fully supported on the PCI Express interface. The primary side advanced error capabilities and control register has both ECRC generation and checking enable control bits. When the checking bit is asserted, all received TLPs are checked for a valid ECRC field. If the generation bit is asserted, then all transmitted TLPs contain a valid ECRC field.

### 8.3.10 Data Error Forwarding Capability

The bridge supports the transfer of data errors in both directions.

If a downstream PCI Express transaction with a data payload is received that targets the internal PCI bus and the EP bit is set indicating poisoned data, then the bridge must ensure that this information is transferred to the PCI bus. To do this, the bridge forces a parity error on each PCI bus data phase by inverting the parity bit calculated for each double-word of data.

If the bridge is the target of a PCI transaction that is forwarded to the PCI Express interface and a data parity error is detected, then this information is passed to the PCI Express interface. To do this, the bridge sets the EP bit in the upstream PCI Express header.

### 8.3.11 General-Purpose I/O Interface

Up to five general-purpose input/output (GPIO) terminals are provided for system customization. These GPIO terminals are 3.3-V tolerant.

The exact number of GPIO terminals varies based on implementing the clock run, power override, and serial EEPROM interface features. These features share four of the five GPIO terminals. When any of the three shared functions are enabled, the associated GPIO terminal is disabled.

All five GPIO terminals are individually configurable as either inputs or outputs by writing the corresponding bit in the GPIO control register at offset B4h (See *Section 8.4.60*). A GPIO data register at offset B6h exists to either read the logic state of each GPIO input or to set the logic state of each GPIO output. The power-up default state for the GPIO control register is input mode.

### 8.3.12 Set Slot Power Limit Functionality

The *PCI Express Specification* provides a method for devices to limit internal functionality and save power based on the value programmed into the captured slot power limit scale (CSPLS) and capture slot power limit value (CSPLV) fields of the PCI Express device capabilities register at offset 74h. See *Section 8.4.50*, *Device Capabilities Register*, for details. The bridge writes these fields when a set slot power limit message is received on the PCI Express interface.


Copyright © 2021 Texas Instruments Incorporated

After the deassertion of $\overline{\text{PERST}}$, the XIO2001 compares the information within the CSPLS and CSPLV fields of the device capabilities register to the minimum power scale (MIN_POWER_SCALE) and minimum power value (MIN_POWER_VALUE) fields in the general control register at offset D4h. See *Section 8.4.66*, *General Control Register*, for details. If the CSPLS and CSPLV fields are less than the MIN_POWER_SCALE and MIN_POWER_VALUE fields, respectively, then the bridge takes the appropriate action that is defined below.

The power usage action is programmable within the bridge. The general control register includes a 3-bit POWER_OVRD field. This field is programmable to the following options:

1. Ignore slot power limit fields.
2. Assert the PWR_OVRD terminal.
3. Disable secondary clocks as specified by the clock mask register at offset D9h (see *Section 8.4.68*).
4. Disable secondary clocks as specified by the clock mask register and assert the PWR_OVRD terminal.
5. Respond with unsupported request to all transactions except type 0/1 configuration transactions and set slot power limit messages

### 8.3.13 PCI Express and PCI Bus Power Management

The bridge supports both software-directed power management and active state power management through standard PCI configuration space. Software-directed registers are located in the power management capabilities structure located at offset 48h (see *Section 8.4.32*). Active state power management control registers are located in the PCI Express capabilities structure located at offset 70h (see *Section 8.4.42*).

During software-directed power management state changes, the bridge initiates link state transitions to L1 or L2/L3 after a configuration write transaction places the device in a low power state. The power management state machine is also responsible for gating internal clocks based on the power state. Table 8-10 identifies the relationship between the D-states and bridge clock operation.

**Table 8-10. Clocking In Low Power States**

| CLOCK SOURCE | D0/L0 | D1/L1 | D2/L1 | D3/L2/L3 |
|---|---|---|---|---|
| PCI express reference clock input (REFCLK) | On | On | On | On/Off |
| Internal PCI bus clock to bridge function | On | Off | Off | Off |

The link power management (LPM) state machine manages active state power by monitoring the PCI Express transaction activity. If no transactions are pending and the transmitter has been idle for at least the minimum time required by the *PCI Express Specification*, then the LPM state machine transitions the link to either the L0s or L1 state. By reading the bridge's L0s and L1 exit latency in the link capabilities register, the system software may make an informed decision relating to system performance versus power savings. The ASLPMC field in the link control register provides an L0s only option, L1 only option, or both L0s and L1 option.

### 8.3.14 Auto Pre-Fetch Agent

The auto pre-fetch agent is an internal logic module that will generate speculative read requests on behalf of a PCI master to improve upstream memory read performance.

The auto pre-fetch agent will generate a read thread on the PCI-express bus when it receives an upstream prefetchable memory read request on the PCI bus. A read thread is a sequence of one or more read requests with contiguous read addresses. The first read of thread will be started by a master on the PCI bus requesting a read that is forwarded to the root complex by the bridge. Each subsequent read in the thread will be initiated by the auto pre-fetch agent. Each subsequent read will use the address that immediately follows the last address of data in the previous read of the thread. Each read request in the thread will be assigned to an upstream request processor. The pre-fetch agent can issue reads for two threads at one time, alternating between the threads.

Copyright © 2021 Texas Instruments Incorporated

## 8.4 Register Maps

### 8.4.1 Classic PCI Configuration Space

The programming model of the XIO2001 PCI-Express to PCI bridge is compliant to the classic PCI-to-PCI bridge programming model. The PCI configuration map uses the type 1 PCI bridge header.

All bits marked with a are sticky bits and are reset by a global reset ( $\overline{\text{GRST}}$) or the internally-generated power-on reset. All bits marked with a ☆ are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

**Table 8-11. Classic PCI Configuration Register Map**

| REGISTER NAME | | | | OFFSET |
|---|---|---|---|---|
| Device ID | | Vendor ID | | 000h |
| Status | | Command | | 004h |
| Class code | | | Revision ID | 008h |
| BIST | Header type | Latency timer | Cache line size | 00Ch |
| Device control base address | | | | 010h |
| Reserved | | | | 014h |
| Secondary latency timer | Subordinate bus number | Secondary bus number | Primary bus number | 018h |
| Secondary status | | I/O limit | I/O base | 01Ch |
| Memory limit | | Memory base | | 020h |
| Prefetchable memory limit | | Prefetchable memory base | | 024h |
| Prefetchable base upper 32 bits | | | | 028h |
| Prefetchable limit upper 32 bits | | | | 02Ch |
| I/O limit upper 16 bits | | I/O base upper 16 bits | | 030h |
| Reserved | | | Capabilities pointer | 034h |
| Expansion ROM base address | | | | 038h |
| Bridge control | | Interrupt pin | Interrupt line | 03Ch |
| Reserved | | Next item pointer | SSID/SSVID CAP ID | 040h |
| Subsystem ID[1] | | Subsystem vendor ID[1] | | 044h |
| Power management capabilities | | Next item pointer | PM CAP ID | 048h |
| PM Data | PMCSR_BSE | Power management CSR | | 04Ch |
| MSI message control | | Next item pointer | MSI CAP ID | 050h |
| MSI message address | | | | 054h |
| MSI upper message address | | | | 058h |
| Reserved | | MSI message data | | 05Ch |
| MSI Mask Bits Register | | | | 060h |
| MSI Pending Bits Register | | | | 064h |
| Reserved | | | | 068h–06Ch |
| PCI Express capabilities register | | Next item pointer | PCI Express capability ID | 070h |
| Device Capabilities | | | | 074h |
| Device status | | Device control | | 078h |
| Link Capabilities | | | | 07Ch |
| Link status | | Link control | | 080h |
| Slot Capabilities | | | | 084h |
| Slot Status | | Slot Control | | 088h |
| Root Capabilities | | Root Control | | 08Ch |
| Root Status | | | | 090h |
| Device Capabilities 2 | | | | 094h |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-11. Classic PCI Configuration Register Map (continued)**

| REGISTER NAME | | | | OFFSET |
|---|---|---|---|---|
| Device Status 2 | | Device Control 2 | | 098h |
| Link Capabilities 2 | | | | 09Ch |
| Link Status 2 | | Link Control 2 | | 0A0h |
| Slot Capabilities 2 | | | | 0A4h |
| Slot Status 2 | | Slot Control 2 | | 0A8h |
| Reserved | | | | 0ACh |
| Serial-bus control and status(1) | Serial-bus slave address(1) | Serial-bus word address(1) | Serial-bus data(1) | 0B0h |
| GPIO data(1) | | GPIO control(1) | | 0B4h |
| Reserved | | | | 0B8h–0BCh |
| TL Control and diagnostic register 0(1) | | | | 0C0h |
| DLL Control and diagnostic register 1(1) | | | | 0C4h |
| PHY Control and diagnostic register 2(1) | | | | 0C8h |
| Reserved | | | | 0CCh |
| Subsystem access(1) | | | | 0D0h |
| General control(1) | | | | 0D4h |
| Reserved | Clock run status(1) | Clock mask | Clock control | 0D8h |
| Reserved | Arbiter time-out status | Arbiter request mask(1) | Arbiter control(1) | 0DCh |
| Serial IRQ edge control(1) | | Reserved | Serial IRQ mode control(1) | 0E0h |
| Reserved | | Serial IRQ status | | 0E4h |
| Cache Timer Transfer Limit | | PFA Request Limit | | 0E8h |
| Cache Timer Upper Limit | | Cache Timer Lower Limit | | 0ECh |
| Reserved | | | | 0F0h–0FCh |

(1) One or more bits in this register are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset. Registers highlighted in gray are reserved or not implemented.

Copyright © 2021 Texas Instruments Incorporated

### 8.4.2 Vendor ID Register

This 16-bit read-only register contains the value 104Ch, which is the vendor ID assigned to Texas Instruments.

PCI register offset: 00h
Register type: Read-only
Default value: 104Ch

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

### 8.4.3 Device ID Register

This 16-bit read-only register contains the value 8231h, which is the device ID assigned by TI for the bridge.

PCI register offset: 02h
Register type: Read-only
Default value: 8240h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |


Copyright © 2021 Texas Instruments Incorporated

### 8.4.4 Command Register

The command register controls how the bridge behaves on the PCI Express interface. See Table 8-12 for a complete description of the register contents.

PCI register offset: 04h
Register type: Read-only, Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-12. Command Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:11 | RSVD | R | Reserved. Returns 00000b when read. |
| 10 | INT_DISABLE | R | $\overline{\text{INTx}}$ disable. This bit enables device specific interrupts. Since the bridge does not generate any internal interrupts, this bit is read-only 0b. |
| 9 | FBB_ENB | R | Fast back-to-back enable. The bridge does not generate fast back-to-back transactions; therefore, this bit returns 0b when read. |
| 8 | SERR_ENB | RW | $\overline{\text{SERR}}$ enable bit. When this bit is set, the bridge can signal fatal and nonfatal errors on the PCI Express interface on behalf of $\overline{\text{SERR}}$ assertions detected on the PCI bus.<br>0 = Disable the reporting of nonfatal errors and fatal errors (default)<br>1 = Enable the reporting of nonfatal errors and fatal errors |
| 7 | STEP_ENB | R | Address/data stepping control. The bridge does not support address/data stepping, and this bit is hardwired to 0b. |
| 6 | PERR_ENB | RW | Controls the setting of bit 8 (DATAPAR) in the status register (offset 06h, see *Section 8.4.5*) in response to a received poisoned TLP from PCI Express. A received poisoned TLP is forwarded with bad parity to conventional PCI regardless of the setting of this bit.<br>0 = Disables the setting of the master data parity error bit (default)<br>1 = Enables the setting of the master data parity error bit |
| 5 | VGA_ENB | R | VGA palette snoop enable. The bridge does not support VGA palette snooping; therefore, this bit returns 0b when read. |
| 4 | MWI_ENB | RW | Memory write and invalidate enable. When this bit is set, the bridge translates PCI Express memory write requests into memory write and invalidate transactions on the PCI interface.<br>0 = Disable the promotion to memory write and invalidate (default)<br>1 = Enable the promotion to memory write and invalidate |
| 3 | SPECIAL | R | Special cycle enable. The bridge does not respond to special cycle transactions; therefore, this bit returns 0b when read. |
| 2 | MASTER_ENB | RW | Bus master enable. When this bit is set, the bridge is enabled to initiate transactions on the PCI Express interface.<br>0 = PCI Express interface cannot initiate transactions. The bridge must disable the response to memory and I/O transactions on the PCI interface (default).<br>1 = PCI Express interface can initiate transactions. The bridge can forward memory and I/O transactions from PCI secondary interface to the PCI Express interface. |
| 1 | MEMORY_ENB | RW | Memory space enable. Setting this bit enables the bridge to respond to memory transactions on the PCI Express interface.<br>0 = PCI Express receiver cannot process downstream memory transactions and must respond with an unsupported request (default)<br>1 = PCI Express receiver can process downstream memory transactions. The bridge can forward memory transactions to the PCI interface. |
| 0 | IO_ENB | RW | I/O space enable. Setting this bit enables the bridge to respond to I/O transactions on the PCI Express interface.<br>0 = PCI Express receiver cannot process downstream I/O transactions and must respond with an unsupported request (default)<br>1 = PCI Express receiver can process downstream I/O transactions. The bridge can forward I/O transactions to the PCI interface. |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.5 Status Register

The status register provides information about the PCI Express interface to the system. See Table 8-13 for a complete description of the register contents.

PCI register offset: 06h
Register type: Read-only, Read/Clear
Default value: 0010h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**Table 8-13. Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15 | PAR_ERR | RCU | Detected parity error. This bit is set when the PCI Express interface receives a poisoned TLP. This bit is set regardless of the state of bit 6 (PERR_ENB) in the command register (offset 04h, see *Section 8.4.4*).<br>0 = No parity error detected<br>1 = Parity error detected |
| 14 | SYS_ERR | RCU | Signaled system error. This bit is set when the bridge sends an ERR_FATAL or ERR_NONFATAL message and bit 8 (SERR_ENB) in the command register (offset 04h, see *Section 8.4.4*) is set.<br>0 = No error signaled<br>1 = ERR_FATAL or ERR_NONFATAL signaled |
| 13 | MABORT | RCU | Received master abort. This bit is set when the PCI Express interface of the bridge receives a completion-with-unsupported-request status.<br>0 = Unsupported request not received on the PCI Express interface<br>1 = Unsupported request received on the PCI Express interface |
| 12 | TABORT_REC | RCUT | Received target abort. This bit is set when the PCI Express interface of the bridge receives a completion-with-completer-abort status.<br>0 = Completer abort not received on the PCI Express interface<br>1 = Completer abort received on the PCI Express interface |
| 11 | TABORT_SIG | RCUT | Signaled target abort. This bit is set when the PCI Express interface completes a request with completer abort status.<br>0 = Completer abort not signaled on the PCI Express interface<br>1 = Completer abort signaled on the PCI Express interface |
| 10:9 | PCI_SPEED | R | DEVSEL timing. These bits are read-only 00b, because they do not apply to PCI Express. |
| 8 | DATAPAR | RCU | Master data parity error. This bit is set if bit 6 (PERR_ENB) in the command register (offset 04h, see *Section 8.4.4*) is set and the bridge receives a completion with data marked as poisoned on the PCI Express interface or poisons a write request received on the PCI Express interface.<br>0 = No uncorrectable data error detected on the primary interface<br>1 = Uncorrectable data error detected on the primary interface |
| 7 | FBB_CAP | R | Fast back-to-back capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b. |
| 6 | RSVD | R | Reserved. Returns 0b when read. |
| 5 | 66MHZ | R | 66-MHz capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b. |
| 4 | CAPLIST | R | Capabilities list. This bit returns 1b when read, indicating that the bridge supports additional PCI capabilities. |
| 3 | INT_STATUS | R | Interrupt status. This bit reflects the interrupt status of the function. This bit is read-only 0b since the bridge does not generate any interrupts internally. |
| 2:0 | RSVD | R | Reserved. Returns 000b when read. |


Copyright © 2021 Texas Instruments Incorporated

### 8.4.6 Class Code and Revision ID Register

This read-only register categorizes the base class, subclass, and programming interface of the bridge. The base class is 06h, identifying the device as a bridge. The subclass is 04h, identifying the function as a PCI-to-PCI bridge, and the programming interface is 00h. Furthermore, the TI device revision is indicated in the lower byte (03h). See Table 8-14 for a complete description of the register contents.

PCI register offset: 08h
Register type: Read-only
Default value: 0604 0000

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-14. Class Code and Revision ID Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:24 | BASECLASS | R | Base class. This field returns 06h when read, which classifies the function as a bridge device. |
| 23:16 | SUBCLASS | R | Subclass. This field returns 04h when read, which classifies the function as a PCI-to-PCI bridge. |
| 15:8 | PGMIF | R | Programming interface. This field returns 00h when read. |
| 7:0 | CHIPREV | R | Silicon revision. This field returns the silicon revision of the function. |

### 8.4.7 Cache Line Size Register

This register is used to determine when a downstream write is memory write (MW) or memory write invalidate (MWI).

A posted write TLP will normally be sent as a MW on the PCI bus. It will be sent as a MWI when the following conditions are met:

- Cacheline size register has a value that is a power of two (1, 2, 4, 8, 16, 32, 64, or 128)
- The write starts on a cacheline boundary
- The write is one or more cachelines in length
- First and last bytes have all lanes enabled
- Memory write invalidates are enabled

PCI register offset: 0Ch
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.8 Primary Latency Timer Register

This read-only register has no meaningful context for a PCI Express device and returns 00h when read.

PCI register offset: 0Dh
Register type: Read only
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.9 Header Type Register

This read-only register indicates that this function has a type one PCI header. Bit 7 of this register is 0b indicating that the bridge is a single-function device.

PCI register offset: 0Eh
Register type: Read only
Default value: 01h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

### 8.4.10 BIST Register

Since the bridge does not support a built-in self test (BIST), this read-only register returns the value of 00h when read.

PCI register offset: 0Fh
Register type: Read only
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.11 Device Control Base Address Register

This register programs the memory base address that accesses the device control registers. By default, this register is read only. If bit 5 of the Control and Diagnostic Register 2 (see *Section 8.4.64*) is set, then the bits 31:12 of this register become read/write. See Table 8-15 for a complete description of the register contents.

PCI register offset: 10h
Register type: Read-only, Read/Write
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-15. Device Control Base Address Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:12 | ADDRESS | R or RW | Memory Address. The memory address field for XIO2001 uses 20 read/write bits indicating that 4096 bytes of memory space are required. While less than this is actually used, typical systems will allocate this space on a 4K boundary. If the BAR0_EN bit (bit 5 at C8h) is '0', then these bits are read-only and return zeros when read. If the BAR0_EN bit is '1', then these bits are read/write. |
| 11:4 | RSVD | R | Reserved. These bits are read-only and return 00h when read. |
| 3 | PRE_FETCH | R | Prefetchable. This bit is read-only 0b indicating that this memory window is not prefetchable. |
| 2:1 | MEM_TYPE | R | Memory type. This field is read-only 00b indicating that this window can be located anywhere in the 32-bit address space. |
| 0 | MEM_IND | R | Memory space indicator. This field returns 0b indicating that memory space is used. |

### 8.4.12 Primary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI Express interface is connected to.

PCI register offset: 18h
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.13 Secondary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI interface is connected to. The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset: 19h
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.14 Subordinate Bus Number Register

This read/write register specifies the bus number of the highest number PCI bus segment that is downstream of the bridge. The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset: 1Ah
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.15 Secondary Latency Timer Register

This read/write register specifies the secondary bus latency timer for the bridge, in units of PCI clock cycles.

PCI register offset: 1Bh
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.16 I/O Base Register

This read/write register specifies the lower limit of the I/O addresses that the bridge forwards downstream. See Table 8-16 for a complete description of the register contents.

PCI register offset: 1Ch
Register type: Read-only, Read/Write
Default value: 01h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Table 8-16. I/O Base Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:4 | IOBASE | RW | I/O base. Defines the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be 000h. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O base upper 16 bits register (offset 30h, see *Section 8.4.25*). |
| 3:0 | IOTYPE | R | I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing. |

### 8.4.17 I/O Limit Register

This read/write register specifies the upper limit of the I/O addresses that the bridge forwards downstream. See Table 8-17 for a complete description of the register contents.

PCI register offset: 1Dh
Register type: Read-only, Read/Write
Default value: 01h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Table 8-17. I/O Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:4 | IOLIMIT | RW | I/O limit. Defines the top address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O limit upper 16 bits register (offset 32h, see *Section 8.4.26*). |
| 3:0 | IOTYPE | R | I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing. |


Copyright © 2021 Texas Instruments Incorporated

### 8.4.18 Secondary Status Register

The secondary status register provides information about the PCI bus interface. See Table 8-18 for a complete description of the register contents.

PCI register offset: 1Eh
Register type: Read-only, Read/Clear
Default value: 02X0h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-18. Secondary Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15 | PAR_ERR | RCU | Detected parity error. This bit reports the detection of an uncorrectable address, attribute, or data error by the bridge on its internal PCI bus secondary interface. This bit must be set when any of the following three conditions are true:<br>• The bridge detects an uncorrectable address or attribute error as a potential target.<br>• The bridge detects an uncorrectable data error when it is the target of a write transaction.<br>• The bridge detects an uncorrectable data error when it is the master of a read transaction (immediate read data).<br>The bit is set irrespective of the state of bit 0 (PERR_EN) in the bridge control register at offset 3Eh (see *Section 8.4.30*).<br>0 = Uncorrectable address, attribute, or data error not detected on secondary interface<br>1 = Uncorrectable address, attribute, or data error detected on secondary interface |
| 14 | SYS_ERR | RCU | Received system error. This bit is set when the bridge detects an $\overline{\text{SERR}}$ assertion.<br>0 = No error asserted on the PCI interface<br>1 = $\overline{\text{SERR}}$ asserted on the PCI interface |
| 13 | MABORT | RCU | Received master abort. This bit is set when the PCI interface of the bridge reports the detection of a master abort termination by the bridge when it is the master of a transaction on its secondary interface.<br>0 = Master abort not received on the PCI interface<br>1 = Master abort received on the PCI interface |
| 12 | TABORT_REC | RCU | Received target abort. This bit is set when the PCI interface of the bridge receives a target abort.<br>0 = Target abort not received on the PCI interface<br>1 = Target abort received on the PCI interface |
| 11 | TABORT_SIG | RCU | Signaled target abort. This bit reports the signaling of a target abort termination by the bridge when it responds as the target of a transaction on its secondary interface.<br>0 = Target abort not signaled on the PCI interface<br>1 = Target abort signaled on the PCI interface |
| 10:9 | PCI_SPEED | R | DEVSEL timing. These bits are 01b indicating that this is a medium speed decoding device. |
| 8 | DATAPAR | RCU | Master data parity error. This bit is set if the bridge is the bus master of the transaction on the PCI bus, bit 0 (PERR_EN) in the bridge control register (offset 3Eh see *Section 8.4.30*) is set, and the bridge either asserts $\overline{\text{PERR}}$ on a read transaction or detects $\overline{\text{PERR}}$ asserted on a write transaction.<br>0 = No data parity error detected on the PCI interface<br>1 = Data parity error detected on the PCI Interface |
| 7 | FBB_CAP | R | Fast back-to-back capable. This bit returns a 1b when read indicating that the secondary PCI interface of bridge supports fast back-to-back transactions. |
| 6 | RSVD | R | Reserved. Returns 0b when read. |
| 5 | 66MHZ | R | 66-MHz capable. The bridge operates at a PCI bus CLK frequency of 66 MHz; therefore, this bit always returns a 1b. |
| 4:0 | RSVD | R | Reserved. Returns 00000b when read. |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.19 Memory Base Register

This read/write register specifies the lower limit of the memory addresses that the bridge forwards downstream. See Table 8-19 for a complete description of the register contents.

PCI register offset: 20h
Register type: Read-only, Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-19. Memory Base Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:4 | MEMBASE | RW | Memory base. Defines the lowest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. |
| 3:0 | RSVD | R | Reserved. Returns 0h when read. |

### 8.4.20 Memory Limit Register

This read/write register specifies the upper limit of the memory addresses that the bridge forwards downstream. See Table 8-20 for a complete description of the register contents.

PCI register offset: 22h
Register type: Read-only, Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-20. Memory Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:4 | MEMLIMIT | RW | Memory limit. Defines the highest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. |
| 3:0 | RSVD | R | Reserved. Returns 0h when read. |

### 8.4.21 Prefetchable Memory Base Register

This read/write register specifies the lower limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 8-21 for a complete description of the register contents.

PCI register offset: 24h
Register type: Read-only, Read/Write
Default value: 0001h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-21. Prefetchable Memory Base Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:4 | PREBASE | RW | Prefetchable memory base. Defines the lowest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. The prefetchable base upper 32 bits register (offset 28h, see *Section 8.4.23*) specifies the bit [63:32] of the 64-bit prefetchable memory address. |
| 3:0 | 64BIT | R | 64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window. |

### 8.4.22 Prefetchable Memory Limit Register

This read/write register specifies the upper limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 8-22 for a complete description of the register contents.

PCI register offset: 26h
Register type: Read-only, Read/Write
Default value: 0001h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Table 8-22. Prefetchable Memory Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:4 | PRELIMIT | RW | Prefetchable memory limit. Defines the highest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The prefetchable limit upper 32 bits register (offset 2Ch, see *Section 8.4.24*) specifies the bit [63:32] of the 64-bit prefetchable memory address. |
| 3:0 | 64BIT | R | 64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window. |

### 8.4.23 Prefetchable Base Upper 32-Bit Register

This read/write register specifies the upper 32 bits of the prefetchable memory base register. See Table 8-23 for a complete description of the register contents.

PCI register offset: 28h
Register type: Read/Write
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-23. Prefetchable Base Upper 32-Bit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:0 | PREBASE | RW | Prefetchable memory base upper 32 bits. Defines the upper 32 bits of the lowest address of the prefetchable memory address range that determines when to forward memory transactions downstream. |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.24 Prefetchable Limit Upper 32-Bit Register

This read/write register specifies the upper 32 bits of the prefetchable memory limit register. See Table 8-24 for a complete description of the register contents.

PCI register offset: 2Ch
Register type: Read/Write
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-24. Prefetchable Limit Upper 32-Bit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:0 | PRELIMIT | RW | Prefetchable memory limit upper 32 bits. Defines the upper 32 bits of the highest address of the prefetchable memory address range that determines when to forward memory transactions downstream. |

### 8.4.25 I/O Base Upper 16-Bit Register

This read/write register specifies the upper 16 bits of the I/O base register. See Table 8-25 for a complete description of the register contents.

PCI register offset: 30h
Register type: Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-25. I/O Base Upper 16-Bit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:0 | IOBASE | RW | I/O base upper 16 bits. Defines the upper 16 bits of the lowest address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be 00000h. |

### 8.4.26 I/O Limit Upper 16-Bit Register

This read/write register specifies the upper 16 bits of the I/O limit register. See Table 8-26 for a complete description of the register contents.

PCI register offset: 32h
Register type: Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-26. I/O Limit Upper 16-Bit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:0 | IOLIMIT | RW | I/O limit upper 16 bits. Defines the upper 16 bits of the top address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be FFFFFh. |

### 8.4.27 Capabilities Pointer Register

This read-only register provides a pointer into the PCI configuration header where the PCI power management block resides. Since the PCI power management registers begin at 40h, this register is hardwired to 40h.

PCI register offset: 34h
Register type: Read-only
Default value: 40h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.28 Interrupt Line Register

This read/write register is programmed by the system and indicates to the software which interrupt line the bridge has assigned to it. The default value of this register is FFh, indicating that an interrupt line has not yet been assigned to the function. Since the bridge does not generate interrupts internally, this register is a scratch pad register.

PCI register offset: 3Ch
Register type: Read/Write
Default value: FFh

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

### 8.4.29 Interrupt Pin Register

The interrupt pin register is read-only 00h indicating that the bridge does not generate internal interrupts. While the bridge does not generate internal interrupts, it does forward interrupts from the secondary interface to the primary interface.

PCI register offset: 3Dh
Register type: Read-only
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.30 Bridge Control Register

The bridge control register provides extensions to the command register that are specific to a bridge. See Table 8-27 for a complete description of the register contents.

PCI register offset: 3Eh
Register type: Read-only, Read/Write, Read/Clear
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-27. Bridge Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:12 | RSVD | R | Reserved. Returns 0h when read. |
| 11 | DTSERR | RW | Discard timer $\overline{\text{SERR}}$ enable. Applies only in conventional PCI mode. This bit enables the bridge to generate either an ERR_NONFATAL (by default) or ERR_FATAL transaction on the primary interface when the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridge. The severity is selectable only if advanced error reporting is supported.<br>0 = Do not generate ERR_NONFATAL or ERR_FATAL on the primary interface as a result of the expiration of the secondary discard timer. Note that an error message can still be sent if advanced error reporting is supported and bit 10 (DISCARD_TIMER_MASK) in the secondary uncorrectable error mask register (offset 130h, see *Section 8.5.10*) is clear (default).<br>1 = Generate ERR_NONFATAL or ERR_FATAL on the primary interface if the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridges. |
| 10 | DTSTATUS | RCU | Discard timer status. This bit indicates if a discard timer expires and a delayed transaction is discarded.<br>0 = No discard timer error<br>1 = Discard timer error |
| 9 | SEC_DT | RW | Selects the number of PCI clocks that the bridge waits for a master on the secondary interface to repeat a delayed transaction request. The counter starts once the delayed completion (the completion of the delayed transaction on the primary interface) has reached the head of the downstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the delayed transaction with the initiating master on the secondary bus). If the master does not repeat the transaction before the counter expires, then the bridge deletes the delayed transaction from its queue and sets the discard timer status bit.<br>0 = The secondary discard timer counts $2^{15}$ PCI clock cycles (default)<br>1 = The secondary discard timer counts $2^{10}$ PCI clock cycles |
| 8 | PRI_DEC | R | Primary discard timer. This bit has no meaning in PCI Express and is hardwired to 0b. |
| 7 | FBB_EN | RW | Fast back-to-back enable. This bit allows software to enable fast back-to-back transactions on the secondary PCI interface.<br>0 = Fast back-to-back transactions are disabled (default)<br>1 = Secondary interface fast back-to-back transactions are enabled |
| 6 | SRST | RW | Secondary bus reset. This bit is set when software wishes to reset all devices downstream of the bridge. Setting this bit causes the $\overline{\text{PRST}}$ signal on the secondary interface to be asserted.<br>0 = Secondary interface is not in reset state (default)<br>1 = Secondary interface is in the reset state |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-27. Bridge Control Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 5 | MAM | RW | Master abort mode. This bit controls the behavior of the bridge when it receives a master abort or an unsupported request.<br>0 = Do not report master aborts. Returns FFFF FFFFh on reads and discard data on writes (default)<br>1 = Respond with an unsupported request on PCI Express when a master abort is received on PCI. Respond with target abort on PCI when an unsupported request completion on PCI Express is received. This bit also enables error signaling on master abort conditions on posted writes. |
| 4 | VGA16 | RW | VGA 16-bit decode. This bit enables the bridge to provide full 16-bit decoding for VGA I/O addresses. This bit only has meaning if the VGA enable bit is set.<br>0 = Ignore address bits [15:10] when decoding VGA I/O addresses (default)<br>1 = Decode address bits [15:10] when decoding VGA I/O addresses |
| 3 | VGA | RW | VGA enable. This bit modifies the response by the bridge to VGA compatible addresses. If this bit is set, then the bridge decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface):<br>• Memory accesses in the range 000A 0000h to 000B FFFFh<br>• I/O addresses in the first 64 KB of the I/O address space (address bits [31:16] are 0000h) and where address bits [9:0] are in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – address bits [15:10] may possess any value and are not used in the decoding)<br>If this bit is set, then forwarding of VGA addresses is independent of the value of bit 2 (ISA), the I/O address and memory address ranges defined by the I/O base and limit registers, the memory base and limit registers, and the prefetchable memory base and limit registers of the bridge. The forwarding of VGA addresses is qualified by bits 0 (IO_ENB) and 1 (MEMORY_ENB) in the command register (offset 04h, see *Section 8.4.4*).<br>0 = Do not forward VGA compatible memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges (default).<br>1 = Forward VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the I/O enable and memory enable bits are set) independent of the I/O and memory address ranges and independent of the ISA enable bit. |
| 2 | ISA | RW | ISA enable. This bit modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O base and I/O limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, then the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1K block.<br>0 = Forward downstream all I/O addresses in the address range defined by the I/O base and I/O limit registers (default)<br>1 = Forward upstream ISA I/O addresses in the address range defined by the I/O base and I/O limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1-KB block) |
| 1 | SERR_EN | RW | $\overline{\text{SERR}}$ enable. This bit controls forwarding of system error events from the secondary interface to the primary interface. The bridge forwards system error events when:<br>• This bit is set<br>• Bit 8 (SERR_ENB) in the command register (offset 04h, see *Section 8.4.4*) is set<br>• $\overline{\text{SERR}}$ is asserted on the secondary interface<br>0 = Disable the forwarding of system error events (default)<br>1 = Enable the forwarding of system error events |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-27. Bridge Control Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 0 | PERR_EN | RW | Parity error response enable. Controls the bridge's response to data, uncorrectable address, and attribute errors on the secondary interface. Also, the bridge always forwards data with poisoning, from conventional PCI to PCI Express on an uncorrectable conventional PCI data error, regardless of the setting of this bit.<br>0 = Ignore uncorrectable address, attribute, and data errors on the secondary interface (default)<br>1 = Enable uncorrectable address, attribute, and data error detection and reporting on the secondary interface |


Copyright © 2021 Texas Instruments Incorporated

### 8.4.31 Capability ID Register

This read-only register identifies the linked list item as the register for Subsystem ID and Subsystem Vendor ID capabilities. The register returns 0Dh when read.

PCI register offset: 40h
Register type: Read-only
Default value: 0Dh

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

### 8.4.32 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 48h pointing to the PCI Power Management Capabilities registers.

PCI register offset: 41h
Register type: Read-only
Default value: 48h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

### 8.4.33 Subsystem Vendor ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem access register at offset D0h. This register is reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: 44h
Register type: Read-only
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.34 Subsystem ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register is reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: 46h
Register type: Read-only
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.35 Capability ID Register

This read-only register identifies the linked list item as the register for PCI Power Management ID Capabilities. The register returns 01h when read.

PCI register offset: 48h

Copyright © 2021 Texas Instruments Incorporated

Register type: Read-only
Default value: 01h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

### 8.4.36 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 50h pointing to the MSI Capabilities registers.

PCI register offset: 49h
Register type: Read-only
Default value: 50h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

### 8.4.37 Power Management Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI power management. See Table 8-28 for a complete description of the register contents.

PCI register offset: 4Ah
Register type: Read-only
Default value: 0603h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-28. Power Management Capabilities Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:11 | PME_SUPPORT | R | $\overline{\text{PME}}$ support. This 5-bit field indicates the power states from which the bridge may assert PME. Because the bridge never generates a $\overline{\text{PME}}$ except on a behalf of a secondary device, this field is read-only and returns 00000b. |
| 10 | D2_SUPPORT | R | This bit returns a 1b when read, indicating that the function supports the D2 device power state. |
| 9 | D1_SUPPORT | R | This bit returns a 1b when read, indicating that the function supports the D1 device power state. |
| 8:6 | AUX_CURRENT | R | 3.3 $V_{AUX}$ auxiliary current requirements. This field returns 000b since the bridge does not generate $\overline{\text{PME}}$ from $D3_{cold}$. |
| 5 | DSI | R | Device specific initialization. This bit returns 0b when read, indicating that the bridge does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it. |
| 4 | RSVD | R | Reserved. Returns 0b when read. |
| 3 | PME_CLK | R | $\overline{\text{PME}}$ clock. This bit returns 0b indicating that the PCI clock is not needed to generate $\overline{\text{PME}}$. |
| 2:0 | PM_VERSION | R | Power management version. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see *Section 8.4.66*) is 0b, then this field returns 010b indicating revision 1.1 compatibility. If PCI_PM_VERSION_CTRL is 1b, then this field returns 011b indicating revision 1.2 compatibility. |

### 8.4.38 Power Management Control/Status Register

This register determines and changes the current power state of the bridge. No internal reset is generated when transitioning from the $D3_{hot}$ state to the D0 state. See Table 8-29 for a complete description of the register contents.

PCI register offset: 4Ch
Register type: Read-only, Read/Write
Default value: 0008h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Table 8-29. Power Management Control/Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15 | PME_STAT | R | $\overline{\text{PME}}$ status. This bit is read-only and returns 0b when read. |
| 14:13 | DATA_SCALE | R | Data scale. This 2-bit field returns 00b when read since the bridge does not use the data register. |
| 12:9 | DATA_SEL | R | Data select. This 4-bit field returns 0h when read since the bridge does not use the data register. |
| 8 | PME_EN | RW | $\overline{\text{PME}}$ enable. This bit has no function and acts as scratchpad space. The default value for this bit is 0b. |
| 7:4 | RSVD | R | Reserved. Returns 0h when read. |
| 3 | NO_SOFT_RESET | R | No soft reset. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see *Section 8.4.66*) is 0b, then this bit returns 0b for compatibility with version 1.1 of the *PCI Power Management Specification*. If PCI_PM_VERSION_CTRL is 1b, then this bit returns 1b indicating that no internal reset is generated and the device retains its configuration context when transitioning from the $D3_{hot}$ state to the D0 state. |
| 2 | RSVD | R | Reserved. Returns 0b when read. |
| 1:0 | PWR_STATE | RW | Power state. This 2-bit field determines the current power state of the function and sets the function into a new power state. This field is encoded as follows:<br>00 = D0 (default)<br>01 = D1<br>10 = D2<br>11 = $D3_{hot}$ |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.39 Power Management Bridge Support Extension Register

This read-only register indicates to host software what the state of the secondary bus will be when the bridge is placed in D3. See Table 8-30 for a complete description of the register contents.

PCI register offset: 4Eh
Register type: Read-only
Default value: 40h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-30. PM Bridge Support Extension Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7 | BPCC | R | Bus power/clock control enable. This bit indicates to the host software if the bus secondary clocks are stopped when the bridge is placed in D3. The state of the BPCC bit is controlled by bit 11 (BPCC_E) in the general control register (offset D4h, see *Section 8.4.66*).<br>0 = The secondary bus clocks are not stopped in D3<br>1 = The secondary bus clocks are stopped in D3 |
| 6 | BSTATE | R | B2/B3 support. This bit is read-only 1b indicating that the bus state in D3 is B2. |
| 5:0 | RSVD | R | Reserved. Returns 00 0000b when read. |

### 8.4.40 Power Management Data Register

The read-only register is not applicable to the bridge and returns 00h when read.

PCI register offset: 4Fh
Register type: Read-only
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.41 MSI Capability ID Register

This read-only register identifies the linked list item as the register for message signaled interrupts capabilities. The register returns 05h when read.

PCI register offset: 50h
Register type: Read-only
Default value: 05h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |


Copyright © 2021 Texas Instruments Incorporated

### 8.4.42 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 70h pointing to the subsystem ID capabilities registers.

PCI register offset: 51h
Register type: Read-only
Default value: 70h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

### 8.4.43 MSI Message Control Register

This register controls the sending of MSI messages. See Table 8-31 for a complete description of the register contents.

PCI register offset: 52h
Register type: Read-only, Read/Write
Default value: 0088h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Table 8-31. MSI Message Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:8 | RSVD | R | Reserved. Returns 00h when read. |
| 7 | 64CAP | R | 64-bit message capability. This bit is read-only 1b indicating that the bridge supports 64-bit MSI message addressing. |
| 6:4 | MM_EN | RW | Multiple message enable. This bit indicates the number of distinct messages that the bridge is allowed to generate.<br>000 = 1 message (default)<br>001 = 2 messages<br>010 = 4 messages<br>011 = 8 messages<br>100 = 16 messages<br>101 = Reserved<br>110 = Reserved<br>111 = Reserved |
| 3:1 | MM_CAP | R | Multiple message capabilities. This field indicates the number of distinct messages that bridge is capable of generating. This field is read-only 100b indicating that the bridge can signal 1 interrupt for each IRQ supported on the serial IRQ stream up to a maximum of 16 unique interrupts. |
| 0 | MSI_EN | RW | MSI enable. This bit enables MSI interrupt signaling. MSI signaling must be enabled by software for the bridge to signal that a serial IRQ has been detected.<br>0 = MSI signaling is prohibited (default)<br>1 = MSI signaling is enabled |

### 8.4.44 MSI Message Lower Address Register

This register contains the lower 32 bits of the address that a MSI message writes to when a serial IRQ is detected. See Table 8-32 for a complete description of the register contents.

PCI register offset: 54h
Register type: Read-only, Read/Write
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Copyright © 2021 Texas Instruments Incorporated

| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-32. MSI Message Lower Address Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:2 | ADDRESS | RW | System specified message address |
| 1:0 | RSVD | R | Reserved. Returns 00b when read. |

### 8.4.45 MSI Message Upper Address Register

This register contains the upper 32 bits of the address that a MSI message writes to when a serial IRQ is detected. If this register contains 0000 0000h, then 32-bit addressing is used; otherwise, 64-bit addressing is used.

PCI register offset: 58h
Register type: Read/Write
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.46 MSI Message Data Register

This register contains the data that software programmed the bridge to send when it send a MSI message. See Table 8-33 for a complete description of the register contents.

PCI register offset: 5Ch
Register type: Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-33. MSI Message Data Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:4 | MSG | RW | System specific message. This field contains the portion of the message that the bridge forwards unmodified. |
| 3:0 | MSG_NUM | RW | Message number. This portion of the message field may be modified to contain the message number is multiple messages are enable. The number of bits that are modifiable depends on the number of messages enabled in the message control register.<br>1 message = No message data bits can be modified (default)<br>2 messages = Bit 0 can be modified<br>4 messages = Bits 1:0 can be modified<br>8 messages = Bits 2:0 can be modified<br>16 messages = Bits 3:0 can be modified |


Copyright © 2021 Texas Instruments Incorporated

### 8.4.47 PCI Express Capability ID Register

This read-only register identifies the linked list item as the register for subsystem ID and subsystem vendor ID capabilities. The register returns 10h when read.

PCI register offset: 70h
Register type: Read-only
Default value: 10h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

### 8.4.48 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 00h, indicating no additional capabilities are supported.

PCI register offset: 71h
Register type: Read-only
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.49 PCI Express Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI Express. See Table 8-34 for a complete description of the register contents.

PCI register offset: 72h
Register type: Read-only
Default value: 0072h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

**Table 8-34. PCI Express Capabilities Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:14 | RSVD | R | Reserved. Returns 00b when read. |
| 13:9 | INT_NUM | R | Interrupt message number. This field is used for MSI support and is implemented as read-only 00000b in the bridge. |
| 8 | SLOT | R | Slot implemented. This bit is not valid for the bridge and is read-only 0b. |
| 7:4 | DEV_TYPE | R | Device/port type. This read-only field returns 0111b indicating that the device is a PCI Express-to-PCI bridge. |
| 3:0 | VERSION | R | Capability version. This field returns 2h indicating revision 2 of the PCI Express capability. |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.50 Device Capabilities Register

The device capabilities register indicates the device specific capabilities of the bridge. See Table 8-35 for a complete description of the register contents.

PCI register offset: 74h
Register type: Read-only
Default value: 0000 8D82

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Table 8-35. Device Capabilities Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:28 | RSVD | R | Reserved. Returns 0h when read. |
| 27:26 | CSPLS | RU | Captured slot power limit scale. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 9:8 are written to this field. The value in this field specifies the scale used for the slot power limit.<br>00 = 1.0x<br>01 = 0.1x<br>10 = 0.01x<br>11 = 0.001x |
| 25:18 | CSPLV | RU | Captured slot power limit value. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 7:0 are written to this field. The value in this field in combination with the slot power limit scale value (bits 27:26) specifies the upper limit of power supplied to the slot. The power limit is calculated by multiplying the value in this field by the value in the slot power limit scale field. |
| 17:16 | RSVD | R | Reserved. Return 00b when read. |
| 15 | RBER | R | Role based error reporting. This bit is hardwired to 1 indicating that this bridge supports Role Based Error Reporting. |
| 14 | PIP | R | Power indicator present. This bit is hardwired to 0b indicating that a power indicator is not implemented. |
| 13 | AIP | R | Attention indicator present. This bit is hardwired to 0b indicating that an attention indicator is not implemented. |
| 12 | ABP | R | Attention button present. This bit is hardwired to 0b indicating that an attention button is not implemented. |
| 11:9 | EP_L1_LAT | RU | Endpoint L1 acceptable latency. This field indicates the maximum acceptable latency for a transition from L1 to L0 state. This field can be programmed by writing to the L1_LATENCY field (bits 15:13) in the general control register (offset D4h, see *Section 8.4.66*). The default value for this field is 110b which indicates a range from 32µs to 64µs. This field cannot be programmed to be less than the latency for the PHY to exit the L1 state. |
| 8:6 | EP_L0S_LAT | RU | Endpoint L0s acceptable latency. This field indicates the maximum acceptable latency for a transition from L0s to L0 state. This field can be programmed by writing to the L0s_LATENCY field (bits 18:16) in the general control register (offset D4h, see *Section 8.4.66*). The default value for this field is 110b which indicates a range from 2µs to 4µs. This field cannot be programmed to be less than the latency for the PHY to exit the L0s state. |
| 5 | ETFS | R | Extended tag field supported. This field indicates the size of the tag field not supported. |
| 4:3 | PFS | R | Phantom functions supported. This field is read-only 00b indicating that function numbers are not used for phantom functions. |
| 2:0 | MPSS | R | Maximum payload size supported. This field indicates the maximum payload size that the device can support for TLPs. This field is encoded as 010b indicating the maximum payload size for a TLP is 512 bytes. |


Copyright © 2021 Texas Instruments Incorporated

### 8.4.51 Device Control Register

The device control register controls PCI Express device specific parameters. See Table 8-36 for a complete description of the register contents.

PCI register offset: 78h
Register type: Read-only, Read/Write
Default value: 2000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-36. Device Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15 | CFG_RTRY_ENB | RW | Configuration retry status enable. When this read/write bit is set to 1b, the bridge returns a completion with completion retry status on PCI Express if a configuration transaction forwarded to the secondary interface did not complete within the implementation specific time-out period. When this bit is set to 0b, the bridge does not generate completions with completion retry status on behalf of configuration transactions. The default value of this bit is 0b. |
| 14:12 | MRRS | RW | Maximum read request size. This field is programmed by host software to set the maximum size of a read request that the bridge can generate. The bridge uses this field to determine how much data to fetch on a read request. This field is encoded as:<br>000 = 128B<br>001 = 256B<br>010 = 512B (default)<br>011 = 1024B<br>100 = 2048B<br>101 = 4096B<br>110 = Reserved<br>111 = Reserved |
| 11 | ENS | R | Enable no snoop. This bit is hardwired to 0 since this device never sets the No Snoop attribute in transactions that it initiates. |
| 10 | APPE | RW | Auxiliary power PM enable. This bit has no effect in the bridge.<br>0 = AUX power is disabled (default)<br>1 = AUX power is enabled |
| 9 | PFE | R | Phantom function enable. Since the bridge does not support phantom functions, this bit is read-only 0b. |
| 8 | ETFE | R | Extended tag field enable. Since the bridge does not support extended tags, this bit is read-only 0b. |
| 7:5 | MPS | RW | Maximum payload size. This field is programmed by host software to set the maximum size of posted writes or read completions that the bridge can initiate. This field is encoded as:<br>000 = 128B (default)<br>001 = 256B<br>010 = 512B<br>011 = 1024B<br>100 = 2048B<br>101 = 4096B<br>110 = Reserved<br>111 = Reserved |
| 4 | ERO | R | Enable relaxed ordering. Since the bridge does not support relaxed ordering, this bit is read-only 0b. |
| 3 | URRE | RW | Unsupported request reporting enable. If this bit is set, then the bridge sends an ERR_NONFATAL message to the root complex when an unsupported request is received.<br>0 = Do not report unsupported requests to the root complex (default)<br>1 = Report unsupported requests to the root complex |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-36. Device Control Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 2 | FERE | RW | Fatal error reporting enable. If this bit is set, then the bridge is enabled to send ERR_FATAL messages to the root complex when a system error event occurs.<br>0 = Do not report fatal errors to the root complex (default)<br>1 = Report fatal errors to the root complex |
| 1 | NFERE | RW | Nonfatal error reporting enable. If this bit is set, then the bridge is enabled to send ERR_NONFATAL messages to the root complex when a system error event occurs.<br>0 = Do not report nonfatal errors to the root complex (default)<br>1 = Report nonfatal errors to the root complex |
| 0 | CERE | RW | Correctable error reporting enable. If this bit is set, then the bridge is enabled to send ERR_COR messages to the root complex when a system error event occurs.<br>0 = Do not report correctable errors to the root complex (default)<br>1 = Report correctable errors to the root complex |

### 8.4.52 Device Status Register

The device status register provides PCI Express device specific information to the system. See Table 8-37 for a complete description of the register contents.

PCI register offset: 7Ah
Register type: Read-only
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-37. Device Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:6 | RSVD | R | Reserved. Returns 00 0000 0000b when read. |
| 5 | PEND | RU | Transaction pending. This bit is set when the bridge has issued a non-posted transaction that has not been completed. |
| 4 | APD | RU | AUX power detected. This bit indicates that AUX power is present.<br>0 = No AUX power detected<br>1 = AUX power detected |
| 3 | URD | RCU | Unsupported request detected. This bit is set by the bridge when an unsupported request is received. |
| 2 | FED | RCU | Fatal error detected. This bit is set by the bridge when a fatal error is detected. |
| 1 | NFED | RCU | Nonfatal error detected. This bit is set by the bridge when a nonfatal error is detected. |
| 0 | CED | RCU | Correctable error detected. This bit is set by the bridge when a correctable error is detected. |

### 8.4.53 Link Capabilities Register

The link capabilities register indicates the link specific capabilities of the bridge. See Table 8-38 for a complete description of the register contents.

PCI register offset: 7Ch
Register type: Read-only
Default value: 000Y XC11h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | y | y |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | y | x | x | x | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-38. Link Capabilities Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:24 | PORT_NUM | R | Port number. This field indicates port number for the PCI Express link. This field is read-only 00h indicating that the link is associated with port 0. |
| 23:22 | RSVD | R | Reserved. Return 00b when read. |
| 21 | LBN_CAP | R | Link bandwidth notification. This bit is hardwired to 0b since this field is not applicable to a bridge. |
| 20 | DLLLAR_CAP | R | DLL link active reporting capable. This bit is hardwired to 0b since the bridge does not support this capability. |
| 19 | SDER_CAP | R | Surprise down error reporting capable. This bit is hardwired to 0b since the bridge does not support this capability. |
| 18 | CLK_PM | R | Clock Power Management. This bit is hardwired to 1 to indicate that XIO2001 supports Clock Power Management through $\overline{\text{CLKREQ}}$ protocol. |
| 17:15 | L1_LATENCY | R | L1 exit latency. This field indicates the time that it takes to transition from the L1 state to the L0 state. Bit 6 (CCC) in the link control register (offset 80h, see *Section 8.4.54*) equals 1b for a common clock and equals 0b for an asynchronous clock.<br>For a common reference clock, the value of this field is determined by bits 20:18 (L1_EXIT_LAT_ASYNC) of the control and diagnostic register 1 (offset C4h, see *Section 8.4.63*).<br>For an asynchronous reference clock, the value of this field is determined by bits 17:15 (L1_EXIT_LAT_COMMON) of the control and diagnostic register 1 (offset C4h, see *Section 8.4.63*). |
| 14:12 | L0S_LATENCY | R | L0s exit latency. This field indicates the time that it takes to transition from the L0s state to the L0 state. Bit 6 (CCC) in the link control register (offset 80h, see *Section 8.4.54*) equals 1b for a common clock and equals 0b for an asynchronous clock.<br>For a common reference clock, the value of 011b indicates that the L1 exit latency falls between 256 ns to less than 512 ns.<br>For an asynchronous reference clock, the value of 100b indicates that the L1 exit latency falls between 512 ns to less than 1 µs. |
| 11:10 | ASLPMS | R | Active state link PM support. This field indicates the level of active state power management that the bridge supports. The value 11b indicates support for both L0s and L1 through active state power management. |
| 9:4 | MLW | R | Maximum link width. This field is encoded 00 0001b to indicate that the bridge only supports a x1 PCI Express link. |
| 3:0 | MLS | R | Maximum link speed. This field is encoded 1h to indicate that the bridge supports a maximum link speed of 2.5 Gb/s. |

### 8.4.54 Link Control Register

The link control register controls link specific behavior. See Table 8-39 for a complete description of the register contents.

PCI register offset: 80h
Register type: Read-only, Read/Write
Default value: 0Y0Xh

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | y | 0 | 0 | 0 | 0 | 0 | 0 | x | x |

**Table 8-39. Link Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:12 | RSVD | R | Reserved. Returns 0h when read. |
| 11 | LABW_IEN | R | Link autonomous bandwidth interrupt enable. This bit is hardwired to 0b since this field is not applicable to a bridge. |
| 10 | LBWN_IEN | R | Link bandwidth management interrupt enable. This bit is hardwired to 0b since this field is not applicable to a bridge. |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-39. Link Control Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 9 | HWAW_DIS | R | Hardware autonomous width disable. This bit is hardwired to 0b since this field is not supported by this bridge. |
| 8 | CPM_EN | RW | Clock Power Management Enable. This bit is used to enable the bridge to use $\overline{\text{CLKREQ}}$ for clock power management<br>0 = Clock Power Management is disabled. $\overline{\text{CLKREQ}}$ is held low.<br>1 = Clock Power Management is enabled and the bridge is permitted to use the $\overline{\text{CLKREQ}}$ signal to allow the REFCLK input to be stopped<br>The default value for this is bit is determined by bit 23 (CPM_EN_DEF_OVRD) in the general control register (offset D4h, see *Section 8.4.66*). |
| 7 | ES | RW | Extended synch. This bit forces the bridge to extend the transmission of FTS ordered sets and an extra TS2 when exiting from L1 prior to entering to L0.<br>0 = Normal synch (default)<br>1 = Extended synch |
| 6 | CCC | RW | Common clock configuration. When this bit is set, it indicates that the bridge and the device at the opposite end of the link are operating with a common clock source. A value of 0b indicates that the bridge and the device at the opposite end of the link are operating with separate reference clock sources. The bridge uses this common clock configuration information to report the L0s and L1 exit latencies.<br>0 = Reference clock is asynchronous (default)<br>1 = Reference clock is common |
| 5 | RL | R | Retrain link. This bit has no function and is read-only 0b. |
| 4 | LD | R | Link disable. This bit has no function and is read-only 0b. |
| 3 | RCB | RW | Read completion boundary. This bit is an indication of the RCB of the root complex. The state of this bit has no affect on the bridge, since the RCB of the bridge is fixed at 128 bytes.<br>0 = 64 bytes (default)<br>1 = 128 bytes |
| 2 | RSVD | R | Reserved. Returns 0b when read. |
| 1:0 | ASLPMC | RW | Active state link PM control. This field enables and disables the active state PM. The default value for this is bit is determined by bits 29:28 (ASPM_CTRL_DEF_OVRD) in the general control register (offset D4h, see Section 8.4.66).<br>00 = Active state PM disabled (default)<br>01 = L0s entry enabled<br>10 = L1 entry enabled<br>11 = L0s and L1 entry enabled |

### 8.4.55 Link Status Register

The link status register indicates the current state of the PCI Express link. See Table 8-40 for a complete description of the register contents.

PCI register offset: 82h
Register type: Read-only
Default value: X011h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

**Table 8-40. Link Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15 | LABW | R | Link autonomous bandwidth status. This bit has no function and is read-only 0b. |
| 14 | LBWM | R | Link bandwidth management status. This bit has no function and is read-only 0b. |
| 13 | DLLLA | R | Data link layer link active. This bit has no function and is read-only 0b. |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-40. Link Status Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 12 | SCC | R | Slot clock configuration. This bit indicates that the bridge uses the same physical reference clock that the platform provides on the connector. If the bridge uses an independent clock irrespective of the presence of a reference on the connector, then this bit must be cleared.<br>0 = Independent 125-MHz reference clock is used<br>1 = Common 100-MHz reference clock is used |
| 11 | LT | R | Link training. This bit has no function and is read-only 0b. |
| 10 | TE | R | Retrain link. This bit has no function and is read-only 0b. |
| 9:4 | NLW | R | Negotiated link width. This field is read-only 00 0001b indicating the lane width is x1. |
| 3:0 | LS | R | Link speed. This field is read-only 1h indicating the link speed is 2.5 Gb/s. |

### 8.4.56 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see *Section 8.4.58*) that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) of the serial-bus control and status register (offset B3h, see *Section 8.4.59*) is cleared. This register is reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: B0h
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.4.57 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to the serial-bus device. The word address is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see *Section 8.4.58*) that initiates the bus cycle. This register is reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: B1h
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.58 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the slave address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle is a read or a write cycle. Writing to this register initiates the cycle on the serial interface. See Table 8-41 for a complete description of the register contents.

PCI register offset: B2h
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-41. Serial-Bus Slave Address Register Descriptions**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:1(1) | SLAVE_ADDR | RW | Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b. |
| 0(1) | RW_CMD | RW | Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle.<br>0 = A single byte write is requested (default).<br>1 = A single byte read is requested. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.59 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial bus. See Table 8-42 for a complete description of the register contents.

PCI register offset: B3h
Register type: Read-only, Read/Write, Read/Clear
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-42. Serial-Bus Control and Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7(1) | PROT_SEL | RW | Protocol select. This bit selects the serial-bus address mode used.<br>0 = Slave address and word address are sent on the serial-bus (default)<br>1 = Only the slave address is sent on the serial-bus |
| 6 | RSVD | R | Reserved. Returns 0b when read. |
| 5(1) | REQBUSY | RU | Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress.<br>0 = No serial-bus cycle<br>1 = Serial-bus cycle in progress |
| 4(1) | ROMBUSY | RU | Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM.<br>0 = No EEPROM activity<br>1 = EEPROM download in progress |
| 3(1) | SBDETECT | RWU | Serial Bus Detect. This bit is set when an EEPROM is detected at $\overline{\text{PERST}}$. |
| 2(1) | SBTEST | RW | Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock.<br>0 = Serial-bus clock at normal operating frequency ~ 60 kHz (default)<br>1 = Serial-bus clock frequency increased for test purposes ~ 4 MHz |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-42. Serial-Bus Control and Status Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 1(1) | SB_ERR | RCU | Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle.<br>0 = No error<br>1 = Serial-bus error |
| 0(1) | ROM_ERR | RCU | Serial EEPROM load error. This bit is set when an error occurs while downloading registers from serial EEPROM.<br>0 = No error<br>1 = EEPROM load error |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.60 GPIO Control Register

This register controls the direction of the five GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO0 ( $\overline{\text{CLKRUN}}$), GPIO1 (PWR_OVRD), GPIO3 (SDA), and GPIO4 (SCL). See Table 8-43 for a complete description of the register contents.

PCI register offset: B4h
Register type: Read-only, Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-43. GPIO Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:5 | RSVD | R | Reserved. Return 000h when read. |
| 4(1) | GPIO4_DIR | RW | GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode.<br>0 = Input (default)<br>1 = Output |
| 3(1) | GPIO3_DIR | RW | GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode.<br>0 = Input (default)<br>1 = Output |
| 2(1) | GPIO2_DIR | RW | GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode.<br>0 = Input (default)<br>1 = Output |
| (1) | GPIO1_DIR | RW | GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode.<br>0 = Input (default)<br>1 = Output |
| 0(1) | GPIO0_DIR | RW | GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode.<br>0 = Input (default)<br>1 = Output |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.61 GPIO Data Register

This register reads the state of the input mode GPIO terminals and changes the state of the output mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO3 (SDA), and GPIO4 (SCL). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. See Table 8-44 for a complete description of the register contents.

PCI register offset: B6h

Copyright © 2021 Texas Instruments Incorporated

Register type: Read-only, Read/Write

Default value: 00XXh

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x |

**Table 8-44. GPIO Data Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:5 | RSVD | R | Reserved. Returns 000h when read. |
| 4(1) | GPIO4_DATA | RW | GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode. |
| 3(1) | GPIO3_DATA | RW | GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode. |
| 2(1) | GPIO2_DATA | RW | GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode. |
| 1(1) | GPIO1_DATA | RW | GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode. |
| 0(1) | GPIO0_DATA | RW | GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.62 TL Control and Diagnostic Register 0

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 8-45 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C0h

Register type: Read/Write

Default value: 0000 0001h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Table 8-45. Control and Diagnostic Register 0 Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:24(1) | PRI_BUS_NUM | R | This field contains the captured primary bus number. |
| 23:19(1) | PRI_DEVICE_ NUM | R | This field contains the captured primary device number. |
| 18 | ALT_ERROR_REP | RW | Alternate Error Reporting. This bit controls the method that the XIO2001 uses for error reporting.<br>0 = Advisory Non-Fatal Error reporting supported (default)<br>1 = Advisory Non-Fatal Error reporting not supported |
| 17:16 | RSVD | R | Reserved. Returns 00b when read. |
| 15:14(1) | RSVD | RW | Reserved. Bits 15:14 default to 00b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 00b. |
| 13:12 | RSVD | R | Reserved. Returns 00b when read. |
| 11:7(1) | RSVD | RW | Reserved. Bits 11:7 default to 00000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 00000b. |
| 6:3 | RSVD | R | Reserved. Returns 0h when read. |
| 2(1) | CFG_ACCESS _MEM_REG | RW | Configuration access to memory-mapped registers. When this bit is set, the bridge allows configuration access to memory-mapped configuration registers. |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-45. Control and Diagnostic Register 0 Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 1[1] | RSVD | RW | Reserved. Bit 1 defaults to 0b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0b. |
| 0[1] | FORCE_CLKREQ | RW | Force $\overline{\text{CLKREQ}}$. When this bit is set, the bridge will force the $\overline{\text{CLKREQ}}$ output to always be asserted. The default setting for this bit is 1b. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.63 Control and Diagnostic Register 1

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 8-46 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C4h
Register type: Read/Write
Default value: 0012 0108h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Table 8-46. Control and Diagnostic Register 1 Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 32:21 | RSVD | R | Reserved. Returns 000h when read. |
| 20:18[1] | L1_EXIT_LAT_ASYNC | RW | L1 exit latency for asynchronous clock. When bit 6 (CCC) of the link control register (offset 80h, see *Section 8.4.54*) is set, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 7Ch, see Section 8.4.53). This field defaults to 100b. |
| 17:15[1] | L1_EXIT_LAT_COMMON | RW | L1 exit latency for common clock. When bit 6 (CCC) of the link control register (offset 80h, see *Section 8.4.54*) is clear, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 7Ch, see *Section 8.4.53*). This field defaults to 100b. |
| 14:11[1] | RSVD | RW | Reserved. Bits 14:11 default to 0000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0000b. |
| 10[1] | SBUS_RESET_MASK | RW | Secondary bus reset bit mask. When this bit is set, the bridge masks the reset caused by bit 6 (SRST) of the bridge control register (offset 3Eh, see Section 8.4.30). This bit defaults to 0b. |
| 9:6[1] | L1ASPM_TIMER | RW | L1ASPM entry timer. This field specifies the value (in 512-ns ticks) of the L1ASPM entry timer. This field defaults to 0100b. |
| 5:2[1] | L0s_TIMER | RW | L0s entry timer. This field specifies the value (in 62.5-MHz clock ticks) of the L0s entry timer. This field defaults to 0010b. |
| 1:0[1] | RSVD | RW | Reserved. Bits 1:0 default to 00b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 00b. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.64 Control and Diagnostic Register 2

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 8-47 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C8h
Register type: Read/Write
Default value: 3214 2000h

Copyright © 2021 Texas Instruments Incorporated

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-47. Control and Diagnostic Register 2 Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:24[1] | N_FTS_ ASYNC_CLK | RW | N_FTS for asynchronous clock. When bit 6 (CCC) of the link control register (offset A0h, see *Section 8.4.54*) is clear, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field shall default to 32h. |
| 23:16[1] | N_FTS_ COMMON_ CLK | RW | N_FTS for common clock. When bit 6 (CCC) of the link control register (offset A0h, see *Section 8.4.54*) is set, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field defaults to 14h. |
| 15:13 | PHY_REV | R | PHY revision number |
| 12:8[1] | LINK_NUM | RW | Link number |
| 7[1] | EN_L2_PWR_ SAVE | RW | Enable L2 Power Savings<br>0= Power savings not enabled when in L2<br>1= Power savings enabled when in L2. |
| 6 | RSVD | R | Reserved. Returns 0b when read. |
| 5[1] | BAR0_EN | RW | BAR 0 Enable.<br>0 = BAR at offset 10h is disabled (default)<br>1 = BAR at offset 10h is enabled |
| 4:0[1] | RSVD | RW | Reserved. Bits 4:0 default to 00000b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 00000b. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.4.65 Subsystem Access Register

The contents of this read/write register are aliased to the subsystem vendor ID and subsystem ID registers at PCI offsets 44h and 46h. See Table 8-48 for a complete description of the register contents.

PCI register offset: D0h
Register type: Read/Write
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-48. Subsystem Access Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:16(1) | SubsystemID | RW | Subsystem ID. The value written to this field is aliased to the subsystem ID register at PCI offset 46h (see *Section 8.4.34*). |
| 15:0(1) | SubsystemVendorID | RW | Subsystem vendor ID. The value written to this field is aliased to the subsystem vendor ID register at PCI offset 44h (see *Section 8.4.33*). |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

### 8.4.66 General Control Register

This read/write register controls various functions of the bridge. See Table 8-49 for a complete description of the register contents.

PCI register offset: D4h
Register type: Read-only, Read/Write
Default value: 8600 025Fh

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

**Table 8-49. General Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:30[1] | CFG_RETRY_CNTR | RW | Configuration retry counter. Configures the amount of time that a configuration request must be retried on the secondary PCI bus before it may be completed with configuration retry status on the PCI Express side.<br>00 = 25 µs<br>01 = 1 ms<br>10 = 25 ms (default)<br>11 = 50 ms |
| 29:28[1] | ASPM_CTRL_DEF_OVRD | RW | Active State Power Management Control Default Override. These bits are used to determine the power up default for bits 1:0 of the Link Control Register in the PCI Express Capability Structure.<br>00 = Power on default indicates that the active state power management is disable (00b)<br>01 = (default)<br>10 = Power on default indicates that the active state power management is enabled for<br>11 = L0s (01b)<br>Power on default indicates that the active state power management is enabled for L1s (10b)<br>Power on default indicates that the active state power management is enabled for L0s and L1s (11b) |
| 27[1] | LOW_POWER_EN | RW | Low-power enable. When this bit is set, the half-amplitude, no pre-emphasis mode for the PCI Express TX drivers is enabled. The default for this bit is 0b. |
| 26[1] | PCI_PM_VERSION_CTRL | RW | PCI power management version control. This bit controls the value reported in bits 2:0 (PM_VERSION) in the power management capabilities register (offset 4Ah, see *Section 8.4.37*). It also controls the value of bit 3 (NO_SOFT_RESET) in the power management control/status register (offset 4Ch, see *Section 8.4.38*).<br>0 = Version fields reports 010b and NO_SOFT_RESET reports 0b for Power Management 1.1 compliance<br>1 = Version fields reports 011b and NO_SOFT_RESET reports 1b for Power Management 1.2 compliance (default) |
| 25[1] | RSVD | RW | Reserved. Bit 25 defaults to 0b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 0b. |
| 24 | RSVD | R | Reserved. Returns 0b when read. |
| 23[1] | CPM_EN_DEF_OVRD | RW | Clock power management enable default override. This bit determines the power-up default for bits 1:0 (CPM_EN) of the link control register (offset 80h, see *Section 8.4.54*) in the PCI Express Capability structure.<br>0 = Power-on default indicates that clock power management is disabled (00b) (default)<br>1 = Power-on default indicates that clock power management is enabled for L0s and L1 (11b) |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-49. General Control Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 22:20[1] | POWER_OVRD | RW | Power override. This bit field determines how the bridge responds when the slot power limit is less than the amount of power required by the bridge and the devices behind the bridge.<br>000 = Ignore slot power limit (default).<br>001 = Assert the PWR_OVRD terminal.<br>010 = Disable secondary clocks selected by the clock mask register.<br>011 = Disable secondary clocks selected by the clock mask register and assert the PWR_OVRD terminal.<br>100 = Respond with unsupported request to all transactions except for configuration transactions (type 0 or type 1) and set slot power limit messages.<br>101,110, 111 = Reserved |
| 19[1] | READ_PREFETCH_DIS | RW | Read Prefetch Disable. This bit is used to control the pre-fetch functionality on PCI memory read transactions.<br>0 = Memory read, memory read line, and memory read multiple will be treated as prefetchable reads (default)<br>1 = Memory read line, and memory read multiple will be treated as pre-fetchable reads. Memory read will not be prefetchable. No auto-prefetch reads will be made for these requests. |
| 18:16[1] | L0s_LATENCY | RW | L0s maximum exit latency. This field programs the maximum acceptable latency when exiting the L0s state. This sets bits 8:6 (EP_L0S_LAT) in the device capabilities register (offset 74h, see *Section 8.4.50*).<br>000 = Less than 64 ns (default)<br>001 = 64 ns up to less than 128 ns<br>010 = 128 ns up to less than 256 ns<br>011 = 256 ns up to less than 512 ns<br>100 = 512 ns up to less than 1 µs<br>101 = 1 µs up to less than 2 µs<br>110 = 2 µs to 4 µs<br>111 = More than 4 µs |
| 15:13[1] | L1_LATENCY | RW | L1 maximum exit latency. This field programs the maximum acceptable latency when exiting the L1 state. This sets bits 11:9 (EP_L1_LAT) in the device capabilities register (offset 74h, see *Section 8.4.50*).<br>000 = Less than 1 µs (default)<br>001 = 1 µs up to less than 2 µs<br>010 = 2 µs up to less than 4 µs<br>011 = 4 µs up to less than 8 µs<br>100 = 8 µs up to less than 16 µs<br>101 = 6 µs up to less than 32 µs<br>110 = 32 µs to 64 µs<br>111 = More than 64 µs |
| 12[1] | VC_CAP_EN | R | VC Capability Structure Enable. This bit is hardwired to 0b indicating that the VC Capability structure is permanently disabled. |
| 11[2] | BPCC_E | RW | Bus power clock control enable. This bit controls whether the secondary bus PCI clocks are stopped when the XIO2001 is placed in the D3 state. It is assumed that if the secondary bus clocks are required to be active, that a reference clock continues to be provided on the PCI Express interface.<br>0 = Secondary bus clocks are not stopped in D3 (default)<br>1 = Secondary bus clocks are stopped on D3 |
| 10[2] | BEACON_ENABLE | RW | Beacon enable. This bit controls the mechanism for waking up the physical PCI Express link when in L2.<br>0 = $\overline{\text{WAKE}}$ mechanism is used exclusively. Beacon is not used (default)<br>1 = Beacon and $\overline{\text{WAKE}}$ mechanisms are used |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-49. General Control Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 9:8[1] | MIN_POWER_SCALE | RW | Minimum power scale. This value is programmed to indicate the scale of bits 7:0 (MIN_POWER_VALUE).<br>00 = 1.0x<br>01 = 0.1x<br>10 = 0.01x (default)<br>11 = 0.001x |
| 7:0[1] | MIN_POWER_VALUE | RW | Minimum power value. This value is programmed to indicate the minimum power requirements. This value is multiplied by the minimum power scale field (bits 9:8) to determine the minimum power requirements for the bridge. The default is 5Fh, indicating that the bridge requires 0.95 W of power. This field can be reprogrammed through an EEPROM or the system BIOS. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.
(2) These bits are sticky and must retain their value when the bridge is powered by $V_{AUX}$.

### 8.4.67 Clock Control Register

This register enables and disables the PCI clock outputs (CLKOUT). See Table 8-50 for a complete description of the register contents.

PCI register offset: D8h
Register type: Read-only, Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-50. Clock Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7[1] | RSVD | R | Reserved. Returns 0b when read. |
| 6[1] | CLOCK6_DISABLE | RW | Clock output 6 disable. This bit disables secondary CLKOUT6.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 5[1] | CLOCK5_DISABLE | RW | Clock output 5 disable. This bit disables secondary CLKOUT5.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 4[1] | CLOCK4_DISABLE | RW | Clock output 4 disable. This bit disables secondary CLKOUT4.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 3[1] | CLOCK3_DISABLE | RW | Clock output 3 disable. This bit disables secondary CLKOUT3.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 2[1] | CLOCK2_DISABLE | RW | Clock output 2 disable. This bit disables secondary CLKOUT2.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 1[1] | CLOCK1_DISABLE | RW | Clock output 1 disable. This bit disables secondary CLKOUT1.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 0[1] | CLOCK0_DISABLE | RW | Clock output 0 disable. This bit disables secondary CLKOUT0.<br>0 = Clock enabled (default)<br>1 = Clock disabled |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.4.68 Clock Mask Register

This register selects which PCI bus clocks are disabled when bits 22:20 (POWER_OVRD) in the general control register (offset D4h, see Section 4.65) are set to 010h or 011h. This register has no effect on the clock outputs if the POWER_OVRD bits are not set to 010h or 011h or if the slot power limit is greater than the power required. See Table 8-51 for a complete description of the register contents.

PCI register offset: D9h
Register type: Read-only, Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-51. Clock Mask Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7 | RSVD | R | Reserved. Returns 0b when read. |
| 6(1) | CLOCK6_MASK | RW | Clock output 6 mask. This bit disables CLKOUT6 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 5(1) | CLOCK5_MASK | RW | Clock output 5 mask. This bit disables CLKOUT5 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 4(1) | CLOCK4_MASK | RW | Clock output 4 mask. This bit disables CLKOUT4 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 3(1) | CLOCK3_MASK | RW | Clock output 3 mask. This bit disables CLKOUT3 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 2(1) | CLOCK2_MASK | RW | Clock output 2 mask. This bit disables CLKOUT2 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 1(1) | CLOCK1_MASK | RW | Clock output 1 mask. This bit disables CLKOUT1 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded.<br>0 = Clock enabled (default)<br>1 = Clock disabled |
| 0 (1) | CLOCK0_MASK | RW | Clock output 0 mask. This bit disables CLKOUT0 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded.<br>0 = Clock enabled (default)<br>1 = Clock disabled |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

### 8.4.69 Clock Run Status Register

The clock run status register indicates the state of the PCI clock-run features in the bridge. See Table 8-52 for a complete description of the register contents.

PCI register offset: DAh
Register type: Read-only
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-52. Clock Run Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:1 | RSVD | R | Reserved. Returns 000 0000b when read. |
| 0(1) | SEC_CLK_STATUS | RU | Secondary clock status. This bit indicates the status of the PCI bus secondary clock outputs.<br>0 = Secondary clock running<br>1 = Secondary clock stopped |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.4.70 Arbiter Control Register

The arbiter control register controls the bridge internal arbiter. The arbitration scheme used is a two-tier rotational arbitration. The bridge is the only secondary bus master that defaults to the higher priority arbitration tier. See Table 8-53 for a complete description of the register contents.

PCI register offset: DCh
Register type: Read/Write
Default value: 40h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-53. Clock Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7(1) | PARK | RW | Bus parking mode. This bit determines where the internal arbiter parks the secondary bus. When this bit is set, the arbiter parks the secondary bus on the bridge. When this bit is cleared, the arbiter parks the bus on the last device mastering the secondary bus.<br>0 = Park the secondary bus on the last secondary bus master (default)<br>1 = Park the secondary bus on the bridge |
| 6(1) | BRIDGE_TIER_SEL | RW | Bridge tier select. This bit determines in which tier the bridge is placed in the arbitration scheme.<br>0 = Lowest priority tier<br>1 = Highest priority tier (default) |
| 5(1) | TIER_SEL5 | RW | $\overline{\text{GNT5}}$ tier select. This bit determines in which tier $\overline{\text{GNT5}}$ is placed in the arbitration scheme.<br>0 = Lowest priority tier (default)<br>1 = Highest priority tier |
| 4(1) | TIER_SEL4 | RW | $\overline{\text{GNT4}}$ tier select. This bit determines in which tier $\overline{\text{GNT4}}$ is placed in the arbitration scheme.<br>0 = Lowest priority tier (default)<br>1 = Highest priority tier |
| 3(1) | TIER_SEL3 | RW | $\overline{\text{GNT3}}$ tier select. This bit determines in which tier $\overline{\text{GNT3}}$ is placed in the arbitration scheme.<br>0 = Lowest priority tier (default)<br>1 = Highest priority tier |
| 2(1) | TIER_SEL2 | RW | $\overline{\text{GNT2}}$ tier select. This bit determines in which tier $\overline{\text{GNT2}}$ is placed in the arbitration scheme.<br>0 = Lowest priority tier (default)<br>1 = Highest priority tier |
| 1(1) | TIER_SEL1 | RW | $\overline{\text{GNT1}}$ tier select. This bit determines in which tier $\overline{\text{GNT1}}$ is placed in the arbitration scheme.<br>0 = Lowest priority tier (default)<br>1 = Highest priority tier |
| 0(1) | TIER_SEL0 | RW | $\overline{\text{GNT0}}$ tier select. This bit determines in which tier $\overline{\text{GNT0}}$ is placed in the arbitration scheme.<br>0 = Lowest priority tier (default)<br>1 = Highest priority tier |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

### 8.4.71 Arbiter Request Mask Register

The arbiter request mask register enables and disables support for requests from specific masters on the secondary bus. The arbiter request mask register also controls if a request input is automatically masked on an arbiter time-out. See Table 8-54 for a complete description of the register contents.

PCI register offset: DDh
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-54. Arbiter Request Mask Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7(1) | ARB_TIMEOUT | RW | Arbiter time-out. This bit enables the arbiter time-out feature. The arbiter time-out is defined as the number of PCI clocks after the PCI bus has gone idle for a device to assert $\overline{\text{FRAME}}$ before the arbiter assumes the device will not respond.<br>0 = Arbiter time disabled (default)<br>1 = Arbiter time-out set to 16 PCI clocks |
| 6(1) | AUTO_MASK | RW | Automatic request mask. This bit enables automatic request masking when an arbiter time-out occurs.<br>0 = Automatic request masking disabled (default)<br>1 = Automatic request masking enabled |
| 5(1) | REQ5_MASK | RW | Request 5 ( $\overline{\text{REQ5}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0.<br>0 = Use request 5 (default)<br>1 = Ignore request 5 |
| 4(1) | REQ4_MASK | RW | Request 4 ( $\overline{\text{REQ4}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0.<br>0 = Use request 4 (default)<br>1 = Ignore request 4 |
| 3(1) | REQ3_MASK | RW | Request 3 ( $\overline{\text{REQ3}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0.<br>0 = Use request 3 (default)<br>1 = Ignore request 3 |
| 2(1) | REQ2_MASK | RW | Request 2 ( $\overline{\text{REQ2}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0.<br>0 = Use request 2 (default)<br>1 = Ignore request 2 |
| 1(1) | REQ1_MASK | RW | Request 1 ( $\overline{\text{REQ1}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0.<br>0 = Use request 2 (default)<br>1 = Ignore request 2 |
| 0(1) | REQ0_MASK | RW | Request 0 ( $\overline{\text{REQ0}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0.<br>0 = Use request 0 (default)<br>1 = Ignore request 0 |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.4.72 Arbiter Time-Out Status Register

The arbiter time-out status register contains the status of each request (request 5–0) time-out. The time-out status bit for the respective request is set if the device did not assert $\overline{\text{FRAME}}$ after the arbiter time-out value. See Table 8-55 for a complete description of the register contents.

PCI register offset: DEh
Register type: Read/Clear
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-55. Arbiter Time-Out Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:6 | RSVD | R | Reserved. Returns 00b when read. |
| 5 | REQ5_TO | RCU | Request 5 Time Out Status<br>0 = No time-out<br>1 = Time-out has occurred |
| 4 | REQ4_TO | RCU | Request 4 Time Out Status<br>0 = No time-out<br>1 = Time-out has occurred |
| 3 | REQ3_TO | RCU | Request 3 Time Out Status<br>0 = No time-out<br>1 = Time-out has occurred |
| 2 | REQ2_TO | RCU | Request 2 Time Out Status<br>0 = No time-out<br>1 = Time-out has occurred |
| 1 | REQ1_TO | RCU | Request 1Time Out Status<br>0 = No time-out<br>1 = Time-out has occurred |
| 0 | REQ0_TO | RCU | Request 0 Time Out Status<br>0 = No time-out<br>1 = Time-out has occurred |

Copyright © 2021 Texas Instruments Incorporated

### 8.4.73 Serial IRQ Mode Control Register

This register controls the behavior of the serial IRQ controller. See Table 8-56 for a complete description of the register contents.

PCI register offset: E0h
Register type: Read-only, Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-56. Serial IRQ Mode Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:4 | RSVD | R | Reserved. Returns 0h when read. |
| 3:2(1) | START_WIDTH | RW | Start frame pulse width. Sets the width of the start frame for a SERIRQ stream.<br>00 = 4 clocks (default)<br>01 = 6 clocks<br>10 = 8 clocks<br>11 = Reserved |
| 1(1) | POLLMODE | RW | Poll mode. This bit selects between continuous and quiet mode.<br>0 = Continuous mode (default)<br>1 = Quiet mode |
| 0(1) | DRIVEMODE | RW | RW Drive mode. This bit selects the behavior of the serial IRQ controller during the recovery cycle.<br>0 = Drive high (default)<br>1 = 3-state |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.74 Serial IRQ Edge Control Register

This register controls the edge mode or level mode for each IRQ in the serial IRQ stream. See Table 8-57 for a complete description of the register contents.

PCI register offset: E2h
Register type: Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-57. Serial IRQ Edge Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15(1) | IRQ15_MODE | RW | IRQ 15 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 14(1) | IRQ14_MODE | RW | IRQ 14 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 13(1) | IRQ13_MODE | RW | IRQ 13 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 12(1) | IRQ12_MODE | RW | IRQ 12 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 11(1) | IRQ11_MODE | RW | IRQ 11 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-57. Serial IRQ Edge Control Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 10(1) | IRQ10_MODE | RW | IRQ 10 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 9(1) | IRQ9_MODE | RW | IRQ 9 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 8(1) | IRQ8_MODE | RW | IRQ 8 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 7(1) | IRQ7_MODE | RW | IRQ 7 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 6(1) | IRQ6_MODE | RW | IRQ 6 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 5(1) | IRQ5_MODE | RW | IRQ 5 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 4(1) | IRQ4_MODE | RW | IRQ 4 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 3(1) | IRQ3_MODE | RW | IRQ 3 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 2(1) | IRQ2_MODE | RW | IRQ 2 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 1(1) | IRQ1_MODE | RW | IRQ 1 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 0(1) | IRQ0_MODE | RW | IRQ 0 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.75 Serial IRQ Status Register

This register indicates when a level mode IRQ is signaled on the serial IRQ stream. After a level mode IRQ is signaled, a write-back of 1b to the asserted IRQ status bit re-arms the interrupt. IRQ interrupts that are defined as edge mode in the serial IRQ edge control register are not reported in this status register. See Table 8-58 for a complete description of the register contents.

PCI register offset: E4h
Register type: Read/Clear
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-58. Serial IRQ Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15(1) | IRQ15 | RCU | IRQ 15 asserted. This bit indicates that the IRQ15 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 14(1) | IRQ14 | RCU | IRQ 14 asserted. This bit indicates that the IRQ14 has been asserted.<br>0 = Deasserted<br>1 = Asserted |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-58. Serial IRQ Status Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 13(1) | IRQ13 | RCU | IRQ 13 asserted. This bit indicates that the IRQ13 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 12(1) | IRQ12 | RCU | IRQ 12 asserted. This bit indicates that the IRQ12 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 11(1) | IRQ11 | RCU | IRQ 11 asserted. This bit indicates that the IRQ11 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 10(1) | IRQ10 | RCU | IRQ 10 asserted. This bit indicates that the IRQ10 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 9(1) | IRQ9 | RCU | IRQ 9 asserted. This bit indicates that the IRQ9 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 8(1) | IRQ8 | RCU | IRQ 8 asserted. This bit indicates that the IRQ8 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 7(1) | IRQ7 | RCU | IRQ 7 asserted. This bit indicates that the IRQ7 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 6(1) | IRQ6 | RCU | IRQ 6 asserted. This bit indicates that the IRQ6 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 5(1) | IRQ5 | RCU | IRQ 5 asserted. This bit indicates that the IRQ5 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 4(1) | IRQ4 | RCU | IRQ 4 asserted. This bit indicates that the IRQ4 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 3(1) | IRQ3 | RCU | IRQ 3 asserted. This bit indicates that the IRQ3 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 2(1) | IRQ2 | RCU | IRQ 2 asserted. This bit indicates that the IRQ2 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 1(1) | IRQ1 | RCU | IRQ 1 asserted. This bit indicates that the IRQ1 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 0(1) | IRQ0 | RCU | IRQ 0 asserted. This bit indicates that the IRQ0 has been asserted.<br>0 = Deasserted<br>1 = Asserted |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.76 Pre-Fetch Agent Request Limits Register

This register is used to set the Pre-Fetch Agent's limits on retrieving data using upstream reads. See Table 8-59 for a complete description of the register contents.

PCI register offset: E8h
Register type: Read/Clear
Default value: 0443h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-59. Pre-Fetch Agent Request Limits Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:12 | RSVD | R | Reserved. Returns 0h when read. |
| 11:8[1] | PFA_REQ_CNT_LIMIT | RW | Request count limit. Determines the number of Pre-Fetch reads that takes place in each burst.<br>4'h0 = Auto-prefetch agent is disabled.<br>4'h1 = Thread is limited to one buffer. No auto-prefetch reads will be generated.<br>4'h2:F = Thread will be limited to initial read and (PFA_REQ_CNT_LIMIT – 1) |
| 7:6 | PFA_CPL_CACHE_MODE | RW | Completion cache mode. Determines the rules for completing the caching process.<br>00 = No caching.<br>• Pre-fetching is disabled.<br>• All remaining read completion data will be discarded after any of the data has been returned to the PCI master.<br>01 = Light caching.<br>• Pre-fetching is enabled.<br>• All remaining read completion data will be discarded after data has been returned to the PCI master and the PCI master terminated the transfer.<br>• All remaining read completion data will be cached after data has been returned to the PCI master and the bridge has terminated the transfer with RETRY.<br>10 = Full caching.<br>• Pre-fetching is enabled.<br>• All remaining read completion data will be cached after data has been returned to the PCI master and the PCI master terminated the transfer.<br>• All remaining read completion data will be cached after data has been returned to the PCI master and the bridge has terminated the transfer with RETRY.<br>11 = Reserved. |
| 5:4 | RSVD | R | Reserved. Returns 00b when read. |
| 3:0 | PFA_REQ_LENGTH_LIMIT | RW | Request Length Limit. Determines the number of bytes in the thread that the pre-fetch agent will read for that thread.<br>0000 = 64 bytes<br>0001 = 128 bytes<br>0010 = 256 bytes<br>0011 = 512 bytes<br>0100 = 1 Kbytes<br>0101 = 2 Kbytes<br>0110 = 4 Kbytes<br>0111 = 8 Kbytes<br>1000:1111 = Reserved |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.77 Cache Timer Transfer Limit Register

This register is used to set the number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded. See Table 8-60 for a complete description of the register contents.

PCI register offset: EAh
Register type: Read/Clear
Default value: 0008h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Table 8-60. Cache Timer Transfer Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:8 | RSVD | R | Reserved. Returns 00h when read. |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-60. Cache Timer Transfer Limit Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:0[1] | CACHE_TMR_XFR_LIMIT | RW | Number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.78 Cache Timer Lower Limit Register

Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the "cache miss limit" check can be triggered. See Table 8-61 for a complete description of the register contents.

PCI register offset: ECh
Register type: Read/Clear
Default value: 007Fh

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 8-61. Cache Timer Lower Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:12 | RSVD | R | Reserved. Returns 0h when read. |
| 11:0[1] | CACHE_TIMER_LOWER_LIMIT | RW | Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the "cache miss limit" check can be triggered. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.4.79 Cache Timer Upper Limit Register

Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer. See Table 8-62 for a complete description of the register contents.

PCI register offset: EEh
Register type: Read/Clear
Default value: 01C0h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-62. Cache Timer Upper Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:12 | RSVD | R | Reserved. Returns 0h when read. |
| 11:0[1] | CACHE_TIMER_UPPER_LIMIT | RW | Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

## 8.5 PCI Express Extended Configuration Space

The programming model of the PCI Express extended configuration space is compliant to the *PCI Express Base Specification* and the *PCI Express to PCI/PCI-X Bridge Specification* programming models. The PCI Express extended configuration map uses the PCI Express advanced error reporting capability.

All bits marked with a ☆ are sticky bits and are reset by a global reset ( $\overline{\text{GRST}}$) or the internally-generated power-on reset. All bits marked with a ☆ are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

**Table 8-63. PCI Express Extended Configuration Register Map**

| REGISTER NAME | | OFFSET |
|---|---|---|
| Next capability offset / capability version(1) | PCI Express advanced error reporting capabilities ID(1) | 100h |
| Uncorrectable error status register | | 104h |
| Uncorrectable error mask register | | 108h |
| Uncorrectable error severity register | | 10Ch |
| Correctable error status register | | 110h |
| Correctable error mask | | 114h |
| Advanced error capabilities and control | | 118h |
| Header log register | | 11Ch |
| Header log register | | 120h |
| Header log register | | 124h |
| Header log register | | 128h |
| Secondary uncorrectable error status | | 12Ch |
| Secondary uncorrectable error mask | | 130h |
| Secondary uncorrectable error severity register | | 134h |
| Secondary error capabilities and control register | | 138h |
| Secondary header log register | | 13Ch |
| Secondary header log register | | 140h |
| Secondary header log register | | 144h |
| Secondary header log register | | 148h |
| Reserved | | 14Ch–FFCh |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.5.1 Advanced Error Reporting Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express advanced error reporting capabilities. The register returns 0001h when read.

PCI Express extended register offset: 100h
Register type: Read-only
Default value: 0001h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Copyright © 2021 Texas Instruments Incorporated

### 8.5.2 Next Capability Offset/Capability Version Register

This read-only register identifies the next location in the PCI Express extended capabilities link list. The upper 12 bits in this register shall be 000h, indicating that the Advanced Error Reporting Capability is the last capability in the linked list. The least significant four bits identify the revision of the current capability block as 1h.

PCI Express extended register offset: 102h
Register type: Read-only
Default value: 0001h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

### 8.5.3 Uncorrectable Error Status Register

The uncorrectable error status register reports the status of individual errors as they occur on the primary PCI Express interface. Software may only clear these bits by writing a 1b to the desired location. See Table 8-64 for a complete description of the register contents.

PCI Express extended register offset: 104h
Register type: Read-only, Read/Clear
Default value: 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-64. Uncorrectable Error Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:22 | RSVD | R | Reserved. Returns 000 0000 0000b when read. |
| 21 | ACS_VIOLATION | R | ACS Violation. Not supported, ths bit returns 0b when read. |
| 20(1) | UR_ERROR | RCU | Unsupported request error. This bit is asserted when an unsupported request is received. |
| 19(1) | ECRC_ERROR | RCU | Extended CRC error. This bit is asserted when an extended CRC error is detected. |
| 18(1) | MAL_TLP | RCU | Malformed TLP. This bit is asserted when a malformed TLP is detected. |
| 17(1) | RX_OVERFLOW | RCU | Receiver overflow. This bit is asserted when the flow control logic detects that the transmitting device has illegally exceeded the number of credits that were issued. |
| 16(1) | UNXP_CPL | RCU | Unexpected completion. This bit is asserted when a completion packet is received that does not correspond to an issued request. |
| 15(1) | CPL_ABORT | RCU | Completer abort. This bit is asserted when the bridge signals a completer abort. |
| 14(1) | CPL_TIMEOUT | RCU | Completion time-out. This bit is asserted when no completion has been received for an issued request before the time-out period. |
| 13(1) | FC_ERROR | RCU | Flow control error. This bit is asserted when a flow control protocol error is detected either during initialization or during normal operation. |
| 12(1) | PSN_TLP | RCU | Poisoned TLP. This bit is asserted when a poisoned TLP is received. |
| 11:6 | RSVD | R | Reserved. Returns 00 0000b when read. |
| 5 | SD_ERROR | R | Surprise down error. Not supported, this bit returns 0b when read. |
| 4(1) | DLL_ERROR | RCU | Data link protocol error. This bit is asserted if a data link layer protocol error is detected. |
| 3:0 | RSVD | R | Reserved. Returns 0h when read. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.5.4 Uncorrectable Error Mask Register

The uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 8-65 for a complete description of the register contents.

PCI Express extended register offset: 108h
Register type: Read-only, Read/Write
Default value: 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-65. Uncorrectable Error Mask Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:22 | RSVD | R | Reserved. Returns 000 0000 0000b when read. |
| 21 | ACS_VIOLATION_MASK | RW | ACS Violation mask. Not supported, this bit returns 0b when read. |
| 20(1) | UR_ERROR_MASK | RW | Unsupported request error mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 19(1) | ECRC_ERROR_MASK | RW | Extended CRC error mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 18(1) | MAL_TLP_MASK | RW | Malformed TLP mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 17(1) | RX_OVERFLOW_MASK | RW | Receiver overflow mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 16(1) | UNXP_CPL_MASK | RW | Unexpected completion mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 15(1) | CPL_ABORT_MASK | RW | Completer abort mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 14(1) | CPL_TIMEOUT_MASK | RW | Completion time-out mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 13(1) | FC_ERROR_MASK | RW | Flow control error mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 12(1) | PSN_TLP_MASK | RW | Poisoned TLP mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 11:6 | RSVD | R | Reserved. Returns 000 0000b when read. |
| 5 | SD_ERROR_MASK | R | SD error mask. Not supported, returns 0b when read. |
| 4(1) | DLL_ERROR_MASK | RW | Data link protocol error mask<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-65. Uncorrectable Error Mask Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 3:0 | RSVD | R | Reserved. Returns 0h when read. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.5.5 Uncorrectable Error Severity Register

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 8-66 for a complete description of the register contents.

PCI Express extended register offset: 10Ch
Register type: Read-only, Read/Write
Default value: 0006 2031h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

**Table 8-66. Uncorrectable Error Severity Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:22 | RSVD | R | Reserved. Returns 000 0000 0000b when read. |
| 21 | ACS_VIOLATION_SEVR | R | ACS violation severity. Not supported, returns 0b when read. |
| 20(1) | UR_ERROR_SEVRO | RW | Unsupported request error severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 19(1) | ECRC_ERROR_SEVRR | RW | Extended CRC error severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 18(1) | MAL_TLP_SEVR | RW | Malformed TLP severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 17(1) | RX_OVERFLOW_SEVR | RW | Receiver overflow severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 16(1) | UNXP_CPL_SEVRP | RW | Unexpected completion severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 15(1) | CPL_ABORT_SEVR | RW | Completer abort severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 14(1) | CPL_TIMEOUT_SEVR | RW | Completion time-out severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 13(1) | FC_ERROR_SEVR | RW | Flow control error severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 12(1) | PSN_TLP_SEVR | RW | Poisoned TLP severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 11:6 | RSVD | R | Reserved. Returns 000 000b when read. |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-66. Uncorrectable Error Severity Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 5 | SD_ERROR_SEVR | R | SD error severity. Not supported, returns 1b when read. |
| 4(1) | DLL_ERROR_SEVR | RW | Data link protocol error severity<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL |
| 3:1 | RSVD | R | Reserved. Retirms 000b wjem read/ |
| 0 | RSVD | R | Reserved. Returns 1h when read. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.5.6 Correctable Error Status Register

The correctable error status register reports the status of individual errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 8-67 for a complete description of the register contents.

PCI Express extended register offset: 110h
Register type: Read-only, Read/Clear
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-67. Correctable Error Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:14 | RSVD | R | Reserved. Returns 000 0000 0000 0000 0000b when read. |
| 13(1) | ANFES | RCU | Advisory Non-Fatal Error Status. This bit is asserted when an Advisor Non-Fatal Error has been reported. |
| 12 (1) | REPLAY_TMOUT | RCU | Replay timer time-out. This bit is asserted when the replay timer expires for a pending request or completion that has not been acknowledged. |
| 11:9 | RSVD | R | Reserved. Returns 000b when read. |
| 8(1) | REPLAY_ROLL | RCU | REPLAY_NUM rollover. This bit is asserted when the replay counter rolls over after a pending request or completion has not been acknowledged. |
| 7(1) | BAD_DLLP | RCU | Bad DLLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a DLLP. |
| 6(1) | BAD_TLP | RCU | Bad TLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a TLP. |
| 5:1 | RSVD | R | Reserved. Returns 00000b when read. |
| 0(1) | RX_ERROR | RCU | Receiver error. This bit is asserted when an 8b/10b error is detected by the PHY at any time. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

### 8.5.7 Correctable Error Mask Register

The correctable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 8-68 for a complete description of the register contents.

PCI Express extended register offset: 114h
Register type: Read-only, Read/Write
Default value: 0000 2000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-68. Correctable Error Mask Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:14 | RSVD | R | Reserved. Returns 000 0000 0000 0000 0000b when read. |
| 13(1) | ANFEM | RW | Advisory Non-Fatal Error Mask.<br>0 = Error condition is unmasked<br>1 = Error condition is masked (default) |
| 12(1) | REPLAY_TMOUT_MASK | RW | Replay timer time-out mask.<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 11:9 | RSVD | R | Reserved. Returns 000b when read. |
| 8(1) | REPLAY_ROLL_MASK | RW | REPLAY_NUM rollover mask.<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 7(1) | BAD_DLLP_MASK | RW | Bad DLLP error mask.<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 6(1) | BAD_TLP_MASK | RW | Bad TLP error mask.<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |
| 5:1 | RSVD | R | Reserved. Returns 00000b when read. |
| 0(1) | RX_ERROR_MASK | RW | Receiver error mask.<br>0 = Error condition is unmasked (default)<br>1 = Error condition is masked |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.5.8 Advanced Error Capabilities and Control Register

The advanced error capabilities and control register allows the system to monitor and control the advanced error reporting capabilities. See Table 8-69 for a complete description of the register contents.

PCI Express extended register offset: 118h
Register type: Read-only, Read/Write
Default value: 0000 00A0h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**Table 8-69. Advanced Error Capabilities and Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:9 | RSVD | R | Reserved. Returns 000 0000 0000 0000 0000 0000b when read. |
| 8(1) | ECRC_CHK_EN | RW | Extended CRC check enable<br>0 = Extended CRC checking is disabled<br>1 = Extended CRC checking is enabled |
| 7 | ECRC_CHK_CAPABLE | R | Extended CRC check capable. This read-only bit returns a value of 1b indicating that the bridge is capable of checking extended CRC information. |
| 6(1) | ECRC_GEN_EN | RW | Extended CRC generation enable<br>0 = Extended CRC generation is disabled<br>1 = Extended CRC generation is enabled |
| 5 | ECRC_GEN_CAPABLE | R | Extended CRC generation capable. This read-only bit returns a value of 1b indicating that the bridge is capable of generating extended CRC information. |
| 4:0(1) | FIRST_ERR | RU | First error pointer. This 5-bit value reflects the bit position within the uncorrectable error status register (offset 104h, see *Section 8.5.3*) corresponding to the class of the first error condition that was detected. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.5.9 Header Log Register

The header log register stores the TLP header for the packet that lead to the most recently detected error condition. Offset 11Ch contains the first DWORD. Offset 128h contains the last DWORD (in the case of a 4DW TLP header). Each DWORD is stored with the least significant byte representing the earliest transmitted. This register shall only be reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI Express extended register offset: 11Ch, 120h, 124h, and 128h
Register type: Read-only
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Copyright © 2021 Texas Instruments Incorporated

### 8.5.10 Secondary Uncorrectable Error Status Register

The secondary uncorrectable error status register reports the status of individual PCI bus errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 8-70 for a complete description of the register contents.

PCI Express extended register offset: 12Ch
Register type: Read-only, Read/Clear
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-70. Secondary Uncorrectable Error Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:14 | RSVD | R | Reserved. Returns 000 0000 0000 0000 0000b when read. |
| 13 | INTERNAL_ERROR | R | Internal bridge error. This error bit is associated with a PCI-X error and returns 0b when read. |
| 12(1) | SERR_DETECT | RCU | $\overline{\text{SERR}}$ assertion detected. This bit is asserted when the bridge detects the assertion of $\overline{\text{SERR}}$ on the secondary bus. |
| 11(1) | PERR_DETECT | RCU | PERR assertion detected. This bit is asserted when the bridge detects the assertion of PERR on the secondary bus. |
| 10(1) | DISCARD_TIMER | RCU | Delayed transaction discard timer expired. This bit is asserted when the discard timer expires for a pending delayed transaction that was initiated on the secondary bus. |
| 9(1) | UNCOR_ADDR | RCU | Uncorrectable address error. This bit is asserted when the bridge detects a parity error during the address phase of an upstream transaction. |
| 8 | UNCOR_ATTRIB | R | Uncorrectable attribute error. This error bit is associated with a PCI-X error and returns 0b when read. |
| 7(1) | UNCOR_DATA | RCU | Uncorrectable data error. This bit is asserted when the bridge detects a parity error during a data phase of an upstream write transaction, or when the bridge detects the assertion of PERR when forwarding read completion data to a PCI device. |
| 6 | UNCOR_SPLTMSG | R | Uncorrectable split completion message data error. This error bit is associated with a PCI-X error and returns 0b when read. |
| 5 | UNXPC_SPLTCMP | R | Unexpected split completion error. This error bit is associated with a PCI-X error and returns 0b when read. |
| 4 | RSVD | R | Reserved. Returns 0b when read. |
| 3(1) | MASTER_ABORT | RCU | Received master abort. This bit is asserted when the bridge receives a master abort on the PCI interface. |
| 2(1) | TARGET_ABORT | RCU | Received target abort. This bit is asserted when the bridge receives a target abort on the PCI interface. |
| 1 | MABRT_SPLIT | R | Master abort on split completion. This error bit is associated with a PCI-X error and returns 0b when read. |
| 0 | TABRT_SPLIT | R | Target abort on split completion status. This error bit is associated with a PCI-X error and returns 0b when read. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.5.11 Secondary Uncorrectable Error Severity

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 8-71 for a complete description of the register contents.

PCI Express extended register offset: 134h


Copyright © 2021 Texas Instruments Incorporated

Register type: Read-only, Read/Write

Default value: 0000 1340h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-71. Secondary Uncorrectable Error Severity Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:14 | RSVD | R | Reserved. Returns 00 0000 0000 0000 0000b when read. |
| 13(1) | INTERNAL_ERROR_SEVR | RW | Internal bridge error. This severity bit is associated with a PCI-X error and has no effect on the bridge. |
| 12(1) | SERR_DETECT_SEVR | RW | $\overline{\text{SERR}}$ assertion detected<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL (default) |
| 11(1) | PERR_DETECT_SEVR | RW | $\overline{\text{PERR}}$ assertion detected<br>0 = Error condition is signaled using ERR_NONFATAL (default)<br>1 = Error condition is signaled using ERR_FATAL |
| 10(1) | DISCARD_TIMER_SEVR | RW | Delayed transaction discard timer expired<br>0 = Error condition is signaled using ERR_NONFATAL (default)<br>1 = Error condition is signaled using ERR_FATAL |
| 9(1) | UNCOR_ADDR_SEVR | RW | Uncorrectable address error<br>0 = Error condition is signaled using ERR_NONFATAL<br>1 = Error condition is signaled using ERR_FATAL (default) |
| 8(1) | UNCOR_ATTRIB_SEVR | RW | Uncorrectable attribute error. This severity bit is associated with a PCI-X error and has no effect on the bridge. |
| 7(1) | UNCOR_DATA_SEVR | RW | Uncorrectable data error<br>0 = Error condition is signaled using ERR_NONFATAL (default)<br>1 = Error condition is signaled using ERR_FATAL |
| 6(1) | UNCOR_SPLTMSG_SEVR | RW | Uncorrectable split completion message data error. This severity bit is associated with a PCI-X error and has no effect on the bridge. |
| 5(1) | UNCOR_SPLTCMP_SEVR | RW | Unexpected split completion error. This severity bit is associated with a PCI-X error and has no effect on the bridge. |
| 4 | RSVD | R | Reserved. Returns 0b when read. |
| 3(1) | MASTER_ABORT_SEVR | RW | Received master abort<br>0 = Error condition is signaled using ERR_NONFATAL (default)<br>1 = Error condition is signaled using ERR_FATAL |
| 2(1) | TARGET_ABORT_SEVR | RW | Received target aborta<br>0 = Error condition is signaled using ERR_NONFATAL (default)<br>1 = Error condition is signaled using ERR_FATAL |
| 1(1) | MABRT_SPLIT_SEVR | RW | Master abort on split completion. This severity bit is associated with a PCI-X error and has no effect on the bridge. |
| 0 | TABRT_SPLIT_SEVR | R | Target abort on split completion. This severity bit is associated with a PCI-X error and has no effect on the bridge. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

### 8.5.12 Secondary Error Capabilities and Control Register

The secondary error capabilities and control register allows the system to monitor and control the secondary advanced error reporting capabilities. See Table 8-72 for a complete description of the register contents.

PCI Express extended register offset: 138h
Register type: Read-only
Default value: 0000 0000h

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-72. Secondary Error Capabilities and Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 31:5 | RSVD | R | Reserved. Return 000 0000 0000 0000 0000 0000 0000b when read. |
| 4:0(1) | SEC_FIRST_ERR | RU | First error pointer. This 5-bit value reflects the bit position within the secondary uncorrectable error status register (offset 12Ch, see *Section 8.5.10*) corresponding to the class of the first error condition that was detected. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.5.13 Secondary Header Log Register

The secondary header log register stores the transaction address and command for the PCI bus cycle that led to the most recently detected error condition. Offset 13Ch accesses register bits 31:0. Offset 140h accesses register bits 63:32. Offset 144h accesses register bits 95:64. Offset 148h accesses register bits 127:96. See Table 8-73 for a complete description of the register contents.

PCI Express extended register offset: 13Ch, 140h, 144h, and 148h
Register type: Read-only
Default value: 0000 0000h

| BIT NUMBER | 127 | 126 | 125 | 124 | 123 | 122 | 121 | 120 | 119 | 118 | 117 | 116 | 115 | 114 | 113 | 112 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 111 | 110 | 109 | 108 | 107 | 106 | 105 | 104 | 103 | 102 | 101 | 100 | 99 | 98 | 97 | 96 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 95 | 94 | 93 | 92 | 91 | 90 | 89 | 88 | 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 79 | 78 | 77 | 76 | 75 | 74 | 73 | 72 | 71 | 70 | 69 | 68 | 67 | 66 | 65 | 64 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-73. Secondary Header Log Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 127:64(1) | ADDRESS | RU | Transaction address. The 64-bit value transferred on AD[31:0] during the first and second address phases. The first address phase is logged to 95:64 and the second address phase is logged to 127:96. In the case of a 32-bit address, bits 127:96 are set to 0. |
| 63:44 | RSVD | R | Reserved. Returns 0 0000h when read. |
| 43:40(1) | UPPER_CMD | RU | Transaction command upper. Contains the status of the $\overline{C/BE}$ terminals during the second address phase of the PCI transaction that generated the error if using a dual-address cycle. |
| 39:36(1) | LOWER_CMD | RU | Transaction command lower. Contains the status of the $\overline{C/BE}$ terminals during the first address phase of the PCI transaction that generated the error. |
| 35:0 | TRANS_ATTRIBUTE | R | Transaction attribute. Because the bridge does not support the PCI-X attribute transaction phase, these bits have no function, and return 0 0000 0000h when read. |

(1) These bits are reset by a PCI Express reset ( $\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

## 8.6 Memory-Mapped TI Proprietary Register Space

The programming model of the memory-mapped TI proprietary register space is unique to this device.

All bits marked with a ☆ are sticky bits and are reset by a global reset ( $\overline{\text{GRST}}$) or the internally-generated power-on reset. All bits marked with a[(1)] are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$ or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

**Table 8-74. Device Control Memory Window Register Map**

| REGISTER NAME | | | | OFFSET |
|---|---|---|---|---|
| Reserved | | Revision ID | Device control map ID | 000h |
| Reserved | | | | 004h–03Ch |
| GPIO data[(1)] | | GPIO control [(1)] | | 040h |
| Serial-bus control and status[(1)] | Serial-bus slave address[(1)] | Serial-bus word address[(1)] | Serial-bus data[(1)] | 044h |
| Serial IRQ edge control[(1)] | | Reserved | Serial IRQ mode control[(1)] | 048h |
| Reserved | | Serial IRQ status[(1)] | | 04Ch |
| Cache Timer Transfer Limit[(1)] | | PFA Request Limit[(1)] | | 050h |
| Cache Timer Upper Limit[(1)] | | Cache Timer Lower Limit[(1)] | | 054h |
| Reserved | | | | 058h–FFFh |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.6.1 Device Control Map ID Register

The device control map ID register identifies the TI proprietary layout for this device control map. The value 04h identifies this as a PCI Express-to-PCI bridge.

Device control memory window register offset: 00h
Register type: Read-only
Default value: 04h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

### 8.6.2 Revision ID Register

The revision ID register identifies the revision of the TI proprietary layout for this device control map. The value 00h identifies the revision as the initial layout.

Device control memory window register offset: 01h
Register type: Read-only
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


Copyright © 2021 Texas Instruments Incorporated

### 8.6.3 GPIO Control Register

This register controls the direction of the five GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO3 (SDA), and GPIO4 (SCL). This register is an alias of the GPIO control register in the classic PCI configuration space(offset B4h, see *Section 8.4.60*). See Table 8-75 for a complete description of the register contents.

Device control memory window register offset: 40h
Register type: Read-only, Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-75. GPIO Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:5 | RSVD | R | Reserved. Returns 0000 0000 000b when read. |
| 4(1) | GPIO4_DIR | RW | GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode.<br>0 = Input (default)<br>1 = Output |
| 3(1) | GPIO3_DIR | RW | GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode.<br>0 = Input (default)<br>1 = Output |
| 2(1) | GPIO2_DIR | RW | GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode.<br>0 = Input (default)<br>1 = Output |
| 1(1) | GPIO1_DIR | RW | GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode.<br>0 = Input (default)<br>1 = Output |
| 0(1) | GPIO0_DIR | RW | GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode.<br>0 = Input (default)<br>1 = Output |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

### 8.6.4 GPIO Data Register

This register reads the state of the input mode GPIO terminals and changes the state of the output mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO3 (SDA), and GPIO4 (SCL). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. This register is an alias of the GPIO data register in the classic PCI configuration space (offset B6h, see *Section 8.4.61*). See Table 8-76 for a complete description of the register contents.

Device control memory window register offset: 42h
Register type: Read-only, Read/Write
Default value: 00XXh

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | x |

**Table 8-76. GPIO Data Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:5 | RSVD | R | Reserved. Returns 000 0000 0000b when read. |
| 4(1) | GPIO4_Data | RW | GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode. |
| 3(1) | GPIO3_Data | RW | GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode. |
| 2(1) | GPIO2_Data | RW | GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode. |
| 1(1) | GPIO1_Data | RW | GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode. |
| 0(1) | GPIO0_Data | RW | GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.6.5 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) in the serial-bus control and status register (offset 47h, see *Section 8.6.8*) is cleared. This register is an alias for the serial-bus data register in the PCI header (offset B0h, see *Section 8.4.56*). This register is reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Device control memory window register offset: 44h
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |


Copyright © 2021 Texas Instruments Incorporated

### 8.6.6 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to on the serial-bus interface. The word address is loaded into this register prior to writing the serial-bus slave address register that initiates the bus cycle. This register is an alias for the serial-bus word address register in the PCI header (offset B1h, see *Section 8.4.57*). This register is reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Device control memory window register offset: 45h
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### 8.6.7 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle will be a read or a write cycle. Writing to this register initiates the cycle on the serial interface. This register is an alias for the serial-bus slave address register in the PCI header (offset B2h, see *Section 8.4.58*). See Table 8-77 for a complete description of the register contents.

Device control memory window register offset: 46h
Register type: Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-77. Serial-Bus Slave Address Register Descriptions**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:1(1) | SLAVE_ADDR | RW | Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b. |
| 0(1) | RW_CMD | RW | Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle.<br>0 = A single byte write is requested (default)<br>1 = A single byte read is requested |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.6.8 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial-bus. This register is an alias for the serial-bus control and status register in the PCI header (offset B3h, see *Section 8.4.59*). See Table 8-78 for a complete description of the register contents.

Device control memory window register offset: 47h
Register type: Read-only, Read/Write, Read/Clear
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-78. Serial-Bus Control and Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7(1) | PROT_SEL | RW | Protocol select. This bit selects the serial-bus address mode used.<br>0 = Slave address and word address are sent on the serial-bus (default)<br>1 = Only the slave address is sent on the serial-bus |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-78. Serial-Bus Control and Status Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 6 | RSVD | R | Reserved. Returns 0b when read. |
| 5(1) | REQBUSY | RU | Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress.<br>0 = No serial-bus cycle<br>1 = Serial-bus cycle in progresss |
| 4(1) | ROMBUSY | RU | Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM.<br>0 = No EEPROM activity<br>1 = EEPROM download in progress |
| 3(1) | SBDETECT | RWU | Serial EEPROM detected. This bit enables the serial-bus interface. The value of this bit controls whether the GPIO3//SDA and GPIO4//SCL terminals are configured as GPIO signals or as serial-bus signals. This bit is automatically set to 1b when a serial EEPROM is detected.<br>**Note:** A serial EEPROM is only detected once following $\overline{\text{PERST}}$.<br>0 = No EEPROM present, EEPROM load process does not happen. GPIO3//SDA and GPIO4//SCL terminals are configured as GPIO signals.<br>1 = EEPROM present, EEPROM load process takes place. GPIO3//SDA and GPIO4//SCL terminals are configured as serial-bus signals. |
| 2(1) | SBTEST | RW | Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock.<br>0 = Serial-bus clock at normal operating frequency ~ 60 kHz (default)<br>1 = Serial-bus clock frequency increased for test purposes ~ 4 MHz |
| 1(1) | SB_ERR | RCU | Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle.<br>0 = No error<br>1 = Serial-bus error |
| 0(1) | ROM_ERR | RCU | Serial EEPROM load error. This bit is set when an error occurs while downloading registers from a serial EEPROM.<br>0 = No error<br>1 = EEPROM load error |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.6.9 Serial IRQ Mode Control Register

This register controls the behavior of the serial IRQ controller. This register is an alias for the serial IRQ mode control register in the classic PCI configuration space (offset E0h, see *Section 8.4.73*). See Table 8-56 for a complete description of the register contents.

Device control memory window register offset: 48h
Register type: Read-only, Read/Write
Default value: 00h

| BIT NUMBER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-79. Serial IRQ Mode Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 7:4 | RSVD | R | Reserved. Returns 0h when read. |
| 3:2(1) | START_WIDTH | RW | Start frame pulse width. Sets the width of the start frame for a SERIRQ stream.<br>00 = 4 clocks (default)<br>01 = 6 clocks<br>10 = 8 clocks<br>11 = Reserved |
| 1(1) | POLLMODE | RW | Poll mode. This bit selects between continuous and quiet mode.<br>0 = Continuous mode (default)<br>1 = Quiet mode |
| 0(1) | DRIVEMODE | RW | RW Drive mode. This bit selects the behavior of the serial IRQ controller during the recovery cycle.<br>0 = Drive high (default)<br>1 = 3-state |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.6.10 Serial IRQ Edge Control Register

This register controls the edge mode or level mode for each IRQ in the serial IRQ stream. This register is an alias for the serial IRQ edge control register in the classic PCI configuration space (offset E2h, see *Section 8.4.74*). See Table 8-80 for a complete description of the register contents.

Device control memory window register offset: 4Ah
Register type: Read/Write
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-80. Serial IRQ Edge Control Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15(1) | IRQ15_MODE | RW | IRQ 15 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 14(1) | IRQ14_MODE | RW | IRQ 14 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 13(1) | IRQ13_MODE | RW | IRQ 13 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 12(1) | IRQ12_MODE | RW | IRQ 12 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 11(1) | IRQ11_MODE | RW | IRQ 11 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 10(1) | IRQ10_MODE | RW | IRQ 10 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 9(1) | IRQ9_MODE | RW | IRQ 9 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 8(1) | IRQ8_MODE | RW | IRQ 8 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 7(1) | IRQ7_MODE | RW | IRQ 7 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 6(1) | IRQ6_MODE | RW | IRQ 6 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 5(1) | IRQ5_MODE | RW | IRQ 5 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 4(1) | IRQ4_MODE | RW | IRQ 4 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 3(1) | IRQ3_MODE | RW | IRQ 3 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 2(1) | IRQ2_MODE | RW | IRQ 2 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 1(1) | IRQ1_MODE | RW | IRQ 1 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |
| 0(1) | IRQ0_MODE | RW | IRQ 0 edge mode<br>0 = Edge mode (default)<br>1 = Level mode |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.6.11 Serial IRQ Status Register

This register indicates when a level mode IRQ is signaled on the serial IRQ stream. After a level mode IRQ is signaled, a write-back of 1b to the asserted IRQ status bit re-arms the interrupt. IRQ interrupts that are defined as edge mode in the serial IRQ edge control register are not reported in this status register. This register is an alias for the serial IRQ status register in the classic PCI configuration space (offset E4h, see *Section 8.4.75*). See Table 8-58 for a complete description of the register contents.

Device control memory window register offset: 4Ch
Register type: Read/Clear
Default value: 0000h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-81. Serial IRQ Status Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15[1] | IRQ15 | RCU | IRQ 15 asserted. This bit indicates that the IRQ15 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 14[1] | IRQ14 | RCU | IRQ 14 asserted. This bit indicates that the IRQ14 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 13[1] | IRQ13 | RCU | IRQ 13 asserted. This bit indicates that the IRQ13 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 12[1] | IRQ12 | RCU | IRQ 12 asserted. This bit indicates that the IRQ12 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 11[1] | IRQ11 | RCU | IRQ 11 asserted. This bit indicates that the IRQ11 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 10[1] | IRQ10 | RCU | IRQ 10 asserted. This bit indicates that the IRQ10 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 9[1] | IRQ9 | RCU | IRQ 9 asserted. This bit indicates that the IRQ9 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 8[1] | IRQ8 | RCU | IRQ 8 asserted. This bit indicates that the IRQ8 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 7[1] | IRQ7 | RCU | IRQ 7 asserted. This bit indicates that the IRQ7 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 6[1] | IRQ6 | RCU | IRQ 6 asserted. This bit indicates that the IRQ6 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 5[1] | IRQ5 | RCU | IRQ 5 asserted. This bit indicates that the IRQ5 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 4[1] | IRQ4 | RCU | IRQ 4 asserted. This bit indicates that the IRQ4 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 3[1] | IRQ3 | RCU | IRQ 3 asserted. This bit indicates that the IRQ3 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 2[1] | IRQ2 | RCU | IRQ 2 asserted. This bit indicates that the IRQ2 has been asserted.<br>0 = Deasserted<br>1 = Asserted |

Copyright © 2021 Texas Instruments Incorporated

**Table 8-81. Serial IRQ Status Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 1(1) | IRQ1 | RCU | IRQ 1 asserted. This bit indicates that the IRQ1 has been asserted.<br>0 = Deasserted<br>1 = Asserted |
| 0(1) | IRQ0 | RCU | IRQ 0 asserted. This bit indicates that the IRQ0 has been asserted.<br>0 = Deasserted<br>1 = Asserted |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.6.12 Pre-Fetch Agent Request Limits Register

This register is used to set the Pre-Fetch Agent's limits on retrieving data using upstream reads. This register is an alias for the pre-fetch agent request limits register in the classic PCI configuration space (offset E8h, see *Section 8.4.76*). See Table 8-82 for a complete description of the register contents.

Device control memory window register offset: 50h
Register type: Read/Clear
Default value: 0443h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |

**Table 8-82. Pre-Fetch Agent Request Limits Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:12 | RSVD | R | Reserved. Returns 0h when read. |
| 11:8(1) | PFA_REQ_<br>CNT_LIMIT | RW | Request count limit. Determines the number of Pre-Fetch reads that takes place in each burst.<br>4'h0 = Auto-prefetch agent is disabled.<br>4'h1 = Thread is limited to one buffer. No auto-prefetch reads will be generated.<br>4'h2:F = Thread will be limited to initial read and (PFA_REQ_CNT_LIMIT – 1) |
| 7:6 | PFA_CPL_CACHE_<br>MODE | RW | Completion cache mode. Determines the rules for completing the caching process.<br>00 = No caching.<br>• Pre-fetching is disabled.<br>• All remaining read completion data will be discarded after any of the data has been returned to the PCI master.<br>01 = Light caching.<br>• Pre-fetching is enabled.<br>• All remaining read completion data will be discarded after data has been returned to the PCI master and the PCI master terminated the transfer.<br>• All remaining read completion data will be cached after data has been returned to the PCI master and the bridge has terminated the transfer with RETRY.<br>10 = Full caching.<br>• Pre-fetching is enabled.<br>• All remaining read completion data will be cached after data has been returned to the PCI master and the PCI master terminated the transfer.<br>• All remaining read completion data will be cached after data has been returned to the PCI master and the bridge has terminated the transfer with RETRY.<br>11 = Reserved. |
| 5:4 | RSVD | R | Reserved. Returns 00b when read. |


Copyright © 2021 Texas Instruments Incorporated

**Table 8-82. Pre-Fetch Agent Request Limits Register Description (continued)**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 3:0 | PFA_REQ_LENGTH_LIMIT | RW | Request Length Limit. Determines the number of bytes in the thread that the pre-fetch agent will read for that thread.<br>0000 = 64 bytes<br>0001 = 128 bytes<br>0010 = 256 bytes<br>0011 = 512 bytes<br>0100 = 1 Kbytes<br>0101 = 2 Kbytes<br>0110 = 4 Kbytes<br>0111 = 8 Kbytes<br>1000:1111 = Reserved |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

### 8.6.13 Cache Timer Transfer Limit Register

This register is used to set the number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded. This register is an alias for the pre-fetch agent request limits register in the classic PCI configuration space (offset EAh, see *Section 8.4.77*). See Table 8-83 for a complete description of the register contents.

Device control memory window register offset: 52h
Register type: Read/Clear
Default value: 0008h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

**Table 8-83. Cache Timer Transfer Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:8 | RSVD | R | Reserved. Returns 00h when read. |
| 7:0(1) | CACHE_TMR_XFR_LIMIT | RW | Number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

### 8.6.14 Cache Timer Lower Limit Register

Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the "cache miss limit" check can be triggered. See Table 8-84 for a complete description of the register contents.

Device control memory window register offset: 54h
Register type: Read/Clear
Default value: 007Fh

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 8-84. Cache Timer Lower Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:12 | RSVD | R | Reserved. Returns 0h when read. |
| 11:0(1) | CACHE_TIMER_LOWER_LIMIT | RW | Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the "cache miss limit" check can be triggered. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.


Copyright © 2021 Texas Instruments Incorporated

### 8.6.15 Cache Timer Upper Limit Register

Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer. See Table 8-85 for a complete description of the register contents.

Device control memory window register offset: 56h
Register type: Read/Clear
Default value: 01C0h

| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESET STATE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 8-85. Cache Timer Upper Limit Register Description**

| BIT | FIELD NAME | ACCESS | DESCRIPTION |
|---|---|---|---|
| 15:12 | RSVD | R | Reserved. Returns 0h when read. |
| 11:0(1) | CACHE_TIMER _UPPER_LIMIT | RW | Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer. |

(1) These bits are reset by a PCI Express reset ( $\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Copyright © 2021 Texas Instruments Incorporated

# 9 Application, Implementation, and Layout

## 9.1 Application Information

shows a typical implementation of the XIO2001 PCI Express (PCIe) to PCI translation bridge. The device serves as a bridge between an upstream PCIe device and up to six downstream PCI bus devices. The XIO2001 operates only with the PCIe interface as the primary bus and the PCI bus interface as the secondary bus. The PCI bus interface is 32 bits wide and the XIO2001 can be set to provide a PCI clock that operates at 25 MHz, 33 MHz, 50 MHz, or 66 MHz.

## 9.2 Typical Application

### 9.2.1 In-Card Implementation

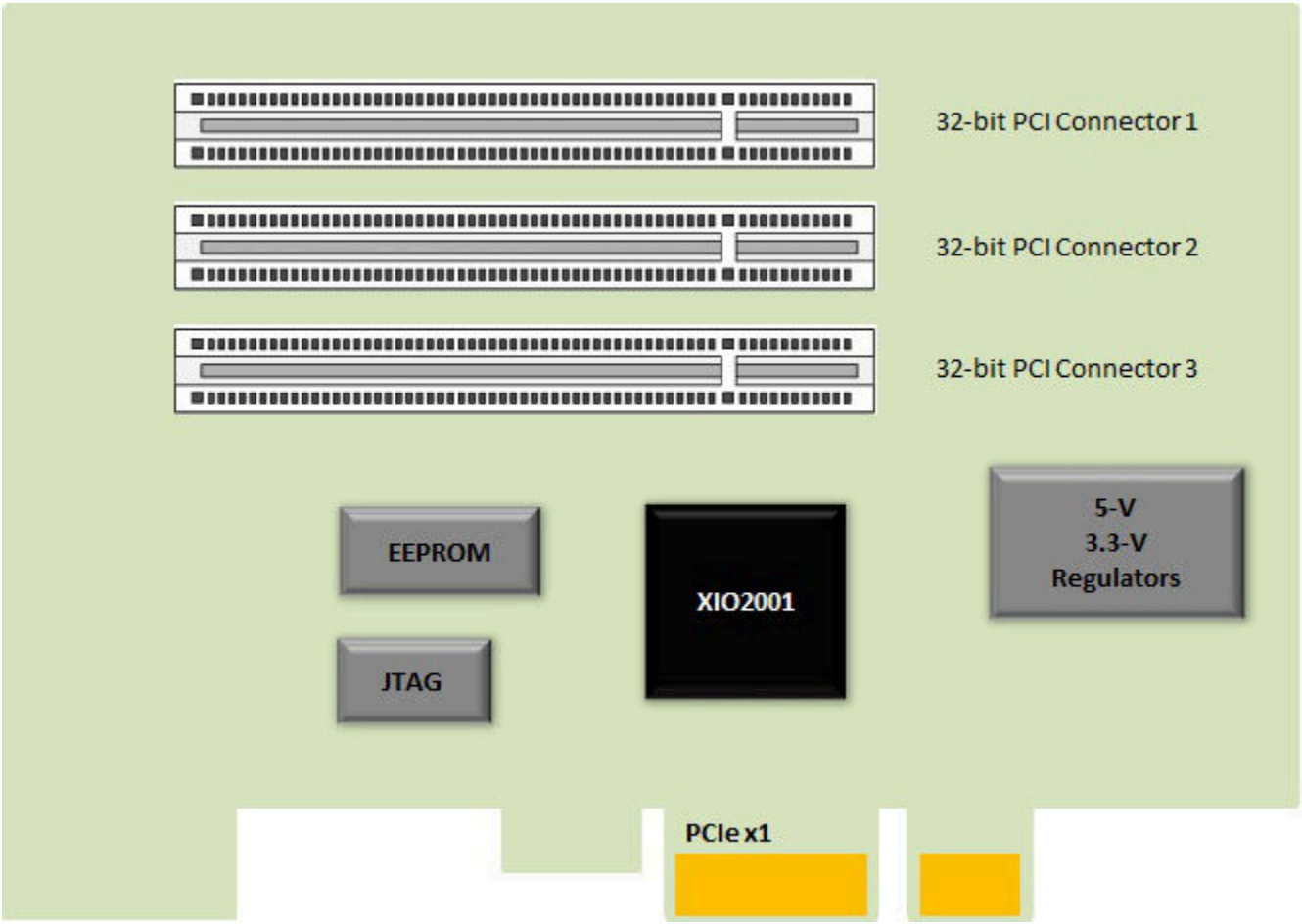



**Figure 9-1. Typical Application**

A common application for the XIO2001 is a PCIe-to-PCI bridge add-in card which implements a peripheral component interconnect (PCI) express to PCI bridge circuit using the Texas Instruments XIO2001 PCI Express to PCI Bus Translation Bridge. Designed as an ×1 add-in card, it is routed on FR4 as a 8-layer (4 signals, 2 power, and 2 ground) board with a 100-Ω differential impedance (50-Ω single-ended) using standard routing guidelines and requirements.

#### *9.2.1.1 Design Requirements*

##### 9.2.1.1.1 $V_{CCP}$ Clamping Rail

The XIO2001 has a PCI bus I/O clamp rail (PCIR) that can be either 3.3 V or 5 V, depending on the system implementation. For 25-MHz or 33-MHz PCI bus implementations, PCIR may be connected to either 3.3 V or 5.0 V. For 50-MHz or 66-MHz PCI bus implementations, a 3.3-V connection is the only approved configuration. The


Copyright © 2021 Texas Instruments Incorporated

power source for this clamp rail is a standard digital supply. The power source for this clamp rail is a standard digital supply. The PCIR terminals should be connected to the digital supply via an inline 1 k Ω resistor. A 0.1- μ F decoupling capacitor is also recommended at each PCIR terminal.

If PCIR is attached to a 5.0-V supply, the XIO2001 will only output 3.3-V amplitude signals on the PCI bus. The received PCI bus signal amplitudes may be either 3.3 V or 5.0 V. The PCI bus I/O cells are 5.0-V tolerant and the XIO2001 device is not damaged by 5.0-V input signal amplitudes.

#### 9.2.1.1.2 Combined Power Outputs

To support $V_{AUX}$ system requirements, the XIO2001 internally combines main power with $V_{AUX}$ power. There are three combined power rails in the XIO2001. These three power rails are distributed to the analog circuits, digital logic, and I/O cells that must operate during the $V_{AUX}$ state. Each of the three power rails has an output terminal for the external attachment of bypass capacitors to minimize circuit switching noise. These terminals are named $V_{DD_15_COMB}$, $V_{DD_33_COMB}$, and $V_{DD_33_COMBIO}$.

The recommended bypass capacitors for each combined output terminal are 1000 pF, 0.01 μF, and 1.0 μF. When placing these capacitors on the bottom side of the circuit board, the smallest capacitor is positioned next to the via associated with the combined output terminal and the largest capacitor is the most distant from the via. The circuit board trace width connecting the combined output terminal via to the capacitors must be at least 12 to 15 mils wide with the trace length as short as possible.

Other than the three recommended capacitors, no external components or devices may be attached to these combined output terminals.

#### 9.2.1.1.3 Auxiliary Power

If $V_{AUX}$ power is available in the system, the XIO2001 has the $V_{DD_33_AUX}$ pin to support this feature. Without fully understanding a system's $V_{AUX}$ power distribution design, recommending external components for the XIO2001 is difficult. At a minimum, a 0.1-μF bypass capacitor is placed near the XIO2001 and attached to the system's $V_{AUX}$ power supply. A robust design may include a Pi filter with bulk capacitors (5 μF to 100 μF) to minimize voltage fluctuations. When the system is cycling main power or is in the $V_{AUX}$ state, the $V_{DD_33_AUX}$ terminal requirements are that the input voltage cannot exceed 3.6 V or drop below 3.0 V for proper operation of the bridge.

If $V_{AUX}$ power is not present within the system, this terminal is connected to $V_{SS}$ through a resistor with a value greater than 3 k Ω.

#### 9.2.1.1.4 $V_{SS}$ and $V_{SSA}$ Pins

For proper operation of the XIO2001, a unified $V_{SS}$ and $V_{SSA}$ ground plane is recommended. The circuit board stack-up recommendation is to implement a layer two ground plane directly under the XIO2001 device. Both the circuit board vias and ground trace widths that connect the $V_{SS}$ and $V_{SSA}$ ball pads to this ground plane must be oversized to provide a low impedance connection.

#### 9.2.1.1.5 Capacitor Selection Recommendations

When selecting bypass capacitors for the XIO2001 device, X7R-type capacitors are recommended. The frequency versus impedance curves, quality, stability, and cost of these capacitors make them a logical choice for most computer systems.

The selection of bulk capacitors with low-ESR specifications is recommended to minimize low-frequency power supply noise. Today, the best low-ESR bulk capacitors are radial leaded aluminum electrolytic capacitors. These capacitors typically have ESR specifications that are less than 0.01 Ω at 100 kHz. Also, several manufacturers sell " D " size surface mount specialty polymer solid aluminum electrolytic capacitors with ESR specifications slightly higher than 0.01 Ω at 100 kHz. Both of these bulk capacitor options significantly reduce low-frequency power supply noise and ripple.

Copyright © 2021 Texas Instruments Incorporated

### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 PCI Bus Interface

The XIO2001 has a 32-bit PCI interface that can operate at 25 MHz, 33 MHz, 50 MHz or 66 MHz. This interface is compliant with the PCI Local Bus Specification , Revision 2.3 and 3.0. The remainder of this section describes implementation considerations for the XIO2001 secondary PCI bus interface.

- AD31:0, C/ $\overline{BE}$[3:0], PAR, $\overline{DEVSEL}$, $\overline{FRAME}$, $\overline{STOP}$, $\overline{TRDY}$, $\overline{PERR}$, $\overline{SERR}$, and $\overline{IRDY}$ are required signals and must be connected to each PCI bus device. The maximum signal loading specification for a 66 MHz bus is 30 pF and for a 33 MHz bus is 50 pF. PCI bus approved pullup resistors connected to $V_{CCP}$ are needed on the following terminals: $\overline{IRDY}$, $\overline{TRDY}$, $\overline{FRAME}$, $\overline{STOP}$, $\overline{PERR}$, $\overline{SERR}$, and $\overline{DEVSEL}$.
- The XIO2001 supports up to six external PCI bus devices with individual CLKOUT, $\overline{REQ}$, and $\overline{GNT}$ signals. An internal PCI bus clock generator function provides six low-skew clock outputs. Plus, there are six $\overline{REQ}$ inputs and six $\overline{GNT}$ outputs from the internal PCI bus arbiter. Each PCI bus device connects to one CLKOUT signal, one $\overline{REQ}$ signal, and one $\overline{GNT}$ signal. All three signals are point-to- point connections. Unused CLKOUT signals can be disabled by asserting the appropriate CLOCK_DISABLE bit in the clock control register at offset D8h. Unused $\overline{REQ}$ signals can be disabled using a weak pullup resistor to $V_{CCP}$. Unused $\overline{GNT}$ signals are no connects.
- An external clock feedback feature is provided to de-skew PCI bus clocks. Connecting the CLKOUT[6] terminal to the CLK terminal is required if any of the other six CLKOUT[5:0] terminals are used to clock PCI bus devices. The CLKOUT signals should be slightly longer than the longest synchronous PCI bus signal trace. Figure 9-2 illustrates the external PCI bus clock feedback feature. The use of series resistors on the seven PCI bus clocks should be considered to reduce circuit board EMI.

**Note**

There is one exception to this length matching rule associated with connecting a CLKOUT signal to PCI socket. For this case, the CLKOUT signal connected to a PCI socket should be 2.5 inches shorter than the other CLKOUT signals.

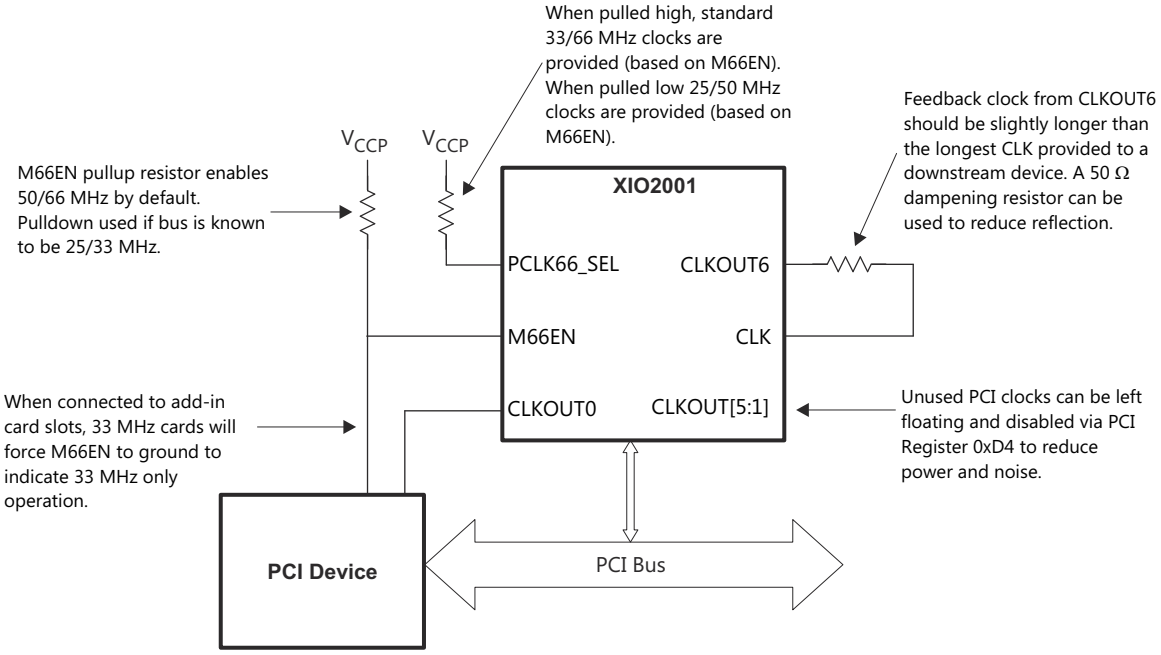



**Figure 9-2. External PCI Bus Clock Configuration**

- The XIO2001 has options providing for four different PCI clock frequencies: 25 MHz, 33 MHz, 50 MHz, and 66MHz. The clock frequency provided is determined by the states of the M66EN and PCLK66_SEL terminals at the de-assertion of $\overline{PERST}$.


Copyright © 2021 Texas Instruments Incorporated

- The PCLK66_SEL terminal determines if the XIO2001 provides either the standard 33/66 MHz frequencies or 25/50 MHz frequencies. If this terminal is pulled high at the de-assertion of $\overline{\text{PERST}}$, then CLKOUTx terminals provide the standard PCI 33/66 MHz frequencies (depending on the state of M66EN). If the terminal is pulled low at the de-assertion of $\overline{\text{PERST}}$, then a 25/50 MHz frequency is provided instead. The determination of what frequency to use is design-specific, and this terminal must be pulled high or low appropriately.
- The M66EN terminal determines if the PCI Bus will operate at low speed (50/25 MHz) or high speed (66/33 MHz). At the de-assertion of $\overline{\text{PERST}}$, the M66EN terminal is checked and if it is pulled to $V_{CCP}$, then the high-speed (66 MHz or 50 MHz) frequencies are used. If the pin is low, then the low-speed (33 MHz or 25 MHz) frequencies are used. If the speed of all devices attached to the PCI bus is known, then this terminal can be pulled appropriately to set the speed of the PCI bus. If add-in card slots are present on a high-speed bus that may have low speed devices attached, then the terminal can be pulled high and connected to the slot, permitting the add-in card to pull the terminal low and reduce the bus speed if a low-speed card is inserted.
- IDSEL for each PCI bus device must be resistively coupled (100 Ω) to one of the address lines between AD31 and AD16. Please refer to the XIO2001 Data Manual for the configuration register transaction device number to AD bit translation chart.
- PCI interrupts can be routed to the $\overline{\text{INT[D:A]}}$ inputs on the XIO2001. These four inputs are asynchronous to the PCI bus clock and will detect state changes even if the PCI bus clock is stopped. For each $\overline{\text{INT[D:A]}}$ input, an approved PCI bus pullup resistor to $V_{CCP}$ is required to keep each interrupt signal from floating. Interrupts on the XIO2001 that are not connected to any device may be tied together and pulled-up through a single resistor.
- $\overline{\text{PRST}}$ is a required PCI bus signal and must be connected to all devices. This output signal is asynchronous to the PCI bus clock. Since the output driver is always enabled and either driving high or low, no pullup resistor is needed.
- $\overline{\text{LOCK}}$ is an optional PCI bus signal. If $\overline{\text{LOCK}}$ is present in a system, it is connected to each PCI bus device that supports the feature and must meet PCI bus loading requirements for the selected clock frequency. An approved PCI bus pullup resistor to $V_{CCP}$ is required to keep this signal from floating, even if it is not connected to devices on the bus. $\overline{\text{LOCK}}$ is a bused signal and synchronous to the PCI bus clock. All synchronous PCI bus signals must be length matched to meet clock setup and hold requirements.
- SERIRQ is an optional PCI bus signal. When $\overline{\text{PERST}}$ is de-asserted, if a pullup resistor to $V_{CCP}$ is detected on terminal M08, the serial IRQ interface is enabled. A pulldown resistor to V SS disables this feature. If SERIRQ is present in a system, it is connected to each PCI bus device that supports the feature and must meet PCI bus loading requirements for the selected clock frequency. An approved PCI bus pullup resistor to $V_{CCP}$ is required to keep this signal from floating. SERIRQ is a bused signal and synchronous to the PCI bus clock. All synchronous PCI bus signals must be length matched to meet clock setup and hold requirements.

**Note**

SERIRQ does not support serialized PCI interrupts and is used for serializing the 16 ISA interrupts.

- CLKRUN is an optional PCI bus signal that is shared with the GPIO0 pin. When $\overline{\text{PERST}}$ is de-asserted and if a pullup resistor to $V_{DD_33}$ is detected on pin C11 (CLKRUN_EN), the clock run feature is enabled. If CLKRUN is required in a system, this pin is connected to each PCI bus device and must meet PCI bus loading requirements for the selected clock frequency. An approved PCI bus pullup resistor to $V_{DD_33}$ is required per the PCI Mobile Design Guide . CLKRUN is a bused signal and synchronous to the PCI bus clock. All synchronous PCI bus signals must be length matched to meet clock setup and hold requirements.

**Note**

If CLKRUN is used in a system, it must be supported by all devices attached to the PCI bus; if a device that does not support CLKRUN is attached to a bus where it is enabled, there is a danger that it will not be able to have a clock when it requires one.

- PWR_OVRD is an optional PCI bus signal that is shared with the GPIO1 terminal. In PWR_OVRD mode, this pin is always an output and is asynchronous to the PCI bus clock. When the power override control bits in the general control register at offset D4h are set to 001b or 011b, the M09 pin operates as the PWR_OVRD signal. Prior to setting the power override control bits, the GPIO1 // PWR_OVRD pin defaults to a standard GPIO pin.

Copyright © 2021 Texas Instruments Incorporated

- $\overline{PME}$ is an optional PCI bus input terminal to detect power management events from downstream devices. The $\overline{PME}$ terminal is operational during both main power states and $V_{AUX}$ states. The $\overline{PME}$ receiver has hysteresis and expects an asynchronous input signal. The board design requirements associated with this $\overline{PME}$ terminal are the same whether or not the terminal is connected to a downstream device. If the system includes a $V_{AUX}$ supply, the $\overline{PME}$ terminal requires a weak pullup resistor connected to $V_{AUX}$ to keep the terminal from floating. If no $V_{AUX}$ supply is present, the pullup resistor is connected to $V_{DD_33}$.
- The bridge supports external PCI bus clock sources. If an external clock is a system requirement, the external clock source is connected to the CLK terminal. The trace length relationship between the synchronous bus signals and the external clock signals that is previously described is still required to meet PCI bus setup and hold. For external clock mode, all seven CLKOUT[6:0] terminals can be disabled using the clock control register at offset D8h. Plus, the XIO2001 clock run feature must be disabled with external PCI bus clocks because there is no method of turning off external clocks.

**Note**

If an external clock with a frequency higher than 33 MHz is used, the M66EN terminal must be pulled up for the XIO2001 to function correctly.

- The XIO2001 supports an external PCI bus arbiter. When $\overline{PERST}$ is deasserted, the logic state of the EXT_ARB_EN pin is checked. If an external arbiter is required, EXT_ARB_EN is connected to $V_{DD_33}$. When connecting the XIO2001 to an external arbiter, the external arbiter's REQ signal is connected to the XIO2001 0 $\overline{GNT}$ output terminal. Likewise, the $\overline{GNT}$ signal from the external arbiter is connected to the XIO2001 0 $\overline{REQ}$ input pin. Unused $\overline{REQ}$ signals on the XIO2001 should be tied together and connected to $V_{CCP}$ through a pull-up resistor. When in external arbiter mode, all internal XIO2001 port arbitration features are disabled. Figure 9-3 illustrates the connectivity of an external arbiter.

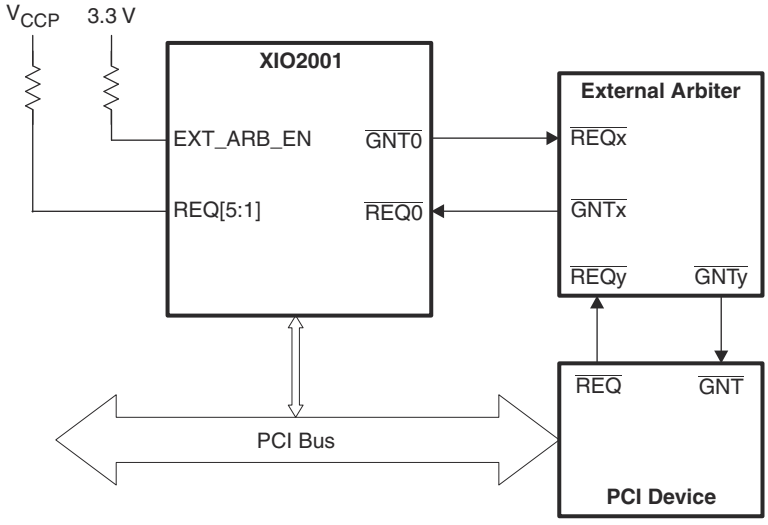



**Figure 9-3. External Arbiter Connections**

#### *9.2.1.2.1.1 Bus Parking*

Because of the shared bus nature of PCI, it is required that if the bus is idle at a given time that some device on the bus must drive some signals to stable states. These signals are the address/data lines, the command/byte enables, and a valid parity. If no devices are requesting use of the bus, it is the responsibility of the arbiter to assign ownership of the bus so that the bus signals are never floating while in idle states.

If the XIO2001 internal arbiter is enabled then there are two modes supported for bus parking. The default mode for bus parking is for the arbiter to continue to assert $\overline{GNT}$ for the last bus master. In this mode once a device has completed its transaction, the arbiter will continue to assert the $\overline{GNT}$ for that bus master and that device is required to drive a stable pattern onto the required signals. This will continue until another device requests use of the bus resulting in the arbiter removing $\overline{GNT}$ from the current bus owner grants it to the new requestor.


Copyright © 2021 Texas Instruments Incorporated

Alternatively, the XIO2001 can be configured to self-park. In this mode if no other devices have their $\overline{REQ}$ asserted, the XIO2001 will remove $\overline{GNT}$ from the current bus owner and drive a stable pattern onto the required lines.

It is suggested that implementations use the default mode of bus parking. The PCI Specification recommends leaving the current $\overline{GNT}$ signal asserted if no devices are asserting $\overline{REQ}$. Some $\overline{PCI}$ bus masters will release their $\overline{REQ}$ signals after having begun a transaction, even if that transaction may require the use of the bus for an extended time. If the XIO2001 self-parks the bus, then these bus masters will have their transaction lengths limited to the latency timer setting. This may result in increased arbitration, higher overhead for transactions, and decreased bus performance.

#### *9.2.1.2.1.2 I/O Characteristics*

Figure 9-4 shows a 3-state bi-directional buffer that represents the I/O cell design for the PCI bus. *Section 6.9*, *Electrical Characteristics over Recommended Operating Conditions*, provides the electrical characteristics of the PCI bus I/O cell.

**Note**

The PCI bus interface on the bridge meets the ac specifications of the *PCI Local Bus Specification*. Additionally, PCI bus terminals (input or I/O) must be held high or low to prevent them from floating.

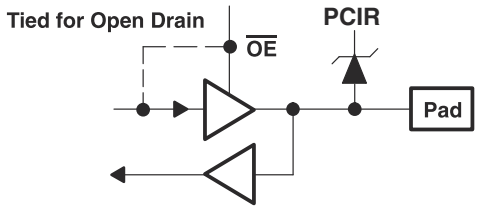



**Figure 9-4. 3-State Bidirectional Buffer**

#### *9.2.1.2.1.3 Clamping Voltage*

In the bridge, the PCI bus I/O drivers are powered from the $V_{DD_33}$ power rail. Plus, the I/O driver cell is tolerant to input signals with 5-V peak-to-peak amplitudes.

For PCI bus interfaces operating at 50 MHz or 66 MHz, all devices are required to output only 3.3-V peak-to-peak signal amplitudes. For PCI bus interfaces operating at 25-MHz or 33-MHz, devices may output either 3.3-V or 5-V peak-to-peak signal amplitudes. The bridge accommodates both signal amplitudes.

Each PCI bus I/O driver cell has a clamping diode connected to the internal $V_{CCP}$ voltage rail that protects the cell from excessive input voltage. The internal $V_{CCP}$ rail is connected to two PCIR terminals. If the PCI signaling is 3.3-V, then PCIR terminals are connected to a 3.3-V power supply via a 1-kΩ resistor. If the PCI signaling is 5-V, then the PCIR terminals are connected to a 5-V power supply via a 1kΩ resistor.

The PCI bus signals attached to the $V_{CCP}$ clamping voltage are identified as follows

- *Pin Functions* table, PCI System Terminals, all terminal names except for $\overline{PME}$
- *Pin Functions* table, Miscellaneous Terminals, the terminal name SERIRQ.

#### *9.2.1.2.1.4 PCI Bus Clock Run*

The bridge supports the clock run protocol as specified in the PCI Mobile Design Guide. When the clock run protocol is enabled, the bridge assumes the role of the central resource master.

To enable the clock run function, terminal CLKRUN_EN is asserted high. Then, terminal GPIO0 is enabled as the $\overline{CLKRUN}$ signal. An external pullup resistor must be provided to prevent the $\overline{CLKRUN}$ signal from floating To verify the operational status of the PCI bus clocks, bit 0 (SEC_CLK_STATUS) in the clock run status register at offset DAh (see *Section 8.4.69*) is read.

Since the bridge has several unique features associated with the PCI bus interface, the system designer must consider the following interdependencies between these features and the $\overline{CLKRUN}$ feature:

Copyright © 2021 Texas Instruments Incorporated

1. If the system designer chooses to generate the PCI bus clock externally, then the $\overline{\text{CLKRUN}}$ mode of the bridge must be disabled. The central resource function within the bridge only operates as a $\overline{\text{CLKRUN}}$ master and does not support the $\overline{\text{CLKRUN}}$ slave mode.
2. If the central resource function has stopped the PCI bus clocks, then the bridge still detects $\overline{\text{INTx}}$ state changes and will generate and send PCI Express messages upstream.
3. If the serial IRQ interface is enabled and the central resource function has stopped the PCI bus clocks, then any PCI bus device that needs to report an IRQ interrupt asserts $\overline{\text{CLKRUN}}$ to start the bus clocks.
4. When a PCI bus device asserts $\overline{\text{CLKRUN}}$, the central resource function turns on PCI bus clocks for a minimum of 512 cycles.
5. If the serial IRQ function detects an IRQ interrupt, then the central resource function keeps the PCI bus clocks running until the IRQ interrupt is cleared by software.
6. If the central resource function has stopped the PCI bus clocks and the bridge receives a downstream transaction that is forwarded to the PCI bus interface, then the bridge asserts $\overline{\text{CLKRUN}}$ to start the bus clocks.
7. The central resource function is reset by PCI bus reset ( $\overline{\text{PRST}}$) assuring that clocks are present during PCI bus resets.

#### *9.2.1.2.1.5 PCI Bus External Arbiter*

The bridge supports an external arbiter for the PCI bus. Terminal (EXT_ARB_EN), when asserted high, enables the use of an external arbiter.

When an external arbiter is enabled, $\overline{\text{GNT0}}$ is connected to the external arbiter as the REQ for the bridge. Likewise, $\overline{\text{REQ0}}$ is connected to the external arbiter as the $\overline{\text{GNT}}$ for the bridge.

#### *9.2.1.2.1.6 MSI Messages Generated from the Serial IRQ Interface*

When properly configured, the bridge converts PCI bus serial IRQ interrupts into PCI Express message signaled interrupts (MSI). classic PCI configuration register space is provided to enable this feature. The following list identifies the involved configuration registers:

1. Command register at offset 04h, bit 2 (MASTER_ENB) is asserted (see Table 8-12).
2. MSI message control register at offset 52h, bits 0 (MSI_EN) and 6:4 (MM_EN) enable single and multiple MSI messages, respectively (see *Section 8.4.43*).
3. MSI message address register at offsets 54h and 58h specifies the message memory address. A nonzero address value in offset 58h initiates 64-bit addressing (see *Section 8.4.38* and *Section 8.4.45*).
4. MSI message data register at offset 5Ch specifies the system interrupt message (see *Section 8.4.46*).
5. Serial IRQ mode control register at offset E0h specifies the serial IRQ bus format (see *Section 8.4.73*).
6. Serial IRQ edge control register at offset E2h selects either level or edge mode interrupts (see *Section 8.4.74*).
7. Serial IRQ status register at offset E4h reports level mode interrupt status (see Section 8.4.75).

A PCI Express MSI is generated based on the settings in the serial IRQ edge control register. If the system is configured for edge mode, then an MSI message is sent when the corresponding serial IRQ interface sample phase transitions from low to high. If the system is configured for level mode, then an MSI message is sent when the corresponding IRQ status bit in the serial IRQ status register changes from low to high.

The bridge has a dedicated SERIRQ terminal for all PCI bus devices that support serialized interrupts. This SERIRQ interface is synchronous to the PCI bus clock input (CLK) frequency. The bridge always generates a 17-phase serial IRQ stream. Internally, the bridge detects only 16 IRQ interrupts, IRQ0 frame through IRQ15 frame. The IOCHCK frame is not monitored by the serial IRQ state machine and never generates an IRQ interrupt or MSI message.

The multiple message enable (MM_EN) field determines the number of unique MSI messages that are sent upstream on the PCI Express link. From 1 message to 16 messages, in powers of 2, are selectable. If fewer than 16 messages are selected, then the mapping from IRQ interrupts to MSI messages is aliased. *Table 9-1* illustrates the IRQ interrupt to MSI message mapping based on the number of enabling messages.


Copyright © 2021 Texas Instruments Incorporated

**Table 9-1. IRQ Interrupt to MSI Message Mapping**

| IRQ INTERRUPT | 1 MESSAGE ENABLED | 2 MESSAGES ENABLED | 4 MESSAGES ENABLED | 8 MESSAGES ENABLED | 16 MESSAGES ENABLED |
|---|---|---|---|---|---|
| IRQ0 | MSI MSG #0 | MSI MSG #0 | MSI MSG #0 | MSI MSG #0 | MSI MSG #0 |
| IRQ1 | MSI MSG #0 | MSI MSG #1 | MSI MSG #1 | MSI MSG #1 | MSI MSG #1 |
| IRQ2 | MSI MSG #0 | MSI MSG #0 | MSI MSG #2 | MSI MSG #2 | MSI MSG #2 |
| IRQ3 | MSI MSG #0 | MSI MSG #1 | MSI MSG #3 | MSI MSG #3 | MSI MSG #3 |
| IRQ4 | MSI MSG #0 | MSI MSG #0 | MSI MSG #0 | MSI MSG #4 | MSI MSG #4 |
| IRQ5 | MSI MSG #0 | MSI MSG #1 | MSI MSG #1 | MSI MSG #5 | MSI MSG #5 |
| IRQ6 | MSI MSG #0 | MSI MSG #0 | MSI MSG #2 | MSI MSG #6 | MSI MSG #6 |
| IRQ7 | MSI MSG #0 | MSI MSG #1 | MSI MSG #3 | MSI MSG #7 | MSI MSG #7 |
| IRQ8 | MSI MSG #0 | MSI MSG #0 | MSI MSG #0 | MSI MSG #0 | MSI MSG #8 |
| IRQ9 | MSI MSG #0 | MSI MSG #1 | MSI MSG #1 | MSI MSG #1 | MSI MSG #9 |
| IRQ10 | MSI MSG #0 | MSI MSG #0 | MSI MSG #2 | MSI MSG #2 | MSI MSG #10 |
| IRQ11 | MSI MSG #0 | MSI MSG #1 | MSI MSG #3 | MSI MSG #3 | MSI MSG #11 |
| IRQ12 | MSI MSG #0 | MSI MSG #0 | MSI MSG #0 | MSI MSG #4 | MSI MSG #12 |
| IRQ13 | MSI MSG #0 | MSI MSG #1 | MSI MSG #1 | MSI MSG #5 | MSI MSG #13 |
| IRQ14 | MSI MSG #0 | MSI MSG #0 | MSI MSG #2 | MSI MSG #6 | MSI MSG #14 |
| IRQ15 | MSI MSG #0 | MSI MSG #1 | MSI MSG #3 | MSI MSG #7 | MSI MSG #15 |

The MSI message format is compatible with the PCI Express request header format for 32-bit and 64-bit memory write transactions. The system message and message number fields are included in bytes 0 and 1 of the data payload.

#### *9.2.1.2.1.7 PCI Bus Clocks*

The bridge has seven PCI bus clock outputs and one PCI bus clock input. Up to six PCI bus devices are supported by the bridge.

Terminal PCLK66_SEL selects the default operating frequency. This signal works in conjunction with terminal M66EN to determine the final output frequency. When PCLK66_SEL is asserted high then the clock frequency will be either 66-MHz or 33-MHz depending on the state of M66EN. When M66EN is asserted high then the clock frequency will be 66-MHz, when M66EN is de-asserted the clock frequency will be 33-MHz. When PCLK66_SEL is de-asserted then the clock frequency will be either 50-MHz or 25-MHz. When M66EN is asserted high then the clock frequency will be 50-MHz, when M66EN is de-asserted the clock frequency will be 25-MHz. The clock control register at offset D8h provides 7 control bits to individually enable or disable each PCI bus clock output (see *Section 8.4.67*). The register default is enabled for all 7 outputs.

The PCI bus clock (CLK) input provides the clock to the internal PCI bus core and serial IRQ core. When the internal PCI bus clock source is selected, PCI bus clock output 6 (CLKOUT6) is connected to the PCI bus clock input (CLK). When an external PCI bus clock source is selected, the external clock source is connected to the PCI bus clock input (CLK). For external clock mode, all seven CLKOUT6:0 terminals must be disabled using the clock control register at offset D8h (see *Section 8.4.67*).

Copyright © 2021 Texas Instruments Incorporated

### 9.2.2 External EEPROM

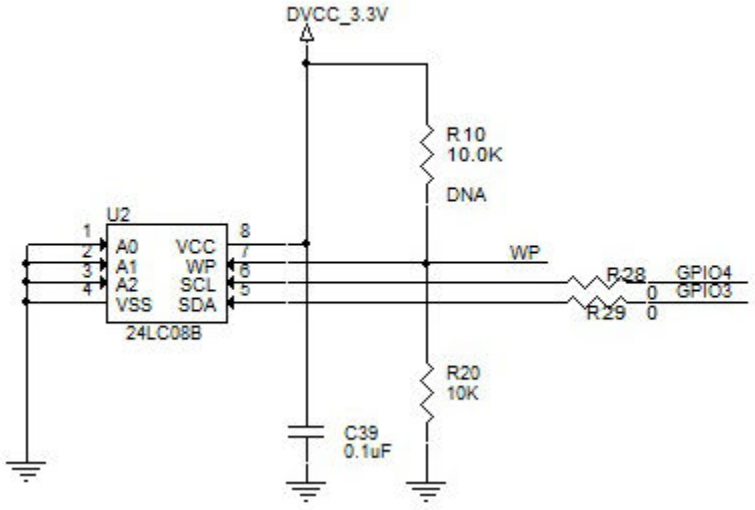



**Figure 9-5. External EEPROM**

#### *9.2.2.1 Design Requirements*

See previous *Section 9.2.1.1*.

#### *9.2.2.2 Detailed Design Procedure*

See previous *Section 9.2.1.2*.

### 9.2.3 JTAG Interface

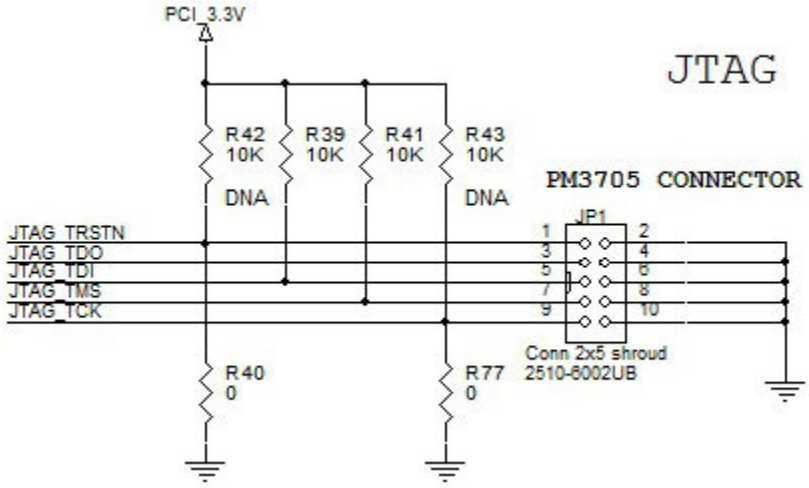



**Figure 9-6. JTAG Interface**

#### *9.2.3.1 Design Requirements*

See previous *Section 9.2.1.1*.

#### *9.2.3.2 Detailed Design Procedure*

See previous *Section 9.2.1.2*.


Copyright © 2021 Texas Instruments Incorporated

### 9.2.4 Combined Power

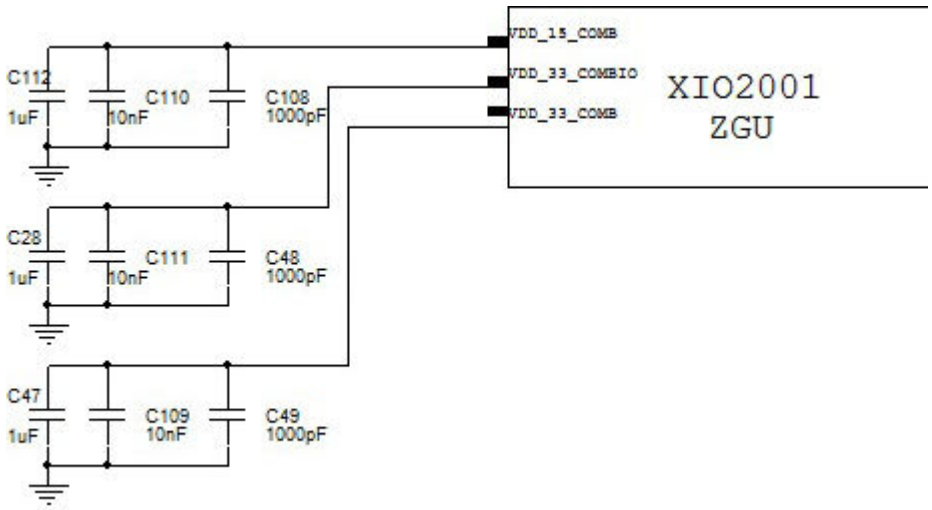



**Figure 9-7. Combined Power**

#### *9.2.4.1 Design Requirements*

See previous *Section 9.2.1.1*.

#### *9.2.4.2 Detailed Design Procedure*

See previous *Section 9.2.1.2*.

### 9.2.5 Power Filtering

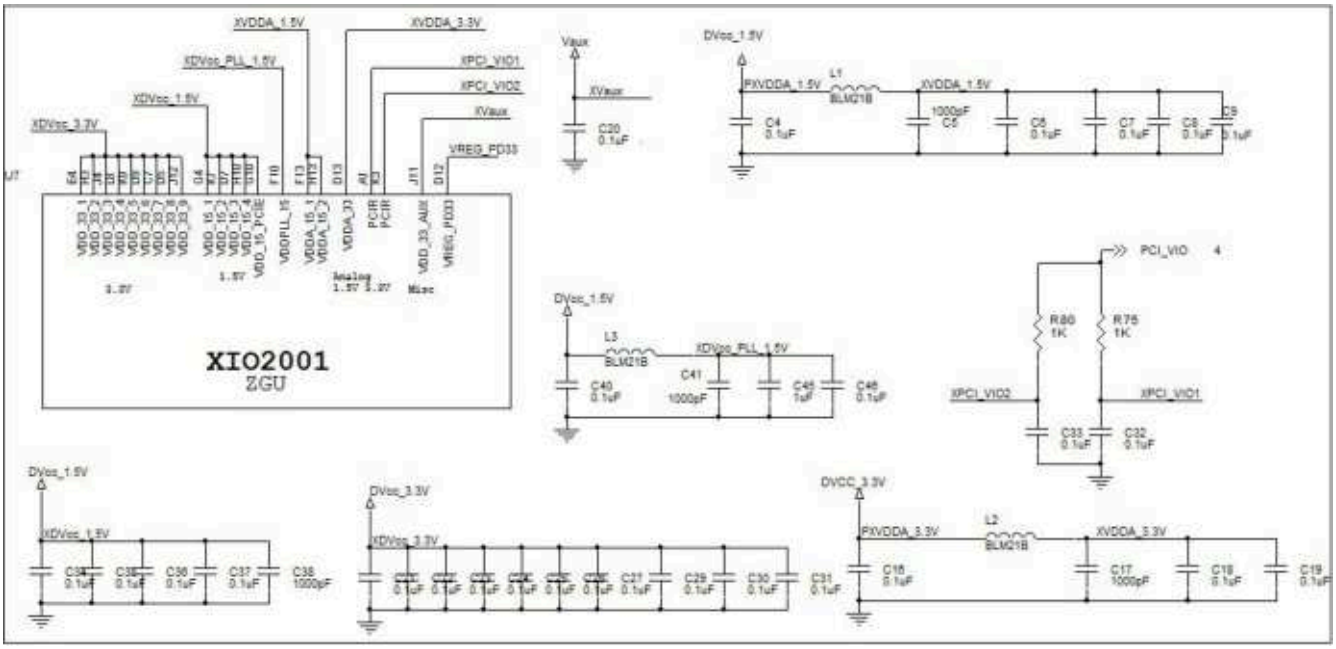



**Figure 9-8. Power Filtering**

#### *9.2.5.1 Design Requirements*

See previous *Section 9.2.1.1*.

#### *9.2.5.2 Detailed Design Procedure*

See previous *Section 9.2.1.2*.

## 9.3 Layout

### 9.3.1 Layout Guidelines

In motherboard designs there is an additional clock delay on the PCI add-in cards. In order to make the overall lengths of the PCI Clock Signals be the same, a rule has been made, which states that the length of the Clock Signal will be fixed to 2.5" on PCI add-in cards. The motherboard design requires that the length of the Clock Signal going to the PCI add-in slots will be less by 2.5" in comparison with the other Clock Signals that do not go to a PCI add-in slot. With the PCI add-in cards inserted, the Clock Signals lengths match. In a design where there is no add-in slot, the length of the PCI Clock Signals should match. A typical embedded system has all PCI devices on the board itself. In such case, the lengths of clock nets should match.

There is no matching requirement on the length of the Address/Data signals with respect to Clock Signal, though, there is a limitation on the maximum length of the Address/Data signal length depending upon the PCI Bus speed. The length matching of clock signals in PCI bus is not very critical. It is however, often, not too difficult to match it within 100 mils. The PCI Clock Signals should be slightly longer than the longest trace on the PCI bus. When 100 mil recommendations become impractical due to board space constraints, this can be relaxed up to a recommended maximum of 250 mils.

All 32 bit PCI slots must be placed so the slot can be put on the board as either a 3 V or a 5 V slot. All pins used as keying pins (A12, A13, A50, A51, B12,B13, B50, B51) should be put on the board and connected to the GND plane. Mounting holes must be placed on either side of the socket.

(CTXn + TXn) and (CTXp + TXp) are a 100 W differential impedance pair (50 W single ended) and must be length matched to within 5 mils. i.e. CTXp must be within 5 mils of CTXn, TXp must be within 5 mils of TXn, and (CTXp + TXp) must be within 5 mils of (CTXn + TXn). The coupling capacitors must be placed as close to the PCI Express Edge connector as possible.

RXp and RXn are a 100 W differential impedance pair (50 W single ended) and must be length matched to within 5 mils.


Copyright © 2021 Texas Instruments Incorporated

### 9.3.2 Layout Example

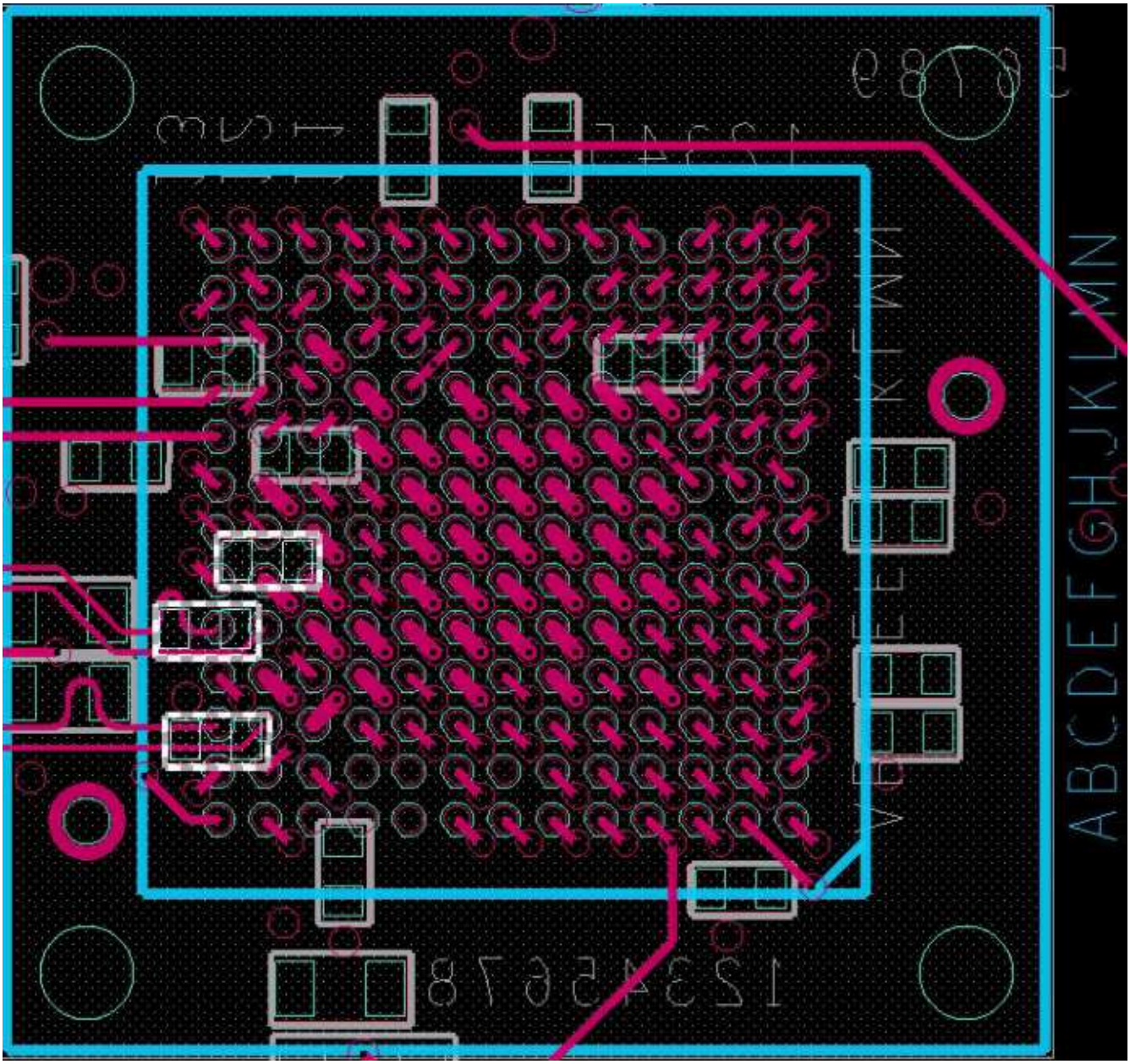



**Figure 9-9. BGA Via Routing Layout**

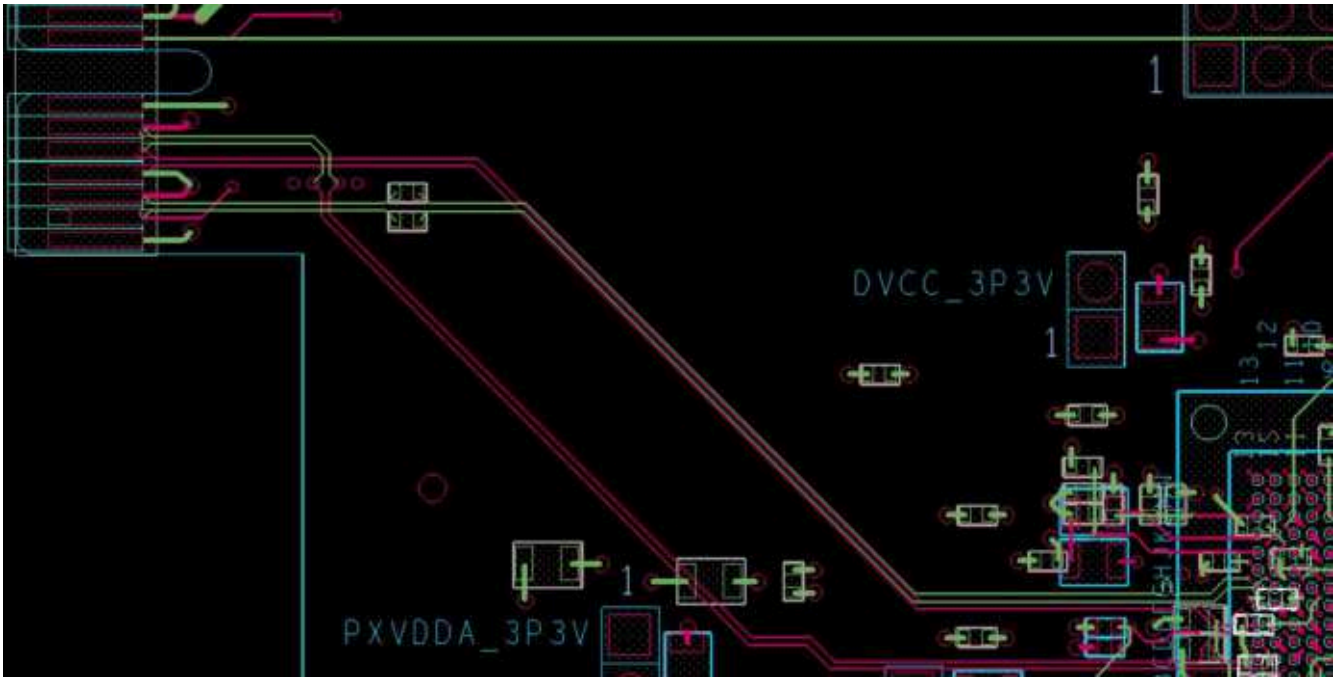



**Figure 9-10. PCIe Routing Layout**

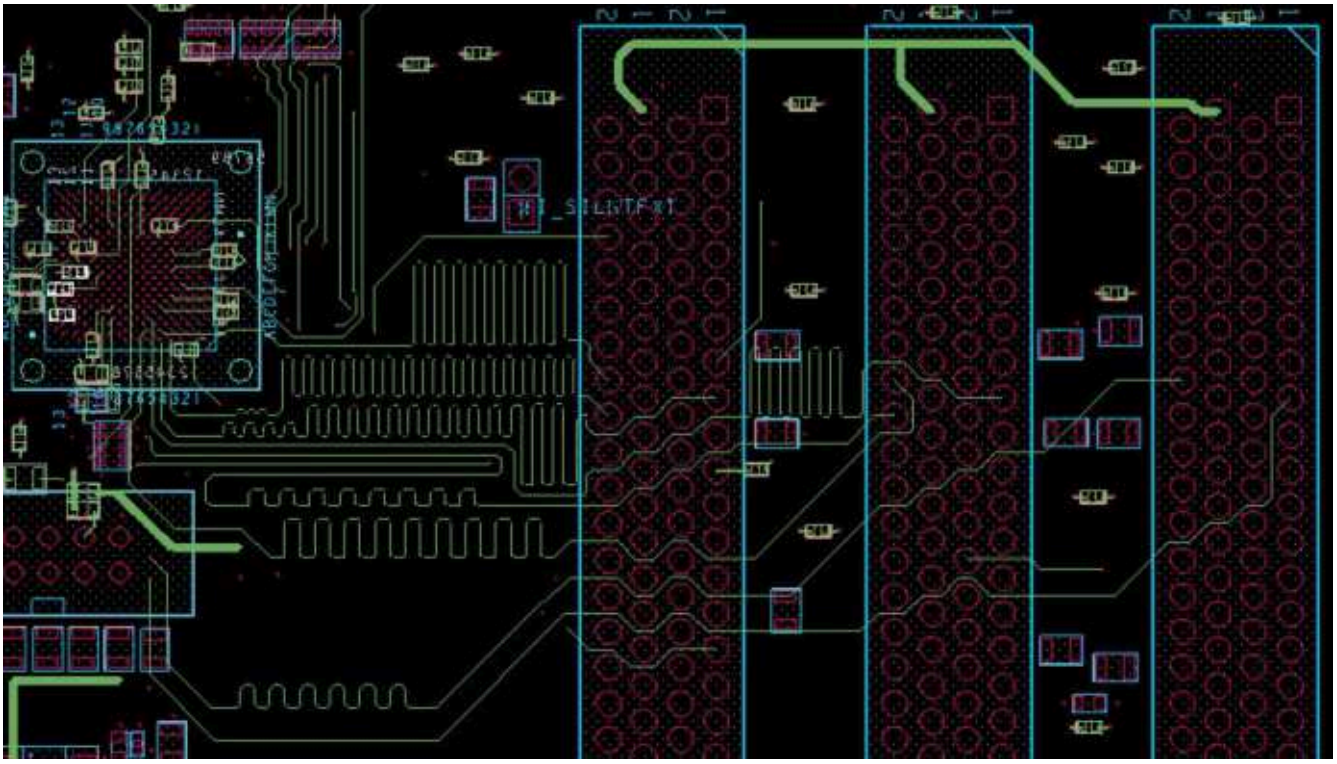


**Figure 9-11. PCI CLK Routing Layout**

## 9.4 Power Supply Recommendations

### 9.4.1 1.5-V and 3.3-V Digital Supplies

The XIO2001 requires both 1.5-V and 3.3-V digital power. The 1.5-V pins are named $V_{DD_15}$. These pins supply power to the digital core. The 1.5-V core allows for a significant reduction in both power consumption and logic


Copyright © 2021 Texas Instruments Incorporated

switching noise. The 3.3-V pins are named $V_{DD_33}$ and supply power to most of the input and output cells. Both the $V_{DD_15}$ and $V_{DD_33}$ supplies must have 0.1-µF bypass capacitors to VSS (ground) in order for proper operation. The recommendation is one capacitor for each power pin. When placing and connecting all bypass capacitors, high-speed board design rules must be followed.

### 9.4.2 1.5-V and 3.3-V Analog Supplies

Both 1.5-V and 3.3-V analog power is required by the XIO2001. Since circuit noise on the analog power terminals must be minimized, a Pi filter is recommended. All VDDA_15 pins must be connected together and share one Pi filter. All $V_{DDA_33}$ terminals must be connected together and share a second Pi filter.

Both the 1.5-V and 3.3-V analog supplies must have 0.1-µF bypass capacitors connected to $V_{SSA}$ (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. In addition, one 1000-pF capacitor per Pi filter is recommended. This 1000-pF capacitor is attached to the device side of the Pi filter and to $V_{SSA}$ (ground). High-speed board design rules must be followed when connecting bypass capacitors to $V_{DDA}$ and $V_{SSA}$.

### 9.4.3 1.5-V PLL Supply

The XIO2001 requires a 1.5-V power supply for the internal PLL (VDDPLL_15). Circuit noise on PLL power must be minimized. A Pi-filter with a 200-mA inductor and 220 Ω @ 100 MHz is recommended for this terminal. The PLL power must have a 0.1- µ F bypass capacitor connected to $V_{SS}$. In addition, a 1000- pF capacitor per Pi-filter is recommended, this 1000-pF capacitor is attached to the device side of the Pi- filter and to $V_{SSA}$ (analog-ground).

### 9.4.4 Power-Up/Down Sequencing

**Note**

The power sequencing recommendations in this section exclude the $V_{DD_33_AUX}$ terminal.

All XIO2001 analog and digital power pins must be controlled during the power-up and power-down sequence. Absolute maximum power pin ratings must not be exceeded to prevent damaging the device. All power pins must remain within 3.6 V to prevent damaging the XIO2001.

### 9.4.5 Power Supply Filtering Recommendations

To meet the PCI-Express jitter specifications, low-noise power supplies are required on several of the XIO2001 voltage terminals. The power terminals that require low-noise power include $V_{DDA_15}$ and $V_{DDA_33}$. This section provides guidelines for the filter design to create low-noise power sources.

The least expensive solution for low-noise power sources is to filter existing 3.3-V and 1.5-V power supplies. This solution requires analysis of the noise frequencies present on the power supplies. The XIO2001 has external interfaces operating at clock rates of 25 MHz, 33 MHz, 50 MHz, 66 MHz, 100 MHz, 125 MHz, and 2.5 GHz. Other devices located near the XIO2001 may produce switching noise at different frequencies. Also, the power supplies that generate the 3.3 V and 1.5 V power rails may add low frequency ripple noise. Linear regulators have feedback loops that typically operate in the 100 kHz range. Switching power supplies typically have operating frequencies in the 500 KHz range. When analyzing power supply noise frequencies, the first, third, and fifth harmonic of every clock source should be considered.

Critical analog circuits within the XIO2001 must be shielded from this power supply noise. The fundamental requirement for a filter design is to reduce power supply noise to a peak-to-peak amplitude of less than 25 mV. This maximum noise amplitude should apply to all frequencies from 0 Hz to 12.5 GHz.

The following information should be considered when designing a power supply filter:

- Ideally, the series resonance frequency for each filter component should be greater than the fifth harmonic of the maximum clock frequency. With a maximum clock frequency of 1.25 GHz, the third harmonic is 3.75 GHz and the fifth harmonic is 6.25 GHz. Finding inductors and capacitors with a series resonance frequency above 6.25 GHz is both difficult and expensive. Components with a series resonance frequency in the 4 to 6 GHz range are a good compromise.

Copyright © 2021 Texas Instruments Incorporated

- The inductor(s) associated with the filter must have a DC resistance low enough to pass the required current for the connected power terminals. The voltage drop across the inductor must be low enough to meet the minus 10% voltage margin requirement associated with each XIO2001 power terminal. Power supply output voltage variation must be considered as well as voltage drops associated with any connector pins and circuit board power distribution geometries.
- The Q versus frequency curve associated with the inductor must be appropriate to reduce power terminal noise to less than the maximum peak-to-peak amplitude requirement for the XIO2001. Recommending a specific inductor is difficult because every system design is different and therefore the noise frequencies and noise amplitudes are different. Many factors will influence the inductor selection for the filter design. Power supplies must have adequate input and output filtering. A sufficient number of bulk and bypass capacitors are required to minimize switching noise. Assuming that board level power is properly filtered and minimal low frequency noise is present, frequencies less than 10 MHz, an inductor with a Q greater than 20 from approximately 10 MHz to 3 GHz should be adequate for most system applications.
- The series component(s) in the filter may either be an inductor or a ferrite bead. Testing has been performed on both component types. When measuring PCI-Express link jitter, the inductor or ferrite bead solutions produce equal results. When measuring circuit board EMI, the ferrite bead is a superior solution.

**Note**

The XIO2001 reference schematics include ferrite beads in the analog power supply filters.

- When designing filters associated with power distribution, the power supply is a low impedance source and the device power terminals are a low impedance load. The best filter for this application is a T filter. See Figure 9-12 for a T-filter circuit. Some system may require this type of filter design if the power supplies or nearby components are exceptionally noisy. This type of filter design is recommended if a significant amount of low frequency noise, frequencies less than 10 MHz, is present in a system.
- For most applications a Pi filter will be adequate. See Figure 9-12 for a Pi-filter circuit. When implementing a Pi filter, the two capacitors and the inductor must be located next to each other on the circuit board and must be connected together with wide low impedance traces. Capacitor ground connections must be short and low impedance.
- If a significant amount of high frequency noise, frequencies greater than 300 MHz, is present in a system, creating an internal circuit board capacitor will help reduce this noise. This is accomplished by locating power and ground planes next to each other in the circuit board stackup. A gap of 0.003 mils between the power and ground planes will significantly reduce this high frequency noise.
- Another option for filtering high-frequency logic noise is to create an internal board capacitor using signal layer copper plates. When a component requires a low-noise power supply, usually the Pi filter is located near the component. Directly under the Pi filter, a plate capacitor may be created. In the circuit board stack-up, select a signal layer that is physically located next to a ground plane. Then, generate an internal 0.25 inch by 0.25 inch plate on that signal layer. Assuming a 0.006 mil gap between the signal layer plate and the internal ground plane, this will generate a 12 pF capacitor. By connecting this plate capacitor to the trace between the Pi filter and the component's power pins, an internal circuit board high frequency bypass capacitor is created. This solution is extremely effective for switching frequencies above 300 MHz.

Figure 9-12 illustrates two different filter designs that may be used with the XIO2001 to provide lownoise power to critical power pins.


Copyright © 2021 Texas Instruments Incorporated

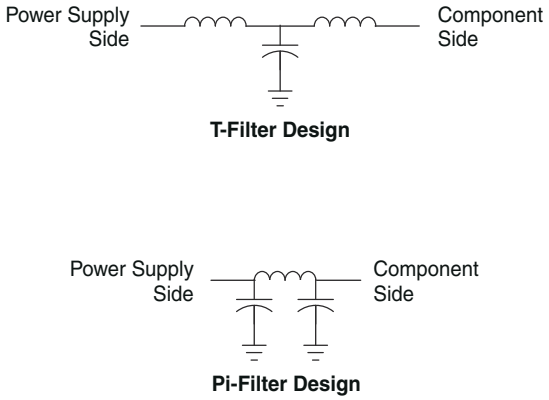



**Figure 9-12. Filter Designs**

# 10 Device and Documentation Support

## 10.1 Documents Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are listed below:

1. To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
2. To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
3. All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
4. If the signal or terminal name has a bar above the name (for example, $\overline{\text{GRST}}$), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
5. Differential signal names end with P, N, +, or – designators. The P or + designators signify the positive signal associated with the differential pair. The N or – designators signify the negative signal associated with the differential pair.
6. RSVD indicates that the referenced item is reserved.
7. In Sections 4 through 6, the configuration space for the bridge is defined. For each register bit, the software access method is identified in an access column. The legend for this access column includes the following entries:
   - r – read access by software
   - u – updates by the bridge internal hardware
   - w – write access by software
   - c – clear an asserted bit with a write-back of 1b by software. Write of zero to the field has no effect
   - s – the field may be set by a write of one. Write of zero to the field has no effect
   - na – not accessible or not applicable

### 10.1.1 XIO2001 Definition

| ACRONYM | DEFINTION |
|---|---|
| BIST | Built-in self test |
| ECRC | End-to-end cyclic redundancy code |
| EEPROM | Electrically erasable programmable read-only memory |
| GP | General purpose |
| GPIO | General-purpose input output |
| ID | Identification |
| IF | Interface |
| IO | Input output |
| $I^2C$ | Intelligent Interface Controller |
| LPM | Link power management |
| LSB | Least significant bit |
| MSB | Most significant bit |
| MSI | Message signaled interrupts |
| PCI | Peripheral component interface |
| PME | PCI power management event |
| RX | Receive |
| SCL | Serial-bus clock |
| SDA | Serial-bus data |
| TC | Traffic class |
| TLP | Transaction layer packet or protocol |
| TX | Transmit |


Copyright © 2021 Texas Instruments Incorporated

| | |
|---|---|
| VC | Virtual channel |

## 10.2 Documentation Support

### 10.2.1 Related Documents

- *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0
- *PCI Express Base Specification*, Revision 2.0
- *PCI Express Card Electromechanical Specification*, Revision 2.0
- *PCI Local Bus Specification*, Revision 2.3
- *PCI-to-PCI Bridge Architecture Specification*, Revision 1.2
- *PCI Bus Power Management Interface Specification*, Revision 1.2
- *PCI Mobile Design Guide*, Revision 1.1
- *Serialized IRQ Support for PCI Systems*, Revision 6.0

#### *10.2.1.1 Receiving Notification of Documentation Updates*

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.4 Trademarks

PCI Express™ is a trademark of PCI-SIG.
PowerPad™ and PowerPAD™ are trademarks of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

| | |
|---|---|
| **TI Glossary** | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2021 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| XIO2001IPNP | Active | Production | HTQFP (PNP) \| 128 | 90 \| TIW TRAY | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IPNP.A | Active | Production | HTQFP (PNP) \| 128 | 90 \| TIW TRAY | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IPNPG4 | Active | Production | HTQFP (PNP) \| 128 | 90 \| TIW TRAY | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IPNPG4.A | Active | Production | HTQFP (PNP) \| 128 | 90 \| TIW TRAY | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IZAJ | Active | Production | NFBGA (ZAJ) \| 144 | 260 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IZAJ.A | Active | Production | NFBGA (ZAJ) \| 144 | 260 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IZWS | Active | Production | NFBGA (ZWS) \| 169 | 160 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IZWS.A | Active | Production | NFBGA (ZWS) \| 169 | 160 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IZWSR | Active | Production | NFBGA (ZWS) \| 169 | 1000 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001IZWSR.A | Active | Production | NFBGA (ZWS) \| 169 | 1000 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | XIO2001I |
| XIO2001PNP | Active | Production | HTQFP (PNP) \| 128 | 90 \| TIW TRAY | Yes | NIPDAU | Level-3-260C-168 HR | 0 to 70 | XIO2001 |
| XIO2001PNP.A | Active | Production | HTQFP (PNP) \| 128 | 90 \| TIW TRAY | Yes | NIPDAU | Level-3-260C-168 HR | 0 to 70 | XIO2001 |
| XIO2001PNPG4 | Active | Production | HTQFP (PNP) \| 128 | 90 \| TIW TRAY | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | XIO2001 |
| XIO2001PNPG4.A | Active | Production | HTQFP (PNP) \| 128 | 90 \| TIW TRAY | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | XIO2001 |
| XIO2001ZAJ | Active | Production | NFBGA (ZAJ) \| 144 | 260 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | 0 to 70 | XIO2001 |
| XIO2001ZAJ.A | Active | Production | NFBGA (ZAJ) \| 144 | 260 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | 0 to 70 | XIO2001 |
| XIO2001ZWS | Active | Production | NFBGA (ZWS) \| 169 | 160 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | 0 to 70 | XIO2001 |
| XIO2001ZWS.A | Active | Production | NFBGA (ZWS) \| 169 | 160 \| JEDEC TRAY (5+1) | Yes | SNAGCU | Level-3-260C-168 HR | 0 to 70 | XIO2001 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

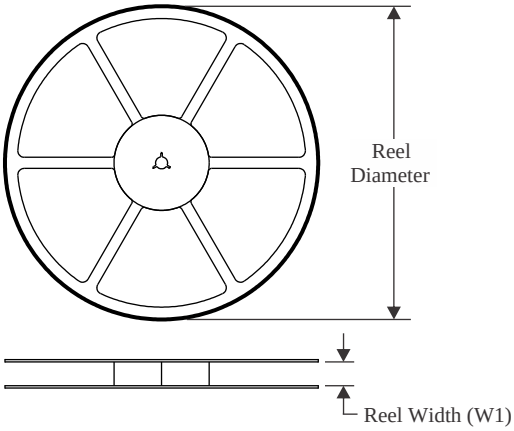
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

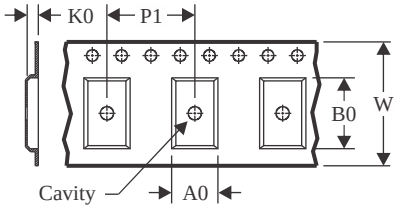
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

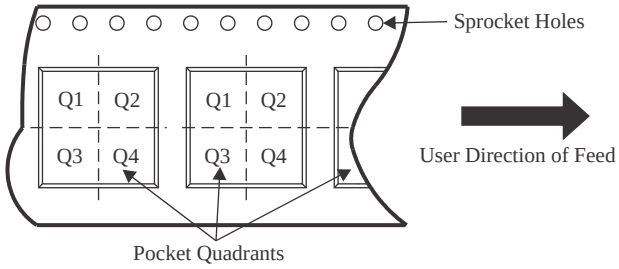



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

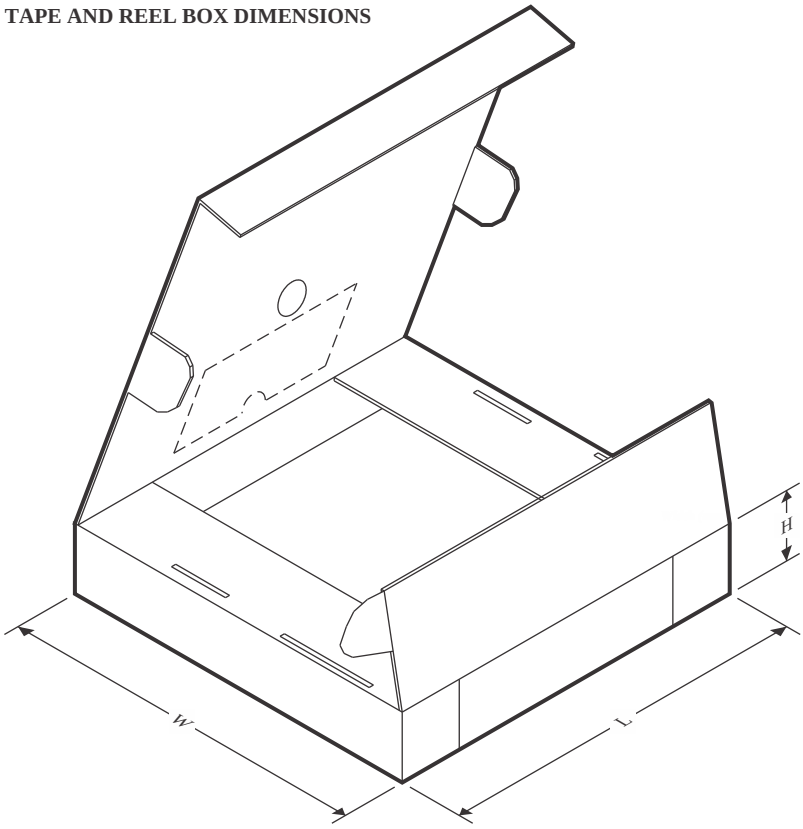
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| XIO2001IZWSR | NFBGA | ZWS | 169 | 1000 | 330.0 | 24.4 | 12.35 | 12.35 | 2.3 | 16.0 | 24.0 | Q1 |

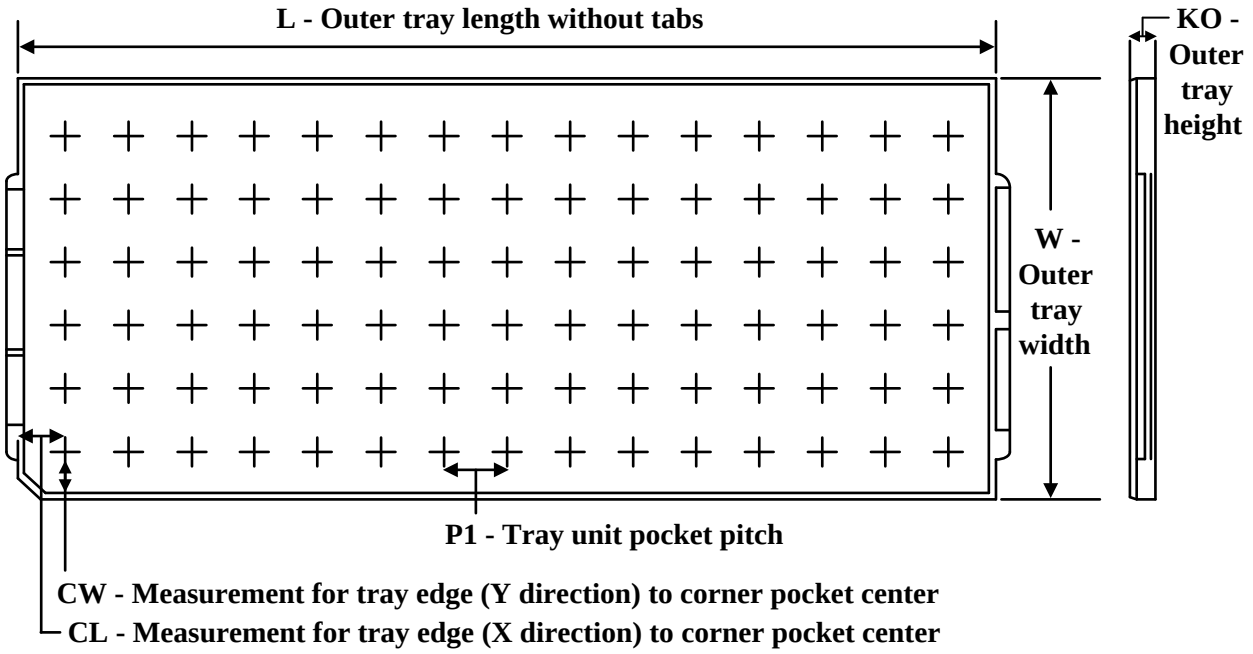
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| XIO2001IZWSR | NFBGA | ZWS | 169 | 1000 | 336.6 | 336.6 | 41.3 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

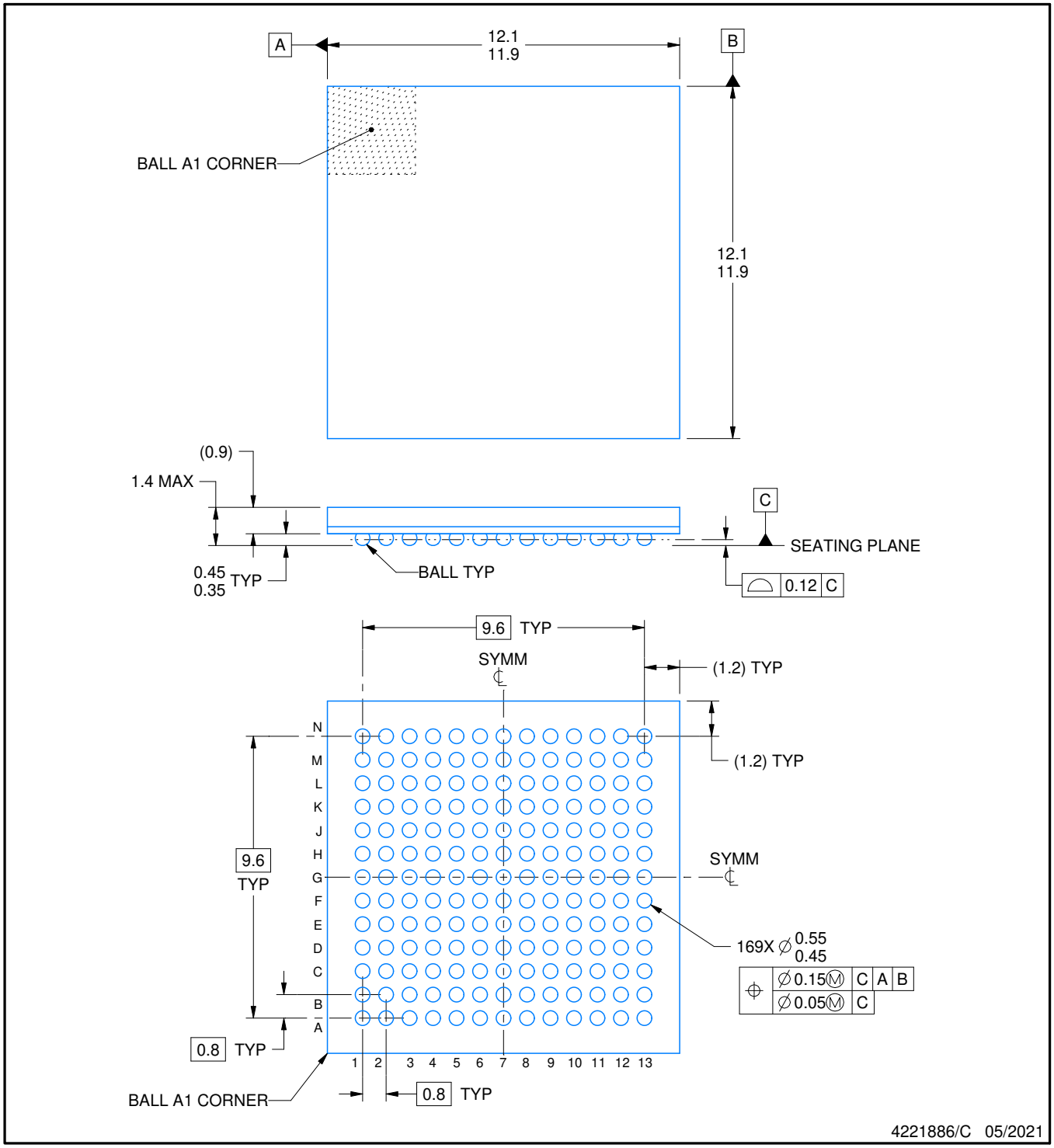
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| XIO2001IPNP | PNP | HTQFP | 128 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XIO2001IPNP.A | PNP | HTQFP | 128 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XIO2001IPNPG4 | PNP | HTQFP | 128 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XIO2001IPNPG4.A | PNP | HTQFP | 128 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XIO2001IZAJ | ZAJ | NFBGA | 144 | 260 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| XIO2001IZAJ.A | ZAJ | NFBGA | 144 | 260 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| XIO2001IZWS | ZWS | NFBGA | 169 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |
| XIO2001IZWS.A | ZWS | NFBGA | 169 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |
| XIO2001PNP | PNP | HTQFP | 128 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XIO2001PNP.A | PNP | HTQFP | 128 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XIO2001PNPG4 | PNP | HTQFP | 128 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XIO2001PNPG4.A | PNP | HTQFP | 128 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XIO2001ZAJ | ZAJ | NFBGA | 144 | 260 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| XIO2001ZAJ.A | ZAJ | NFBGA | 144 | 260 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |
| XIO2001ZWS | ZWS | NFBGA | 169 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |
| XIO2001ZWS.A | ZWS | NFBGA | 169 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.4 | 11.2 | 19.65 |

# PACKAGE OUTLINE

## ZWS0169A

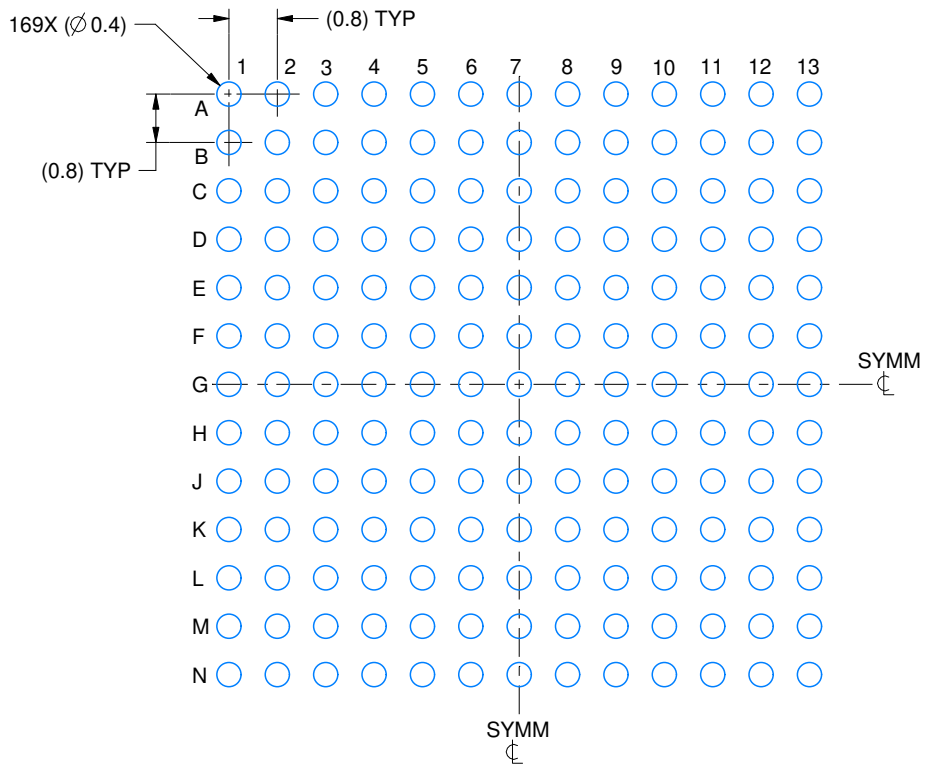
## NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

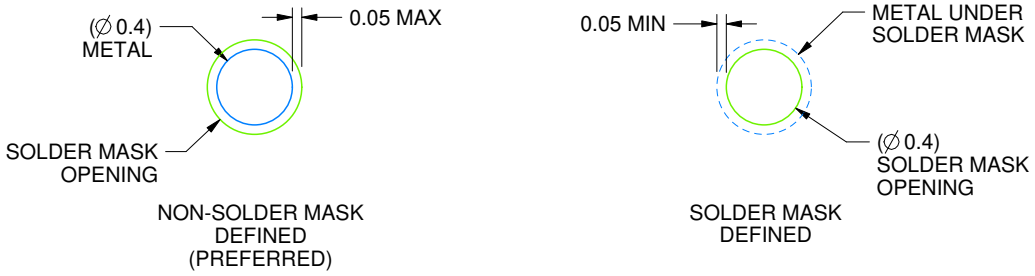



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:8X

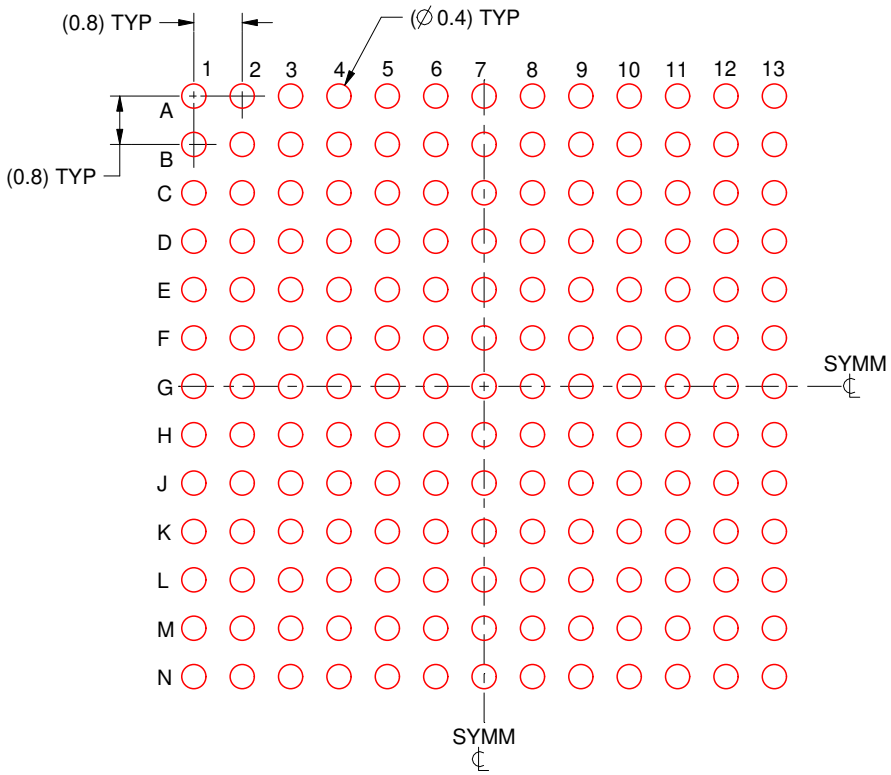



SOLDER MASK DETAILS
NOT TO SCALE

4221886/C 05/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSZA002 (www.ti.com/lit/ssza002).



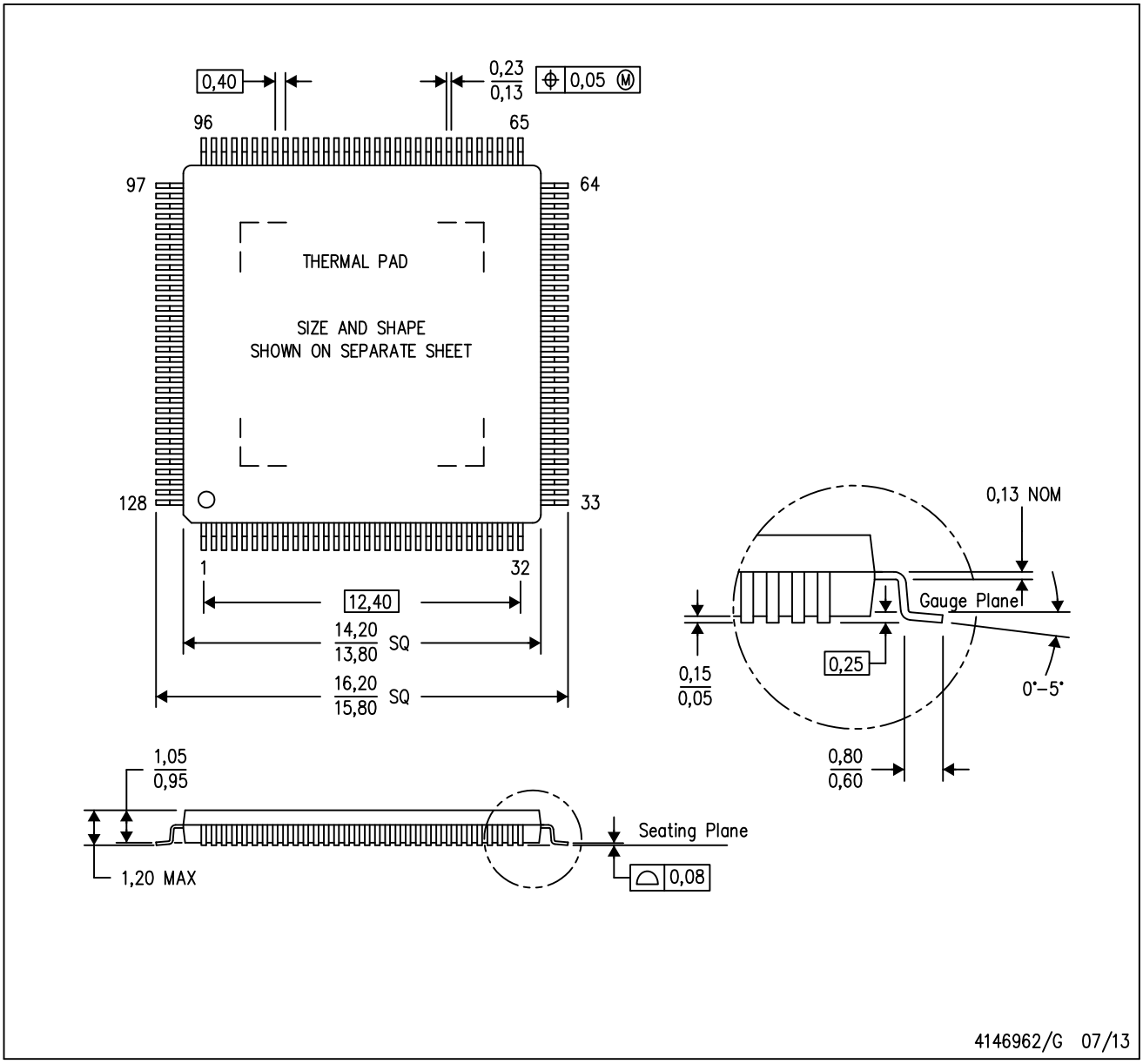

SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4221886/C 05/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PNP (S–PQFP–G128) PowerPAD™ PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

PowerPAD is a trademark of Texas Instruments.

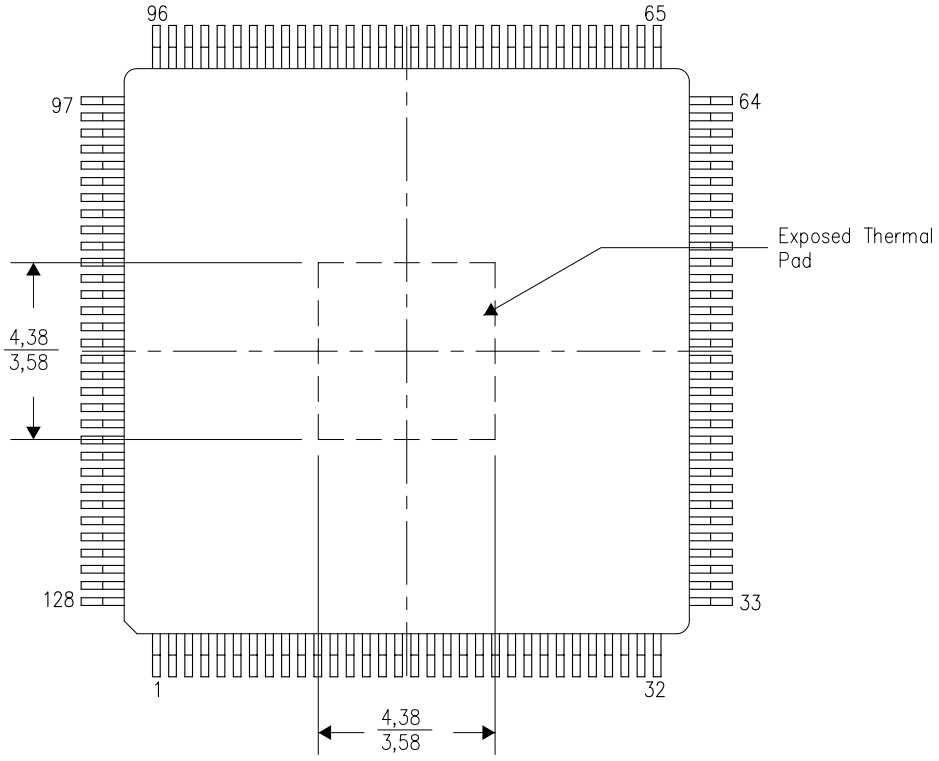
PNP (S–PQFP–G128) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

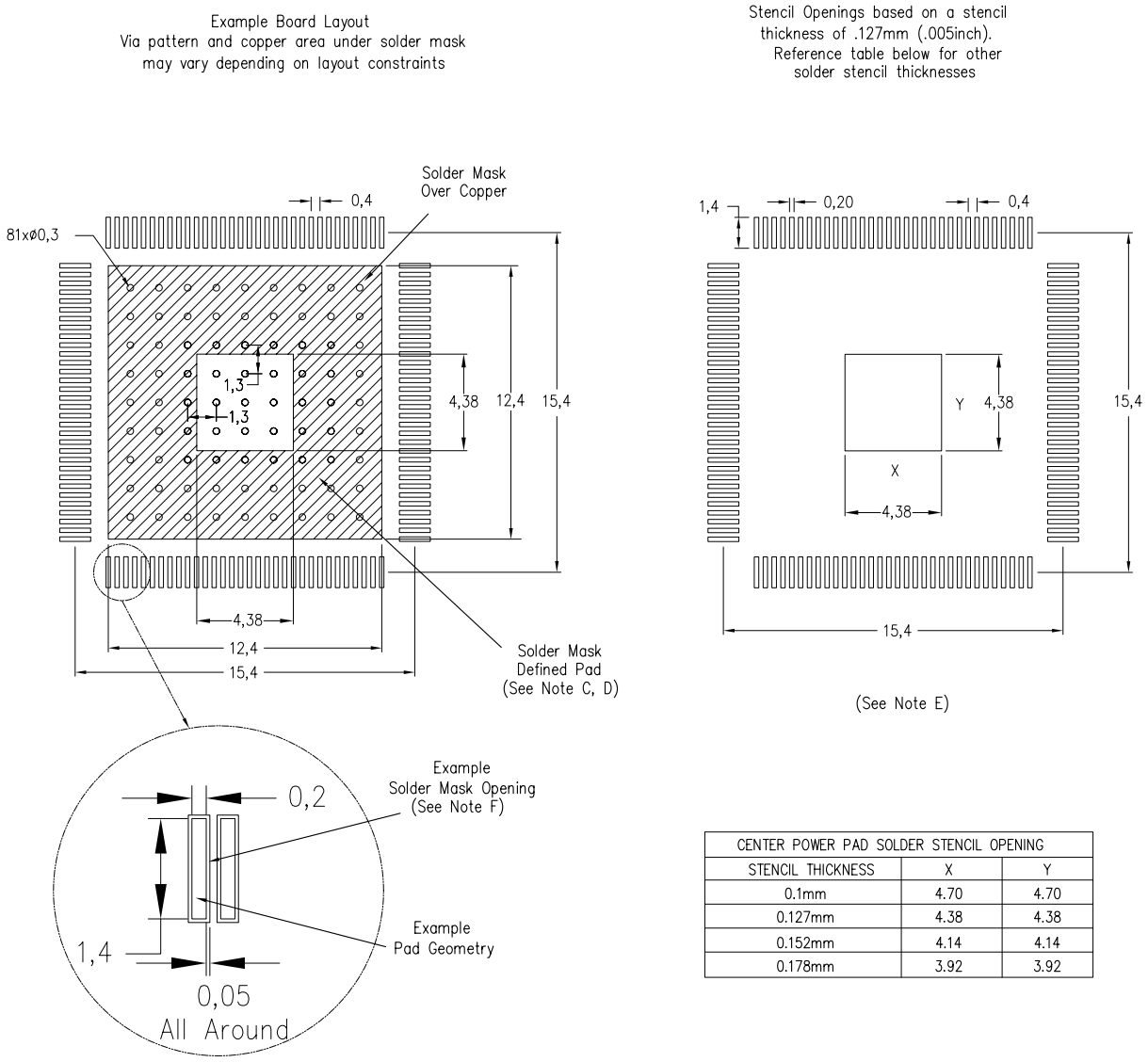
Exposed Thermal Pad Dimensions

4206232–13/L 10/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# PNP (S–PQFP–G128) PowerPAD PLASTIC QUAD FLAT PACK

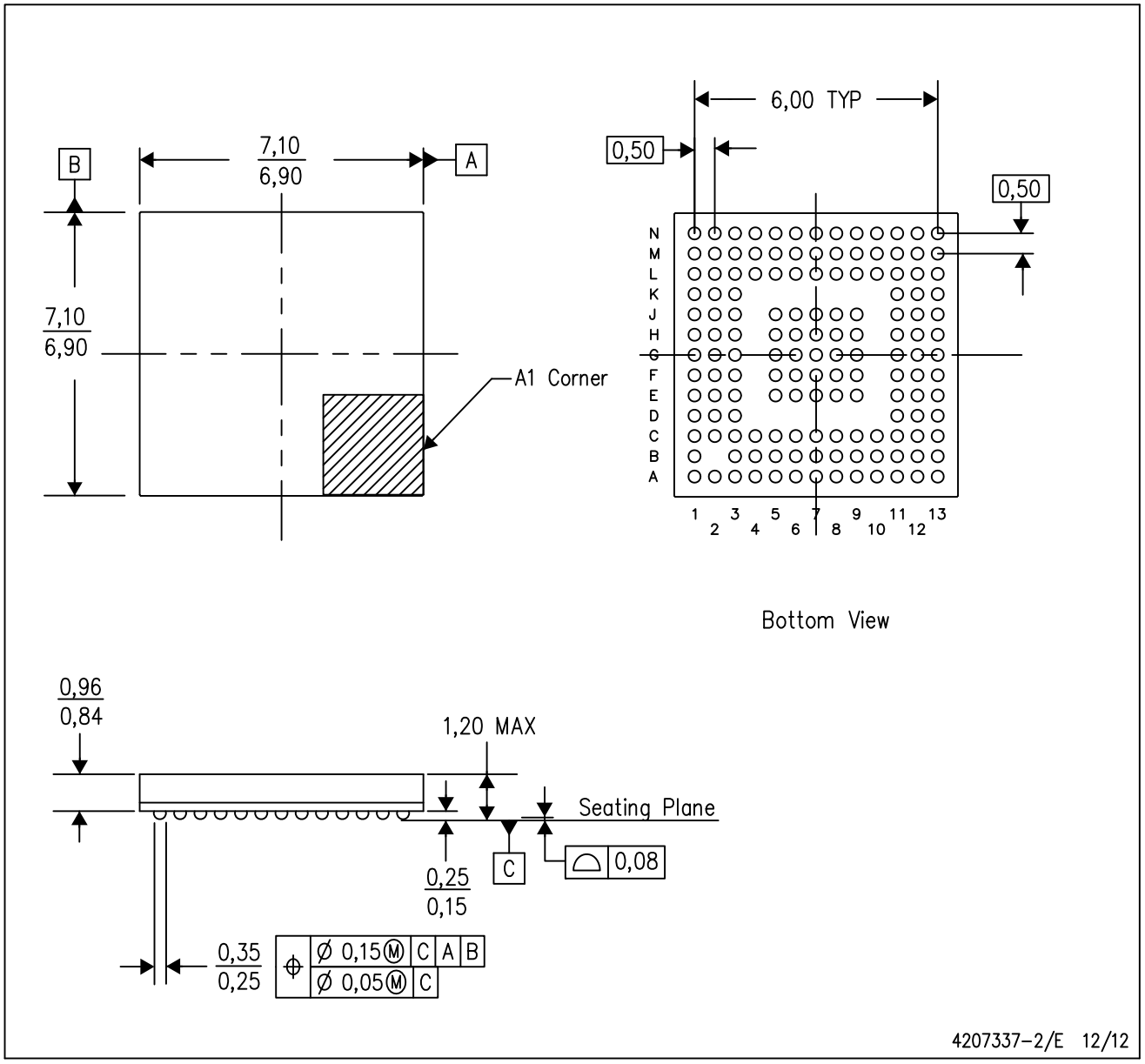



| CENTER POWER PAD SOLDER STENCIL OPENING | | |
|---|---|---|
| STENCIL THICKNESS | X | Y |
| 0.1mm | 4.70 | 4.70 |
| 0.127mm | 4.38 | 4.38 |
| 0.152mm | 4.14 | 4.14 |
| 0.178mm | 3.92 | 3.92 |

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

**PowerPAD is a trademark of Texas Instruments.**

ZAJ (S–PBGA–N144) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025